HMC284MS8G MSOP8 SPDT NON-REFLECTIVE SWITCH DC - 3.5 GHz

FEBRUARY 2001 v02.0101

Features

HIGH ISOLATION: >45 dB

POSITIVE CONTROL: 0/+5V

NON-REFLECTIVE DESIGN

ULTRA SMALL PACKAGE: MSOP8G

General Description

The HMC284MS8G is a low-cost SPDT switch in an 8-lead grounded base MSOP package. The device can control signals from DC to 3.5 GHz and is especially suited for Cellular, PCS, 2.4 GHz ISM, and 3.5 GHz WLL frequency bands. The design has been optimized to provide high isolation with minimal insertion loss for medium and low power applications. On-chip circuitry allows positive voltage control operation at very low DC currents with control inputs compatible with CMOS and most TTL logic families. In the "OFF" state, RF1 or RF2 is non-reflective. Applications include local oscillator or receive antenna multiplexing in cellular/PCS base station applications. See reflective high isolation SPDT version, HMC194MS8.

Guaranteed Performance V_{ctl} = 0/ +5 Vdc, 50 Ohm System, -40 to +85 deg. C

Parameter		Frequency	Min.	Typ.	Max.	Units
Insertion Loss		DC - 2.0 GHz DC - 3.0 GHz DC - 3.5 GHz		0.5 0.6 0.7	0.8 0.9 1.1	dB dB dB
Isolation	RF1 & RF2 RF1 / RF2 RF1 / RF2 RF1 & RF2	DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz DC - 3.5 GHz	41 38/41 34/36 30	45 41/45 37/39 33		dB dB dB dB
Return Loss (On State)		DC - 2.0 GHz DC - 2.5 GHz DC - 3.5 GHz	21 13 10	25 17 12		dB dB dB
Return Loss (Off State)		0.5 - 3.5 GHz	10	13		dB
Input Power for 1dB Compression		0.5 - 1.0 GHz 0.5 - 3.5 GHz	20 18	25 24		dBm dBm
Input Third Order Intercept (Two Tone Input Power= 0 dBm Each Tone)		0.5 - 3.5 GHz	43	48		dBm
Switching Characteristics tRISE / tFALL (10/90% RF / 90/10% RF) tON / tOFF (50% CTL to 10/90% RF)		DC - 3.5 GHz		 40 60		 nS nS

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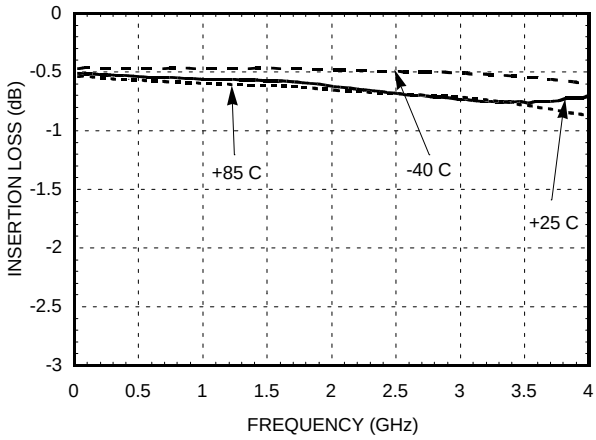
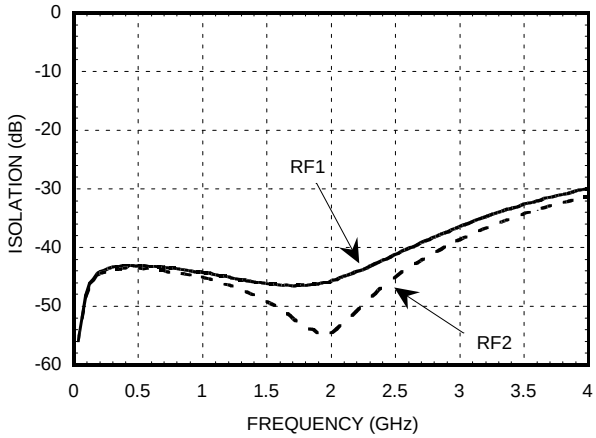
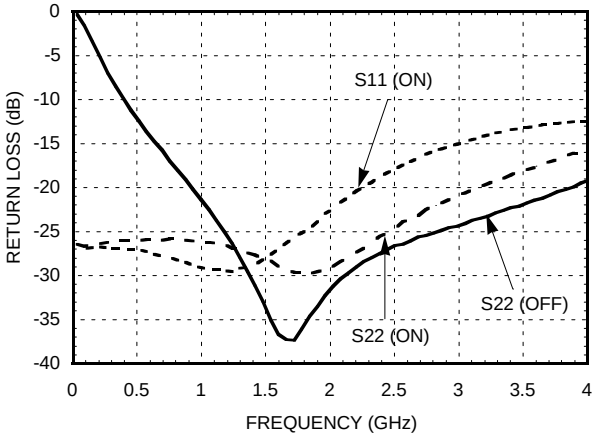
Insertion Loss



Isolation



Return Loss



Compression vs Frequency

	Carrier at 900MHz		Carrier at 1900MHz	
CTL Input	Input Power for 0.1dB Compression	Input Power for 1dB Compression	Input Power for 0.1dB Compression	Input Power for 1dB Compression
(Vdc)	(dBm)	(dBm)	(dBm)	(dBm)
+5	23	25	22	24

Caution: Do not operate continuously at RF power input greater than 1dB compression and do not "hot switch" power levels greater than +18 dBm (Control =0/ +5Vdc).

Distortion vs Frequency

Control Input	Third Order Intercept (dBm) 0 dBm Each Tone	
(Vdc)	900 MHz	1900 MHz
+5	48	50

*S-Parameter data is available On-Line at **www.hittite.com***

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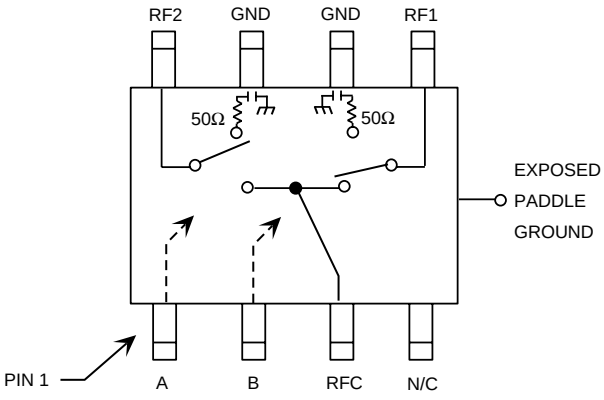
Functional Diagram



Absolute Maximum Ratings

Control Voltage Range (A & B)	-0.2 to +7.5 Vdc
Storage Temperature	-65 to +150 deg C
Operating Temperature	-40 to +85 dec C
RF Input Power Vctl = 0/+5V	+26 dBm

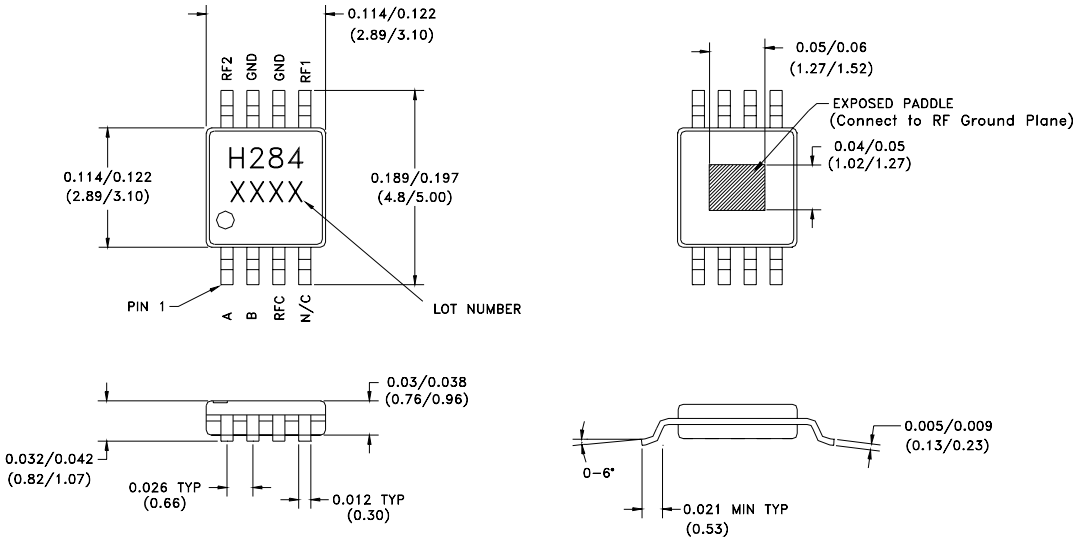
Truth Table

**Control Input Tolerances are +/- 0.2 Vdc*

Control Input *		Control Current		Signal Path	
A (Vdc)	B (Vdc)	Ia (uA)	Ib (uA)	RF to RF1	RF to RF2
0	+5	-25	25	On	Off
+5	0	25	-25	Off	On

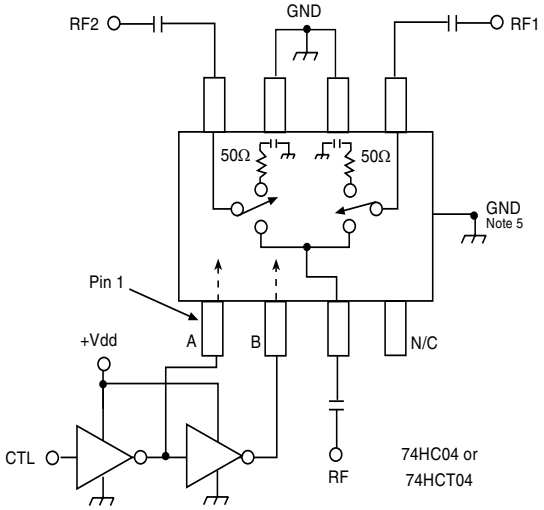
DC blocks are required at ports RFC, RF1, RF2.

Outline Drawing



1) MATERIAL:
A) PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED
B) LEADFRAME & PADDLE MATERIAL: COPPER ALLOY
2. PLATING: LEAD-TIN SOLDER PLATE
3. DIMENSIONS ARE IN INCHES (MILLIMETERS)
UNLESS OTHERWISE SPECIFIED TOL. ARE ±0.005(±0.13)

Typical Application Circuit



Notes:

1. Set A / B control to 0/+5V, Vdd = +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd = +5 Volts applied to the CMOS logic gates.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with Vdd = +7V and A/B set to 0/+7V.
5. Back side paddle must be connected to RF ground.
6. A grounded coplanar waveguide PCB layout technique is recommended to achieve high isolation. The component side ground plane between RFC/grounded paddle and RF1/RF2 should not be continuous, see below. There should be a continuous ground plane under component side layout.