

GaAS MMIC MSOP8 SPDT SWITCH DC - 3 GHz

FEBRUARY 2001

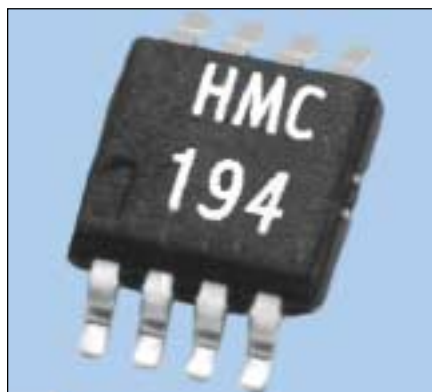
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Features

ULTRA SMALL PACKAGE: MSOP8

HIGH ISOLATION: 50 dB

POSITIVE CONTROL: 0/+3 to 0/+7V



General Description

The HMC194MS8 is a low-cost SPDT switch in an 8-lead MSOP package for use in applications which require high isolation between two RF paths. The device can control signals from DC to 3 GHz and is especially suited for PDC, DCS, PCS, and 2.4 GHz ISM frequency bands. The design has been optimized to provide extremely high isolation with minimal insertion loss in medium and low power applications. On chip circuitry allows positive voltage control operation at very low DC currents with control inputs compatible with CMOS and most TTL logic families. RF 1 or RF2 is a reflective open when "OFF". Applications include local oscillator multiplexing in cellular/PCS basestation applications which require high isolation.

Guaranteed Performance $V_{ctl} = 0/+5 V_{dc}$, 50 Ohm System, -40 to +85 deg. C

Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 1.0 GHz		0.7	0.9	dB
	DC - 2.0 GHz		0.7	0.9	dB
	DC - 2.5 GHz		0.8	1.1	dB
	DC - 3.0 GHz		0.9	1.2	dB
Isolation RF1 / RF2 RF1 / RF2	DC - 1.0 GHz	45 / 47	49 / 51		dB
	DC - 2.0 GHz	39 / 43	42 / 46		dB
	DC - 2.5 GHz	31	35		dB
	DC - 3.0 GHz	24	28		dB
Return Loss	DC - 1.0 GHz	18	21		dB
	DC - 2.0 GHz	14	17		dB
	DC - 2.5 GHz	13	17		dB
	DC - 3.0 GHz	13	17		dB
Input Power for 1dB Compression 0/+5V Control	0.5 - 1.0 GHz	19	23		dBm
	0.5 - 3.0 GHz	17	21		dBm
Input Third Order Intercept 0/+5V Control (+7 dBm Each Tone)	0.5 - 1.0 GHz	39	43		dBm
	0.5 - 3.0 GHz	37	41		dBm
Switching Characteristics	DC - 3.0 GHz				
			10		nS
			24		nS

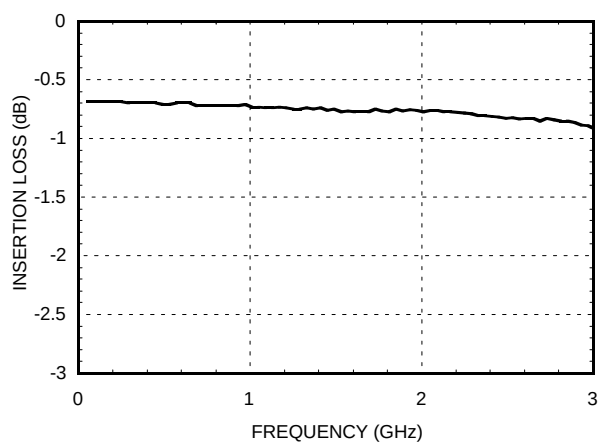


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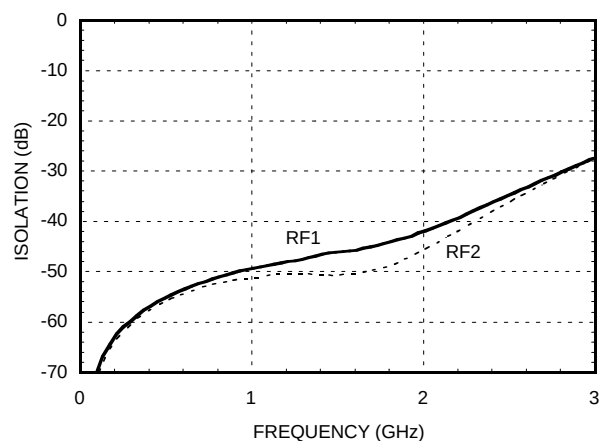
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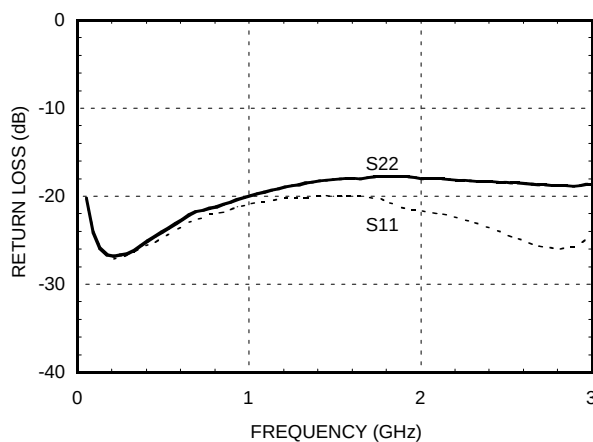
Insertion Loss



Isolation



Return Loss

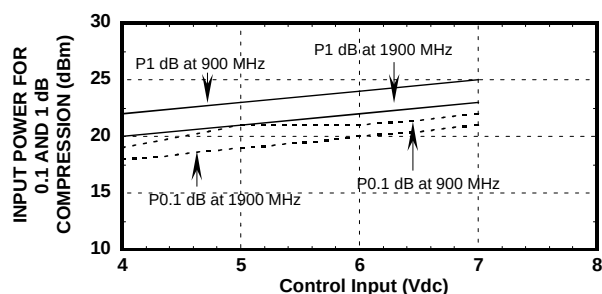


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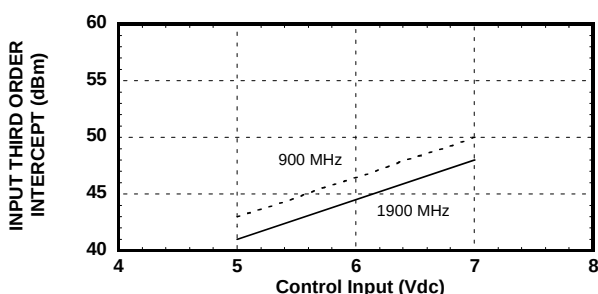
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Input 0.1 and 1.0 dB Compression vs Control Voltage



Input Third Order Intercept vs Control Voltage



Compression vs Control Voltage

Bias Vdd (Vdc)	Carrier at 900MHz		Carrier at 1900MHz	
	Input Power for 0.1dB Compression (dBm)	Input Power for 1dB Compression (dBm)	Input Power for 0.1dB Compression (dBm)	Input Power for 1dB Compression (dBm)
+4	19	22	18	20
+5	21	23	19	21
+6	21	24	20	22
+7	22	25	21	23

Distortion vs Control Voltage

Control Input (Vdc)	Third Order Intercept (dBm) +7 dBm Each Tone	
	900 MHz	1900 MHz
+5	43	41
+7	50	48

Caution: Do not operate in 1dB compression at power levels above +25 dBm and do not 'hot switch' power levels greater than +18 dBm (Control =0/ +5Vdc).

DC blocks are required at ports RF, RF1, RF2.

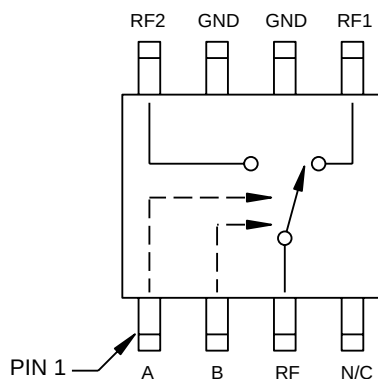


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Functional Diagram



Truth Table

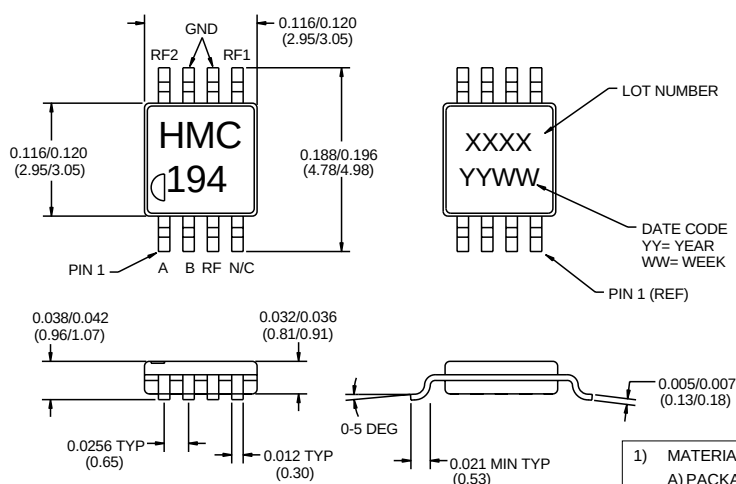
*Control Input Tolerances are +/- 0.2 Vdc

Control Input *		Control Current		Signal Path	
A (Vdc)	B (Vdc)	Ia (uA)	Ib (uA)	RF to RF1	RF to RF2
0	+3	-85	0	ON	OFF
+3	0	0	-85	OFF	ON
0	+5	-392	66	ON	OFF
+5	0	66	-392	OFF	ON
0	+7	-2000	270	ON	OFF
+7	0	270	-2000	OFF	ON

Absolute Maximum Ratings

Control Voltage Range (A & B)	-0.2 to +7.5 Vdc
Storage Temperature	-65 to +150 deg C
Operating Temperature	-40 to +85 dec C

Outline



- 1) MATERIAL:
A) PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED
B) LEADFRAME MATERIAL: COPPER ALLOY
2. PLATING: LEAD-TIN SOLDER PLATE
3. DIMENSIONS ARE IN INCHES (MILLIMETERS)
UNLESS OTHERWISE SPECIFIED TOL. ARE $\pm 0.005 (\pm 0.13)$

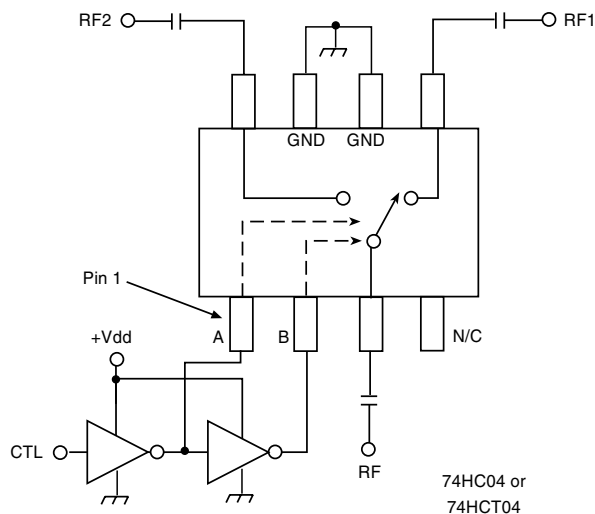


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Typical Application Circuit



Notes:

1. Set logic gate and switch Vdd = +3v to +5v, and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of 3 to 7 Volts applied to the CMOS logic gates.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with Control set to 0/+7V.

**See "Design Techniques Enhance Isolation in Switch Assemblies"
for HMC194MS8 Applications, Page 8-24**

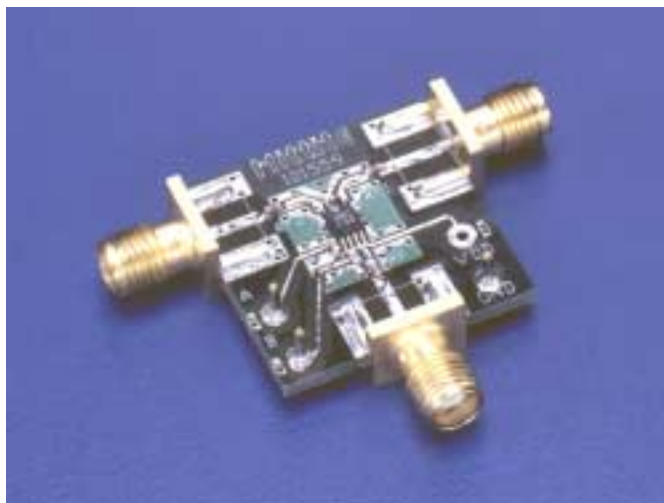


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Evaluation Circuit Board



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown below. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board as shown is available from Hittite upon request.

Evaluation Circuit Board Layout Design Details

Layout Technique	Grounded Co-Planar Waveguide (GCPW)
Material	FR4
Dielectric Thickness	0.028" (0.71 mm)
50 Ohm Line Width	0.037" (0.94 mm)
Gap to Ground Edge	0.010" (0.25 mm)
Ground VIA Hole Diameter	0.014" (0.36 mm)
Connectors	SMA-F (EF - Johnson P/N 142-0701-806)

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SWITCHES
SPDT
SMT

