HMC291

4 dB LSB GaAs IC 2 - BIT DIGITAL ATTENUATOR 0.7 - 4.0 GHz

FEBRUARY 2001 v00.0600

Features

4 dB LSB STEPS to 12 dB

SINGLE POSITIVE CONTROL PER BIT, 0/+3V

+/- 0.2 dB TYPICAL BIT ERROR

MINIATURE SOT 26 PACKAGE: 9 mm²

General Description

The HMC291 is a broadband 2 - bit positive control GaAs IC digital attenuator in a 6 lead SOT26 surface mount plastic package. Covering 0.7 to 4 GHz the insertion loss is typically less than 0.7 to 1.3 dB. The attenuator bit values are 4 (LSB) and 8 dB for a total attenuation of 12 dB. Accuracy is excellent at ± 0.2 dB typical with an IIP3 of up to +54 dBm. Two bit control voltage inputs, toggled between 0 and +3 to +5 volts, are used to select each attenuation state at less than 50 uA each. A single Vdd bias of +3 to +5 volts applied through an external 5KΩ resistor is required. The HMC291 is ideal for cellular, PCS, ISM, MMDS, and WLL handset & basestation applications. Occupying less than 9 mm², this is the smallest 2 - bit digital attenuator available.

Guaranteed Performance

With Vdd =+3V to +5V & Vctl = 0/Vdd (Unless Otherwise Stated), -40 to +85 deg C

Parameter		Frequency	Min.	Typ.	Max.	Units
Insertion Loss		0.7 - 1.4 GHz 1.4 - 2.3 GHz 2.3 - 2.7 GHz 2.7 - 4.0 GHz		0.7 0.9 1.0 1.1	1.0 1.3 1.4 1.6	dB dB dB dB
Attenuation Range		0.7 - 4.0 GHz		12		dB
Return Loss (RF1 & RF2, All Atten. States)		0.7 - 1.4 GHz 1.4 - 4.0 GHz	14 16	17 22		dB dB
Attenuation Accuracy: (Referenced to Insertion Loss)						
All Attenuation States All Attenuation States All Attenuation States All Attenuation States		0.7 - 1.4 GHz 1.4 - 2.3 GHz 2.3 - 2.7 GHz 2.7 - 4.0 GHz	± 0.3 + 3% of Atten. Setting Max ± 0.2 + 2% of Atten. Setting Max ± 0.2 + 3% of Atten. Setting Max ± 0.4 + 5% of Atten. Setting Max			dB dB dB dB
Input Power for 0.1 dB Compression	5V 3V	0.7 - 4.0 GHz		26 22		dBm dBm
Input Third Order Intercept Point (Two-Tone Input Power = 0dBm Each)	5V 3V	0.7 - 4.0 GHz		54 50		dBm dBm
Switching Characteristics tRISE, tFALL (10/90%RF) tON/tOFF (50% CTL to 10/90%RF)		0.7 - 4.0 GHz		 560 600		 ns ns

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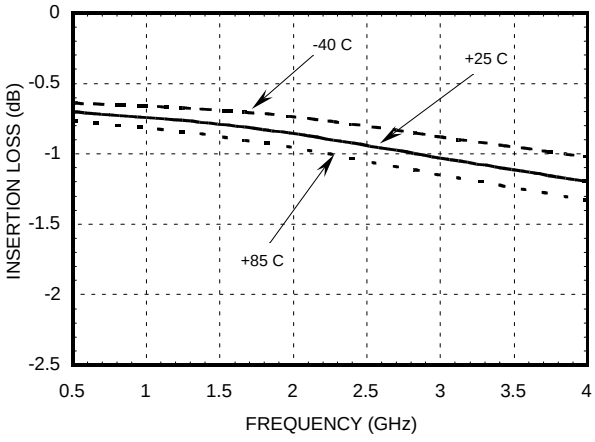
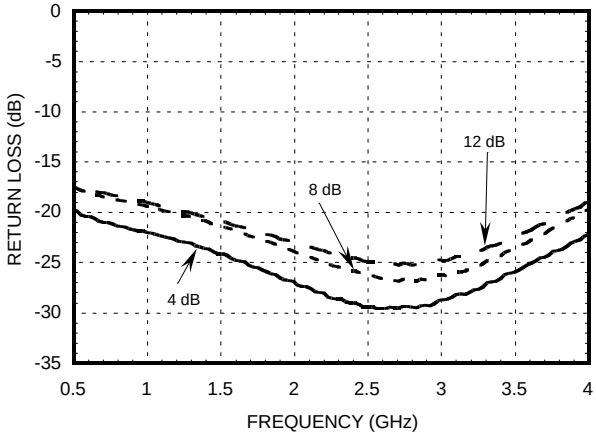
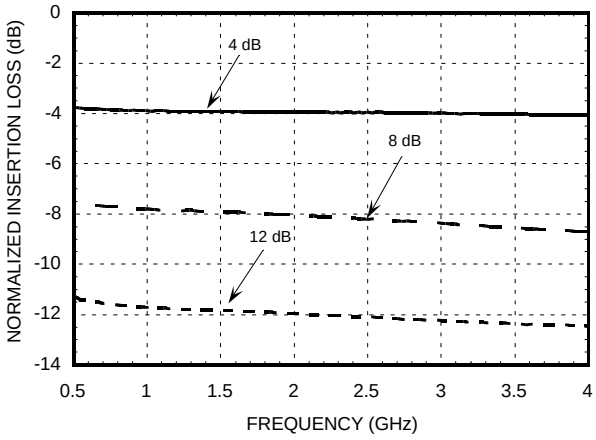
Insertion Loss



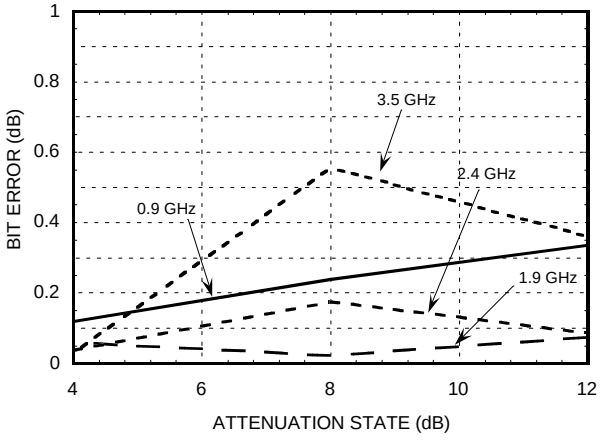
Return Loss RF1, RF2



Normalized Attenuation



Absolute Bit Error vs Attenuation State



Note: All Data Typical Over Voltage (+3V to +5V) & Temperature (-40 to +85 deg.C).

*S-Parameter data is available On-Line at **www.hittite.com***

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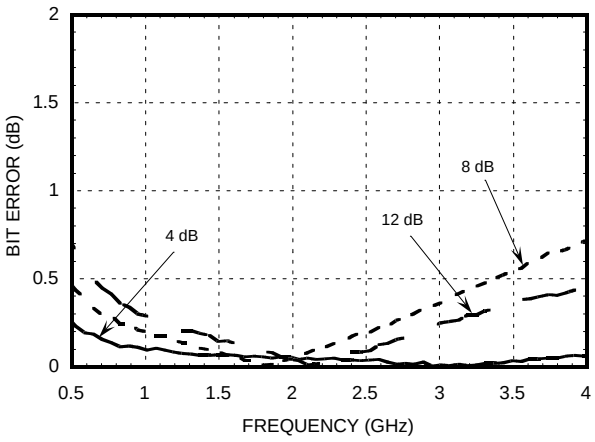
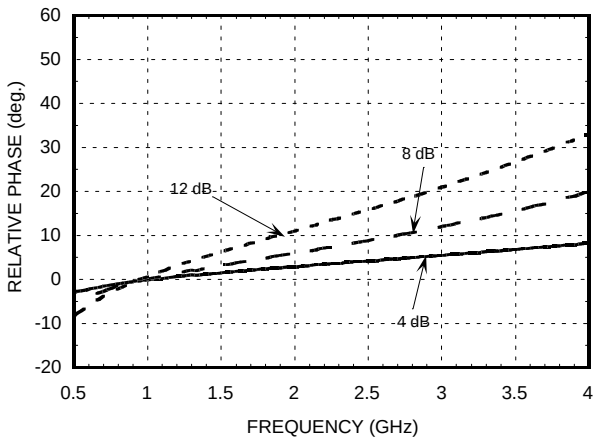
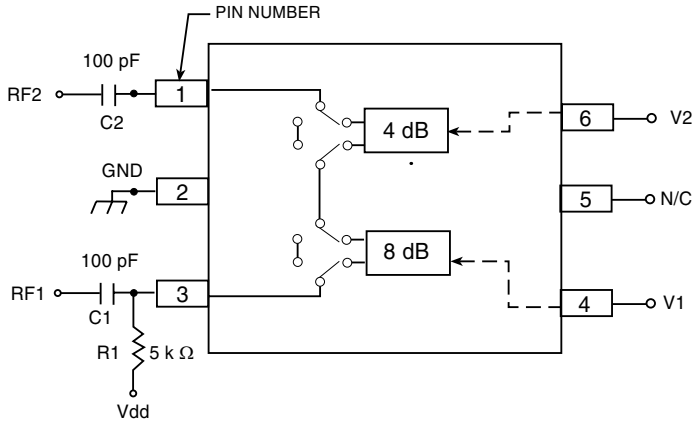
Absolute Bit Error vs Frequency



Relative Phase vs Frequency



Functional Diagram/ Application Circuit



DC blocking capacitors C1 & C2 are required on RF1 & RF2. Choose C1 = C2 = 100 ~ 300 pF to allow lowest customer specific frequency to pass with minimal loss. R1 = 5KΩ is required to supply voltage to the circuit through either PIN 3 or PIN 1.

Truth Table

Control Voltage Input		Attenuation Setting RF1 -RF2
V1 8 dB	V2 4 dB	
High	High	Reference I.L.
High	Low	4 dB
Low	High	8 dB
Low	Low	12 dB Max Atten.
Any combination of above states will provide an attenuation approximately equal to the sum of the bits selected.		

Control & Bias Voltages

State	Bias Condition
Low	0 to +0.2V@ 20 uA Max
High	Vdd ± 0.2 V @ 50 uA Typ
Note: Vdd = +3V to +5V ± 0.2V	

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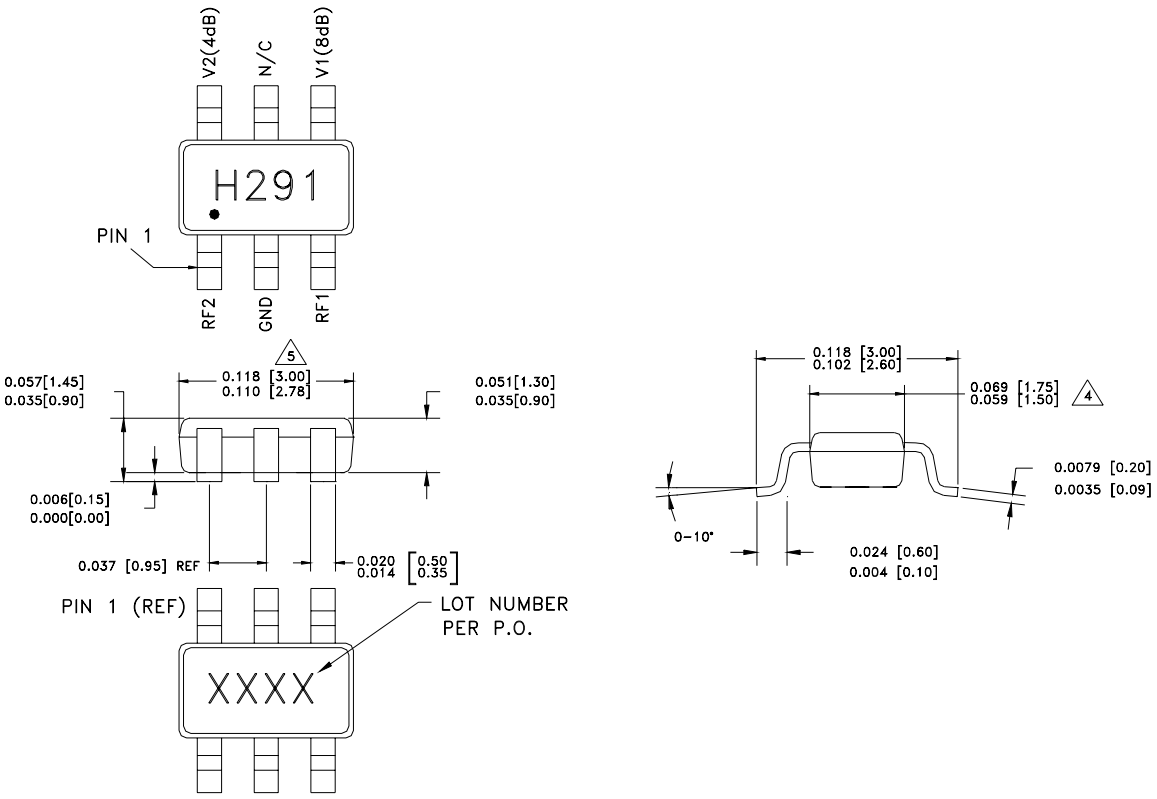
Absolute Maximum Ratings

Control Voltage (V1, V2)	Vdd + 0.5 Vdc
Bias Voltage (Vdd)	+8.0 Vdc
Storage Temperature	-65 to +150 deg C
Operating Temperature	-40 to +85 deg C
RF Input Power (0.7 - 4 GHz)	+28 dBm

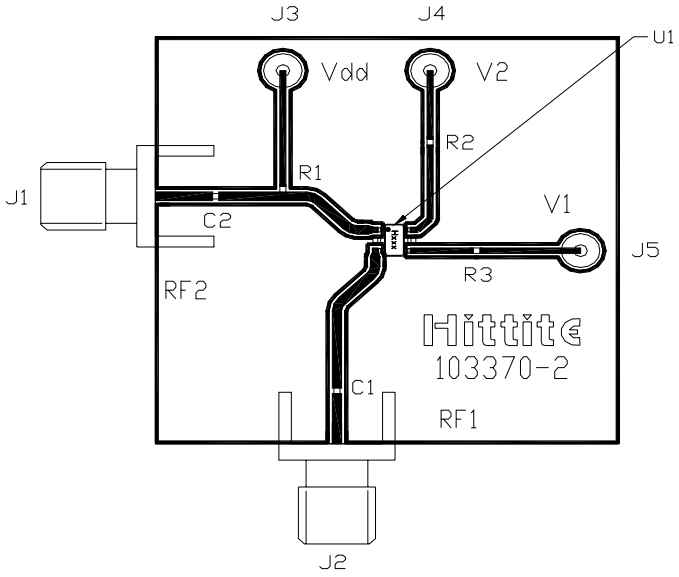
Outline



1. MATERIAL:
   A) PACKAGE BODY - LOW STRESS INJECTION-MOLDED PLASTIC.
   B) LEADFRAME MATERIAL: COPPER ALLOY
2. PLATING : LEAD - TIN SOLDER PLATE
3. DIMENSIONS ARE IN INCHES (MILLIMETERS).
   UNLESS OTHERWISE SPECIFIED ALL TOL. ARE ±0.005(±0.13).

4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15 MM PER SIDE
5. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25 MM PER SIDE

Evaluation Circuit Board



** R2 = R3 = 100 Ω .*
These resistors are optional and may be used to enhance decoupling of the RF path from the control inputs.

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown above. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board as shown is available from Hittite upon request.

Evaluation Circuit Board Layout Design Details

Item	Description
J1 - J2	PC Mount SMA Connector
J3 - J6	DC Pin
R1	5k Ω Resistor, 0402 Chip
R2, R3	100 Ω Resistor, 0402 Chip
C1, C2	0402 Chip Capacitor, Select for Lowest Frequency of Operation
U1	HMC291 Digital Attenuator
PCB*	103370 Evaluation PCB 1.5" x 1.5"
*Circuit Board Material: Rogers 4350	

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NOTES: