National Semiconductor

MILITARY DATA SHEET

MNHPC16083-20-X REV 0A0

Original Creation Date: 08/25/94
Last Update Date: 08/25/94
Last Major Revision Date: 08/25/94

16 BIT HIGH PERFORMANCE MICROCONTROLLER

General Description

The HPC16083 and HPC16003 are members of the HPC family of High Performance microControllers. Each member of the family has the same core CPU with a unique memory and I/O configuration to suit specific applications. The HPC16083 has 8k bytes of on-chip ROM. The HPC16003 has no on-chip ROM and is intended for use with external direct memory. Each part is fabricated in National's advanced microCMOS technology. This process combined with an advanced architecture provides fast, flexible I/O control, efficient data manipulation, and high speed computation.

The HPC devices are complete microcomputers on a single chip. All system timing, internal logic, ROM, RAM, and I/O are provided on the chip to produce a cost effective solution for high performance applications. On-chip functions such as UART, up to eight 16-bit timers with 4 input capture registers, vectored interrupts, WATCHDOG(TM) logic and MICROWIRE/PLUS(TM) provide a high level of system integration. The ability to address up to 64k bytes of external memory enables the HPC to be used in powerful applications typically performed by microprocessors and expensive peripheral chips.

The microCMOS process results in very low current drain and enables the user to select the optimum speed/power product for his/her system. The IDLE and HALT modes provide further current savings. The HPC is available in a 68-pin PGA package.

Industry Part Number

HPC16083

NS Part Numbers

HPC083XXX/U/883

Prime Die

HPCS083

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- HPC family-core features:
  - 16-bit architecture, both byte and word
  - 16 bit data bus, ALU, and registers
  - 64k bytes of external direct memory addressing
  - FAST-200 ns for fastest instruction when using 20.0MHz clock
  - High code efficiency-most instructions are single byte
  - 16 x 16 multiply and 32 x 16 divide
  - Eight vectored interrupt sources
  - Four 16-bit timer/counters with 4 synchronous outputs and WATCHDOG logic
  - MICROWIRE/PLUS serial I/O interface
  - CMOS-very low power with two power save modes: IDLE and HALT
- UART-full duplex, programmable baud rate
- Four additional 16-bit timer/counters with pulse width modulated outputs
- Four input capture registers
- 52 general purpose I/O lines (memory mapped)
- 8k bytes of ROM, 256 bytes of RAM on chip
- ROMless version available (HPC16003)
- -55 C to +125 C temperature range

(Absolute Maximum Ratings)

(Note 1)

Total Allowable Source or Sink	100mA
Storage Temperature Range	-65 C to +150 C
Lead Temp. (Soldering, 10 Sec)	300 C
Vcc with Respect to GND	-0.5V to 7.0V
Voltage All Other Pins	Vcc+0.5V to GND-0.5V

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih1	Logical 1 Input Voltage	RESET, NMI, CKI AND WO, B10-B13, B15	1, 2		.9Vcc		V	1, 2, 3
Vih2	Logical 1 Input Voltage	All Inputs Except Port A	1, 2		.7Vcc		V	1, 2, 3
Vih3	Logical 1 Input Voltage	Port A, Vcc = 4.5V	1		3.95		V	1, 2, 3
		Port A, Vcc = 5.5V	1		4.65		V	1, 2, 3
Vil1	Logical 0 Input Voltage	RESET, NMI, CKI AND WO	1, 2			.1Vcc	V	1, 2, 3
Vil2	Logical 0 Input Voltage	All Inputs Except Port A	1, 2			.2Vcc	V	1, 2, 3
Vil3	Logical 0 Input Voltage	Port A, Vcc = 4.5V	2			.5	V	1, 2, 3
		Port A, Vcc = 5.5V	2			.7	V	1, 2, 3
Voh2	Logical 1 Output Voltage	Ioh = -7mA (A0-A15, B10-B12, B15, CK2)	1, 2		2.4		V	1, 2, 3
Voh3	Logical 1 Output Voltage	Ioh3 = -1.6mA (B0-B9, B13-B14, P0-P3), WO (Open Drain)	1, 2		2.4		V	1, 2, 3
Voh4	Logical 1 Output Voltage	Ioh = -6mA (ST1, ST2)	1, 2		2.4		V	1, 2, 3
Voh5	Logical 1 Output Voltage	Ioh=-1mA(A0-A15,B10-B12,B15)when used as an external address/data bus	1, 2		2.4		V	1, 2, 3
Vol2	Logical 0 Output Voltage	Iol=3mA (CK2, A0-A15, B10-B12, B15)	1, 2			.4	V	1, 2, 3
Vol3	Logical 0 Output Voltage	Iol=.5mA (B0-B9, B13-B14, P0-P3), WO (Open Drain)	1, 2			.4	V	1, 2, 3
Vol4	Logical 0 Output Voltage	Iol=1.6mA (ST1, ST2)	1, 2			.4	V	1, 2, 3
Vol5	Logical 0 Output Voltage	Iol=3mA(A0-A15,B10-B12,B15)when used as an external address/databus	1, 2			.4	V	1, 2, 3
Ioz	TRI-STATE Leakage	Vss <= Vin <= Vcc (WO, PORT A, PORT B), Vcc = 5.5V	1, 2			+/-5	uA	1, 2, 3
Ili1	Input Leakage Current	Vss <= Vin <= Vcc, Vcc=5.5V (I0-I7,D0-D7,CKI, RESET, EXM, EI)	1, 2			+/-2	uA	1, 2, 3
Ili2	Input Pullup Current	Vin=0 (RDY/HLD, EXUI), Vcc=5.5V	1, 2		-50	-3	uA	1, 2, 3
Ili3	PORT B12 Pulldown During Reset	Vin=Vcc, PORT B12, Vcc=5.5V	1, 2		1	7	mA	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VRAM	RAM Keep Alive Voltage	Test Duration is 100mS	1, 2		2.5		V	1, 2, 3
Icc1	Supply Current Dynamic	Fin=20MHz, $\overline{\text{RESET}}$=Vss, Ioh=0mA, Iol=0mA, Vcc=5.5V	6			55	mA	1, 2, 3
Icc2	Idle Mode Current	Fin=20MHz, External Clock	6			3.5	mA	1, 2, 3
Icc3	HALT Mode Current	NMI=Vcc	6			2	mA	1, 2, 3
CI	Input Capacitance	ftest=1.0MHz, Input pin to ground	3			10	pF	4
CI/O	Input/Output Capacitance	ftest=1.0MHz, I/O pin to ground	3			20	pF	4

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 4.5V and 5.5V

fC=CKI freq.	Operating Frequency		4		2	20	MHz	9, 10, 11
tC1=1/FC	Clock Period		4		50		nS	9, 10, 11
tC=2/FC	Timing Cycle		4		100		nS	9, 10, 11
tLL=1/2tC - 9	ALE Pulse Width		5		41		nS	9, 10, 11
tST=1/4tC - 7	Address Valid to ALE Falling Edge		5		18		nS	9, 10, 11
tWAIT = tC = WS	Wait State Period		4		100		nS	9, 10, 11
FMW = 0.0625fC	External Microwire/Plus CLK Input Freq.		5			1.25	MHz	9, 10, 11
fU=0.125fC	External UART Clock Input Frequency		4			2.5	MHz	9, 10, 11
tDCIC2	CK2 Delay From CKI		5, 7			55	nS	9, 10, 11
tARR=1/4tC - 5	ALE Falling Edge to $\overline{\text{RD}}$ Falling Edge		5		20		nS	9, 10, 11
tRW=1/2tC + WS - 10	$\overline{\text{RD}}$ Pulse Width		5, 8		140		nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 4.5V and 5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tDR=3/4tC - 15	Data Hold After Rising Edge of $\overline{RD}$		5		0	60	nS	9, 10, 11
tRD=1/2tC+ WS-65	$\overline{RD}$ Falling Edge to Data In Valid		5, 8			85	nS	9, 10, 11
tRDA=tC-15	$\overline{RD}$ Rising Edge to Address Valid		5		85		nS	9, 10, 11
tVP=1/4tC - 5	Address Hold from ALE Falling Edge		5		20		nS	9, 10, 11
tARW=1/2tC - 5	ALE Trailing Edge to $\overline{WR}$ Falling Edge		5		45		nS	9, 10, 11
tWW=3/4tC+ WS-15	$\overline{WR}$ Pulse Width		5, 8		160		nS	9, 10, 11
tHW=1/4tC - 5	Data Hold After Trailing Edge of $\overline{WR}$		5		20		nS	9, 10, 11
tV=1/2tC + WS-5	Data Valid Before Rising Edge of $\overline{WR}$		5, 8		145		nS	9, 10, 11
tDAR=1/4tC +WS-50	Falling Edge of ALE to Falling Edge of RDY		5, 8			75	nS	9, 10, 11
tRWP=tC	RDY Pulse Width		5		100		nS	9, 10, 11
tSALE=3/4 tC + 40	Falling Edge of $\overline{HLD}$ to Rising Edge of ALE		5		115		nS	9, 10, 11
tHWP=tC+10	$\overline{HLD}$ Pulse Width		5		110		nS	9, 10, 11
tHAD=3/4tC +85	Rising Edge on $\overline{HLD}$ to Rising Edge on $\overline{HLDA}$		5			160	nS	9, 10, 11
tHAE = tC + 100	Falling Edge on $\overline{HLD}$ to Falling Edge on $\overline{HLDA}$		5, 9			200	nS	9, 10, 11
tBF=1/2tC + 66	BUS Float After Falling Edge on $\overline{HLDA}$		5			116	nS	9, 10, 11
tBE=1/2tC + 66	BUS Enable From Rising Edge of $\overline{HLDA}$		5		116		nS	9, 10, 11
tUAS	Address Setup Time to Falling Edge of $\overline{URD}$		5		10		nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 4.5V and 5.5V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tUAH	Address Hold Time From Rising Edge of $\overline{URD}$		5		10		nS	9, 10, 11
tRPW	$\overline{URD}$ Pulse Width		5		100		nS	9, 10, 11
tOE	$\overline{URD}$ Falling Edge to Data Out Valid		5			60	nS	9, 10, 11
tDRDY	$\overline{RDRDY}$ Delay From Rising Edge of $\overline{URD}$		5			70	nS	9, 10, 11
tWDW	$\overline{UWR}$ Pulse Width		5		40		nS	9, 10, 11
tUDS	Data Invalid Before Trailing Edge of $\overline{UWR}$		5		10		nS	9, 10, 11
tUDH	Data In Hold After Rising Edge of $\overline{UWR}$		5		20		nS	9, 10, 11
tA	$\overline{WRRDY}$ Delay From Rising Edge of $\overline{UWR}$		5			70	nS	9, 10, 11

Note 1: PORT A Vih test limit includes 700mV offset caused by output loads being on during Data Drive Time.
Note 2: PORT A Vil test limit includes 400mV offset caused by output loads being on during Data Drive Time
Note 3: Verified at initial qual only
Note 4: Tested in functional patterns. Not directly measured
Note 5: CL=70pF. AC testing inputs are driven at Vih for a logic 1 and Vil for a logic 0. Output timing measurements are made at 2.0V for a logic 1 and 0.8V for a logic 0.
Note 6: Icc1, Icc2, Icc3 measured with no external drive (Ioh=Iol=0, Iih=Iil=0). Icc1 measured with RESET=Vss. Icc3 with measured NMI=Vcc, CKI driven to Vih1 and Vil1, with rise and fall times less than 10nS.
Note 7: These AC characteristics are guaranteed with external clock drive on CKI having 50% duty cycle and with less than 15pF load on CKO with rise and fall times (tCKIR and tCKIL) on CKI input less than 2.5nS.
Note 8: WS = tWAIT*number of pre-programmed wait states. Min and Max values are calculated from Max operating frequency, Tc = 20MHz, with one wait state programmed.
Note 9: tHAE is spec'd for case with HLD falling edge occurring at the latest time it can be accepted during the present CPU cycle being executed. If HLD falling edge occurs later, tHAE as long as (3tC + 4WS + 72tC +90) may occur depending on the following CPU instruction cycles, its wait state and ready input.

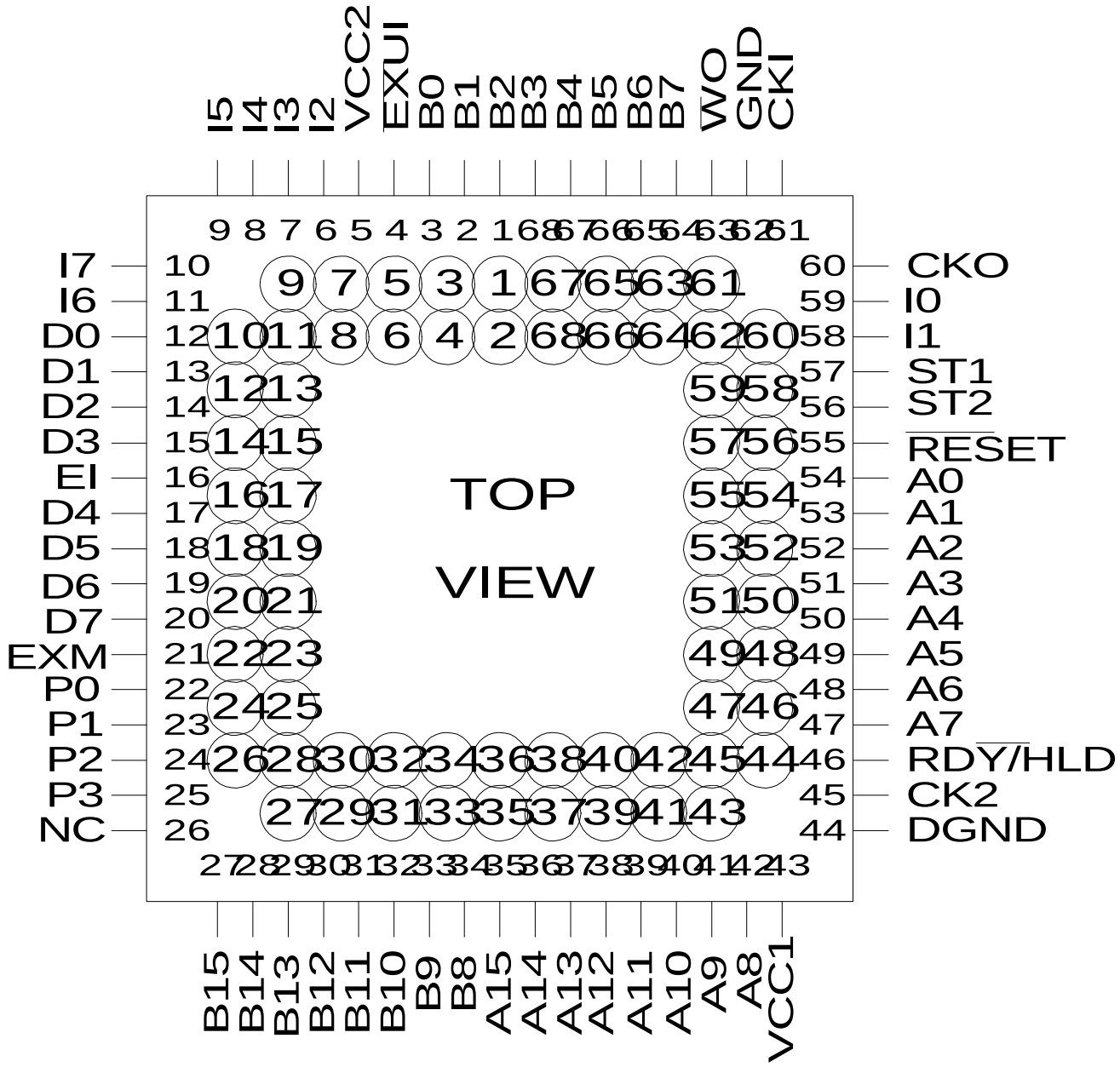
Burn-in/QCI Electrical End-Point Tests

OP#	Operation description	Sub-Groups
01	(When Required) for Group C and D	1,2,9,10

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
5864HRA1	PIN GRID ARRAY, CERAMIC, 68 PIN (B/I CKT)
P000006A	PIN GRID ARRAY, CERAMIC, 68 PIN (PIN OUT)
U68CRB	PIN GRID ARRAY, CERAMIC, 68 PIN (P/P DWG)

See attached graphics following this page.

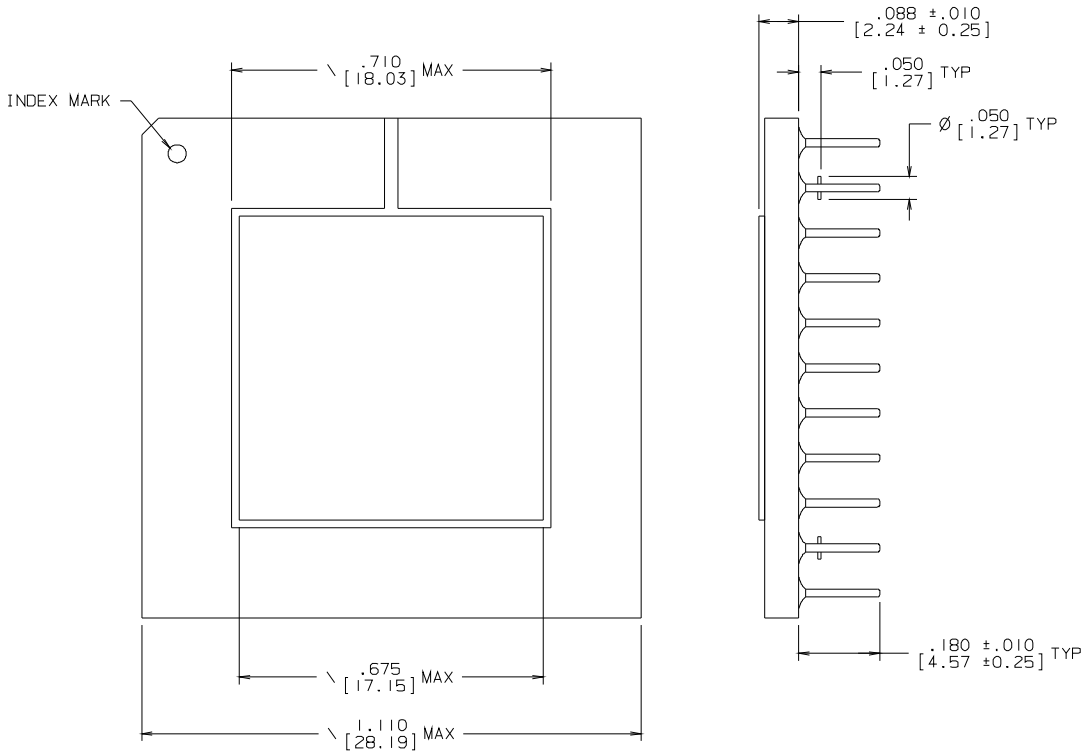


HPC003U20/883, HPC083XXX/U/883
HPC004U20/883, HPC064XXX/U/883

CONNECTION DIAGRAM
68 - LEAD PGA (TOP VIEW)

P000006A

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
B	REVISE PER CURRENT STD & REDRAW; ADD MIL/AERO STAMP	09999	09/15/93	TL/



NOTES: UNLESS OTHERWISE SPECIFIED

1. 50 MICROINCHES / 1.27 MICROMETERS MINIMUM GOLD PLATE OVER 50 MICROINCHES / 1.27 MICROMETERS MINIMUM NICKEL.
2. REFERENCE JEDEC REGISTRATION MO-066, VARIATION AC, DATED 05/87.

MIL/AERO
CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

PIN GRID ARRAY,
CERAMIC,
68 PIN

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-U68C	B

DO NOT SCALE DRAWING | SHEET 1 OF 1