HCS412

KEELOQ® Code Hopping Encoder and Transponder

FEATURES

Security

- Programmable 64-bit encoder key
- Two 64-bit transponder keys
- 32-bit bi-directional challenge and response using one of two keys
- 69-bit transmission length
- 32-bit uni-directional code hopping, 37-bit nonencrypted portion
- Encoder keys are read protected
- Programmable 28/32-bit serial number
- 60-bit, read-protected seed for secure learning
- Two IFF encryption algorithms
- Delayed increment mechanism
- Asynchronous transponder communication
- Queuing information transmitted

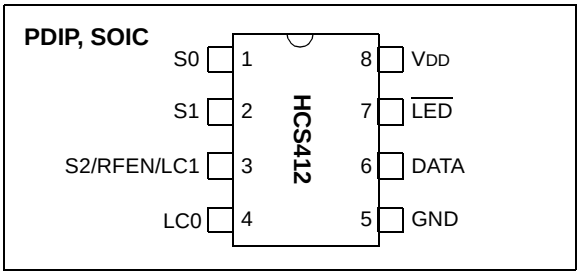
Operating

- 2.0V to 6.3V operation
- Three switch inputs: S2, S1, S0 – seven functions
- Batteryless bi-directional transponder
- Selectable baud rate and code-word blanking
- Automatic code-word completion
- Battery low detector
- Nonvolatile synchronization
- PWM or Manchester data encoding
- Combined transmitter, transponder operation
- Anti-collision of multiple transponders
- Passive proximity activation
- Device protected against reverse battery
- Intelligent damping for high Q LC-circuits
- 100mV pp sensitive LC input

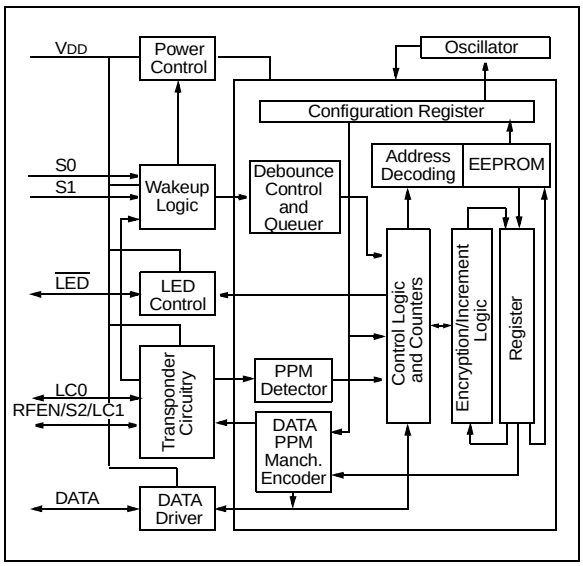
Typical Applications

- Automotive remote entry systems
- Automotive alarm systems
- Automotive immobilizers
- Gate and garage openers
- Electronic door locks (Home/Office/Hotel)
- Burglar alarm systems
- Proximity access control

PACKAGE TYPES



BLOCK DIAGRAM



Other

- 37-bit nonencrypted part contains 28/32-bit serial number, 4/0-bit function code, 1-bit battery low, 2-bit CRC, 2-bit queue
- Simple programming interface
- On-chip tunable RC oscillator (±10%)
- On-chip EEPROM
- 64-bit user EEPROM in transponder mode
- Battery-low LED indication
- SQTP serialization quick-time programming
- 8-pin PDIP/SOIC
- ASK and FSK PLL interface option
- RF Enable output
- Built in amplifier on LC inputs

GENERAL DESCRIPTION

The HCS412 combines the patented KEELOQ code hopping technology and bi-directional transponder challenge-and-response security into a single chip solution for logical and physical access control. High security learning mechanisms make this a turnkey solution when used with the KEELOQ decoders.

When the HCS412 is used as a code hopping encoder device, it is ideally suited to keyless entry systems, primarily for vehicles and home garage door openers. It is meant to be a cost-effective, yet secure solution to such systems. The HCS412 can also be used as a secure bi-directional transponder for verification of a token. This makes the HCS412 ideal for secure access control and identification applications. A single HCS412 can be used as an encoder for Remote Keyless Entry (RKE) and a transponder for immobilization in the same circuit and thereby dramatically reducing the cost of hybrid transmitter/transponder circuits.

1.0 SYSTEM OVERVIEW

1.1 Key Terms

The following is a list of key terms used throughout this datasheet. For additional information on terminology, please refer to the KEELOQ introductory Technical Brief (TB003).

- Anti-collision - A scheme whereby transponders in the same field can be addressed individually preventing simultaneous response to a command
- Code Hopping - A method by which a code changes in a predictable way each time it is transmitted
- Code-word - A block of data that is repeatedly transmitted during a ***Transmission***
- Decoder - A Device that can interpret (Decrypt) data sent by an ***Encoder***
- Decryption algorithm - A recipe whereby scrambled data can be unscrambled using the same ***Encryption key*** used to scramble the data
- Encoder - A device that can generate and encode (Encrypt) data
- Encryption algorithm - A recipe whereby data is scrambled using an ***Encryption key*** before it becomes public. The data can only be interpreted by using a ***Decryption algorithm*** using the same ***Encryption key***
- Encryption key - A unique and secret digital number used to encrypt and decrypt data
- IFF - Identify Friend or Foe
- Learning - An ***Encoder*** can be matched with a ***Decoder*** by enabling the decoder to accept the encoder as a valid encoder
- Manufacturer's Code - A unique and secret code used to generate unique ***Encryption keys*** for each ***Encoder***
- Proximity Activation - A method whereby an encoder can be activated by detecting a inductive field
- PKE - Passive Keyless Entry
- RKE - Remote Keyless Entry
- Transmission - A stream of data consisting of repeating ***Code-words***
- Transport code - A code known by the manufacturer allowing the programming of certain secure areas

1.2 KEELOQ Code Hopping Encoders

Most keyless entry systems transmit the same code from a transmitter every time a button is pushed. The relative number of code combinations for a low-end system is also a relatively small number. These shortcomings provide the means for a sophisticated thief to create a device that 'grabs' a transmission and retransmits it later or a device that scans all possible combinations until the correct one is found.

The HCS412 employs the KEELOQ code hopping technology and an encryption algorithm to achieve a high level of security. Code hopping is a method by which the code transmitted from the transmitter to the receiver is different every time a transmission is initiated. This method, coupled with a transmission length of 69 bits, virtually eliminates the use of code 'grabbing' or code 'scanning'.

A 16-bit synchronization counter value is the basis for the transmitted code changing with every transmission, and is incremented each time a code hopping transmission is initiated. Because of the complexity of the encryption algorithm, a change in one bit of the synchronization counter value will result in a large change in the actual transmitted code.

When a code hopping encoder is activated, the encoder reads the button inputs and updates the synchronization counter. The counter, button inputs and a discrimination value are then encrypted using the encoder key to form the code-hopping portion of the transmission.

The 32-bit code-hopping portion is combined with additional fixed data form the code-word that is transmitted to the receiver. The code-word format is explained in detail in Section 3.1.

1.3 KEELOQ Identify Friend or Foe (IFF)

Validation of a token involves a random challenge being sent to the token. The token then generates and replies with a calculated response using an encoder key. To verify that it is a valid token, the same calculation is done by the challenger and compared to the reply from the token. If the responses match, the token is identified as a valid token and the decoder can take appropriate action. This process is called Identify Friend or Foe (IFF).

The HCS412 does a 32-bit IFF using one of two possible encryption algorithms. In addition there are up to two encoder keys that can be used by the HCS412 to calculate the response.

The bi-directional communication required for IFF is done through the inductive communication path. A command that chooses between algorithms and keys is presented to the HCS412 before the challenge.

2.0 DEVICE DESCRIPTION

2.1 Pinout Description

The HCS412 has the same footprint as most of the other encoders in the KEELOQ family, except for the two pins that are reserved for transponder operation. Below is a summary of the HCS412 pin descriptions.

TABLE 2-1: PINOUT SUMMARY

Pin Name	Pin Number	Description
S0	1	Button input pin with Schmitt trigger detector and an internal 60kΩ (nominal) pull-down resistor.
S1	2	Button input pin with Schmitt trigger detector and an internal 60kΩ (nominal) pull-down resistor.
S2/RFEN/ LC1	3	Multi-purpose input / output pin and is used as: • Button input pin with Schmitt trigger detector and an internal pull-down resistor. • RFEN output driver. • LC1 transponder interface communication output driver and LC bias. • Programming input clock signal.
LC0	4	Transponder interface communication input detector with automatic gain control amplifier and inductive communication output driver.
GND	5	Power ground connection.
DATA	6	Transmission data output driver. Programming input / output data signal.
LED	7	LED output driver.
VDD	8	Supply voltage connection.

FIGURE 2-1: S0/S1 PIN DIAGRAM

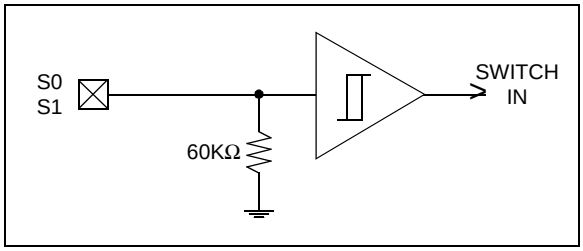


FIGURE 2-2: S2/RFEN/LC1 PIN DIAGRAM

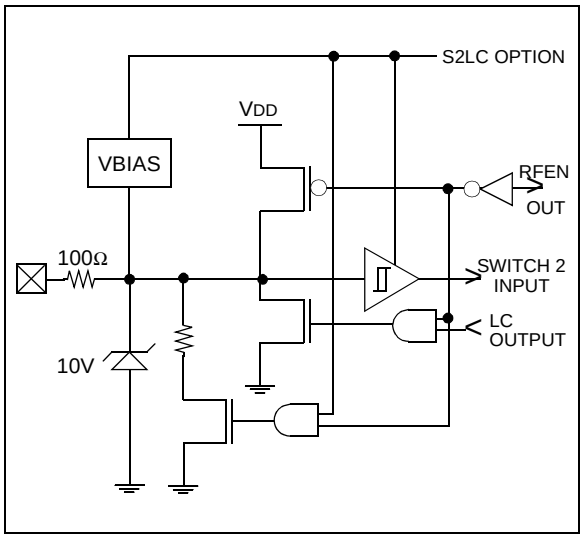


FIGURE 2-3: LC0 PIN DIAGRAM

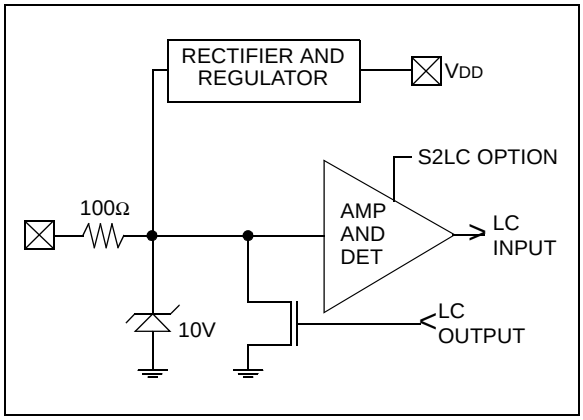


FIGURE 2-4: DATA PIN DIAGRAM

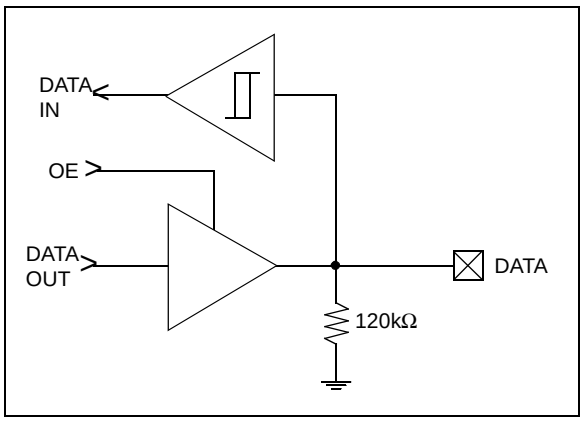
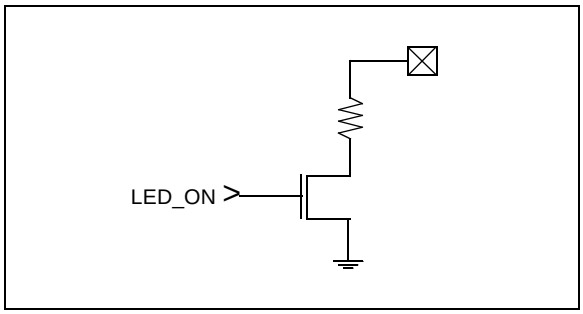


FIGURE 2-5: LED PIN DIAGRAM



2.2 Architecture Overview

2.2.1 WAKE-UP LOGIC AND POWER DISTRIBUTION

If power is applied to the HCS412, it will automatically go into a low power standby mode until it is activated. Power is supplied to the minimum required circuitry to detect a wakeup condition. This allows for low power consumption making the HCS412 ideal for battery operated applications.

The HCS412 will wake up from this low power mode when one or more of the button inputs are pulled high or a signal is detected on the LC0 transponder interface pin. Upon wakeup, power is switched on to the main logic circuitry that controls the operation of the device until it powers down again. The device will try to determine what caused the activation by sampling the button and transponder inputs.

If it is determined that a button input was raised, the device will enter Code Hopping Mode or CH Mode. If the device detects a signal on the transponder interface, it will enter IFF mode. CH Mode has priority over IFF mode. This implies that if there is a signal on the transponder input and the button input, the transponder input would be ignored, until the button input is released.

2.2.2 CONTROL LOGIC

A dedicated state machine controls functional operation of the HCS412. This state machine together with a 32-bit shift register and additional timing counters perform all the control, timing and data manipulation required. This includes the reading and writing of the onboard EEPROM, executing the encryption algorithms and controlling the data modulation.

2.2.3 EEPROM

The HCS412 has onboard nonvolatile EEPROM, which is used to store user programmable options, 64-bits of user EEPROM and the synchronization counter.

The configuration options are programmed at the time of production and include the security-related information such as encoder keys, serial number and discrimination value. All the security related options are read protected. The user 64-bit EEPROM is read/write accessible through the transponder communication path.

The initial counter value is also programmed at the time of production. From then on, the device maintains the counter itself. The counter is implemented with a Grey code counter to minimize EEPROM writing during the lifecycle of the product. The transmitted counter is converted to binary format. Counter corruption is protected by the use of a semaphore word.

Before every EEPROM write, the internal circuitry also ensures that the High Voltage required to write to the EEPROM is at an acceptable level.

Programming of the EEPROM for production can be done through the DATA pin using the S2 pin as a clock input. The EEPROM can also be programmed through the transponder communication path.

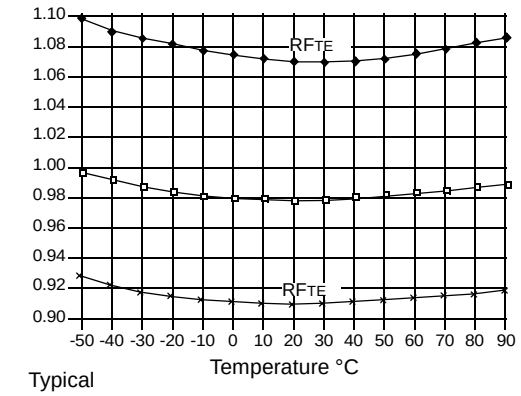
2.2.4 CONFIGURATION REGISTER

After wake-up, the HCS412 loads the configuration options from the EEPROM into a configuration register. The values are then used to control various options related to the device operation. The configuration register is also used to store the tune values for the onboard RC oscillator.

2.2.5 ONBOARD RC OSCILLATOR

The HCS412 has an onboard RC oscillator. Due to variations in process parameters, temperature and battery operating voltage, the oscillator can be tuned to provide better output timing characteristics. There are four bits making up the Oscillator Tune Value (OSCT) that allow the oscillator to be tuned, so that it is accurate within ±10% over temperature variations.

FIGURE 2-6: HCS412 NORMALIZED RF_{TE} VERSUS TEMP



Note: Values are for calibrated oscillator.

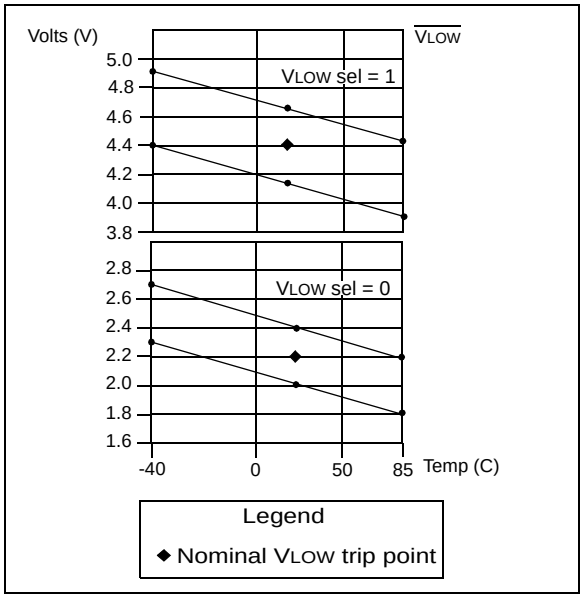
2.2.6 LOW VOLTAGE DETECTOR

A low battery voltage detector onboard the HCS412 can indicate when the operating voltage drops below a predetermined value. There are two options available, depending on the Low Voltage Trip Point Select (VLOWSEL) configuration option. The two options provided are:

- A 2.2 V nominal level for 3V battery operation
- A 4.4 V nominal level for 6V battery operation

The output of the low voltage detector is transmitted in CH Mode so the receiver can give an indication to the user that the transmitter battery is low. Operation of the LED changes to further indicate that the battery is low and need replacing.

FIGURE 2-7: TYPICAL VOLTAGE TRIP POINTS



2.2.7 TRANSPONDER INTERFACE AND THE S2/RFEN/LC1 PIN

The S2/RFEN/LC1 pin can be used as a normal button input, a RF enable output or as part of the transponder interface circuitry. Selecting between the transponder input and S2/RFEN is done with Button/transponder select (S2LC) Configuration option. Please refer to the pin diagrams in Section 2.1.

2.2.7.1 BUTTON INPUT

The transponder input is selected by default. If the S2/RFEN/LC1 pin is used as a button input the device must be powered up and activated once to allow reading of the configuration option. This will then switch off the transponder bias circuitry and therefore reduce the standby current. The internal pull-down resistor is also enabled, when the S2/RFEN/LC1 pin is configured as a button input.

2.2.7.2 TRANSPONDER INTERFACE

Connecting a LC resonant circuit between the S2/RFEN/LC0 and the LC1 pins creates the transponder communication path on the HCS412. The internal circuitry on the HCS412 provides the following functions:

- Input protection through onboard 10V zener diodes
- Amplification and signal detection circuitry to detect incoming signals from the decoder to the HCS412
- Clamping transistors to communicate from the HCS412 to the decoder through the inductive field
- Damping circuitry to allow reliable communication for LC circuits with a high Q factor
- Rectifier and regulator for the VDD supply voltage in a transponder only configuration

During normal transponder operation, the S2/RFEN/LC1 pin functions as a bias pin to bias the amplifier input. The amplifier gain is controlled to achieve the optimum level of amplification, depending on the strength of the incoming signal. The signal is then detected with an envelope detector before it is passed on to the logic circuit for interpretation.

2.2.7.3 RF ENABLE OUTPUT

The RFEN signal out is driven high when the HCS412 transmits data on the DATA pin. It also provides the PLL interface with the DATA pin. This function is enabled with the RF enable (RFEN) configuration option.

3.0 DEVICE OPERATION

3.1 Code Hopping Mode (CH Mode)

Upon detecting a button input, the HCS412 delays the debounce time (T_{DBP}) for switch debounce after which the button inputs are sampled to determine the button code. Depending on which button code is detected, the HCS412 can transmit a code-hopping or seed transmission. If required, the code-hopping portion of the transmission is generated and transmitted through the DATA pin after the total power-up time (T_{TD}). When a seed transmission is required, the values programmed into the EEPROM are transmitted straight through the DATA pin. Table 3-1 indicates the button input function codes to activate a code-hopping or Seed transmission.

A code-hopping transmission can also be activated if a field is detected on the transponder input. This is called Proximity activation and must be enabled by setting the appropriate configuration option in the EEPROM.

TABLE 3-1: CH MODE ACTIVATION

LC0 (Note 2)	S2	S1	S0	Transmission Description
X	0	0	1	Code-hopping code-words only
X	0	1	0	Code-hopping code-words only
X	0	1	1	Code-hopping code-words until time = T_{DSD} and then seed code-words. **(Note 1)**
X	1	0	0	Code-hopping code-words only
X	1	0	1	Code-hopping code-words only
X	1	1	0	Code-hopping code-words only
X	1	1	1	Code-hopping code-words only or seed code-words only. **(Note 1)**
1	0	0	0	Proximity activated code-hopping code words only.

Note 1: Requires certain configuration options to be set in the EEPROM.

2: If the device detects a field while a button is pressed, LC0 will be set

If, during the transmit process, it is detected that a new button(s) was added, a reset will immediately be forced and the code-word will not be completed. A new code-word will be generated and the transmission will start again. If a button is removed, it will have no effect on the code-word unless no buttons remain pressed, in which case the current code-word will be completed and the device will power down. For a detail flow diagram describing CH Mode operation, please refer to Figure 3-1.

3.1.1 HOPPING CODE-WORD DATA FORMAT

The HCS412 hopping code-word consists of 69 bits made up of several components. The first component is 32 bits of code hopping data. This is followed by fixed data stored in the EEPROM that is normally used as a serial number. At the end of the code-word is 5 status bits. Figure 3-2 shows the hopping code-word data format.

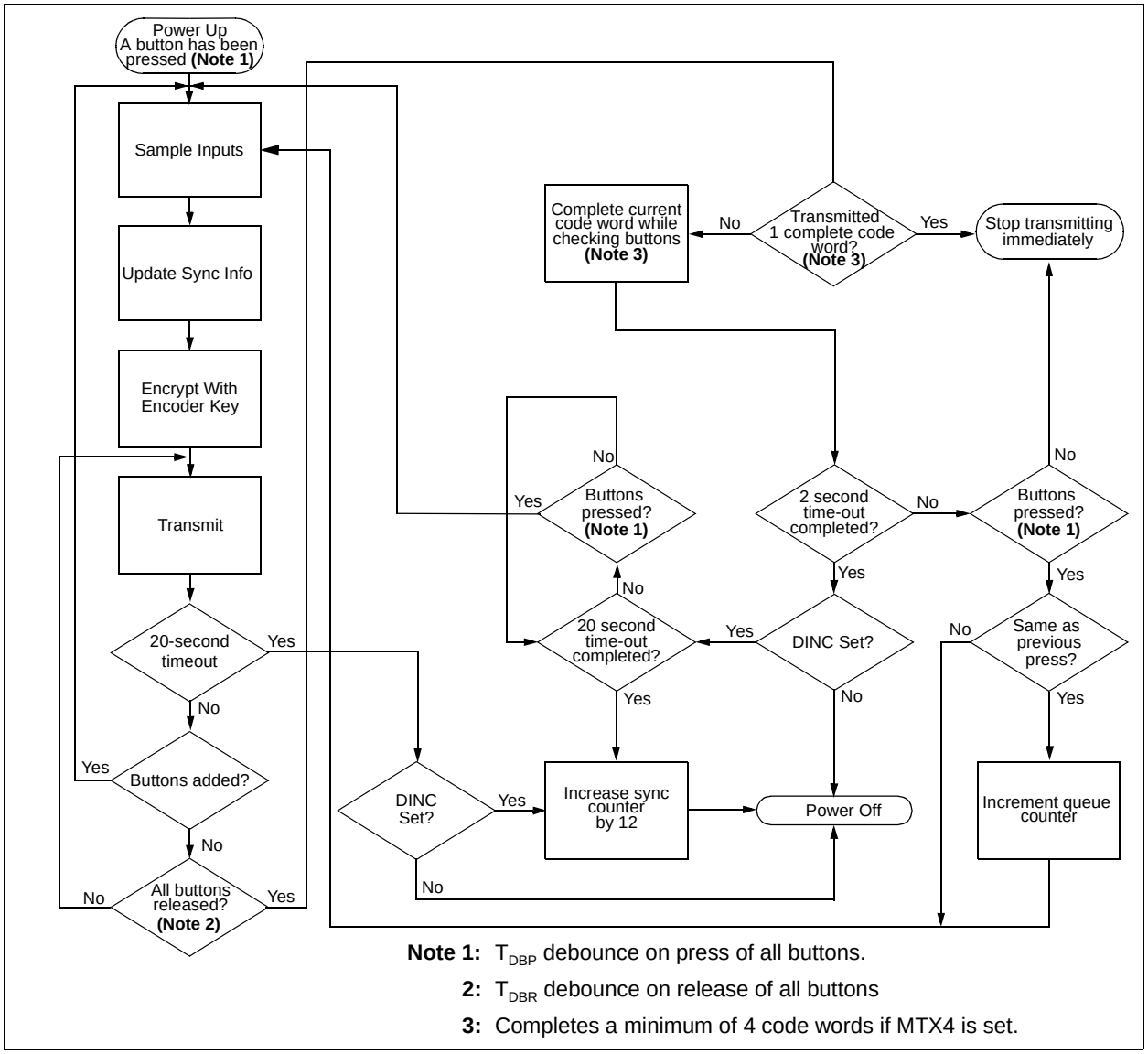
The code hopping data is generated by encrypting 32-bits of data using the Encoder Key. The data is made up of the 16-bit synchronization counter, 2 counter overflow bits, 10 discrimination bits and 4 bits indicating the status of the button and transponder inputs. These 4 bits of input status is also known as the Function Code or Button Code.

The two Counter Overflow Bits (OVR) are cleared sequentially when the synchronization counter wraps from FFFFh to 0000h. This increases the total number of possible counter values from 65535 to 196605. The 10 bit Discrimination Value (DISC) is a fixed value stored in the EEPROM

The fixed data can be either 28-bits or 32-bits depending on the Extended Serial number (XSER) configuration option. If the 28-bit option is selected, the 4 bits indicating the status of the button and transponder inputs are repeated.

The 5 status bits are made up of the Low Voltage Detector status (VLOW), a 2 bit cyclic redundancy check (CRC) and the queue counter (QUE).

FIGURE 3-1: CODE HOPPING ENCODER OPERATION

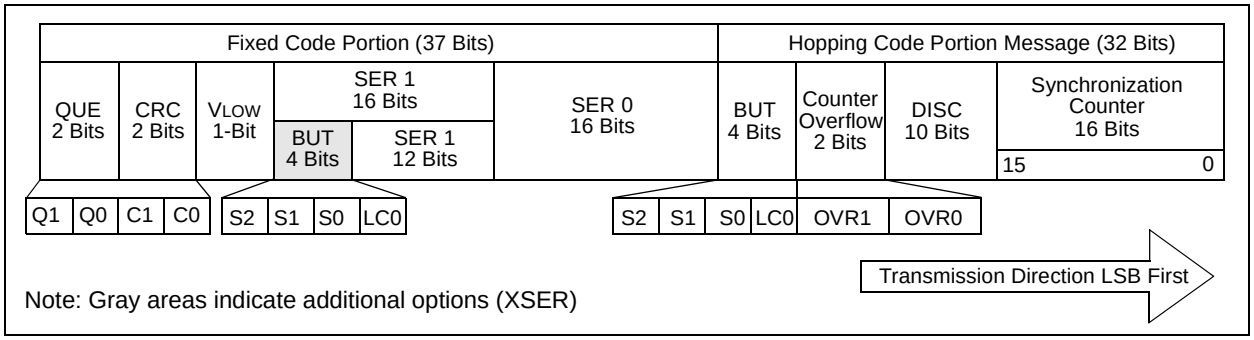


Note 1: T_{DBP} debounce on press of all buttons.

2: T_{DBR} debounce on release of all buttons

3: Completes a minimum of 4 code words if MTX4 is set.

FIGURE 3-2: CODE-WORD DATA FORMAT



Note: Gray areas indicate additional options (XSER)

3.1.1.1 LOW VOLTAGE DETECTOR STATUS (VLOW)

The low voltage detector output is transmitted in every code-word. If the V_{DD} voltage drops below the selected voltage, a '1' will be transmitted indicating that the battery is low. Under normal operation, this bit will always be set to '0'. The HCS412 samples the voltage detector output at the onset of a transmission and then just before the bit is transmitted in each code-word.

3.1.1.2 CYCLE REDUNDANCY CHECK (CRC)

The CRC bits are calculated on the 65 previously transmitted bits. The decoder can use the CRC bits to check the data integrity before processing starts. The CRC can detect all single bit and 66% of double bit errors. The CRC is computed as follows:

EQUATION 3-1: CRC CALCULATION

$$CRC[1]_{n+1} = CRC[0]_n \oplus Di_n$$

and

$$CRC[0]_{n+1} = (CRC[0]_n \oplus Di_n) \oplus CRC[1]_n$$

with

$$CRC[1,0]_0 = 0$$

and Di_n the nth transmission bit $0 \le n \le 64$

3.1.1.3 QUEUE COUNTER VALUE (QUE)

If a button is pressed, released for more than the Debounce Time (T_{DBR}), and pressed again within the Queue Time (T_{QUE}), the QUE counter is incremented. The current transmission is aborted and a new transmission is begun with the new QUE value. The queue counter is a 2-bit counter that does not wrap. These bits can be used by the decoder to perform secondary functions using only a single button, without the requirement that the decoder receive more than one completed transmission. Figure 3-3 shows the timing diagram to increment the queue counter value.

3.1.2 SEED CODE-WORD DATA FORMAT

In order to increase the level of security in a system, it is possible for the receiver to implement what is known as a secure learning function. Utilizing the seed value on the HCS412 allows the user to implement a secure learning system.

The seed code-word also consist of 69 bits, but the 32 bits of code hopping data and the 28 bits of fixed data is replaced by a 60 bit seed value stored in the EEPROM. The seed code-word format is shown in Figure 3-4.

Seed transmissions can be either disabled, enabled until the synchronization counter wraps at a 7Fh boundary, or always enabled. These options can be changed with the Seed Enable (SEED) and the Temporary Seed Enable (TMPSD) configuration options.

FIGURE 3-3: QUE COUNTER TIMING DIAGRAM

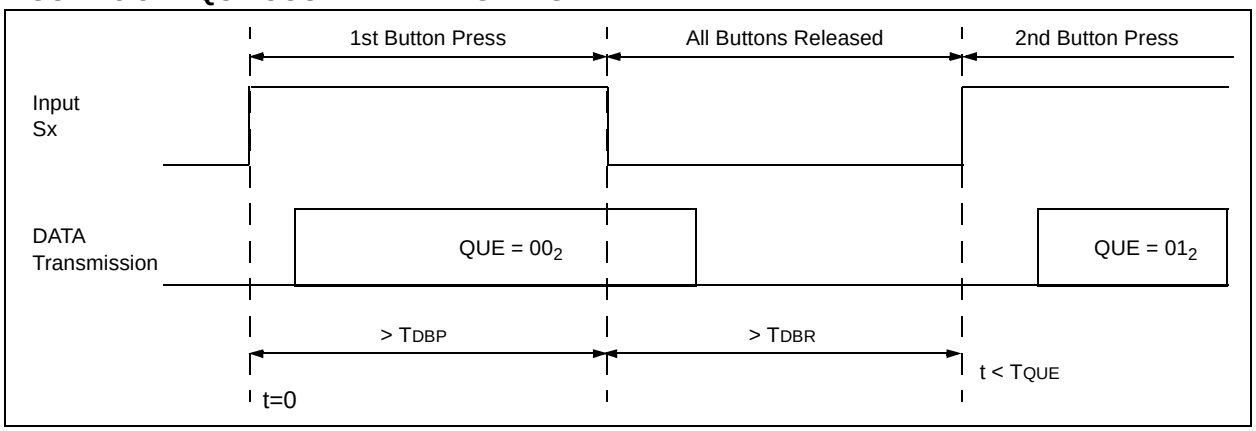
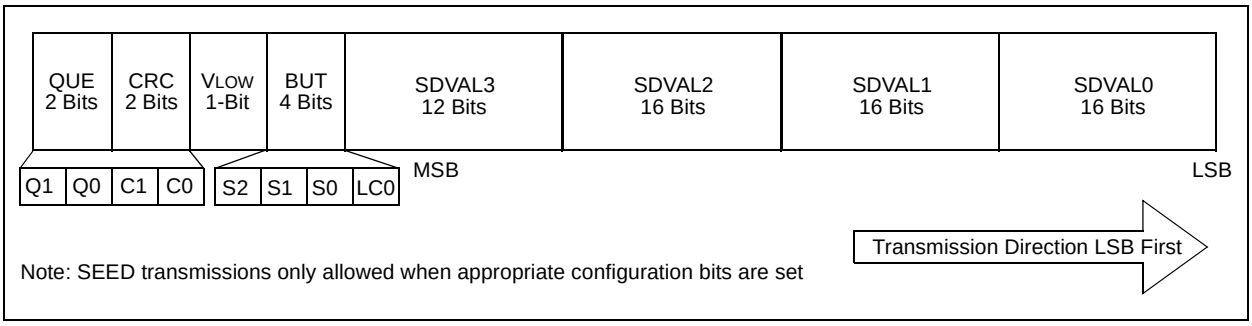


FIGURE 3-4: SEED CODE-WORD DATA FORMAT



Note: SEED transmissions only allowed when appropriate configuration bits are set

3.1.3 TRANSMISSION DATA MODULATION

The Data Modulation Format (DMF) is selectable between Pulse Width Modulation (PWM) format and Manchester encoding with the Manchester Enable (MANCH) configuration option. A preamble and synchronization header precedes the data for each code-word to allow receiver wakeup, stabilization and synchronization. The Manchester modulation format has a leading and closing '1' for each code-word. (Start bit and Stop bit)

The same code-word is continuously sent as long as the input pins are kept high, a timeout has not occurred or a delayed seed transmission is not activated. A guard time separates the code-words. All of the timing values are in multiples of a Basic Timing Element (RFTE), which can be changed, using the Transmission Baud Rate (RFBSL) configuration option. The modulation formats are shown in Figure 3-5 and Figure 3-6.

FIGURE 3-5: PWM TRANSMISSION FORMAT—MANCH = 0

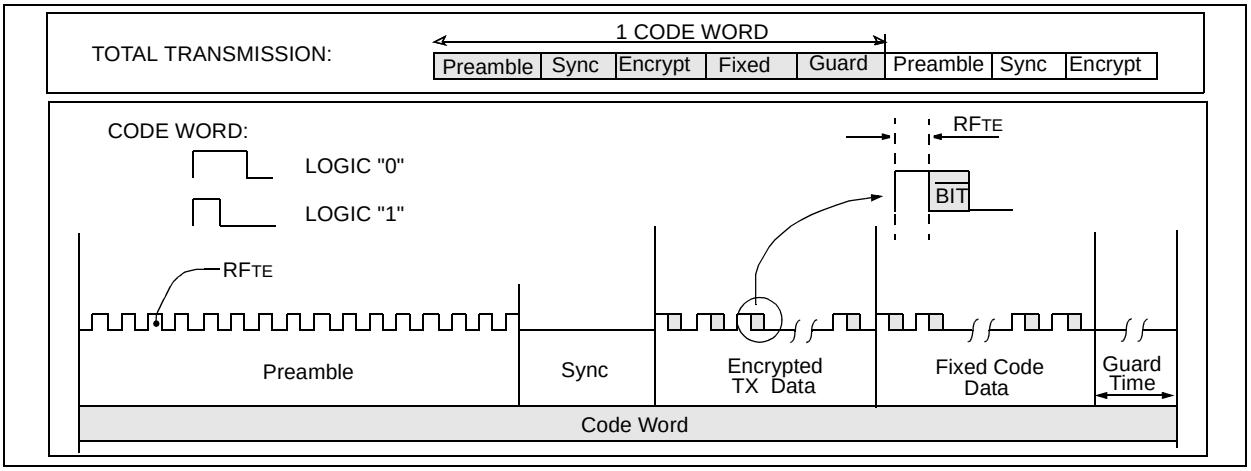


FIGURE 3-6: MANCHESTER TRANSMISSION FORMAT—MANCH = 1

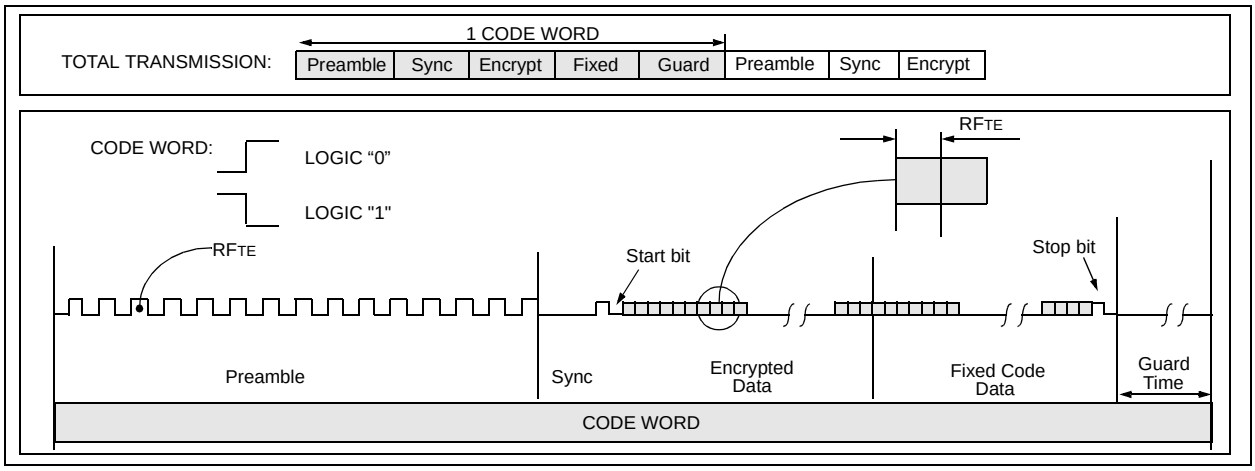


TABLE 3-1: CH MODE TIMING SPECIFICATIONS

V_{DD} = +2.0 to 6.6V Commercial (C): T_{AMB} = 0°C to +70°C Industrial (I): T_{AMB} = -40°C to +85°C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remarks**
Time to second button press	T_{BP}	44 + Code Word Time	58 + Code Word Time	63 + Code Word Time	ms	**Note 1**
Transmit delay from button detect	T_{TD}	20	30	40	ms	**Note 2**
Debounce delay on button press	T_{DBP}	14	20	26	ms	
Debounce delay on button release	T_{DBR}		20		ms	
Auto-shutoff time-out period	T_{TO}	18	20	22	s	**Note 3**
Long preamble	T_{LPRE}		64		ms	
LED on time	T_{LEDON}		32		ms	**Note 4**
LED off time	T_{LEDOFF}		480		ms	**Note 4**
LED on time (V_{DD} < V_{LOW} Trip Point)	T_{LEDL}		200		ms	**Note 5**
Time to delayed SEED transmission	T_{DSD}		3		s	
Queue Time	T_{QUE}		30		ms	

Note 1: T_{BP} is the time in which a second button can be pressed without completion of the first code word where the intention was to press the combination of buttons.
2: Transmit delay maximum value, if the previous transmission was successfully transmitted.
3: The auto-shutoff timeout period is not tested.
4: The LED times specified for V_{DD} > V_{TRIP} specified by V_{LOW} in the configuration word.
5: LED on time if V_{DD} < V_{TRIP} specified by V_{LOW} in the configuration word.

The HCS412 has the option to increase the first preamble transmission time. The Long Preamble Enable (LPRE) configuration option will extend the first preamble to a Long Preamble Time (T_{LPRE}). The long preamble is transmitted before the first code-word to wakeup and stabilize the receiver circuit. The long preamble will be a square wave at the selected Timing Element (RF_{TE}).

3.1.4 CODE-WORD COMPLETION AND MINIMUM CODE-WORDS

Code-word completion is an automatic feature that ensures that at least one code-word is transmitted, even if the button input is removed before the code-word is completed. The HCS412 will complete the first code-word that is transmitted and then powers itself down after the command is finished. In addition, this feature can be extended so that a minimum of 4 code words is completed. This is done by setting the Minimum Four Code-words (MTX4) configuration option.

3.1.5 AUTO-SHUTOFF

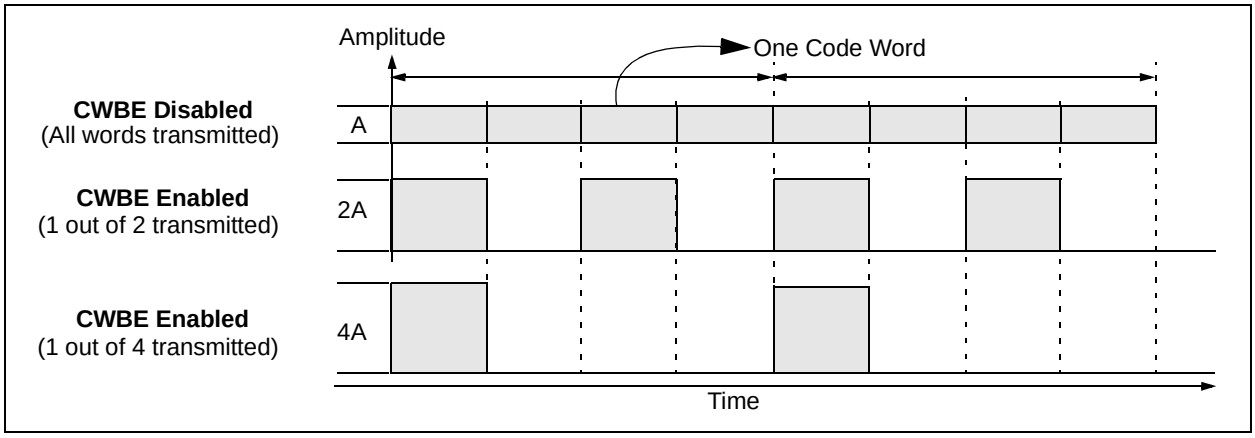
The Auto-shutoff function automatically stops the device from transmitting when a button inadvertently gets pressed for a long period of time. This will prevent the device from draining the battery when a button gets pressed while the transmitter is in a pocket or purse. The device will power itself down after the time-out period (T_{TO}) has expired. Total current consumption will then be reduced to the leakage across the internal pull-down resistors on the stuck button.

3.1.6 CODE-WORD BLANKING ENABLE

Federal Communications Commission Rules, Part 15 specify the limits on fundamental power and harmonics that can be transmitted. Power is calculated on the worst case average power transmitted in a 100ms window. It is therefore advantageous to minimize the duty cycle of the transmission. This can be achieved by blanking out consecutive code-words as can be seen in Figure 3-7.

The Code-word Blanking Enable (CWBE) configuration option is used for reducing the average power of a transmission. Using this option allows the user to transmit a higher amplitude transmission, if the duty cycle is lower. The HCS412 will either transmit all code-words, every second code-word or every fourth code-word, depending on the Transmission Baud Rate (RFBSL) configuration option.

FIGURE 3-7: CODE-WORD BLANKING



3.1.7 DELAYED INCREMENT

The HCS412 has a Delayed Increment (DINC) feature that increments the synchronization counter by 12 after the timeout (TTO) period expires, for additional security. If a button is released before the timeout time has elapsed, the HCS412 will stop transmitting, but the device will remain powered until the timeout period expires. The device will then increment the synchronization counter by 12 before it powers down. If another press occurs during this wait time, the timeout counter will reset and the queue counter will increment. The queue counter is cleared after the buttons have been released for more than the queue time (TQUE).

3.1.8 PLL INTERFACE

If the RFEN/S2/LC1 pin is configured as an RF enable output, the behavior of this pin in conjunction with the DATA pin can be changed to enable either ASK or FSK when interfacing to a PLL. The PLL Interface (AFSK) configuration option controls the output as shown in Figure 3-8.

3.1.9 LED OUTPUT

When the HCS412 is transmitting data, the LED pin will be driven low periodically as demonstrated in Figure 3-9. If the low voltage detector indicates that the VDD level is lower than the preset value, the LED pin will be driven low only once for a longer period of time as shown in Figure 3-9.

FIGURE 3-8: RF ENABLE/ASK/FSK OPTIONS

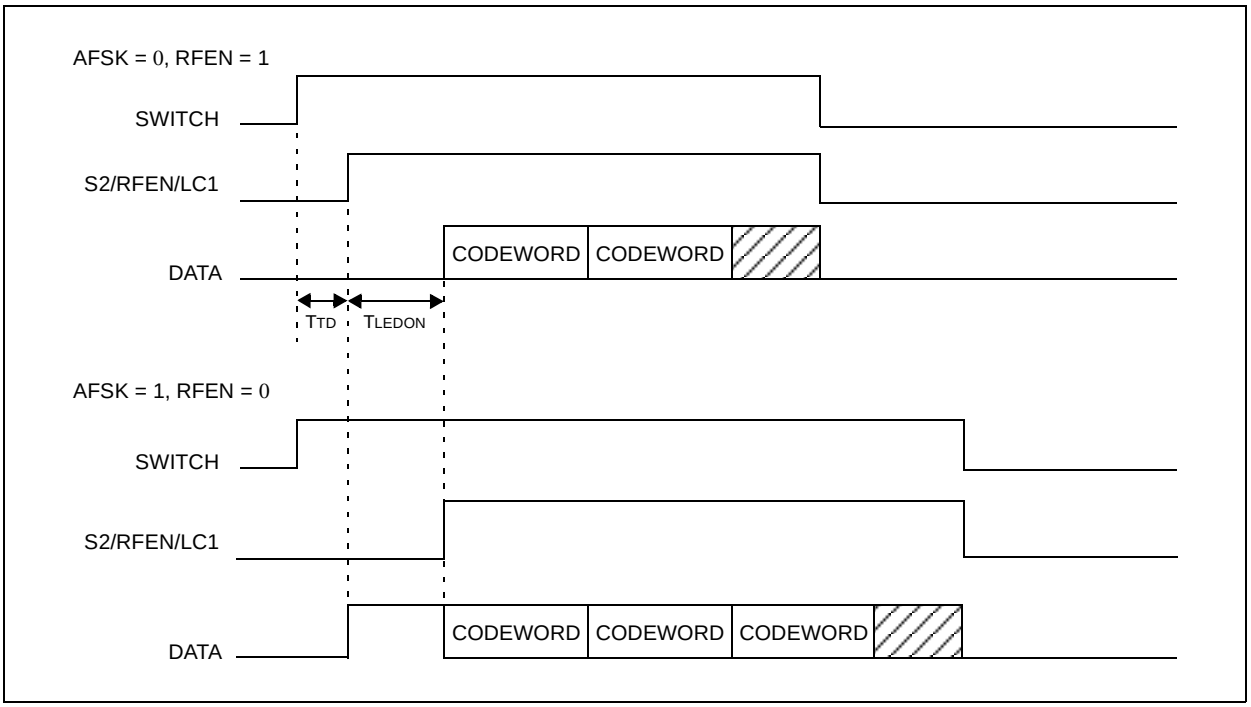
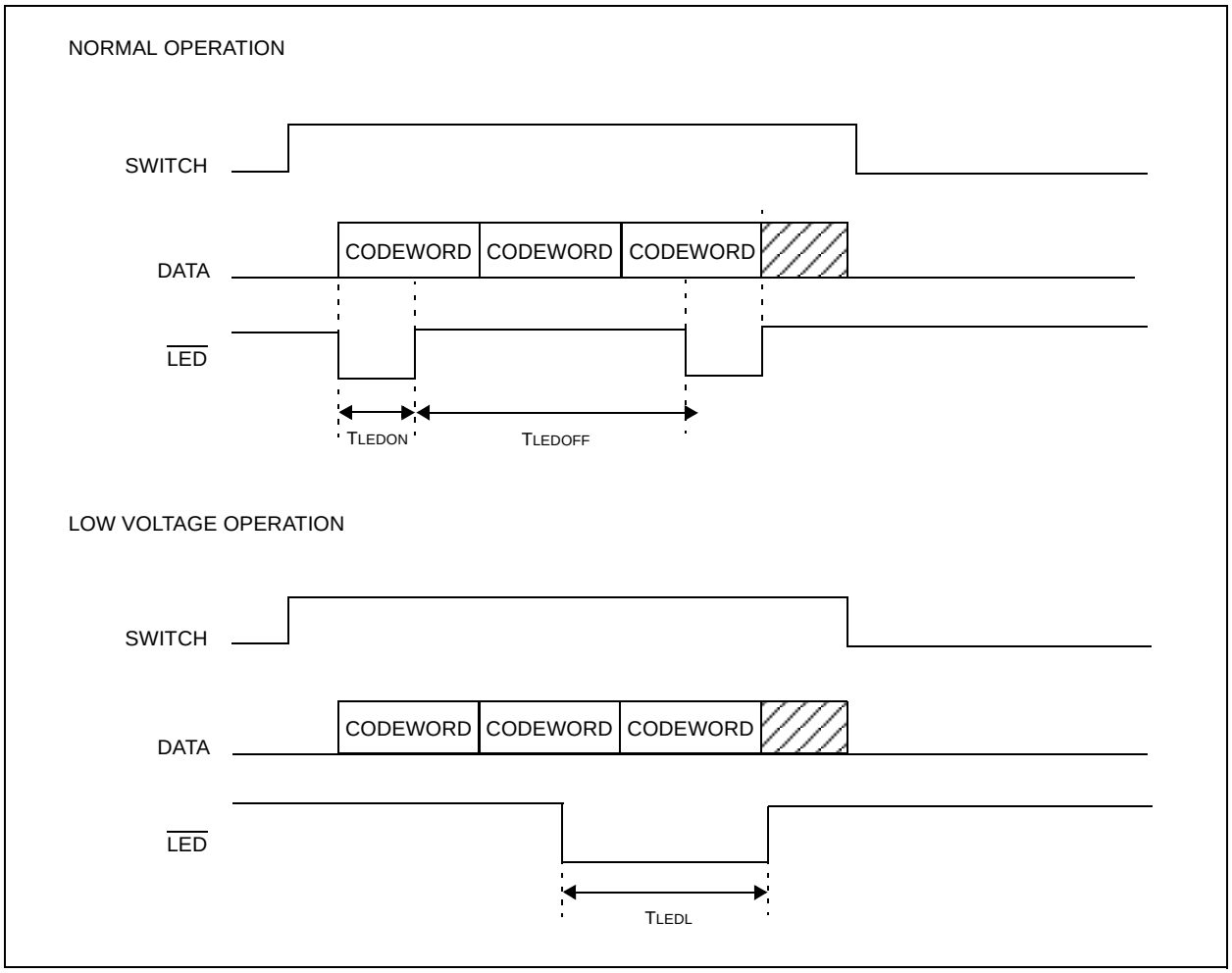


FIGURE 3-9: LED OPERATION



3.1.10 SPECIAL FEATURES

The HCS412 has a Special Feature (QLVS) configuration option that if set enables the following options:

- Reduces the time (T_{DSD}) before a delayed seed transmission starts
- Disables data transmission on the DATA pin when the LED pin is driven low. If the PLL Interface option is set to ASK, the data pin will be driven low when the LED is also driven low. If the PLL Interface option is set to FSK, the DATA pin will be driven high and the RFEN output will be driven low. If the battery is low, the HCS412 will only transmit until the LED goes on.

Please refer to Figure 3-10 for detail waveforms.

- Latches the output of the low voltage detector the first time it drops below the preset value. Once it is latched, the HCS412 will use this latched value until the battery is removed. In order to ensure that the latch is cleared, the HCS412 must be activated without the battery connected to discharge all internal and external capacitors before the power is applied again
- Allows the disabling of seed code-words with a special button sequence. If the Temporary Seed Enable (TMPSD) option is set, the seed transmission can be disabled by applying the button sequence shown in Figure 3-11

FIGURE 3-10: LED, DATA, RFEN INTERACTION WHEN QLVS IS SET

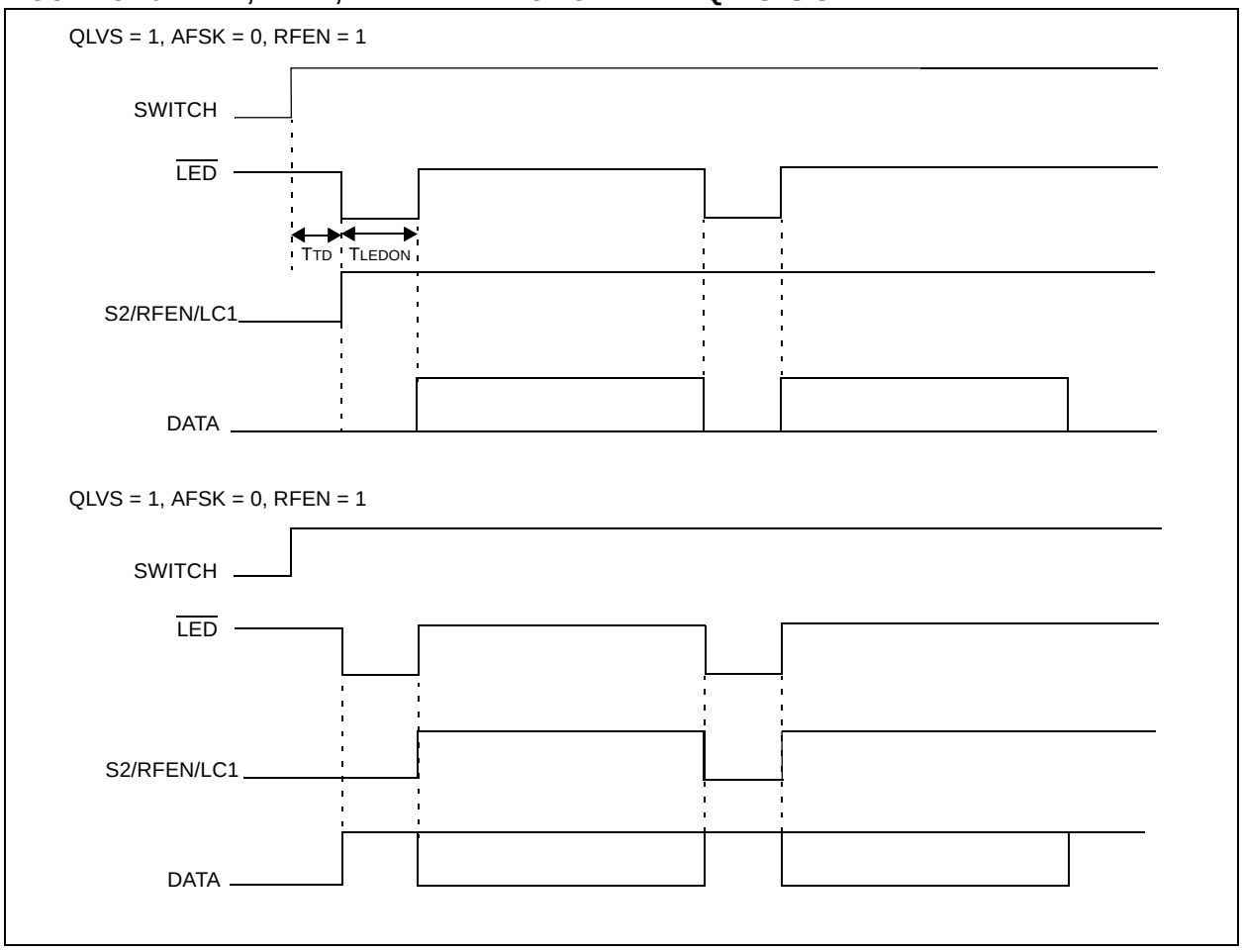
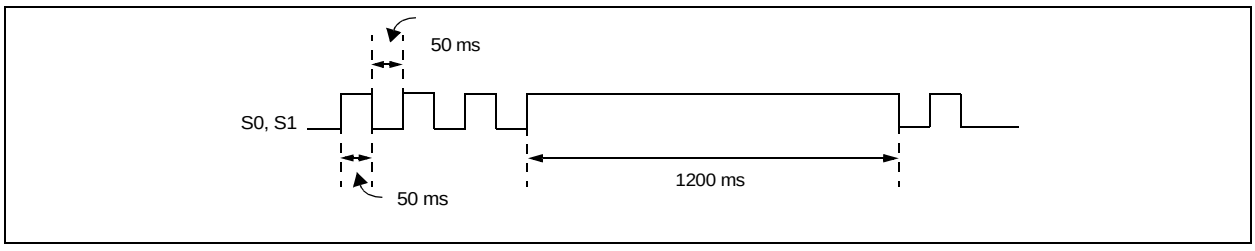


FIGURE 3-11: SEED DISABLE WAVEFORM



3.2 IFF Mode

In IFF Mode, the HCS412 functions as token or transponder with bi-directional communication capabilities. This mode allows a decoder to send commands and data to the HCS412, with the HCS412 then responding to the commands. This allows the user to perform:

- A bi-directional challenge and response sequence for IFF validation. There are two different encryption algorithms and two encoder keys that can be used to perform an IFF validation
- Reading of selected areas in the EEPROM
- Writing to selected areas in the EEPROM
- Incrementing the synchronization counter and generating the hopping portion of a code hopping transmission
- Proximity Activation of CH Mode

The HCS412 will enter IFF mode when it detects a signal on the LC0 pin. The device will respond by giving acknowledge pulses after the power up time (T_{PU}). This indicates that the HCS412 is in IFF Mode and is ready to receive commands. The HCS412 can respond on both the LC pin as well as the DATA pin, depending on the device configuration.

3.2.1 IFF COMMUNICATION DATA FORMAT

Depending on the command, the data to the HCS412 and the response will have a different format. Data to and from the HCS412 is send LSB first. All read and write data contains 16-bits of data. All challenge and response data is 32 bits long.

Responses on the DATA pin have the standard CH Mode format with the 32-bit hopping portion replaced by the response data. If the response is only 16-bits, the 32-bits will contain 2 copies of the response. The data format is shown in Figure 3-12.

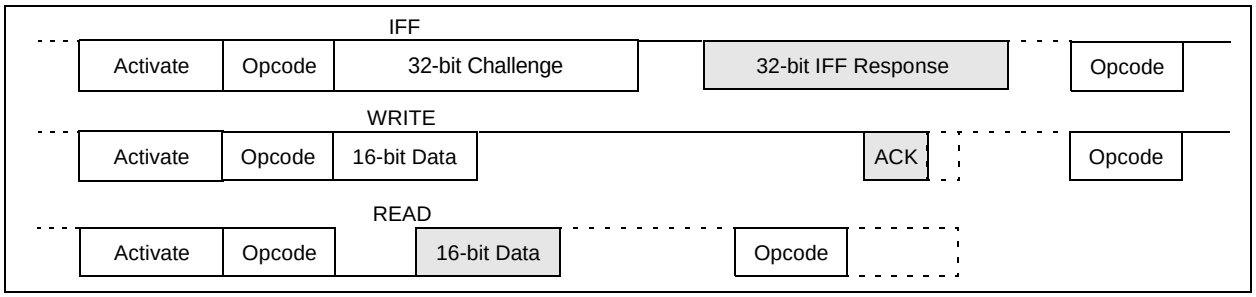
3.2.1.1 IFF READ

The decoder must send a read command indicating the 16-bit word to be read. Each read command is followed by a 16-bit data response. The areas open for reading are:

- The 64-bit general purpose user EEPROM. (USER[0:3])
- The 32-bit serial number (SER[0:1]). This is the same data transmitted in the fixed code portion of the CH Mode code-word
- A 16 bit configuration word containing all the non-security related configuration options. The configuration word is at address 080h-08Fh

Please refer to Section 4.0 for the configuration word format.

FIGURE 3-12: OVERVIEW OF IFF OPERATION



3.2.1.2 IFF WRITE

The decoder can write to the same areas that are readable. To write to the general purpose user EEPROM, the decoder first sends a command indicating what the area is to be written. This is followed by the 16-bit value that the decoder wants to write. The HCS412 will write the values into the EEPROM and respond with an acknowledge pulse when the writing was successful.

To prevent accidental change of the serial number and configuration word, these locations are protected by a Transport Code. The decoder will therefore give the command followed by a 28-bit transport code and then the 16-bits of data to write. The HCS412 will again acknowledge when the write is complete.

The response time will vary depending on the number of bits changed.

3.2.1.3 IFF CHALLENGE RESPONSE

The decoder must send a command indicating which encryption algorithm and which key the HCS412 must use to encrypt the challenge. The second encoder key and the seed value transmitted in CH Mode seed transmissions occupy the same area in the EEPROM. Therefore, in order to use the second encoder key for IFF, the Seed Enable (SEED) and the Temporary Seed Enable (TMPSD) configuration options must be set. This will disable seed transmissions and prevent the second key being transmitted in CH Mode. If this is not done, KEY1 will always be used for IFF.

After the command, the decoder must send the 32-bit challenge. The HCS412 will encrypt the challenge using the selected algorithm and encoder key and

respond with 32-bits of data. The decoder can then compare this data with the expected value to validate the encoder.

3.2.1.4 IFF HOP

After receiving this command, the HCS412 will increment the counter and build the 32-bit code hopping portion of a code hopping code-word. The data format will be the same as described in Section 3.1.1.

3.2.2 IFF COMMUNICATION MODULATION

All communication to and from the HCS412 over the transponder path uses a Basic Timing Element (LFTE). This value can be set to either 100 µs or 200 µs depending on the value of the IFF Baud Rate Select (LFBSL) configuration options. The response over the DATA pin uses the CH Mode Basic Timing Element (RFTE) and the modulation format set by the Manchester Enable (MANCH) option.

The decoder initiates each transaction by sending a command and data to the HCS412. If the HCS412 does not receive a command within 255 LFTE's, the HCS412 will repeat the acknowledge pulses. Commands are initiated by a start signal of 2 LFTE. The data is Pulse Position Modulated (PPM) as shown in Figure 3-13. The input signal should remain high for 6 LFTE's after the last bit is transmitted.

Data response by the HCS412 is started by a pulse of 1 LFTE. This is followed by a 01b before the data start. The data is also PPM format as shown in Figure 3-13. For detail waveforms and timing of the different commands, please refer to Figure 3-14.

FIGURE 3-13: MODULATION FOR IFF COMMUNICATION

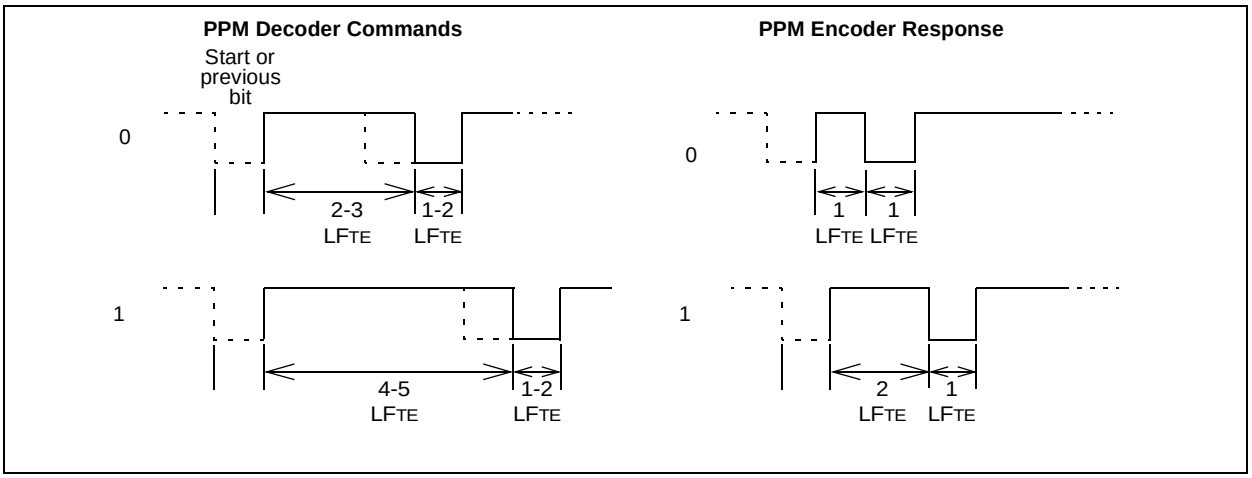


FIGURE 3-14: DECODER IFF COMMANDS AND WAVEFORMS

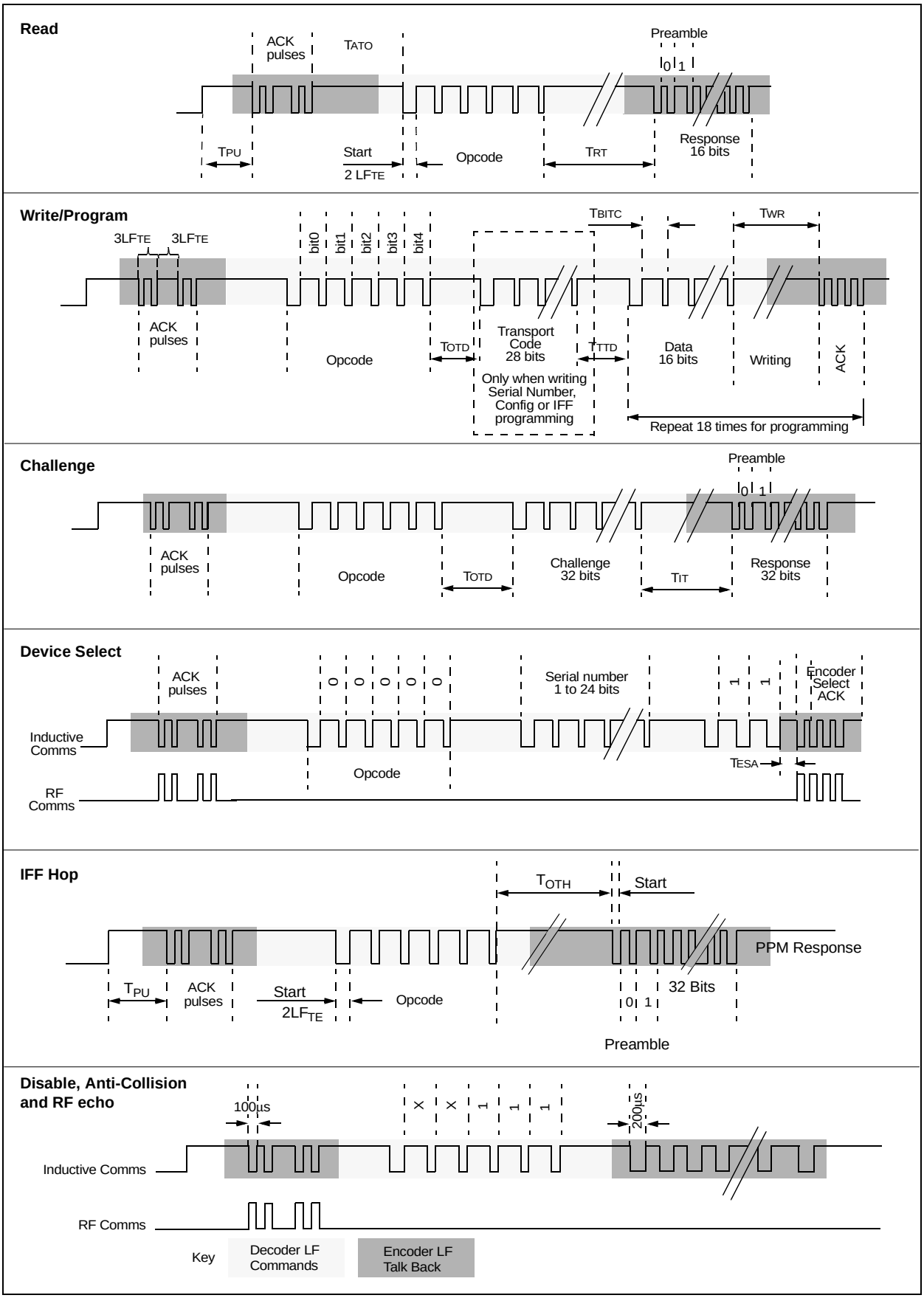


TABLE 3-1: IFF TIMING PARAMETERS

Parameter	Symbol	Min.	Typ.	Max.	Units
Time Element IFFB = 0 IFFB = 1	LFTE	— —	200 100	— —	µs
Power Up Time	TPU	—	6	—	ms
Acknowledge to Opcode Time IFFB = 0 IFFB = 1	TATO	2.6 1.3	— —	— —	ms
PPM Command Bit Time Data = 1 Data = 0	TBITC	3.5 5.5	4 6	— —	LFTE
PPM Response Bit Time Data = 1 Data = 0	TBITR	— —	2 3	— —	LFTE
Read Response Time IFFB = 0 IFFB = 1	TRT	— —	2.6 1.8	— —	ms
IFF Response Time	TIT	—	4.3	—	ms
Opcode to Data Input Time	TOTD	2.6	—	—	ms
Transport Code to Data Input Time	TTTD	2.2	—	—	ms
Encoder Select Acknowledge Time	TESA	—	LFTE+100	—	µs
IFF EEPROM Write Time (16 bits)	TWR	—	30	—	ms
Op Code to Hop Code Response Time	TOTH	—	114	—	ms

3.2.3 ANTI-COLLISION

When multiple transponders are in the same inductive field, all the transponders will respond to the commands simultaneously. This will cause collision of the responses making it impossible for the decoder to communicate with any one of the encoders in the field. Anti-Collision prevents this from happening by addressing each encoder individually. Anti-collision must be enabled by setting the Anti-Collision Enable (ACOLI) configuration option.

To address an individual encoder, the decoder needs to send a ‘select encoder’ command to the HCS412. This is followed by 1 to 24 bits of the HCS412's serial number, starting with bit 3 of the serial number (SER). The decoder then sends out a string of PPM 1’s to address bits 0 to 2. The first ‘1’ sent, sets the 3 LSB’s of the serial number to 000, the second to 001 and so on.

If the resultant serial number transmitted matches the HCS412’s serial number, the HCS412 will respond with an encoder select acknowledge pulse. The remaining encoders in the field will not respond to any subsequent commands.

3.2.4 PASSIVE PROXIMITY ACTIVATION

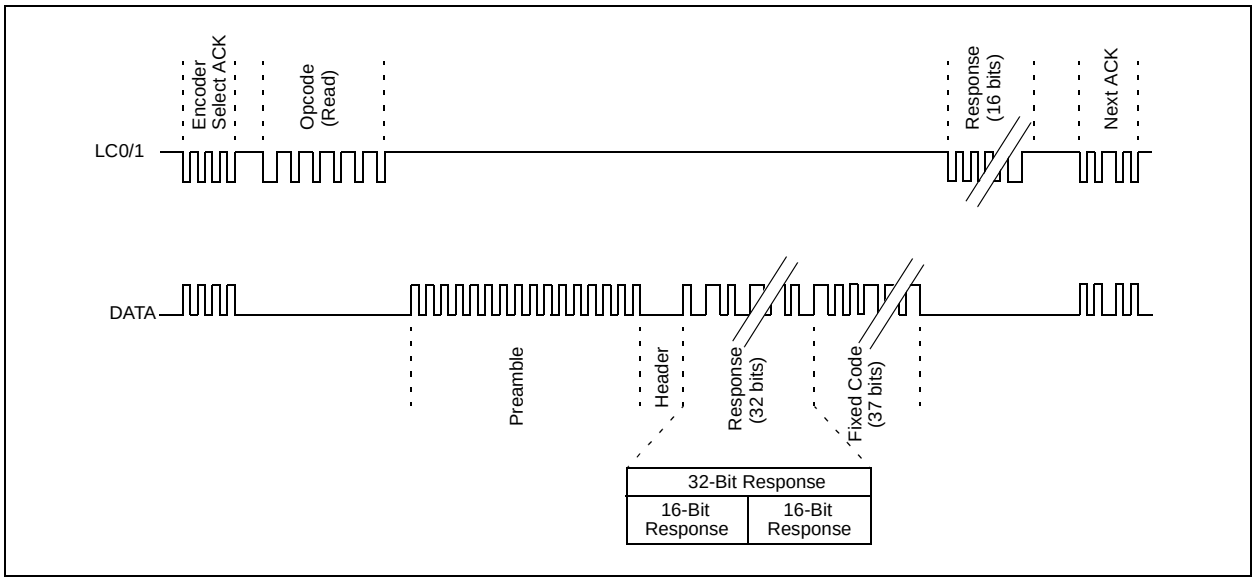
If the Proximity Activation Enable (PXMA) configuration option is set, the HCS412 will transmit a hopping code transmission when a signal is present on the LC0 pin.

In this mode, the HCS412 sends out ACK pulses on the LC lines. If the HCS412 doesn't receive a command after the first set of acknowledge pulses [within 255 LFte‘s], the HCS412 will transmit a normal code hopping transmission for 2 seconds on the DATA pin. The function code during this transmission will indicate that it was a field induced transmission.

3.2.5 TRANSPONDER IN/RF OUT

If both the Proximity Activation Enable (PXMA) and the Anti-Collision Enable (ACOLI) options are set, the data response is echoed on the DATA output line. After transmitting the data on the DATA line, the data is then transmitted on the LC pins, as indicated in Figure 3-15.

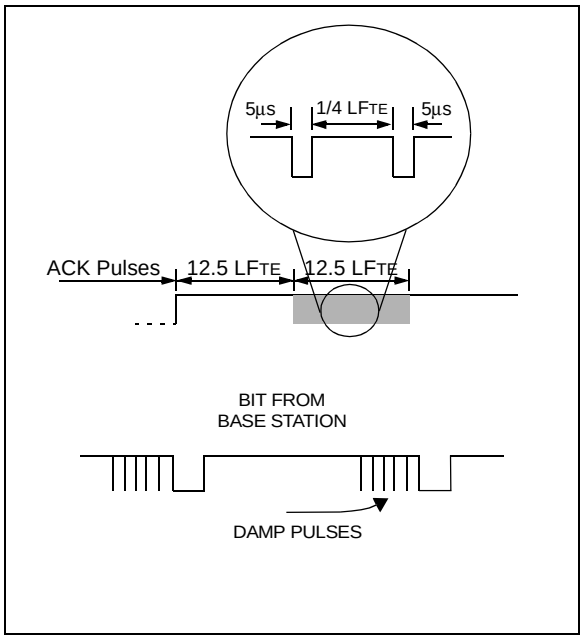
FIGURE 3-15: RF ECHO WAVEFORM AND CODE WORD FORMAT



3.2.6 INTELLIGENT DAMPING

If the LC circuit on the transponder has a high Q-factor, the circuit will keep resonating for a long time after the reader shut down the field. This makes fast communication from the reader to the HCS412 difficult. If the Intelligent Damping Enable (IDAMP) configuration option is enabled, the HCS412 will clamp the LC pins for 5 µs every 1/4 LFTE, whenever the HCS412 is expecting data from the decoder. The intelligent damping pulses start 12.5 LFTE after the acknowledge pulses have been sent and continue for 12.5 LFTE. If the HCS412 detects data from the base station while sending out damping pulses, the damping pulses will continue to be sent.

FIGURE 3-16: INTELLIGENT DAMPING OPTION



3.2.7 ENABLE DEFAULT IFF COMMUNICATION

This command allows the decoder to disable all special features when communicating to the HCS412. This means that the transponder has anti-collision disabled, RF echo disabled and the transponder is working at the slow IFF baud rate.

3.3 IFF Commands

TABLE 3-2: LIST OF IFF COMMANDS

Command	Description	Expected data In	Response
00000	Select HCS412, used if Anticollision enabled	1 to 24 bits of the serial number (SER)	Encoder select acknowledge if serial number match
00001	Read configuration word	None	16-bit configuration word
00010	Read low serial number	None	Lower 16 bits of serial number (SER0)
00011	Read high serial number	None	Higher 16 bits of serial number (SER1)
00100	Read user EEPROM 0	None	16 Bits of User EEPROM USR0
00101	Read user EEPROM 1	None	16 Bits of User EEPROM USR1
00110	Read user EEPROM 2	None	16 Bits of User EEPROM USR2
00111	Read user EEPROM 3	None	16 Bits of User EEPROM USR3
01000	Program HCS412 EEPROM	Transport code (28 bits); Complete memory map: 18 x 16 bit words (288 bits)	Write acknowledge pulse after each 16-bit word, 288 bits transmitted in 18 bursts of 16-bit words
01001	Write configuration word	Transport code (28 bits); 16 Bit configuration word	Write acknowledge pulse
01010	Write low serial number	Transport code (28 bits); Lower 16 bits of serial number (SER0)	Write acknowledge pulse
01011	Write high serial number	Transport code (28 bits); Higher 16 bits of serial number (SER1)	Write acknowledge pulse
01100	Write user EEPROM 0	16 Bits of User EEPROM USR0	Write acknowledge pulse
01101	Write user EEPROM 1	16 Bits of User EEPROM USR1	Write acknowledge pulse
01110	Write user EEPROM 2	16 Bits of User EEPROM USR2	Write acknowledge pulse
01111	Write user EEPROM 3	16 Bits of User EEPROM USR3	Write acknowledge pulse
10000	IFF1 using key-1 and IFF algorithm	32-Bit Challenge	32-Bit Response
10001	IFF1 using key-1 and HOP algorithm	32-Bit Challenge	32-Bit Response
10100	IFF2 32-bit using key-2 and IFF algorithm	32-Bit Challenge	32-Bit Response
10101	IFF2 32-bit using key-2 and HOP algorithm	32-Bit Challenge	32-Bit Response
11000	Increments the counter and generates a hopping code portion for a transmission	None	32-Bit Hopping Code
11100-11111	Disable anticollision, RF echo and sets to slow IFF baud rate	None	Data in the user EEPROM given by the 2 LS bits of the op code

4.0 EEPROM ORGANIZATION

The 288-bit HCS412 EEPROM is organized in 18 words of 16 bits each. A complete description of the HCS412 memory map can be found in table below. For Programming of the HCS412, please refer to the Programming Specification or contact your local FAE.

TABLE 4-1: HCS412 EEPROM ORGANIZATION

Address (hex)	Symbol	Description		
000 – 03F	KEY1	64 bit Encoder Key 1		
040 – 07B	SDVAL	60 bit seed value transmitted in CH Mode.	SEED = 1 SEED = 0	TMPSD = 0 TMPSD = 1
	KEY2	LSB 60 bits of Encoder Key 2. The MSB 4 bits are set to XXXX	SEED = 1	TMPSD = 1
	TRNS	28 bit Transport Code stored at 060h – 07Bh		
07C	AFSK	PLL Interface Select.	ASK = 0	FSK = 0
07D	RFEN	RF Enable output active.	Disable = 0	Enable = 1
07E	LPRE	Long Preamble Enable.	Disable = 0	Enable = 1
07F	QLVS	Special Features Enable.	Disable = 0	Enable = 1
080 – 083	OSCT	Oscillator Tune Value.	1000b	Fastest
			0000b	Nominal
			0111b	Slowest
084	VLOWSEL	Low Voltage Trip Point Select	2.2 Volt = 0	4.4 Volt = 1
085	IDAMP	Intelligent Damping Enable	Disable = 1	Enable = 0
086	ACOLI	Anti-Collision Enable (**Note 1**)	Disable = 0	Enable = 1
087	PXMA	Proximity Activation Enable (**Note 1**)	Disable = 0	Enable = 1
088	IFFB	IFF Baud Rate Select (LFTE)	200 us = 0	100 us = 1
089	MANCH	Manchester Enable	PWM = 0	Manch = 1
08A	CWBE	Code-word Blanking Enable	Disable = 0	Enable = 1
08B	MTX4	Minimum Four Code-words	Disable = 0	Enable = 1
08C – 08D	RFBSL	Transmission Baud Rate (RFTE)	Value	PWM / Manch
			00b	400 us / 800 us
			01b	200 us / 400 us
			10 b	100 us / 200 us
			11 b	100 us / 200 us
08E	S2LC	S2/RFEN/LC1 Pin Configuration bit.	LC = 0	S Input = 1
08F	—	Reserved, Set to 0	—	—
090	TMPSD	Temporary Seed Enable (**Note 2**)	Disable = 0	Enable = 1
091	SEED	Seed Transmission Enable (**Note 2**)	Disable = 0	Enable = 1
092	XSER	Extended Serial number	Disable = 0	Enable = 1
093	DINC	Delayed Increment	Disable = 0	Enable = 1
094 – 09D	DISC	10 bit Discrimination value		
09E – 09F	OVR	Counter Overflow Value		
0A0 – 0BF	SER	32 bit Serial Number		
0C0 – 0FF	USR	64 bit user EEPROM area		
100 – 10F	CNT	16 bit Synchronization counter		
110 – 11F	—	Reserved set 0000h		

Note 1: If ACOLI = 1 and PXMA = 1, the RF echo feature is enabled (Section 3.2.5).
2: If TMPSD = 1 and SEED = 1, IFF with KEY2 is enabled.

5.0 ELECTRICAL CHARACTERISTICS

TABLE 5-1: ABSOLUTE MAXIMUM RATING

Symbol	Item	Rating	Units
V_{DD}	Supply voltage	-0.3 to 6.6	V
V_{IN}*	Input voltage	-0.3 to V_{DD} + 0.3	V
V_{OUT}	Output voltage	-0.3 to V_{DD} + 0.3	V
I_{OUT}	Max output current	50	mA
T_{STG}	Storage temperature	-55 to +125	C **(Note)**
T_{LSOL}	Lead soldering temp	300	C **(Note)**
V_{ESD}	ESD rating (Human Body Model)	4000	V

Note: Stresses above those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device.

* If a battery is inserted in reverse, the protection circuitry switches on, protecting the device and draining the battery.

TABLE 5-2: DC AND TRANSPONDER CHARACTERISTICS

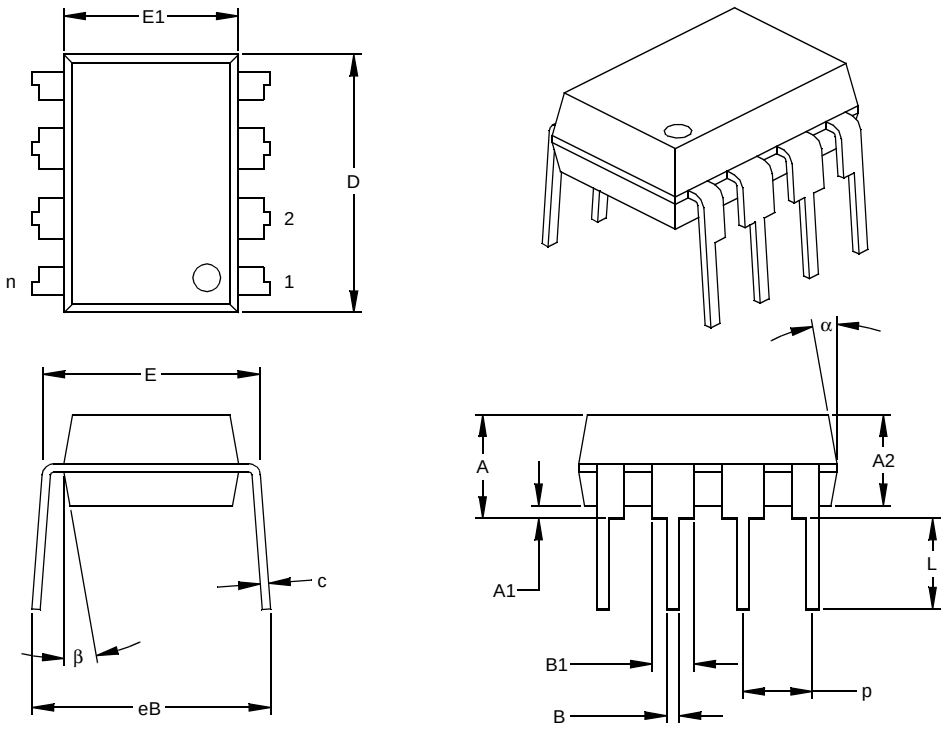
Commercial (C): T_{AMB} **= 0°C to 70°C**
Industrial (I): T_{AMB} **= -40°C to 85°C**

Parameter	Symbol	2.0V < V_{DD} < 6.3V			Unit	Conditions
		Min	Typ[1]	Max		
Average operating current **Note 2**	I_{DD} (avg)	—	50 200	100 300	µA	V_{DD} = 3.0V V_{DD} = 6.3V
Programming current	I_{DDP}	—	1.0 2.3	2.0 4.0	mA	V_{DD} = 3.0V V_{DD} = 6.3V
Standby current	I_{DDS}	—	0.1	100	nA	LC = off else < 5µA
High level input voltage	V_{IH}	0.55 V_{DD}	—	V_{DD} + 0.3	V	
Low level input voltage	V_{IL}	-0.3	—	0.15 V_{DD}	V	
High level output voltage	V_{OH}	0.8 V_{DD} 0.8 V_{DD}	—	—	V	V_{DD} = 2V, I_{OH} =- .45 mA V_{DD} = 6.3V, I_{OH},= -2 mA
Low level output voltage	V_{OL}	— —	— —	0.08 V_{DD} 0.08 V_{DD}	V	V_{DD} = 2V, I_{OH} = 0.5 mA V_{DD} = 6.3V,I_{OH} = 5mA
LED output current	I_{LED}	3.0	4.0	7.0	mA	V_{DD} = 3.0V, V_{LED} = 1.5V
Switch input resistor	R_S	40	60	80	kΩ	S0/S1 not S2
DATA input resistor	R_{DATA}	80	120	160	kΩ	
LC input current	I_{LC}	—	—	10.0	mA	V_{LCC}=10 V_{P-P}
LC input clamp voltage	V_{LCC}	—	10	—	V	I_{LC} <10 mA
LC induced output current	V_{DDI}	—		2.0	mA	V_{LCC} > 10V
LC induced output voltage	V_{DDV}	— —	4.5 4.0	— —	V	10 V < V_{LCC}, I_{DD} = 0 mA 10 V < V_{LCC}, I_{DD} = -1 mA
Carrier frequency	fc	—	125		kHz	
LC input sensitivity	V_{LCS}	—	100	—	mVp-p	**Note 3**

Note 1: Typical values at 25°C.
2: No load connected.
3: Not tested.

6.0 PACKAGING INFORMATION

Package Type: 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

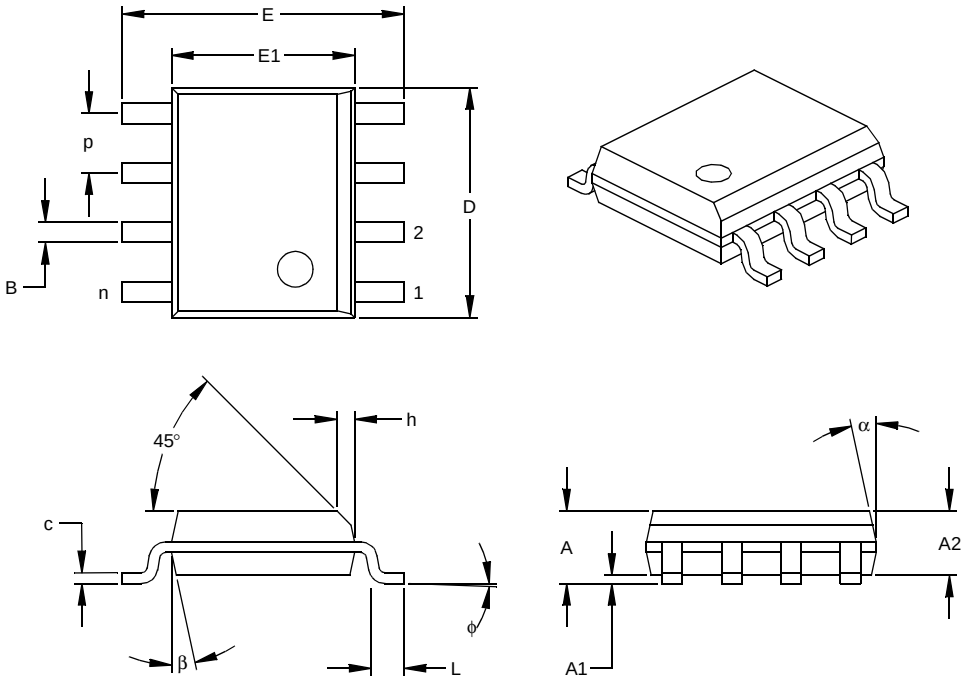


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

Package Type: 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



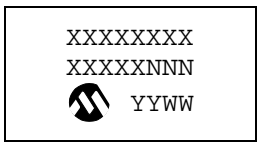
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

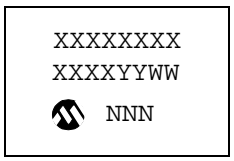
6.1 Package Marking Information

8-Lead PDIP (300 mil)



Example

8-Lead SOIC (150 mil)



Example

Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard marking consists of Microchip part number, year code, week code and traceability code. For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For SQTP devices, any special marking adders are included in SQTP price.

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp://ftp.microchip.com

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

Systems Information and Upgrade Hot Line

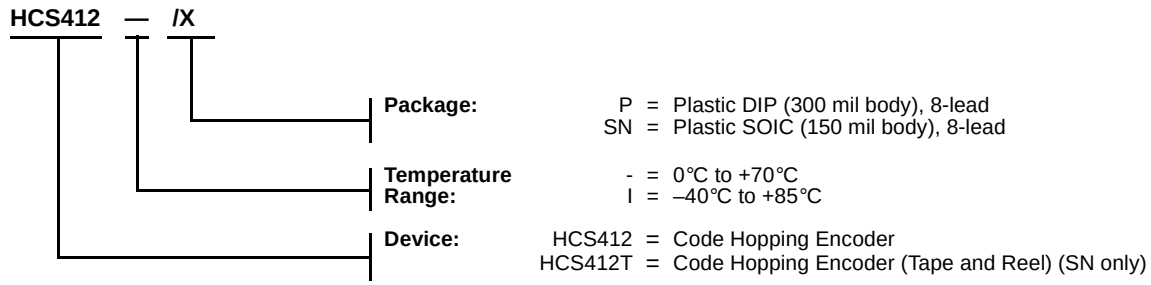
The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits.The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

7.0 HCS412 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277.
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System
Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

NOTES:

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton
Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

China - Beijing
Microchip Technology Beijing Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Shanghai
Microchip Technology Shanghai Office
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

Hong Kong
Microchip Asia Pacific
RM 2101, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

ASIA/PACIFIC (continued)

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Denmark ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

10/01/00

DNV Certification, Inc. USA — ANSI-RAB QMS ACCREDITED — DNV — DNV MSC The Netherlands Accredited by the RvA
ISO 9001 / QS-9000 REGISTERED FIRM

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.