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March 2003 FN4259.4

14-Bit, 5MSPS A/D Converter

The HI5905 is a monolithic, 14-bit, 5MSPS Analog-to-Digital Converter fabricated in an advanced BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth, low power consumption and excellent SINAD performance are essential. With a 100MHz full power input bandwidth and high frequency accuracy, the converter is ideal for many types of communication systems employing digital IF architectures.

The HI5905 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold amplifier (S/H). The HI5905 has excellent dynamic performance while consuming 350mW power at 5MSPS.

Data output latches are provided which present valid data to the output bus with a low data latency of 4 clock cycles.

Part Number Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI5905IN	-40 to 85	44 Ld MQFP	Q44.10x10
HI5905EVAL2	25	Low Frequency Eval Platform	

Features

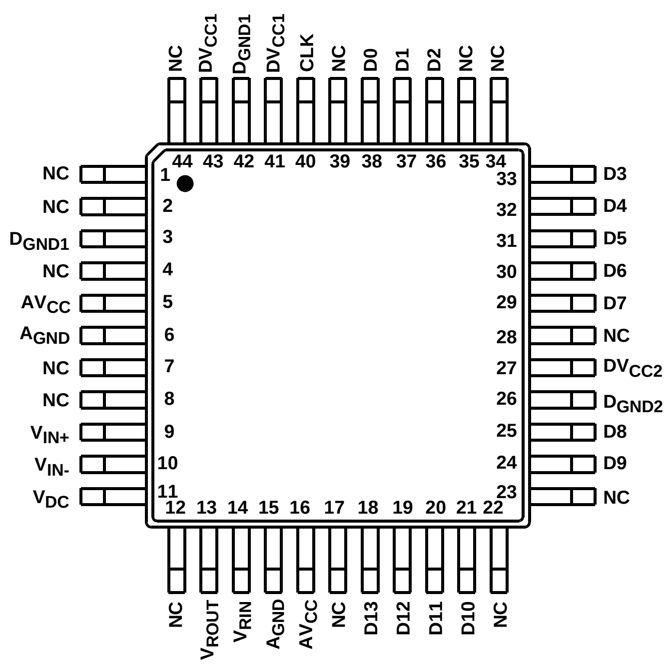
- Sampling Rate 5MSPS
- Low Power at 5MSPS 350mW
- Internal Sample and Hold
- Fully Differential Architecture
- Full Power Input Bandwidth 100MHz
- SINAD at 1MHz . . . . >70dB
- Low Data Latency
- Internal Voltage Reference
- TTL Compatible Clock Input
- CMOS Compatible Digital Data Outputs

Applications

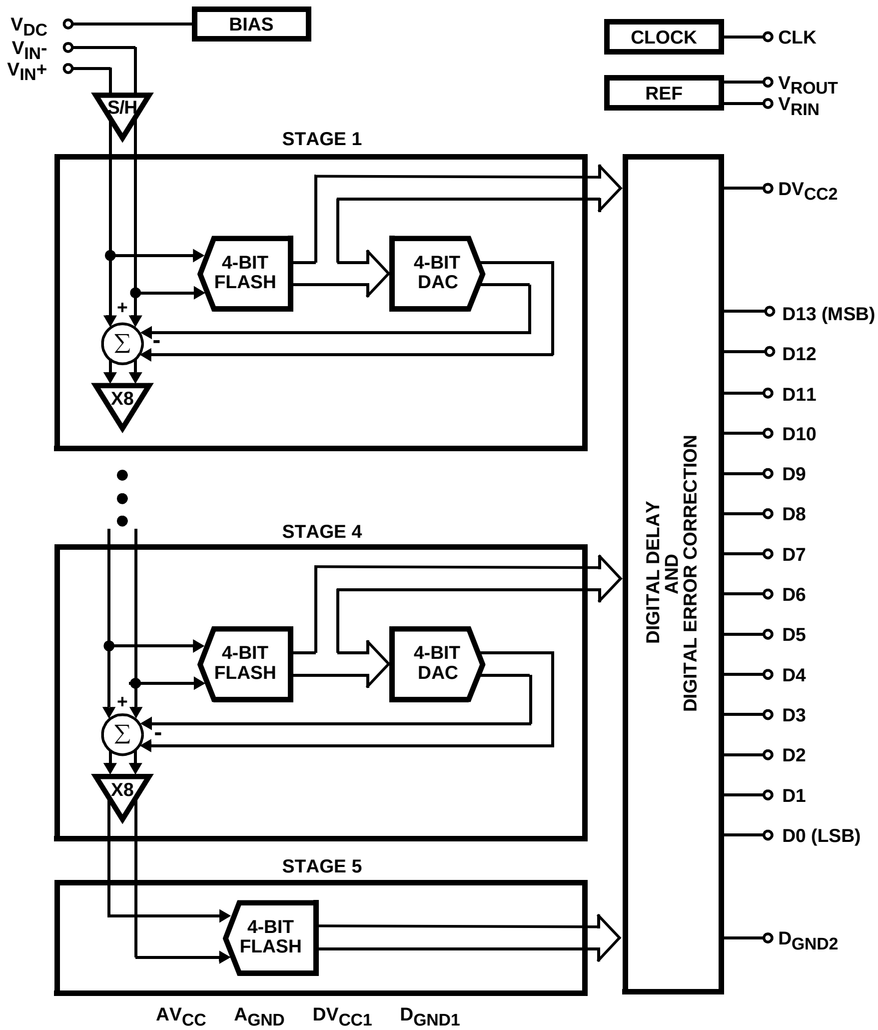
- Digital Communication Systems
- Undersampling Digital IF
- Asymmetric Digital Subscriber Line (ADSL)
- Document Scanners
- Reference Literature
  - AN9214, Using Intersil High Speed A/D Converters
  - AN9785, Using the Intersil HI5905 EVAL2 Evaluation Board

Pinout

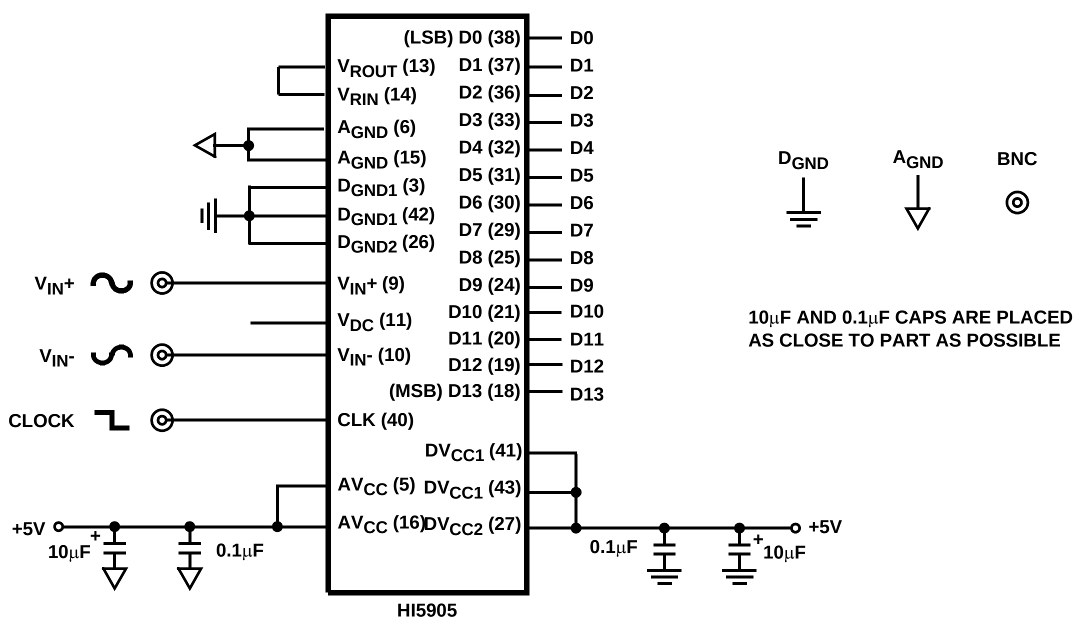
HI5905 (MQFP)
TOP VIEW



Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage, AV_{CC} or DV_{CC} to A_{GND} or D_{GND} . . . . +6.0V
D_{GND} to A_{GND} 0.3V
Digital I/O Pins . . . . D_{GND} to DV_{CC}
Analog I/O Pins . . . . A_{GND} to AV_{CC}

Operating Conditions

Temperature Range (HI5905IN) . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
MQFP Package	65

Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = DV_{CC2}$ = +5.0V, f_S = 5MSPS at 50% Duty Cycle, $V_{RIN} = V_{ROUT}$, C_L = 15pF, T_A = 25°C, Differential Analog Input, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		14	-	-	Bits
Integral Linearity Error, INL	Sinewave Histogram	-	±2.5	-	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	Sinewave Histogram	-1	±0.5	+1.5	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	-	120	LSB
Full Scale Error, FSE	f_{IN} = DC	-	-	164	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes (Note 2)	-	-	0.5	MSPS
Maximum Conversion Rate	No Missing Codes	5	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	11.2	11.7	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	69	72.2	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	71	74.6	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-73	75.7	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-95		dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-77	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	80	-	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	74	-	dBc
Transient Response		-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive	-	2	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range (V_{IN}+ - V_{IN}-)		-	±2.0	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	4.0	-	V
Analog Input Resistance, R_{IN}	(Notes 1, 2)	1	-	-	MΩ
Analog Input Capacitance, C_{IN}	(Note 2)	-	10	16	pF
Analog Input Bias Current, I_B+ or I_B-	(Note 3)	-50	-	+50	µA
Differential Analog Input Bias Current $I_{B\ DIFF}$ = (I_B+ - I_B-)		-	±0.5	-	µA

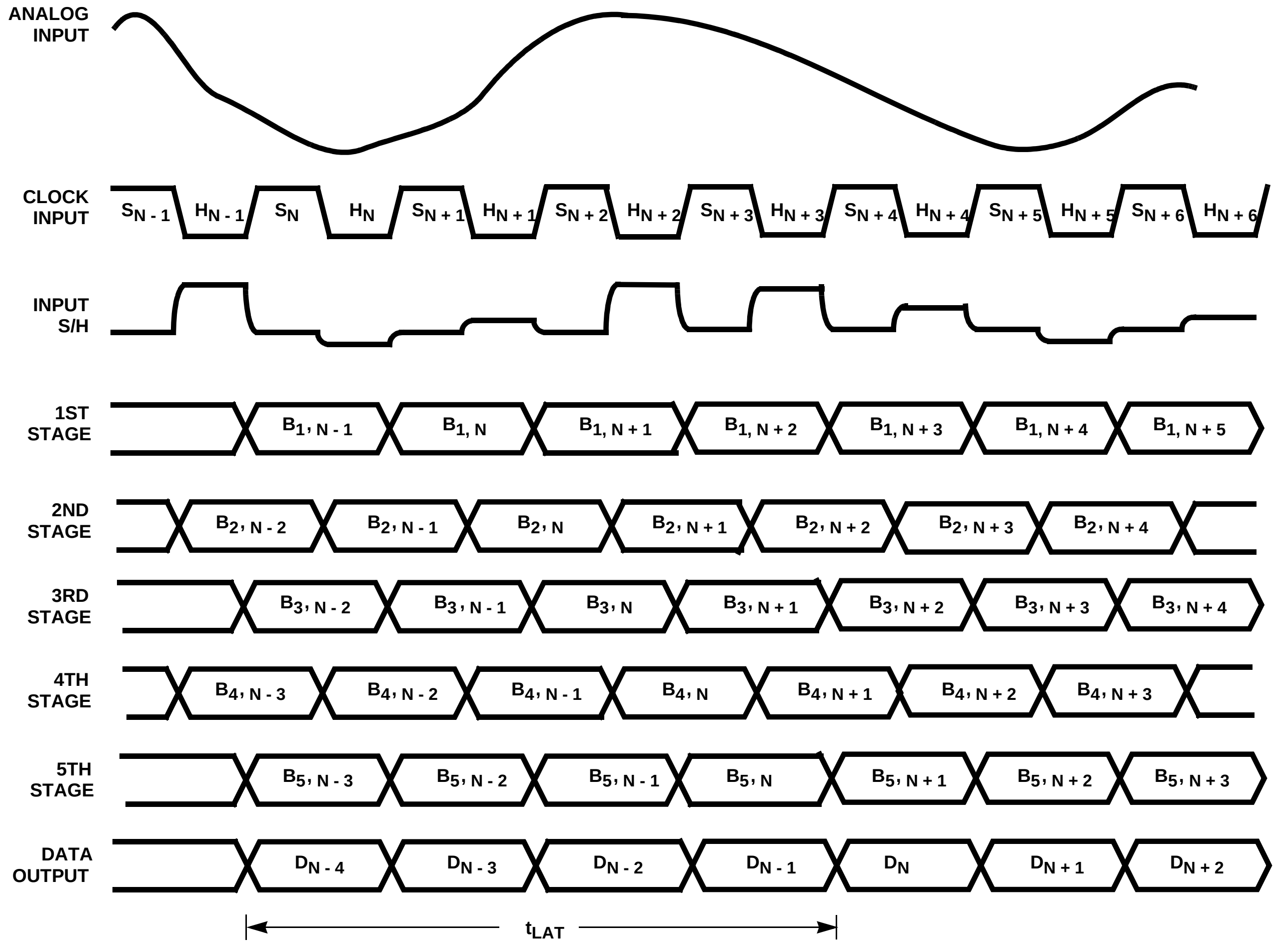
Electrical Specifications $AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$, f_S = 5MSPS at 50% Duty Cycle, $V_{RIN} = V_{ROUT}$, C_L = 15pF, $T_A = 25^oC$, Differential Analog Input, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Full Power Input Bandwidth (FPBW)		-	100	-	MHz
Analog Input Common Mode Voltage Range (V_{IN}+ + V_{IN}-)/2	Differential Mode (Note 2)	1	2.3	4	V
INTERNAL VOLTAGE REFERENCE					
Reference Output Voltage, V_{ROUT}		3.95	4.0	4.05	V
Reference Output Current		-	-	0.75	mA
Reference Temperature Coefficient		-	125	-	ppm/^oC
REFERENCE VOLTAGE INPUT					
Reference Voltage Input, V_{RIN}		-	4.0	-	V
Total Reference Resistance, R_L		-	5.6	-	kΩ
Reference Current		-	715	-	μA
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	2.3	-	V
Max Output Current (Not To Exceed)		-	-	1	mA
DIGITAL INPUTS (CLK)					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	V_{CLK} = 5V	-10.0	-	+10.0	μA
Input Logic Low Current, I_{IL}	V_{CLK} = 0V	-10.0	-	+10.0	μA
Input Capacitance, C_{IN}		-	10	-	pF
DIGITAL OUTPUTS (D0-D13)					
Output Logic High Voltage, V_{OH}	I_{OH} = 100μA	3.5	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 100μA	-	-	1.5	V
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	7	-	ns
Aperture Jitter, t_{AJ}		-	1	-	ps (RMS)
Data Output Delay, t_{OD}		-	50	60	ns
Data Output Hold, t_H	(Note 2)	5	8	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	4	Cycles
Clock Pulse Width (Low)	5MSPS Clock (Note 2)	95	100	105	ns
Clock Pulse Width (High)	5MSPS Clock (Note 2)	95	100	105	ns
POWER SUPPLY CHARACTERISTICS					
Total Supply Current, I_{CC}	V_{IN}+ = V_{IN}- = V_{DC}	-	70	80	mA
Analog Supply Current, AI_{CC}	V_{IN}+ = V_{IN}- = V_{DC}	-	50	-	mA
Digital Supply Current, DI_{CC1}	V_{IN}+ = V_{IN}- = V_{DC}	-	14	-	mA
Output Supply Current, DI_{CC2}	V_{IN}+ = V_{IN}- = V_{DC}	-	6	-	mA
Power Dissipation	V_{IN}+ = V_{IN}- = V_{DC}	-	350	400	mW
Offset Error PSRR, ΔV_{OS}	AV_{CC} or DV_{CC} = 5V ± 5%	-	2	-	LSB
Gain Error PSRR, ΔFSE	AV_{CC} or DV_{CC} = 5V ± 5%	-	45	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock off (clock low, hold mode).

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. INTERNAL CIRCUIT TIMING

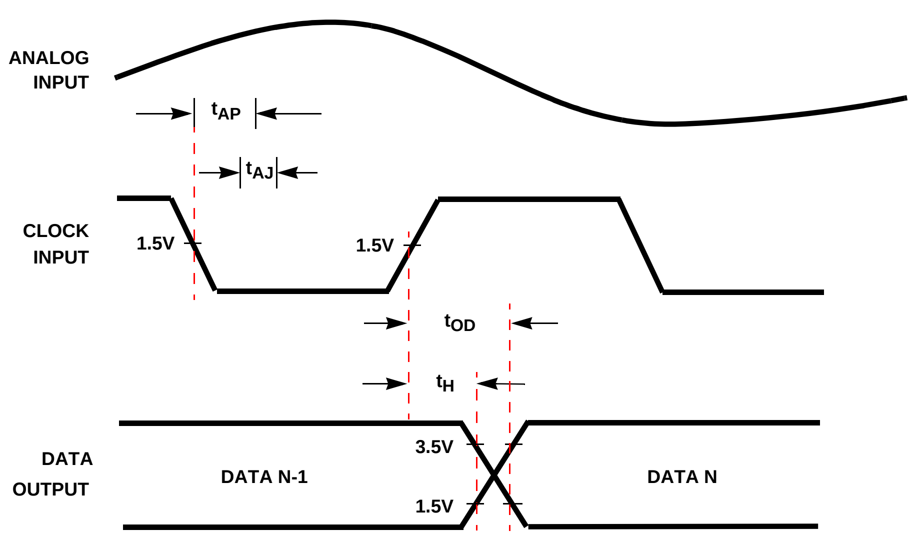


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

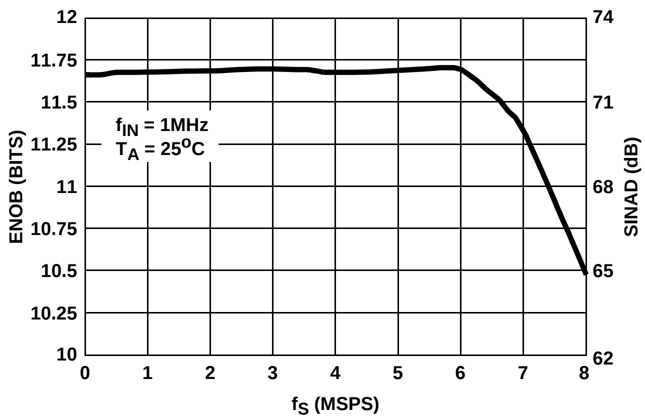


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) AND SINAD vs SAMPLE CLOCK FREQUENCY

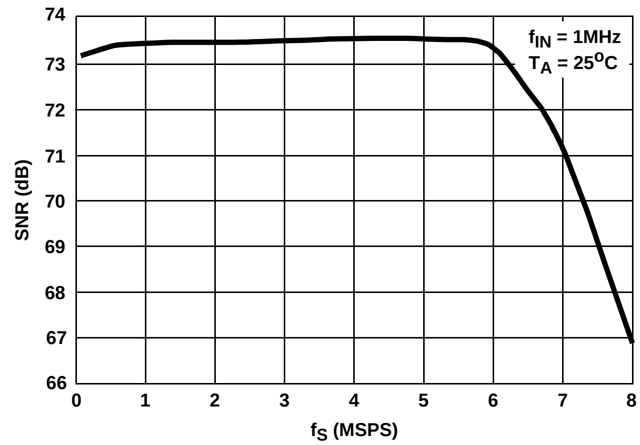


FIGURE 4. SNR vs SAMPLE CLOCK FREQUENCY

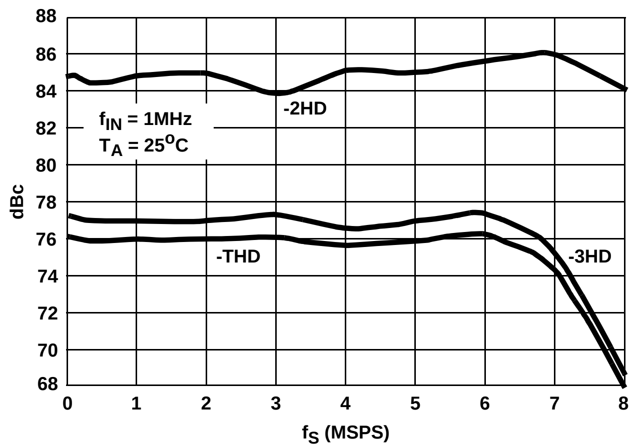


FIGURE 5. -2HD, -3HD AND -THD vs SAMPLE CLOCK FREQUENCY

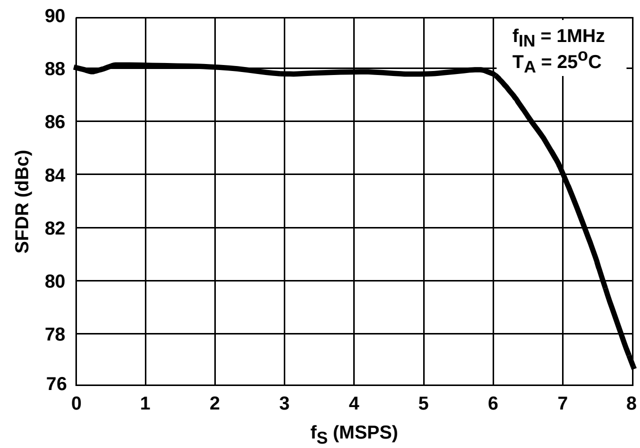


FIGURE 6. SFDR vs SAMPLE CLOCK FREQUENCY

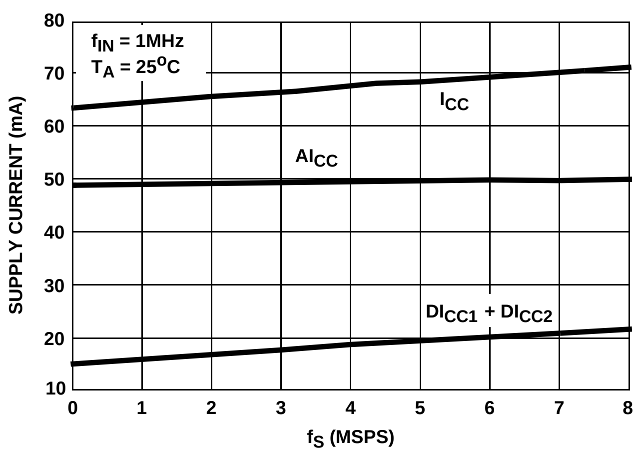


FIGURE 7. SUPPLY CURRENT vs SAMPLE CLOCK FREQUENCY

Pin Descriptions

PIN #	NAME	DESCRIPTION
1	NC	No Connection
2	NC	No Connection
3	D_{GND1}	Digital Ground
4	NC	No Connection
5	AV_{CC}	Analog Supply (5.0V)
6	A_{GND}	Analog Ground
7	NC	No Connection
8	NC	No Connection
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{DC}	DC Bias Voltage Output
12	NC	No Connection
13	V_{ROUT}	Reference Voltage Output
14	V_{RIN}	Reference Voltage Input
15	A_{GND}	Analog Ground
16	AV_{CC}	Analog Supply (5.0V)
17	NC	No Connection
18	D13	Data Bit 11 Output (MSB)
19	D12	Data Bit 11 Output
20	D11	Data Bit 11 Output
21	D10	Data Bit 10 Output
22	NC	No Connection
23	NC	No Connection
24	D9	Data Bit 9 Output
25	D8	Data Bit 8 Output
26	D_{GND2}	Digital Ground
27	DV_{CC2}	Digital Supply (5.0V)
28	NC	No Connection
29	D7	Data Bit 7 Output
30	D6	Data Bit 6 Output
31	D5	Data Bit 5 Output
32	D4	Data Bit 4 Output
33	D3	Data Bit 3 Output
34	NC	No Connection
35	NC	No Connection
36	D2	Data Bit 2 Output
37	D1	Data Bit 1 Output
38	D0	Data Bit 0 Output (LSB)
39	NC	No Connection
40	CLK	Input Clock
41	DV_{CC1}	Digital Supply (5.0V)
42	D_{GND1}	Digital Ground
43	DV_{CC1}	Digital Supply (5.0V)
44	NC	No Connection

Detailed Description

Theory of Operation

The HI5905 is a 14-bit fully differential sampling pipeline A/D converter with digital error correction. Figure 8 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 100MHz for the converter.

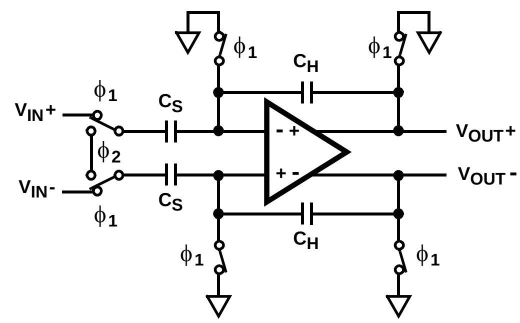


FIGURE 8. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, four identical pipeline subconverter stages, each containing a four-bit flash converter, a four-bit digital-to-analog converter and an amplifier with a voltage gain of 8, follow the S/H circuit with the fifth stage being only a 4-bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal, with the result that alternate stages in the pipeline will perform the same operation.

The output of each of the four-bit subconverter stages is a four-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the four identical four-bit subconverter stages with the corresponding output of the fifth stage flash converter before applying the twenty bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final fourteen bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus on the 4th cycle of the clock after the analog sample is taken. This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is synchronized to the external sampling clock with a latch. The digital output data is available in two's complement binary format (see Table 1, A/D Code Table).

Internal Reference Generator, V_{ROUT} and V_{RIN}

The HI5905 has an internal reference generator, therefore, no external reference voltage is required. V_{ROUT} must be connected to V_{RIN} when using the internal reference voltage.

The HI5905 can be used with an external reference. The converter requires only one external reference voltage connected to the V_{RIN} pin with V_{ROUT} left open.

The HI5905 is tested with V_{ROUT}, equal to 4.0V, connected to V_{RIN}. Internal to the converter, two reference voltages of 1.3V and 3.3V are generated for a fully differential input signal range of ±2V.

In order to minimize overall converter noise, it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{RIN}.

Analog Input, Differential Connection

The analog input to the HI5905 can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 9) will give the best performance for the converter.

Since the HI5905 is powered off a single +5V supply, the analog input must be biased so it lies within the analog input common mode voltage range of 1.0V to 4.0V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

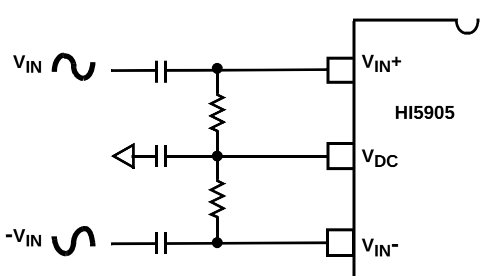


FIGURE 9. AC COUPLED DIFFERENTIAL INPUT

A 2.3V DC bias voltage source, V_{DC}, half way between the top and bottom internal reference voltages, is made available to the user to help simplify circuit design when using a differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the analog input common mode voltage range over temperature.

The difference between the converter's two internal voltage references is 2V. For the AC coupled differential input, (Figure 9), if V_{IN} is a $2V_{P-P}$ sinewave with $-V_{IN}$ being 180 degrees out of phase with V_{IN}, then $V_{IN}+$ is a $2V_{P-P}$ sinewave riding on a DC bias voltage equal to V_{DC} and $V_{IN}-$ is a $2V_{P-P}$ sinewave riding on a DC bias voltage equal to V_{DC}. Consequently, the converter will be at positive full scale, resulting in a digital data output code with D13 (MSB) equal to a logic "0" and D0-D12 equal to logic "1" (see Table 1, A/D Code Table), when the $V_{IN}+$ input is at V_{DC}+1V and the $V_{IN}-$ input is at VDC-1V ($V_{IN}+ - V_{IN}- = 2V$). Conversely, the ADC will be at negative full scale, resulting in a digital data output code with D13 (MSB) equal to a logic "1" and D0-D12 equal to logic "0" (see Table 1, A/D Code Table), when the $V_{IN}+$ input is equal to V_{DC}-1V and $V_{IN}-$ is at V_{DC}+1V ($V_{IN}+ - V_{IN}- = -2V$). From this, the converter is seen to have a peak-to-peak differential analog input voltage range of ±2V.

The analog input can be DC coupled (Figure 10) as long as the inputs are within the analog input common mode voltage range (1.0V ≤ VDC ≤ 4.0V).

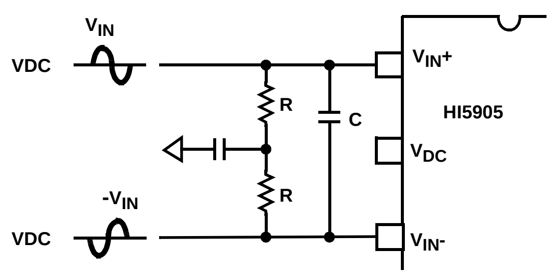


FIGURE 10. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 10 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE † (USING INTERNAL REFERENCE)	TWO'S COMPLEMENT BINARY OUTPUT CODE													
		MSB													LSB
		D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - 1/4 LSB	+1.99994V	0	1	1	1	1	1	1	1	1	1	1	1	1	1
+FS - 1 1/4 LSB	1.99969V	0	1	1	1	1	1	1	1	1	1	1	1	1	0
+ 3/4 LSB	183.105μV	0	0	0	0	0	0	0	0	0	0	0	0	0	0
- 1/4 LSB	-61.035μV	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-FS + 1 3/4 LSB	-1.99957V	1	0	0	0	0	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + 3/4 LSB	-1.99982V	1	0	0	0	0	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal center of each two's complement binary output code shown.

Analog Input, Single-Ended Connection

The configuration shown in Figure 11 may be used with a single ended AC coupled input. Sufficient headroom must be provided such that the input voltage never goes above +5V or below A_{GND}.

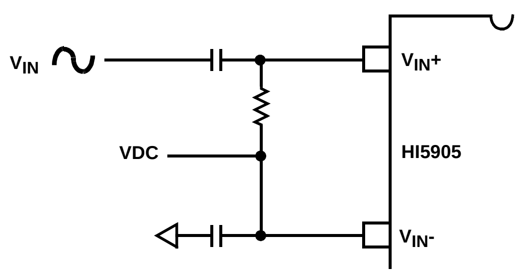


FIGURE 11. AC COUPLED SINGLE ENDED INPUT

Again, the difference between the two internal voltage references is 2V. If V_{IN} is a $4V_{P-P}$ sinewave, then V_{IN}+ is a $4V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when V_{IN}+ is at VDC + 2V (V_{IN}+ - V_{IN}- = 2V) and will be at negative full scale when V_{IN}+ is equal to VDC - 2V (V_{IN}+ - V_{IN}- = -2V). In this case, VDC could range between 2V and 3V without a significant change in ADC performance. The simplest way to produce VDC is to use the V_{DC} bias voltage output of the HI5905.

The single ended analog input can be DC coupled (Figure 12) as long as the input is within the analog input common mode voltage range.

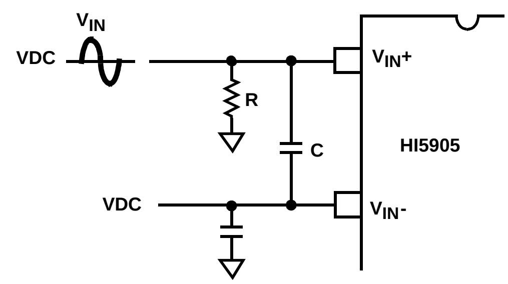


FIGURE 12. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 12 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from V_{IN}+ to V_{IN}- will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source will give better overall system performance if it is first converted to differential before driving the HI5905.

Digital I/O and Clock Requirements

The HI5905 provides a standard high-speed interface to external TTL/CMOS logic families. The digital CMOS clock input has TTL level thresholds. The low input bias current allows the HI5905 to be driven by CMOS logic. The digital CMOS outputs have a separate +5.0V digital supply input pin.

In order to ensure rated performance of the HI5905, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5905 will only be guaranteed at conversion rates above 0.5MSPS. This ensures proper performance of the internal dynamic circuits.

Supply and Ground Considerations

The HI5905 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5905 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the Application Note AN9214, “Using Intersil High Speed A/D Converters” for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level 1/4 LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is 3/4 LSB below positive full-scale with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection Ratio (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5905. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full-scale for all these tests. SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD + V_{CORR} - 1.76)/6.02$$

where: V_{CORR} = 0.5dB (Typical)

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component (excluding the first 5 harmonic components) in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are $(f_1 + f_2)$, $(f_1 - f_2)$, $(2f_1)$, $(2f_2)$, $(2f_1 + f_2)$, $(2f_1 - f_2)$, $(f_1 + 2f_2)$, $(f_1 - 2f_2)$. The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a fullscale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 14-bit accuracy.

Over-Voltage Recovery

Over-voltage Recovery is measured by providing a fullscale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 14-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sinewave. The input sinewave has an amplitude which swings from $-f_S$ to $+f_S$. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Refer to Figure 1, Internal Circuit Timing, and Figure 2, Input-To-Output Timing, for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture Jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is still valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data is output on the bus at the third cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input sample by 4 clock cycles.