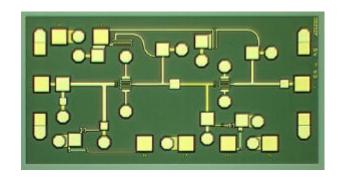


# HEMT LNA 37-40GHz

#### **Features**

- 2 Stage LNA
- 15dB Gain
- 3 dB Noise Figure



## **Description**

This datasheet gives the performance of a 37 - 40GHz Gallium Arsenide Low Noise Amplifier. This product is intended for use in fixed-point and point to point microwave systems. The LNA has a single drain supply, with access to each of the gates to enable customer optimization.

The die is fabricated using Caswell Technology's 0.20µm gate length, pHEMT process and is fully protected using Silicon Nitride passivation for excellent performance and reliability.

#### **Electrical Performance**

Ambient Temperature  $22 \pm 3$  °C,  $Z_0 = 50\Omega$ , Vd1/2 = 2V, Vg1 set for Id1 = 12mA, Vg2 set for Id2 = 20mA U.O.S

Parameter	Conditions	Min	Тур	Max	Units
Small Signal Gain	37 – 40GHz	12	15		dB
Input Return Loss	37 - 40 GHz	4	6		dB
Output Return Loss	37 - 40 GHz	10	16		dB
Noise Figure	37 – 40GHz		3	4	dB
Stage 1 Drain Current	By adjustment of Vg1		12		mA
Stage 2 Drain Current	By adjustment of Vg2		20		mA

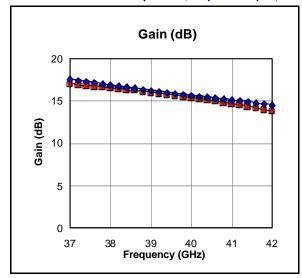
#### **Notes**

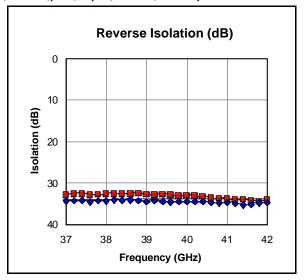
All parameters measured on wafer

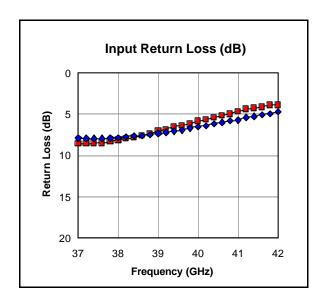
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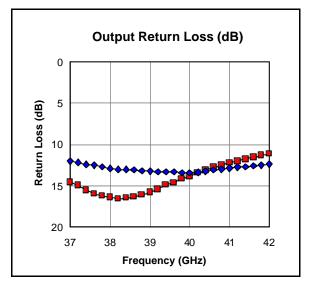


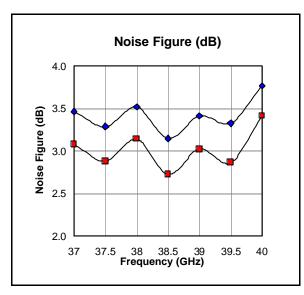
RFOW Performance (Vd Id1,Id2) - (2V, 12mA, 20mA,) - (2V, 20mA, 20mA)











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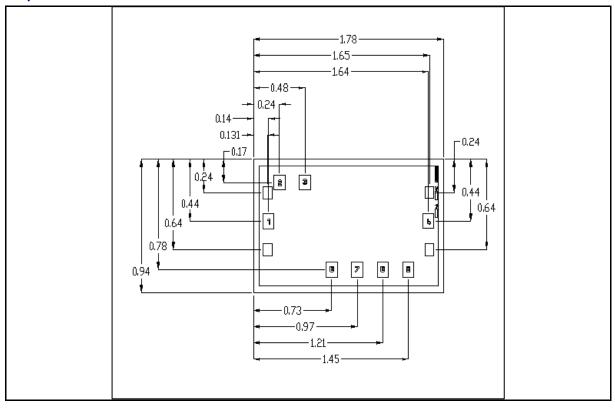


# Typical S-parameters (RFOW) (Vd=2V ,Id1=12mA, Id2=20mA)

Frequency	S	11	S	21	S	12	S	22
(GHz)	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
37	0.40	16.4	7.56	146.2	0.019	92.9	0.25	-148
37.2	0.40	16	7.42	141.8	0.0193	89.1	0.25	-147.2
37.4	0.40	15.4	7.30	137.5	0.0194	86.2	0.24	-146.9
37.6	0.40	15.2	7.20	133.3	0.0185	82.9	0.24	-145.5
37.8	0.40	14.5	7.06	129	0.0192	80.7	0.23	-144.9
38	0.40	14.1	6.96	124.8	0.019	76.3	0.23	-143.8
38.2	0.41	13	6.87	121	0.0195	74.2	0.22	-142.1
38.4	0.42	12.5	6.77	116.7	0.0194	69.9	0.22	-141.1
38.6	0.42	12.1	6.67	112.5	0.0196	66.9	0.22	-140
38.8	0.42	11.7	6.58	108.5	0.0193	64.5	0.22	-139
39	0.43	10	6.48	104.4	0.0188	60.2	0.22	-138.1
39.2	0.44	9.4	6.40	100.5	0.0193	56.2	0.22	-137.1
39.4	0.44	8.6	6.32	96.5	0.0189	52.7	0.22	-136
39.6	0.45	7.5	6.22	92.2	0.0185	52.4	0.22	-135.2
39.8	0.46	6	6.12	88.4	0.0186	49.8	0.21	-134
40	0.47	3.8	6.04	84.6	0.0187	47.6	0.21	-133.1
40.2	0.48	3.3	5.96	80.9	0.0187	43.1	0.21	-131.8
40.4	0.49	1.5	5.91	76.9	0.0187	37.2	0.22	-131
40.6	0.50	0.5	5.82	72.8	0.0182	35.4	0.22	-130.6
40.8	0.51	-1.7	5.75	68.9	0.0181	35.4	0.22	-130.3
41	0.52	-3.5	5.67	65.1	0.0183	32.6	0.23	-130.2
41.2	0.54	-5.2	5.63	61	0.0176	29.4	0.23	-130.4
41.4	0.54	-7	5.54	57	0.0171	27.2	0.23	-130.2
41.6	0.56	-8.9	5.44	52.9	0.0174	23.5	0.24	-129.8
41.8	0.57	-10.7	5.38	49.1	0.018	22.1	0.24	-129.6
42	0.58	-13.2	5.30	45.2	0.0182	16.7	0.24	-129.6



# **Chip Outline**



Die size:  $1.78 \times 0.94$ mm RF bond pads (1 & 4):  $120\mu$ m x  $120\mu$ m x  $120\mu$ m x  $120\mu$ m x  $120\mu$ m

Die Thickness: 100μm

## **Pad Details**

Pad	Function
1	RF Input
2	N/C
3	Vdd
4	RF Output
5	N/C
6	Vg2 N/C
7	N/C
8	Vg1



#### **Handling and Assembly Information**

Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Dice are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded anti-static workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

GaAs Products from Caswell Technology's pHEMT Foundry process are  $100\mu m$  thick and have through GaAs vias to enable grounding to the circuit. Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die.

The surface to which the die are to be attached should be cleaned with a proprietary de-greasing cleaner.

Conductive epoxy mounting is recommended. Recommended epoxies are Ablestick 84-1LMI or 84-1LMIT cured at 150°C for 1 hour in a nitrogen atmosphere. The epoxy should be applied sparingly to avoid encroachment of the epoxy on to the top surface of the die. An epoxy fillet should be visible around the total die periphery.

Eutectic mounting can be used and entails the use of a gold-tin (AuSn) preform, approximately 0.001" thick, placed between the die and the attachment surface. The preferred method of mounting is the use of a machine such as a Mullins 8-140 die bonder. This utilises a heated collet and workstation with a facility for applying a scrubbing action to ensure total wetting and avoid the formation of voids. Dry nitrogen gas is directed across the work piece.

The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately  $280^{\circ}$ C (Note: Gold Germanium with a higher melting temperature should be avoided, in particular for MMICs). The work station temperature should be  $310^{\circ}$ C  $\pm 10^{\circ}$ C. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. The strength of the bonding formed by this method will result in fracture of the die, rather than the bond under die strength testing.

The P35-5117-000-200 amplifier die has gold bond pads. The recommended wire bonding procedure uses  $25\mu m$  (0.001") 99.99% pure gold wire with 0.5-2% elongation. Thermo-compression wedge bonding is preferred though thermosonic wire bonding may be used providing the ultrasonic content of the bond is minimised. A work station temperature of  $260^{\circ}C \pm 10^{\circ}C$  with a wedge tip temperature of  $120^{\circ}C \pm 10^{\circ}C$  is recommended. The wedge force should be  $45 \pm 5$  grams. Bonds should be made from the bond pads on the die to the package or substrate.

The RF bond pads at the input and output are 120μm x 120μm; all other bond pads are 120μm x 120μm.

The P35-5118-000-200 has been designed to include the inductance of two 25 $\mu$ m bond wires at both the input and output, facilitating the integration of the die into a 50 $\Omega$  environment, these should be kept to a minimum length.

### Operating and Biasing of the P35-5118-000-200

The P35-5118-000-200 is a three-stage low noise amplifier. The drain bias for both stages (Vd1 & Vd2) is linked on chip and 2 volts should be connected to Vdd. The gate voltages (Vg1 & Vg2) are set to give 12mA of drain current for the first stage and 20mA in the second stage drain. The separate gate voltage supplies for both stages can be combined into single supply (Vgg). DC bias supplies should be decoupled to ground using 100pF chip capacitors placed close to the chip with short bondwires to the amplifier bond pads.

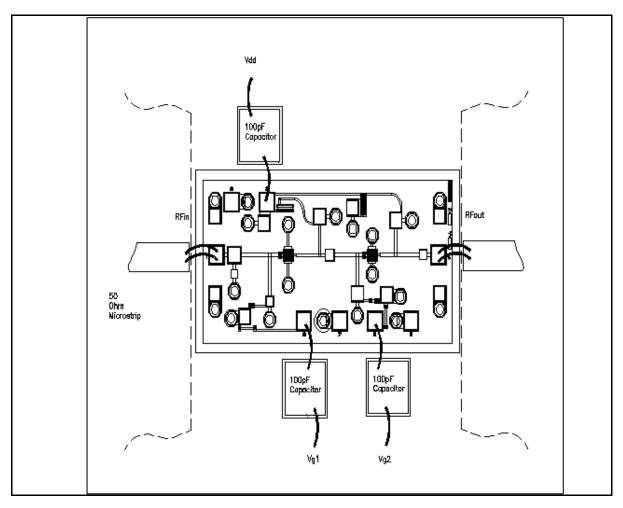
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# Typical bonding detail



# **Absolute maximum Ratings**

 $\begin{array}{ll} \text{Max Vdd} & +5\text{V} \\ \text{Max Vgg} & -2\text{V} \\ \text{Max channel temperature} & 150^{\circ}\text{C} \\ \end{array}$ 

Storage temperature -65 °C to +150 °C

# **Ordering Information**

P35-5118-000-200

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