Agilent HCPL-3020/HCPL-0302 0.2 Amp Output Current IGBT Gate Drive Optocoupler

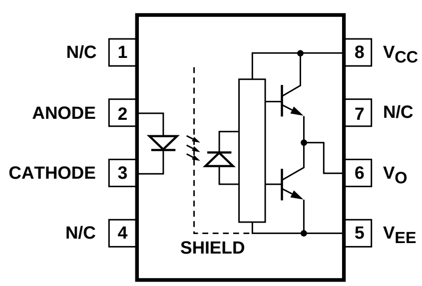
Data Sheet

Features

- 0.2 A minimum peak output current
- High speed response: 0.7 µs maximum propagation delay over temperature range
- Ultra high CMR: minimum 10 kV/µs at V_{CM} = 1000 V
- Bootstrappable supply current: maximum 3 mA
- Wide operating temperature range: –40°C to 100°C
- Wide V_{CC} operating range: 10 V to 30 V over temperature range
- Available in DIP 8 and SO-8 packages
- Safety approvals: UL approval, 2500 V_{RMS} for 1 minute
- CSA approval pending
- VDE approval pending
  V_{IORM} = 630 V_{PEAK} (HCPL-3020),
  V_{IORM} = 566 V_{PEAK} (HCPL-0302)

Description

The HCPL-3020 and HCPL-0302 consist of a GaAsP LED optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate-controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving small or medium power IGBTs. For IGBTs with higher ratings, the HCPL-0314/3140 (0.4 A), HCPL-3150 (0.5 A) or HCPL-3120 (2.0 A) gate drive opto-couplers can be used.



Truth Table

LED	V_O
OFF	LOW
ON	HIGH

Applications

- Isolated IGBT/power MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters
- Air conditioner
- Washing machine
- Induction heater for cooker
- Switching power supplies (SPS)

Agilent Technologies

Ordering Information

Specify part number followed by option number (if desired).

Example:

HCPL-3020-XXX

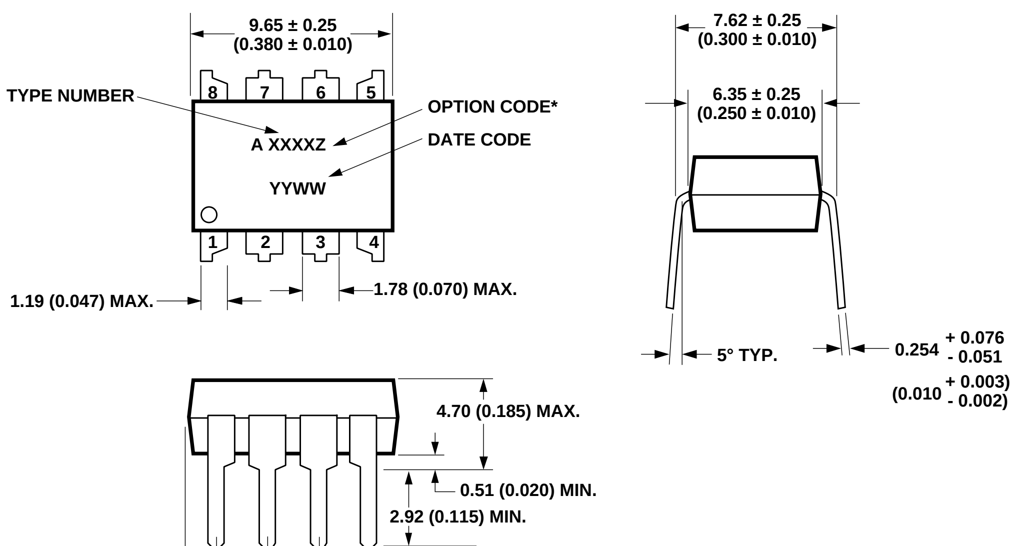
- No option = Standard DIP package, 50 per tube
- 300 = Gull Wing Surface Mount Option, 50 per tube
- 500 = Tape and Reel Packaging Option
- 060 = VDE 0884, V_{IORM} = 630 V_{PEAK}

HCPL-0302-XXX

- No option = Standard SO-8 package, 100 per tube
- 500 = Tape and Reel Packaging Option
- 060 = VDE 0884, V_{IORM} = 566 V_{PEAK}

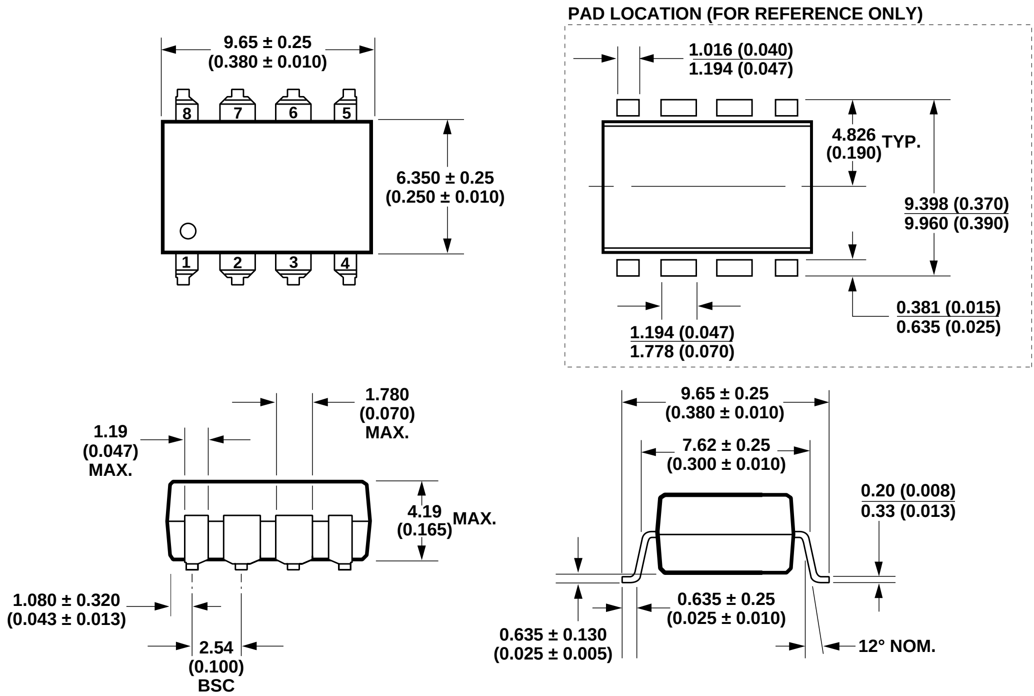
Package Outline Drawings

HCPL-3020 Standard DIP Package



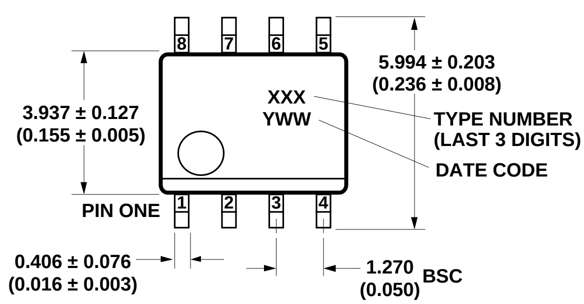
DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

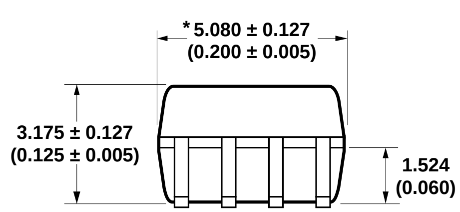
HCPL-3020 Gull Wing Surface Mount Option 300

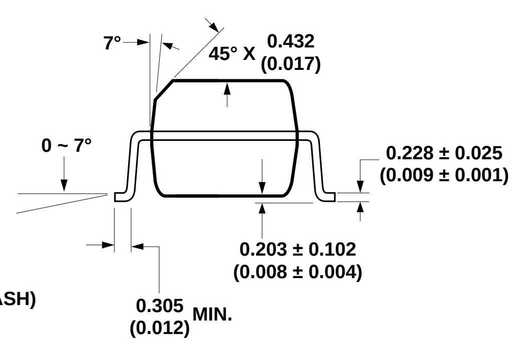


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

HCPL-0302 Small Outline SO-8 Package



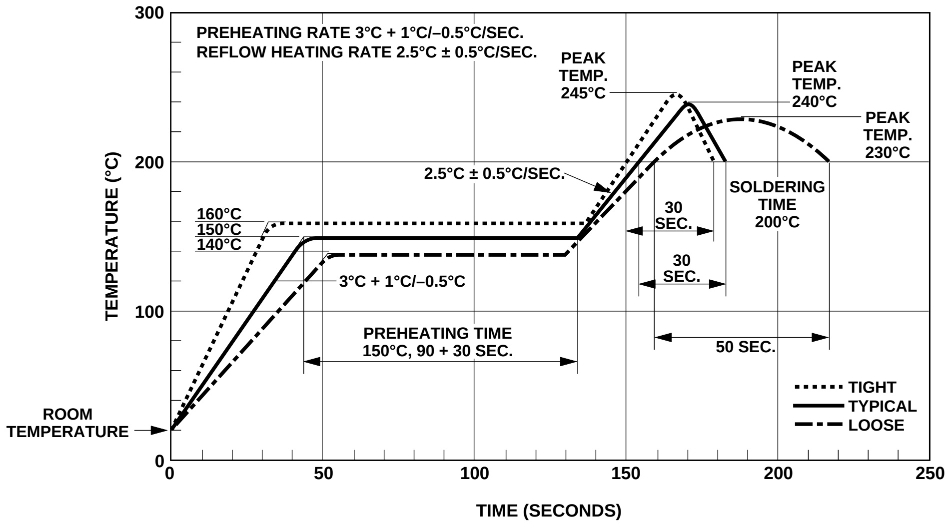




*TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

Solder Reflow Temperature Profile



Regulatory Information

The HCPL-0302/3020 has been approved / is pending approval by the following organizations:

VDE

Pending approval under VDE 0884/06.92 with V_{IORM} = 630 V_{PEAK} (HCPL-3020) and 566 V_{PEAK} (HCPL-0302).

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 2500 V_{RMS}. File E55361.

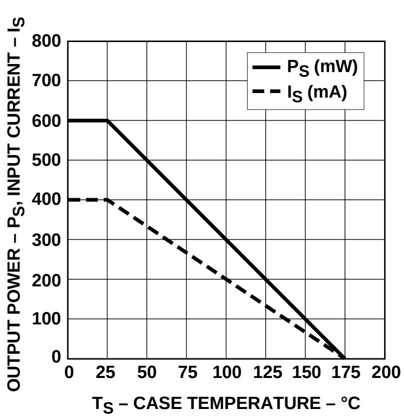
CSA

Pending approval under CSA Component Acceptance Notice #5, File CA 88324.

VDE 0884 Insulation Characteristics (HCPL-3020 and HCPL-0302 Option 060)

Description	Symbol	HCPL-3020	HCPL-0302	Unit
Installation Classification per DIN VDE 0110/1.89, Table 1				
for Rated Mains Voltage ≤ 150 V_{rms}		I – IV	I – IV	
for Rated Mains Voltage ≤ 300 V_{rms}		I – III	I – III	
for Rated Mains Voltage ≤ 600 V_{rms}		I – II		
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	630	566	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	1050	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	840	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	6000	4000	V_{peak}
Safety-Limiting Values – Maximum Values Allowed in the Event of a Failure.				
Case Temperature	T_S	175	150	°C
Input Current**	$I_{S, INPUT}$	230	150	mA
Output Power**	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	Ω

*Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (VDE 0884), for a detailed description of Method a and Method b partial discharge test profiles.
**Refer to the following figure for dependence of P_S and I_S on ambient temperature.



Insulation and Safety Related Specifications

Parameter	Symbol	HCPL-3020	HCPL-0302	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature	T_A	–40	100	°C	
Average Input Current	$I_{F(AVG)}$		20	mA	1
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		0.4	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		0.4	A	2
Supply Voltage	$V_{CC} – V_{EE}$	–0.5	35	V	
Output Voltage	$V_{O(PEAK)}$	–0.5	V_{CC}	V	
Output Power Dissipation	P_O		250	mW	3
Input Power Dissipation	P_I		105	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply	V_{CC} - V_{EE}	10	30	V	
Input Current (ON)	$I_{F(ON)}$	7	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	–3.0	0.8	V	
Operating Temperature	T_A	–40	100	°C	

Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	0.15			A	$V_O = V_{CC} - 4$		5
		0.2	0.3		A	$V_O = V_{CC} - 10$	2	2
Low Level Output Current	I_{OL}	0.15			A	$V_O = V_{EE} + 2.5$		5
		0.2	0.3		A	$V_O = V_{EE} + 10$	4	2
High Level Output Voltage	V_{OH}	$V_{CC} - 4$	$V_{CC} - 1.8$		V	$I_O = -100$ mA	1	6, 7
Low Level Output Voltage	V_{OL}		0.4	1	V	$I_O = 100$ mA	3	
High Level Supply Current	I_{CCH}		0.7	3	mA	$I_O = 0$ mA	5, 6	14
Low Level Supply Current	I_{CCL}		1.2	3	mA	$I_O = 0$ mA		
Threshold Input Current Low to High	I_{FLH}			6	mA	$I_O = 0$ mA, $V_O > 5$ V	7, 13	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V			
Input Forward Voltage	V_F	1.2	1.5	1.8	V	$I_F = 10$ mA	14	
Temperature Coefficient of Input Forward Voltage	DV_F/DT_A		–1.6		mV/°C			
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10$ µA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, $V_F = 0$ V		

Switching Specifications (AC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.1	0.2	0.7	µs	$R_g = 75\ \Omega$, $C_g = 1.5$ nF, f = 10 kHz, Duty Cycle = 50%, $I_F = 7$ mA, $V_{CC} = 30$ V	8, 9 10, 11 12, 15	14
Propagation Delay Time to Low Output Level	t_{PHL}	0.1	0.2	0.7	µs			
Propagation Delay Difference Between Any Two Parts or Channels	PDD	–0.5		0.5	µs			10
Rise Time	t_R		50		ns			
Fall Time	t_F		50		ns			
Output High Level Common Mode Transient Immunity	$\lvert CM_H \rvert$	10			kV/µs	$T_A = 25°C$, $V_{CM} = 1000$ V	16	11
Output Low Level Common Mode Transient Immunity	$\lvert CM_L \rvert$	10			kV/µs		16	12

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	2500			V_{rms}	T_A = 25°C, RH < 50%		8, 9
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		9
Input-Output Capacitance	C_{I-O}		0.6		pF	Freq = 1 MHz		

Notes:

1. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.2 A. See Application section for additional details on limiting I_{OL} peak.
3. Derate linearly above 85°C, free air temperature at the rate of 4.0 mW/°C.
4. Input power dissipation does not require derating.
5. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
6. In this test, V_{OH} is measured with a DC load current. When driving capacitive load V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 µs, maximum duty cycle = 20%.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage >3000 V_{rms} for 1 second (leakage detection current limit I_{I-O} < 5 µA). This test is performed before 100% production test for partial discharge (method B) shown in the VDE 0884 Insulation Characteristics Table, if applicable.
9. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
10. PDD is the difference between t_{PHL} and t_{PLH} between any two parts or channels under the same test conditions.
11. Common mode transient immunity in the high state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse V_{CM} to assure that the output will remain in the high state (i.e. V_O > 6.0 V).
12. Common mode transient immunity in a low state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e. V_O < 1.0 V).
13. This load condition approximates the gate load of a 1200 V/20 A IGBT.
14. The power supply current increases when operating frequency and C_g of the driven IGBT increases.

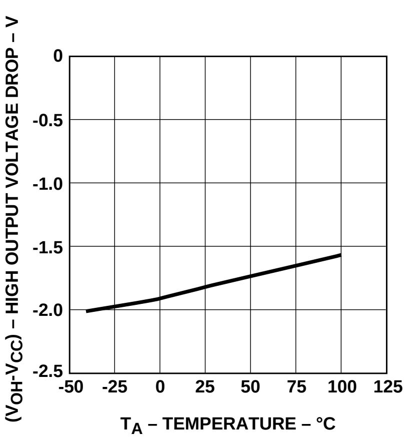


Figure 1. V_{OH} vs. temperature.

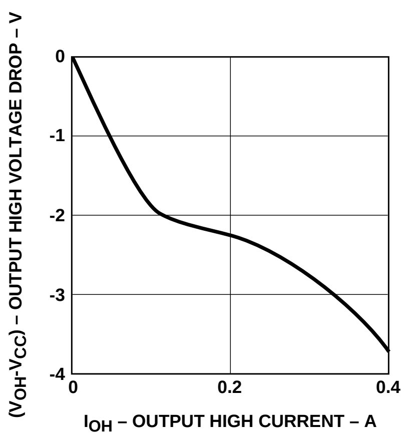


Figure 2. V_{OH} vs. I_{OH}.

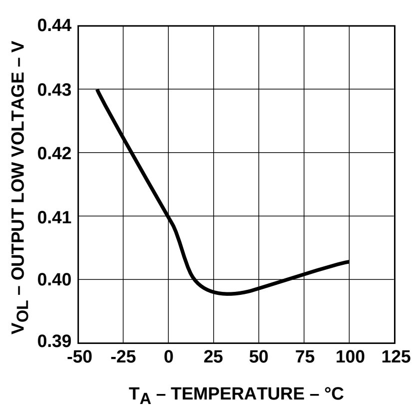


Figure 3. V_{OL} vs. temperature.

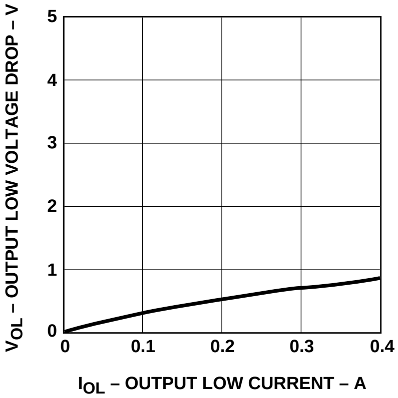


Figure 4. V_{OL} vs. I_{OL}.

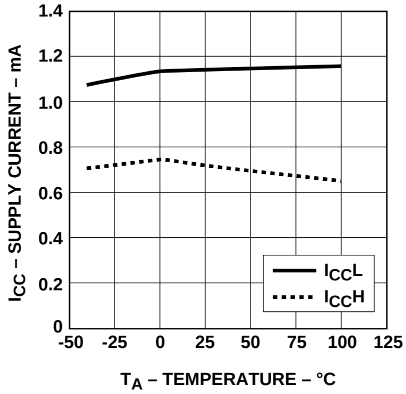


Figure 5. I_{CC} vs. temperature.

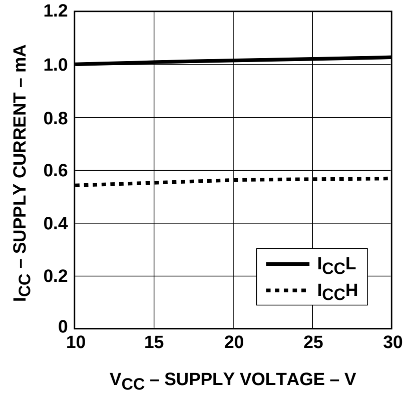


Figure 6. I_{CC} vs. V_{CC}.

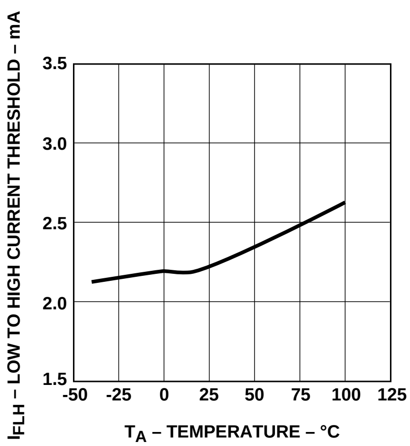


Figure 7. I_{FLH} vs. temperature.

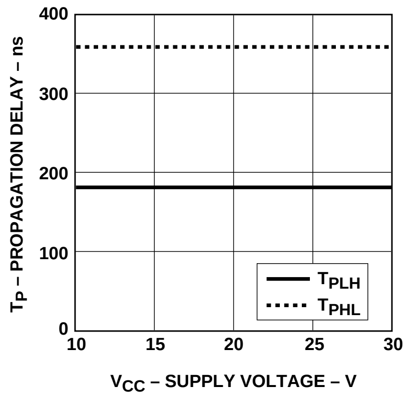


Figure 8. Propagation delay vs. V_{CC}.

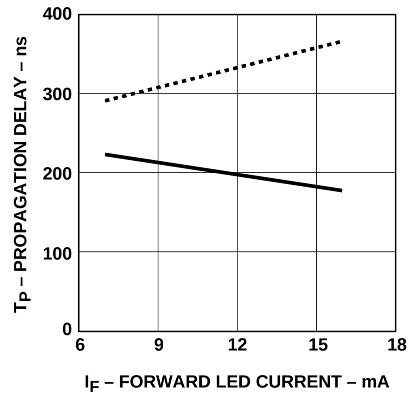


Figure 9. Propagation delay vs. I_F.

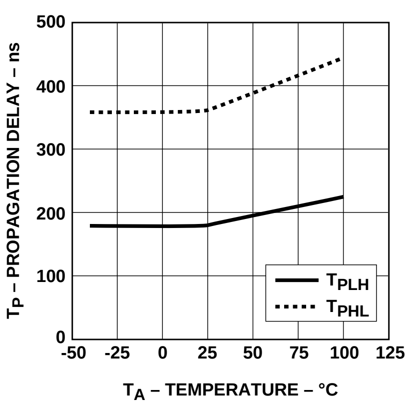


Figure 10. Propagation delay vs. temperature.

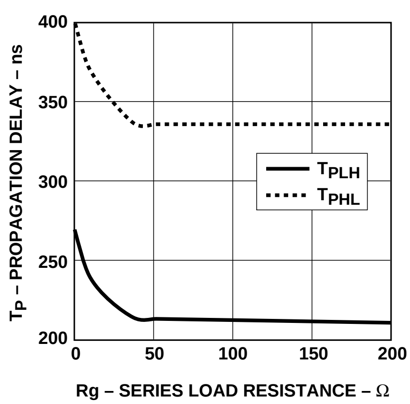


Figure 11. Propagation delay vs. R_g.

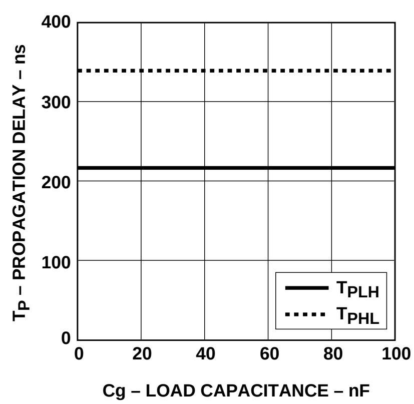


Figure 12. Propagation delay vs. C_g.

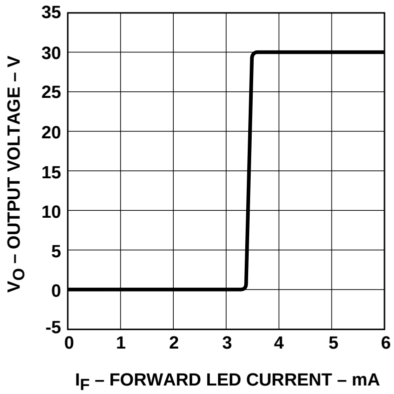


Figure 13. Transfer characteristics.

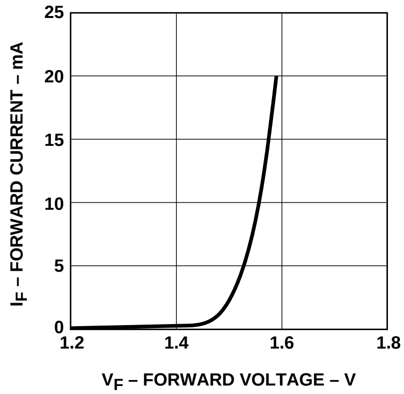


Figure 14. Input current vs. forward voltage.

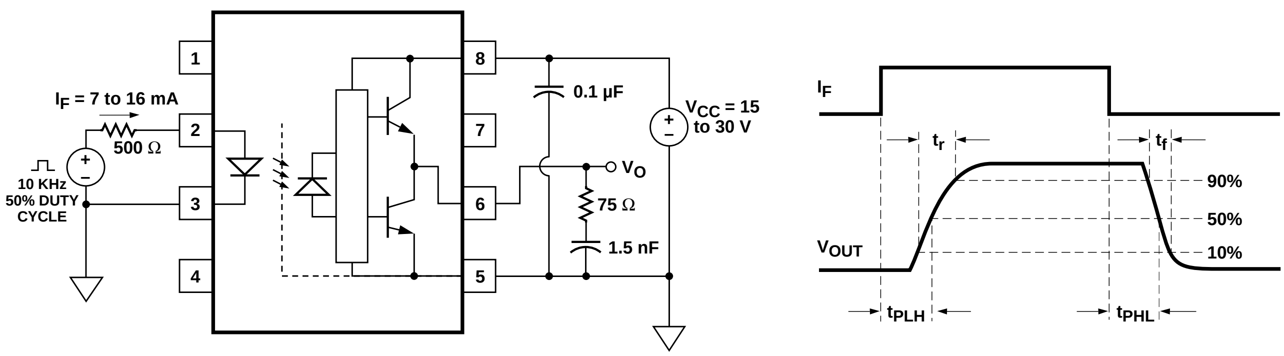


Figure 15. Propagation delay test circuits and waveforms.

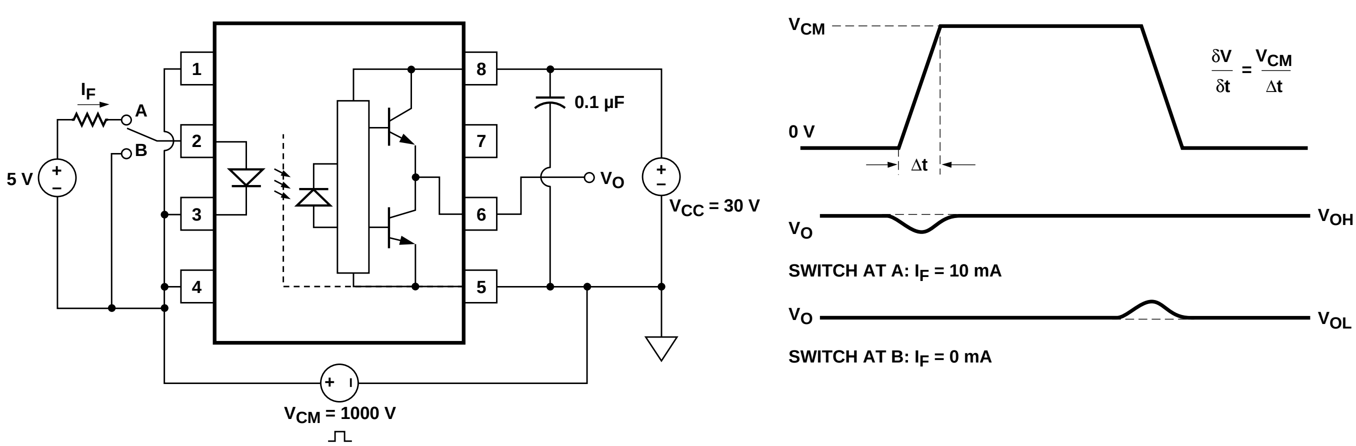


Figure 16. CMR test circuits and waveforms.

Applications Information Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-3020 and HCPL-0302 have a very low maximum V_{OL} specification of 1.0 V. Minimizing R_g and the lead inductance from the HCPL-3020 or HCPL-0302 to the IGBT gate and emitter (possibly by mounting the HCPL-3020 or HCPL-0302 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 17. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-3020 or HCPL-0302 input as this can result in unwanted coupling of transient signals into the input of HCPL-3020 or HCPL-0302 and degrade performance. (If the IGBT drain must be routed near the HCPL-3020 or HCPL-0302 input, then the LED should be reverse biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-3020 or HCPL-0302.

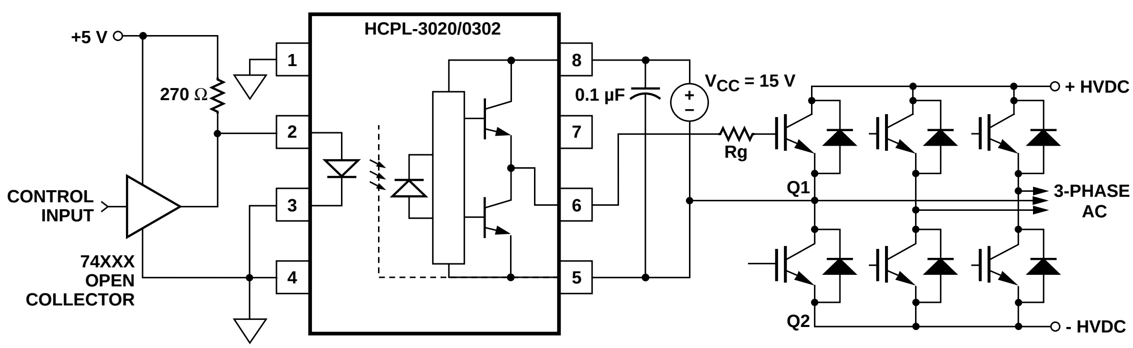


Figure 17. Recommended LED drive and application circuit for HCPL-3020 and HCPL-0302.

Selecting the Gate Resistor (R_g) for HCPL-3020

Step 1: Calculate R_g minimum from the I_{OL} peak specification. The IGBT and R_g in Figure 17 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3020.

$$R_g \geq \frac{V_{CC} - V_{OL}}{I_{OLPEAK}}$$

$$= \frac{24 - 1}{0.4}$$

$$= 57.5\ \Omega$$

The V_{OL} value of 1 V in the previous equation is the V_{OL} at the peak current of 0.4 A. (See Figure 4).

Step 2: Check the HCPL-3020 power dissipation and increase R_g if necessary. The HCPL-3020 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$$P_T = P_E + P_O$$

$$P_E = I_F \bullet V_F \bullet \text{Duty Cycle}$$

$$P_O = P_{O(BIAS)} + P_{O(SWITCHING)} = I_{CC} \bullet V_{CC} + E_{SW}(R_g;Q_g) \bullet f$$

$$= (I_{CCBIAS} + K_{ICC} \bullet Q_g \bullet f) \bullet V_{CC} + E_{SW}(R_g;Q_g) \bullet f$$

where $K_{ICC} \bullet Q_g \bullet f$ is the increase in I_{CC} due to switching and K_{ICC} is a constant of 0.001 mA/(nC*kHz). For the circuit in Figure 17 with I_F (worst case) = 10 mA, R_g = 57.5 Ω, Max Duty Cycle = 80%, Q_g = 100 nC, f = 20 kHz and T_{AMAX} = 85°C:

$$P_E = 10\ \text{mA} \bullet 1.8\ \text{V} \bullet 0.8 = 14\ \text{mW}$$

$$P_O = [(3\ \text{mA} + (0.001\ \text{mA/nC} \bullet \text{kHz}) \bullet 20\ \text{kHz} \bullet 100\ \text{nC})] \bullet 24\ \text{V} + 0.31 \bullet 20\ \text{kHz}$$

$$= 126\ \text{mW} \leq 250\ \text{mV}\ (P_{O(MAX)})$$

The value of 3 mA for I_{CC} in the previous equation is the max. I_{CC} over entire operating temperature range.

Since P_O for this case is less than $P_{O(MAX)}$, R_g = 57.5 Ω is alright for the power dissipation.

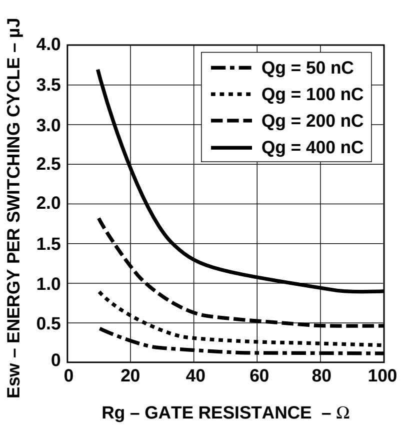


Figure 18. Energy dissipated in the HCPL-3020 and HCPL-0302 and for each IGBT switching cycle.

LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 19. The HCPL-3020 and HCPL-0302 improve CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 20. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 17), can achieve 10 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

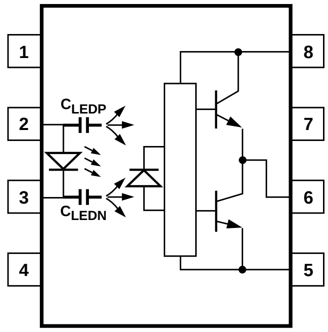


Figure 19. Optocoupler input to output capacitance model for unshielded optocouplers.

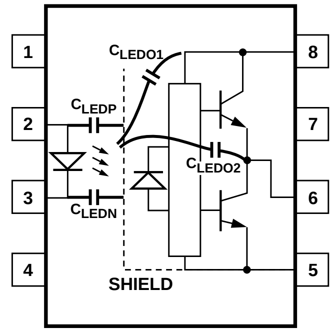


Figure 20. Optocoupler Input to output capacitance model for shielded optocouplers.

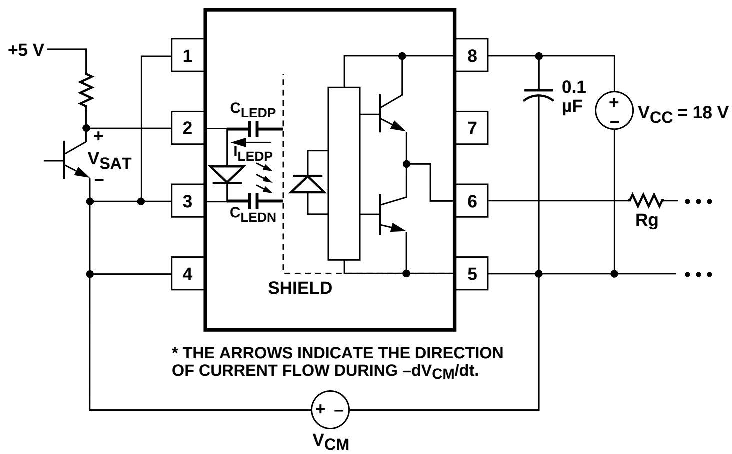


Figure 21. Equivalent circuit for figure 15 during common mode transient.

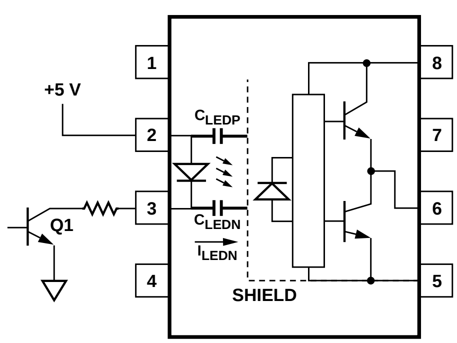


Figure 22. Not recommended open collector drive circuit.

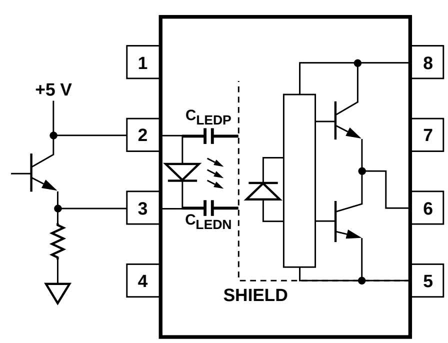


Figure 23. Recommended LED drive circuit for ultra-high CMR IPM dead time and propagation delay specifications.

CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 7 mA provides adequate margin over the maximum I_{FLH} of 6 mA to achieve 10 kV/μs CMR.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a -dV_{CM}/dt transient in Figure 21, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$ the LED will remain off and no common mode failure will occur.

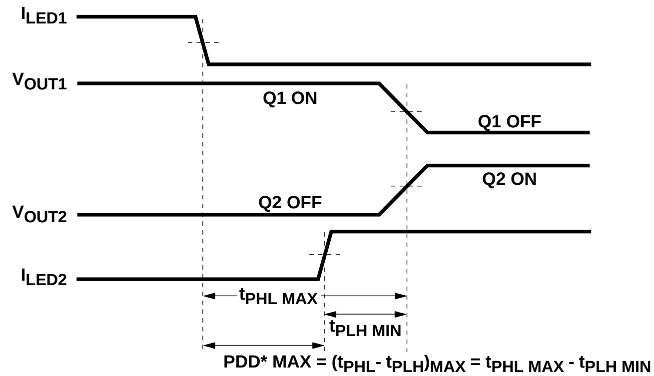
The open collector drive circuit, shown in Figure 22, cannot keep the LED off during a $+dV_{CM}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR_1 performance. The alternative drive circuit, which likes the recommended application circuit (Figure 17), does achieve ultra high CMR performance by shunting the LED in the off state.

Dead Time and Propagation Delay Specifications

The HCPL-3020 and HCPL-0302 include a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time high and low side power transistors are off. Any overlap in Ql and Q2 conduction will result in large currents flowing through the power devices from the high voltage to the low-voltage motor rails. To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 24. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD max, which is specified to be 500 ns over the operating temperature range of –40° to 100°C.

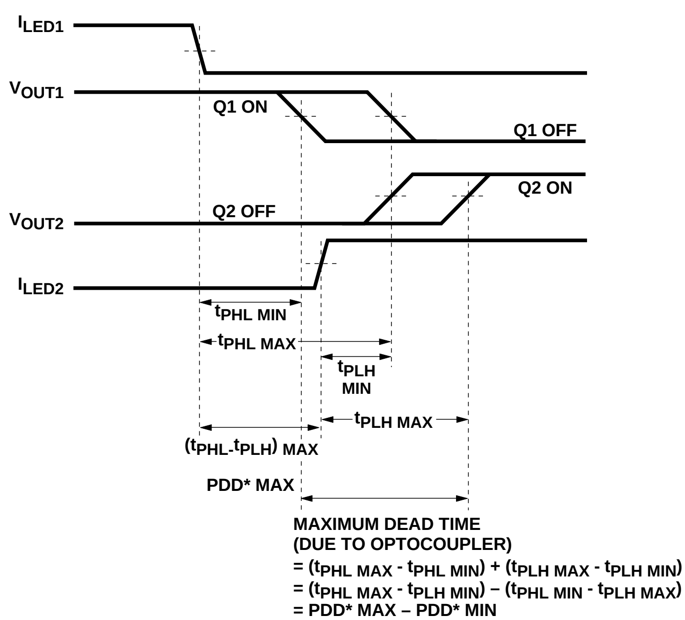
Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 25. The maximum dead time for the HCPL-3020 and HCPL-0302 is 1 ms (= 0.5 μs – (–0.5 μs)) over the operating temperature range of –40°C to 100°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 24. Minimum LED skew for zero dead time.



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 25. Waveforms for dead time.

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