Agilent HMPS-282x Series MiniPak Surface Mount RF Schottky Barrier Diodes

Data Sheet

Features

- **Surface mount MiniPak package**
  - low height, 0.7 mm (0.028") max.
  - small footprint, 1.75 mm^2 (0.0028 $inch^2$)
- **Better thermal conductivity for higher power dissipation**
- **Single and dual versions**
- **Matched diodes for consistent performance**
- **Low turn-on voltage (as low as 0.34 V at 1 mA)**
- **Low FIT (Failure in Time) rate***
- **Six-sigma quality level**

* For more information, see the Surface Mount Schottky Reliability Data Sheet.

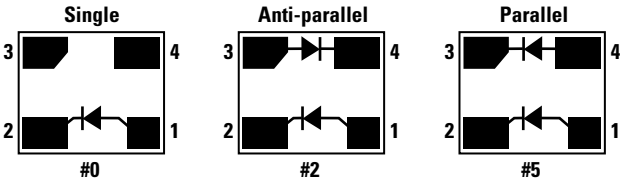
Description/Applications

These ultra-miniature products represent the blending of Agilent Technologies' proven semiconductor and the latest in leadless packaging. This series of Schottky diodes is the most consistent and best all-round device available, and finds applications in mixing, detecting, switching, sampling, clamping and wave shaping at frequencies up to 6 GHz. The MiniPak package offers reduced parasitics when compared to conventional leaded diodes, and lower thermal resistance.

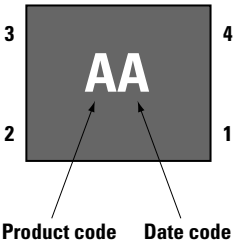
The HMPS-282x family of diodes offers the best all-around choice for most applications, featuring low series resistance, low forward voltage at all current levels and good RF characteristics.

Note that Agilent's manufacturing techniques assure that dice found in pairs and quads are taken from adjacent sites on the wafer, assuring the highest degree of match.

Package Lead Code Identification (Top View)



Pin Connections and Package Marking



Notes:

1. Package marking provides orientation and identification.
2. See "Electrical Specifications" for appropriate package marking.

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HMPS-282x Series Absolute Maximum Ratings[1], T_C = 25°C

Symbol	Parameter	Units	MiniPak 1412
I_f	Forward Current (1 μs pulse)	A	1
P_{IV}	Peak Inverse Voltage	V	15
T_j	Junction Temperature	°C	150
T_{stg}	Storage Temperature	°C	-65 to +150
θ_{jc}	Thermal Resistance[2]	°C/W	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

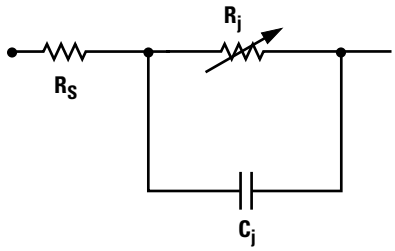
ESD WARNING:
Handling Precautions Should Be Taken To Avoid Static Discharge.

Electrical Specifications, T_C = +25°C, Single Diode[4]

Part Number HMPS-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (V) @ I_F (mA)	Maximum Reverse Leakage I_R (nA) @ V_R (V)	Maximum Capacitance C_T (pF)	Typical Dynamic Resistance R_D (Ω)[4]
2820	L	0	Single	15	340	0.5 10	100 1	1.0	12
2822	K	2	Anti-parallel						
2825	J	5	Parallel						
Test Conditions				I_R = 100 μA	I_F = 1 mA[1]		V_F = 0 V f = 1 MHz[2]	I_F = 5 mA

Notes:
1. ΔV_F for diodes in pairs is 15 mV maximum at 1 mA.
2. ΔC_{TO} for diodes in pairs is 0.2 pF maximum.
3. Effective carrier lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 5 mA.
4. $R_D = R_S + 5.2\Omega$ at 25°C and I_f = 5 mA.

Linear Equivalent Circuit Model Diode Chip



R_S = series resistance (see Table of SPICE parameters)

C_j = junction capacitance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5}\ nT}{I_b + I_s}$$

where

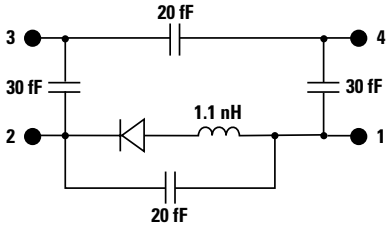
I_b = externally applied bias current in amps

I_s = saturation current (see table of SPICE parameters)

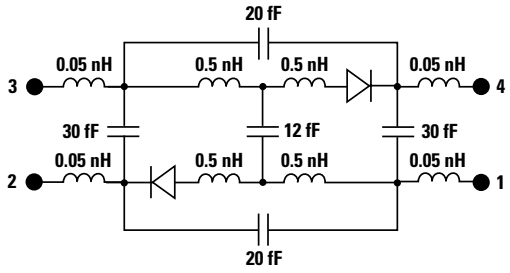
T = temperature, °K

n = ideality factor (see table of SPICE parameters)

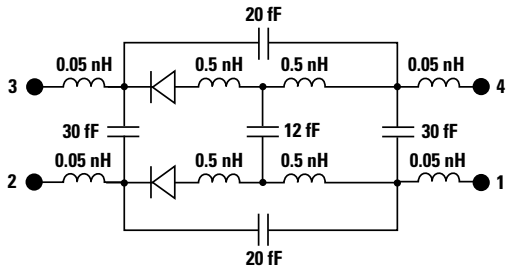
Linear Circuit Model of the Diode's Package



Single diode package (HMPx-x8x0)



Anti-parallel diode package (HMPx-x8x2)



Parallel diode package (HMPx-x8x5)

SPICE Parameters

Parameter	Units	HMPS-282x
B_V	V	15
C_{J0}	pF	0.7
E_G	eV	0.60
I_{BV}	A	1E-4
I_S	A	2.2E-8
N		1.08
R_S	Ω	8.0
P_B	V	0.65
P_T		2
M		0.5

HMPS-282x Series Typical Performance

T_c = 25°C (unless otherwise noted), Single Diode

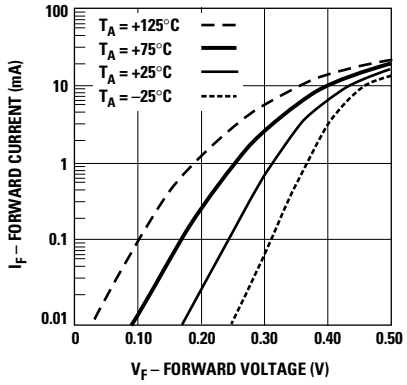


Figure 1. Forward Current vs. Forward Voltage at Temperatures.

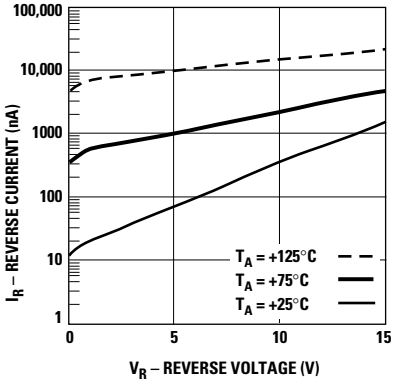


Figure 2. Reverse Current vs. Reverse Voltage at Temperatures.

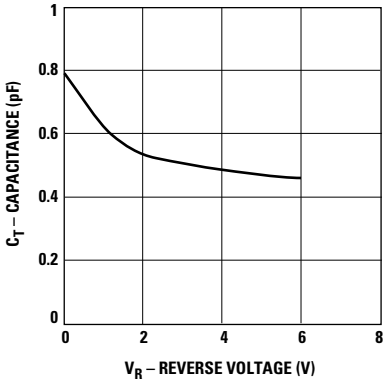


Figure 3. Total Capacitance vs. Reverse Voltage.

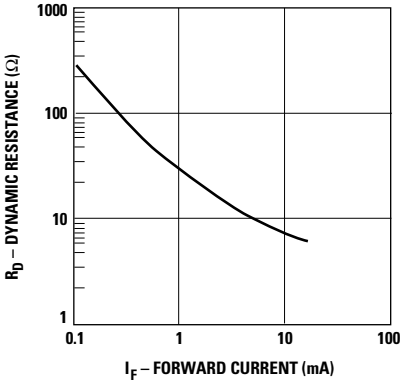


Figure 4. Dynamic Resistance vs. Forward Current.

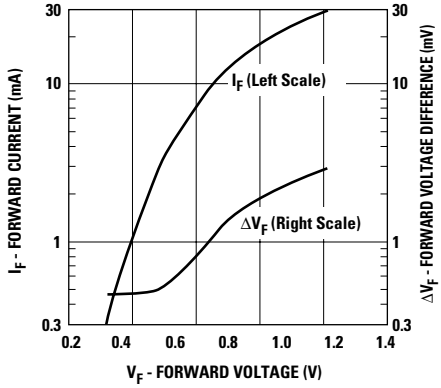


Figure 5. Typical V_f Match, Series Pairs and Quads at Mixer Bias Levels.

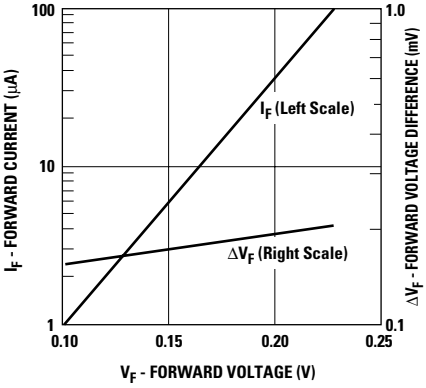


Figure 6. Typical V_f Match, Series Pairs at Detector Bias Levels.

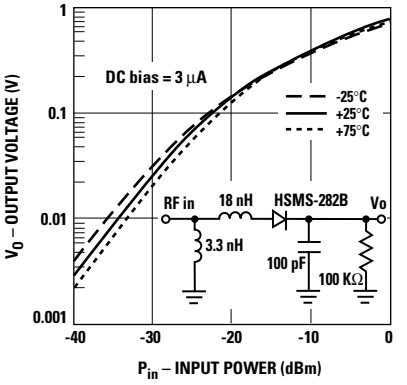


Figure 7. Typical Output Voltage vs. Input Power, Small Signal Detector Operating at 850 MHz.

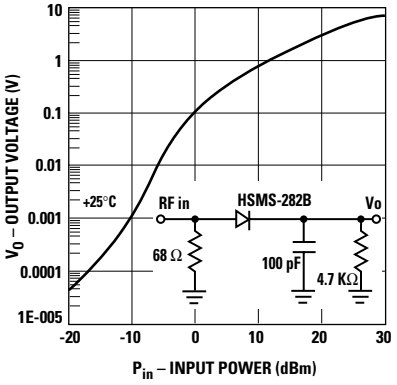


Figure 8. Typical Output Voltage vs. Input Power, Large Signal Detector Operating at 915 MHz.

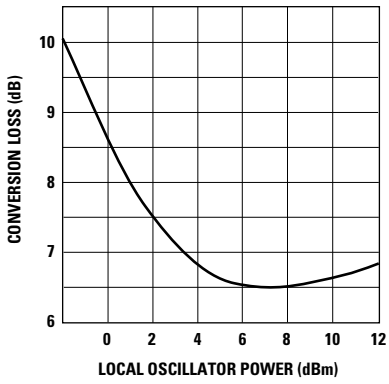


Figure 9. Typical Conversion Loss vs. L.O. Drive, 2.0 GHz (Ref AN997).

Assembly Information

The MiniPak diode is mounted to the PCB or microstrip board using the pad pattern shown in Figure 10.

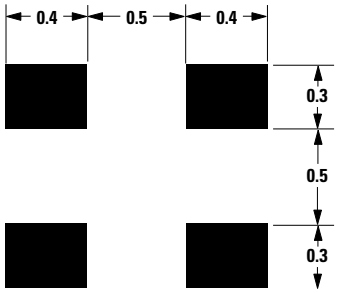


Figure 10. PCB Pad Layout, MiniPak (dimensions in mm).

This mounting pad pattern is satisfactory for most applications. However, there are applications where a high degree of isolation is required between one diode and the other is required. For such applications, the mounting pad pattern of Figure 11 is recommended.

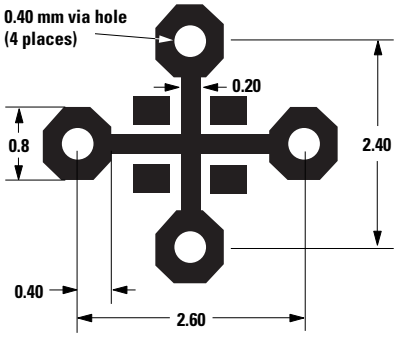


Figure 11. PCB Pad Layout, High Isolation MiniPak (dimensions in mm).

This pattern uses four via holes, connecting the crossed ground strip pattern to the ground plane of the board.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the MiniPak package, will reach solder reflow temperatures faster than those with a greater mass.

Agilent's diodes have been qualified to the time-temperature profile shown in Figure 12. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 255°C.

These parameters are typical for a surface mount assembly process for Agilent diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

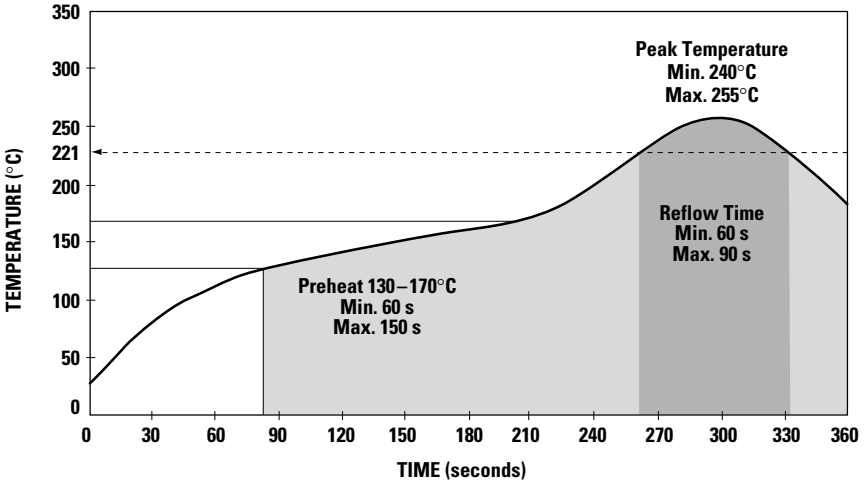
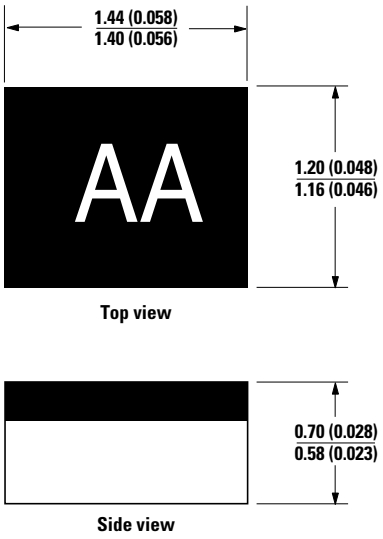
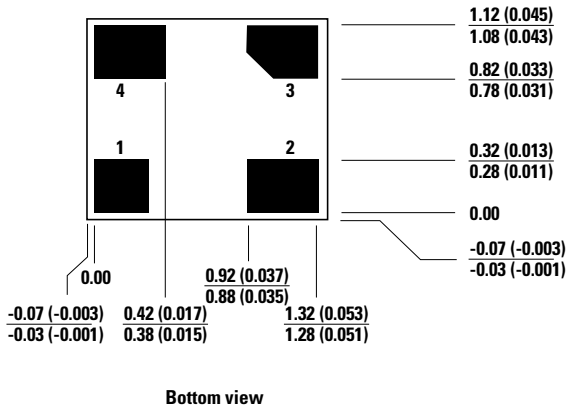


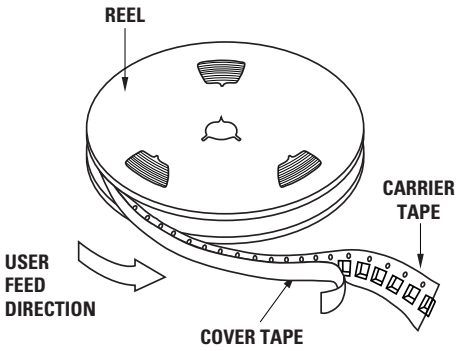
Figure 12. Surface Mount Assembly Temperature Profile.

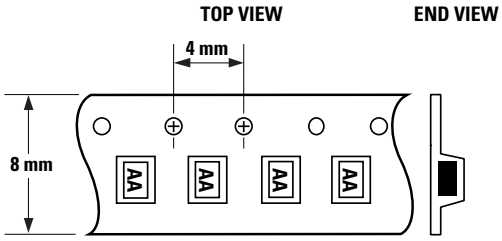
MiniPak Outline Drawing





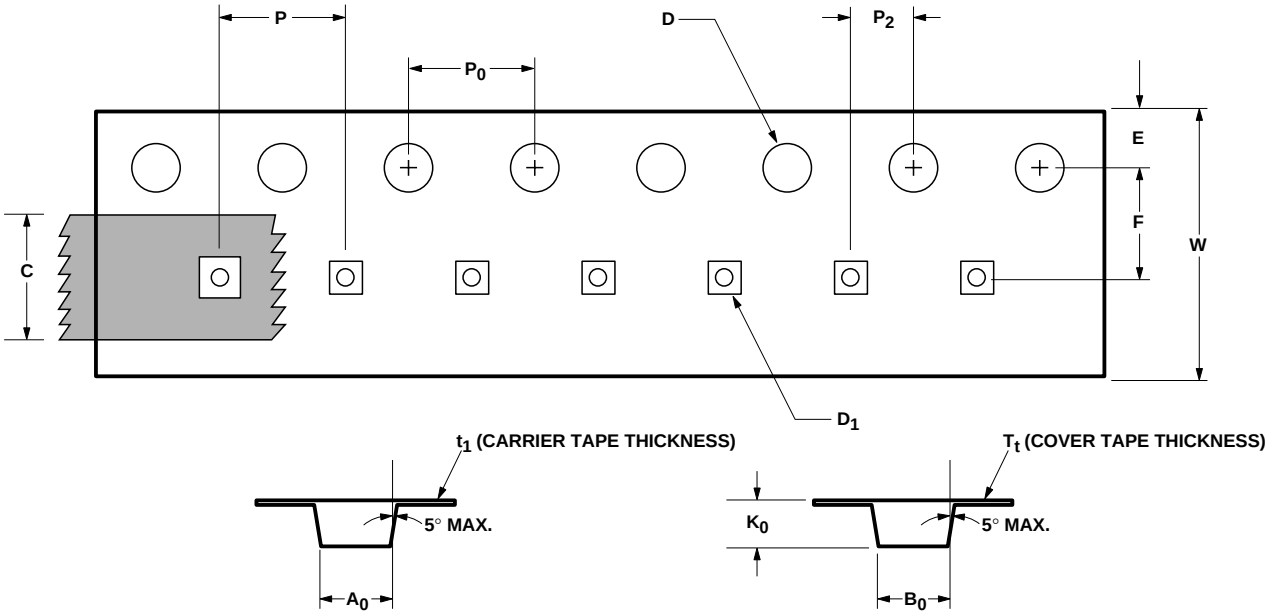
Device Orientation





Note: "AA" represents package marking code. Package marking is right side up with carrier tape perforations at top. Conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement." Standard quantity is 3,000 devices per reel.

Tape Dimensions and Product Orientation For Outline 4T (MiniPak 1412)



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	1.40 ± 0.05	0.055 ± 0.002
	WIDTH	B_0	1.63 ± 0.05	0.064 ± 0.002
	DEPTH	K_0	0.80 ± 0.05	0.031 ± 0.002
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	0.80 ± 0.05	0.031 ± 0.002
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.060 ± 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 - 0.10	0.315 + 0.012 - 0.004
	THICKNESS	t_1	0.254 ± 0.02	0.010 ± 0.001
COVER TAPE	WIDTH	C	5.40 ± 0.10	0.213 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.002 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

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