Data Sheet | January 2003 | FN9025.1

100V/2A Peak, Low Cost, High Frequency Half Bridge Driver

The HIP2101 is a high frequency, 100V Half Bridge N-Channel power MOSFET driver IC available in both 8 lead SOIC and 16 lead MLFP plastic packages. It is equivalent to the HIP2100 with the added advantage of full TTL/CMOS compatible logic input pins. The low-side and high-side gate drivers are independently controlled and matched to 13ns. This gives users total control over dead-time for specific power circuit topologies. Undervoltage protection on both the low-side and high-side supplies force the outputs low. An on-chip diode eliminates the discrete diode required with other driver ICs. A new level-shifter topology yields the low-power benefits of pulsed operation with the safety of DC operation. Unlike some competitors, the high-side output returns to its correct state after a momentary undervoltage of the high-side supply.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HIP2101IB	-40^{o}C to 85^{o}C	8 Ld SOIC	M8.15
HIP2101IBT	-40^{o}C to 85^{o}C	8 Ld SOIC Tape and Reel	M8.15
HIP2101IBZ (Note 1)	-40^{o}C to 85^{o}C	8 Ld SOIC (Lead Free)	M8.15
HIP2101IBZT (Note 1)	-40^{o}C to 85^{o}C	8 Ld SOIC Tape and Reel (Lead Free)	M8.15
HIP2101IR	-40^{o}C to 85^{o}C	16 Ld MLFP	L16.5x5
HIP2101IRT	-40^{o}C to 85^{o}C	16 Ld MLFP Tape and Reel	L16.5x5

NOTE:

1. These products are packaged in 8 ld SOIC packages that are MSL level 1 at 255-260^{o}C peak reflow temperature, which exceeds the IPC J Std-020B requirements for MSL level 1. The lead free and green products employ special lead free material sets including 100% matte tin plate termination finish, which is compatible with either Sn/Pb or lead free soldering operations.

Features

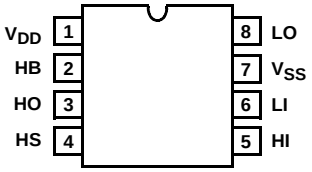
- Drives N-Channel MOSFET Half Bridge
- Space Saving SO8 and Low R_{C-S} Micro Leadframe Packages.
- Lead Free Product Now Available (SO8)
- Bootstrap Supply Max Voltage to 114VDC
- On-Chip 1Ω Bootstrap Diode
- Fast Propagation Times Needed for Multi-MHz Circuits
- Drives 1000pF Load with Rise and Fall Times Typ. 10ns
- TTL/CMOS Input Thresholds Increase Flexibility
- Independent Inputs for Non-Half Bridge Topologies
- No Start-Up Problems
- Outputs Unaffected by Supply Glitches, HS Ringing Below Ground, or HS Slewing at High dv/dt
- Low Power Consumption
- Wide Supply Range
- Supply Undervoltage Protection
- 3Ω Output Resistance

Applications

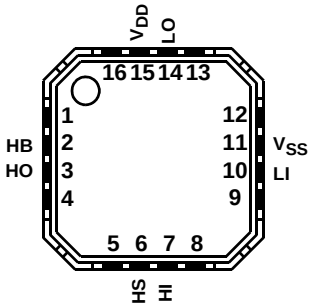
- Telecom Half Bridge Power Supplies
- Avionics DC-DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

Pinouts

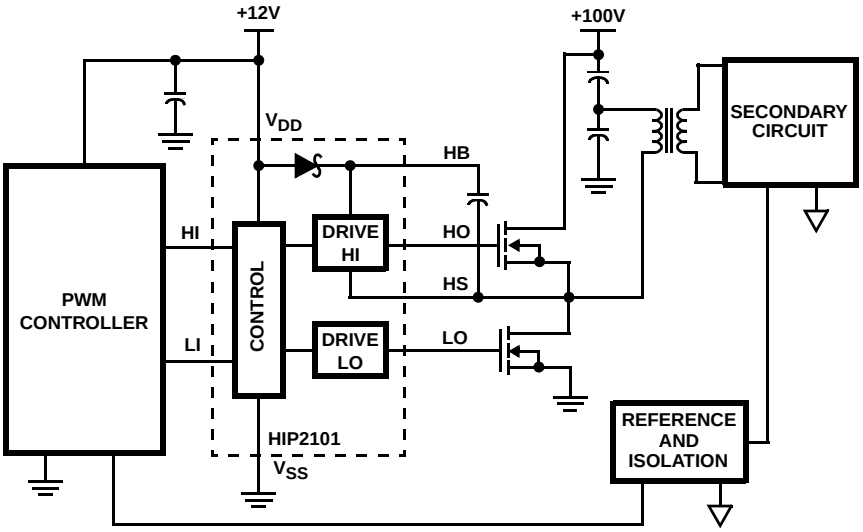
HIP2101 (SOIC)
TOP VIEW



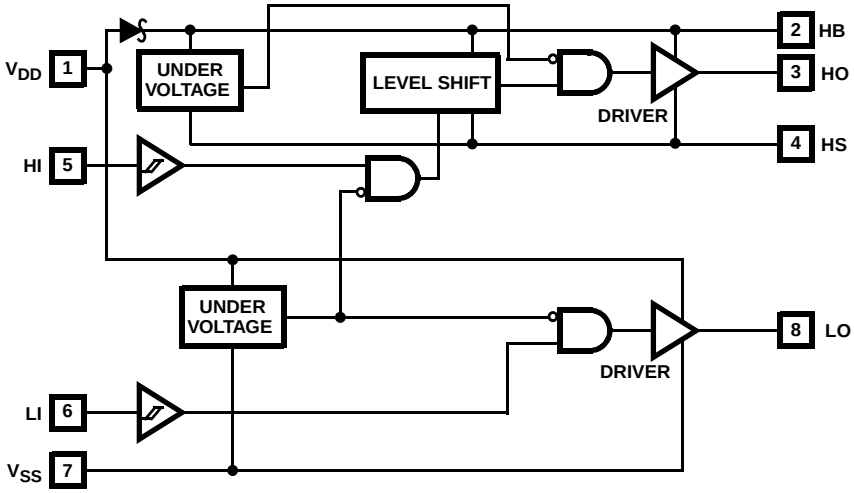
HIP2101 (MLFP)
TOP VIEW



Application Block Diagram



Functional Block Diagram



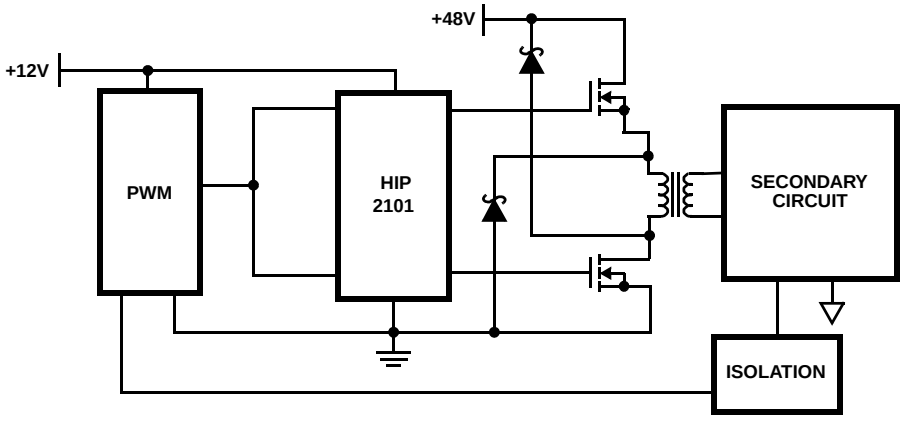


FIGURE 1. TWO-SWITCH FORWARD CONVERTER

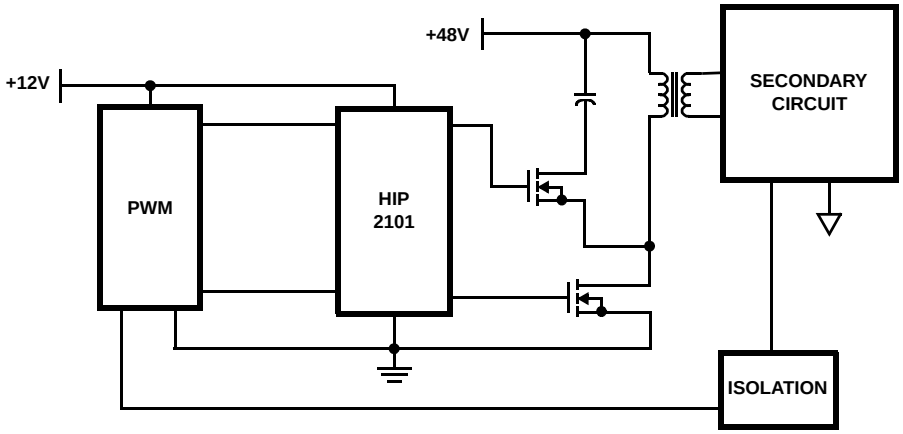


FIGURE 2. FORWARD CONVERTER WITH AN ACTIVE CLAMP

Absolute Maximum Ratings

Supply Voltage, V_{DD}, V_{HB}-V_{HS} (Notes 2, 3) . . . . . -0.3V to 18V
LI and HI Voltages (Note 3) . . . . . -0.3V to 7.0V
Voltage on LO (Note 3) . . . . . -0.3V to V_{DD} +0.3V
Voltage on HO (Note 3) . . . . . V_{HS} -0.3V to V_{HB} +0.3V
Voltage on HS (Continuous) (Note 3) . . . . . -1V to 110V
Voltage on HB (Note 3) . . . . . +118V
Average Current in V_{DD} to HB diode 100mA
ESD Classification . . . . . Class 1 (1kV)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (^{O}C/W)
SOIC (Note 4)	160
MLFP on Thermal Conductive Copper (Note 5)	35

Max Power Dissipation at 25^{O}C in Free Air (SOIC, Note 4). 780mW
Max Power Dissipation at 25^{O}C in Free Air (MLFP, Note 5). . . .3.5W
Storage Temperature Range . . . . . -65^{O}C to 150^{O}C
Junction Temperature Range. . . . . -55^{O}C to 150^{O}C
Lead Temperature (Soldering 10s - Lead Tips Only). . . . . 300^{O}C

Maximum Recommended Operating Conditions

Supply Voltage, V_{DD} . . . . . .+9V to 14.0VDC
Voltage on HS . . . . . -1V to 100V
Voltage on HS . . . . . .(Repetitive Transient) -5V to 105V
Voltage on HB V_{HS} +8V to V_{HS} +14.0V and V_{DD} -1V to V_{DD} +100V
HS Slew Rate. . . . . .< 50V/ns

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the recommended operating conditions of this specification is not implied.

NOTES:

2. The HIP2100 is capable of derated operation at supply voltages exceeding 14V. Figure 16 shows the high-side voltage derating curve for this mode of operation.
3. All Voltages Referenced to Pin 7, V_{SS} Unless Otherwise Specified.
4. θ_{JA} is measured with the component mounted on a low thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Electrical Specifications

V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = 25^{O}C			T_J = -40^{O}C TO 125^{O}C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS								
V_{DD} Quiescent Current	I_{DD}	LI = HI = 0V	-	0.3	0.45	-	0.6	mA
V_{DD} Operating Current	I_{DDO}	f = 500kHz	-	1.7	3.0	-	3.4	mA
Total HB Quiescent Current	I_{HB}	LI = HI = 0V	-	0.1	0.15	-	0.2	mA
Total HB Operating Current	I_{HBO}	f = 500kHz	-	1.5	2.5	-	3	mA
HB to V_{SS} Current, Quiescent	I_{HBS}	V_{HS} = V_{HB} = 114V	-	0.05	1.5	-	10	μA
HB to V_{SS} Current, Operating	I_{HBSO}	f = 500kHz	-	0.7	-	-	-	mA
INPUT PINS								
Low Level Input Voltage Threshold	V_{IL}		0.8	1.65	-	0.8	-	V
High Level Input Voltage Threshold	V_{IH}		-	1.65	2.2	-	2.2	V
Input Pulldown Resistance	R_I		-	200	-	100	500	kΩ
UNDER VOLTAGE PROTECTION								
V_{DD} Rising Threshold	V_{DDR}		7	7.3	7.8	6.5	8	V
V_{DD} Threshold Hysteresis	V_{DDH}		-	0.5	-	-	-	V
HB Rising Threshold	V_{HBR}		6.5	6.9	7.5	6	8	V
HB Threshold Hysteresis	V_{HBH}		-	0.4	-	-	-	V
BOOT STRAP DIODE								
Low-Current Forward Voltage	V_{DL}	I_{VDD-HB} = 100μA	-	0.45	0.70	-	0.7	V
High-Current Forward Voltage	V_{DH}	I_{VDD-HB} = 100mA	-	0.7	0.92	-	1	V
Dynamic Resistance	R_D	I_{VDD-HB} = 100mA	-	0.8	1	-	1.5	Ω

Electrical Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^oC$			$T_J = -40^oC$ TO 125^oC		UNITS
			MIN	TYP	MAX	MIN	MAX	
LO GATE DRIVER								
Low Level Output Voltage	V_{OLL}	I_{LO} = 100mA	-	0.25	0.3	-	0.4	V
High Level Output Voltage	V_{OHL}	I_{LO} = -100mA, $V_{OHL} = V_{DD}-V_{LO}$	-	0.25	0.3	-	0.4	V
Peak Pullup Current	I_{OHL}	V_{LO} = 0V	-	2	-	-	-	A
Peak Pulldown Current	I_{OLL}	V_{LO} = 12V	-	2	-	-	-	A
HO GATE DRIVER								
Low Level Output Voltage	V_{OLH}	I_{HO} = 100mA	-	0.25	0.3	-	0.4	V
High Level Output Voltage	V_{OHH}	I_{HO} = -100mA, $V_{OHH} = V_{HB}-V_{HO}$	-	0.25	0.3	-	0.4	V
Peak Pullup Current	I_{OHH}	V_{HO} = 0V	-	2	-	-	-	A
Peak Pulldown Current	I_{OLH}	V_{HO} = 12V	-	2	-	-	-	A

Switching Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^oC$			$T_J = -40^oC$ TO 125^oC		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}		-	25	43	-	56	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}		-	25	43	-	56	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}		-	25	43	-	56	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}		-	25	43	-	56	ns
Delay Matching: Lower Turn-On and Upper Turn-Off	t_{MON}		-	2	13	-	16	ns
Delay Matching: Lower Turn-Off and Upper Turn-On	t_{MOFF}		-	2	13	-	16	ns
Either Output Rise/Fall Time	t_{RC},t_{FC}	C_L = 1000pF	-	10	-	-	-	ns
Either Output Rise/Fall Time (3V to 9V)	t_R,t_F	C_L = 0.1µF	-	0.5	0.6	-	0.8	us
Either Output Rise Time Driving DMOS	t_{RD}	C_L = IRFR120	-	20	-	-	-	ns
Either Output Fall Time Driving DMOS	t_{FD}	C_L = IRFR120	-	10	-	-	-	ns
Minimum Input Pulse Width that Changes the Output	t_{PW}		-	-	-	-	50	ns
Bootstrap Diode Turn-On or Turn-Off Time	t_{BS}		-	10	-	-	-	ns

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Supply to lower gate drivers. De-couple this pin to V_{SS} (Pin 7). Bootstrap diode connected to HB (pin 2).
2	HB	High-Side Bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
3	HO	High-Side Output. Connect to gate of High-Side power MOSFET.
4	HS	High-Side Source connection. Connect to source of High-Side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
5	HI	High-Side input.
6	LI	Low-Side input.
7	V_{SS}	Chip negative supply, generally will be ground.
8	LO	Low-Side Output. Connect to gate of Low-Side power MOSFET.

Timing Diagrams

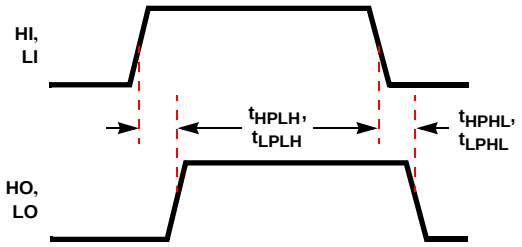


FIGURE 3.

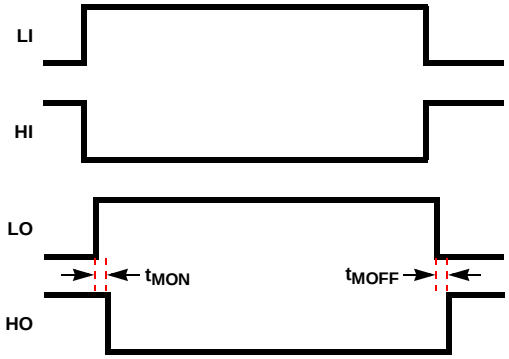


FIGURE 4.

Typical Performance Curves

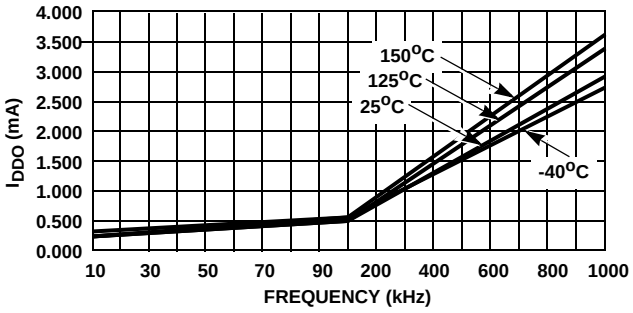


FIGURE 5A.

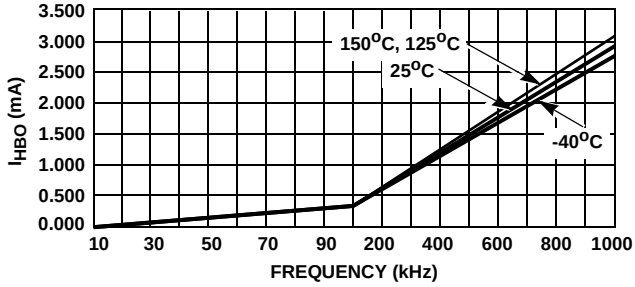


FIGURE 5B.

FIGURE 5. OPERATING CURRENT vs FREQUENCY

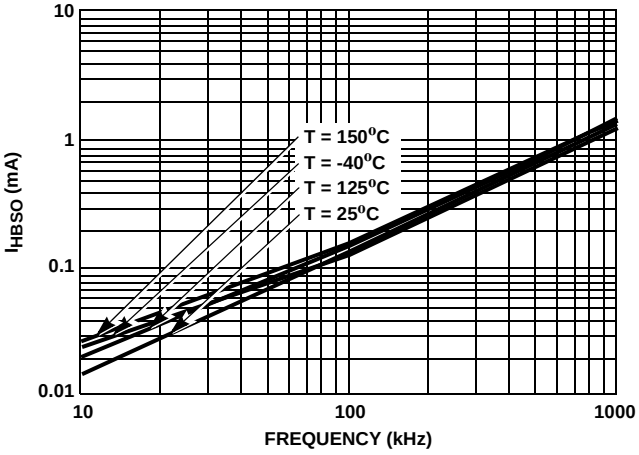


FIGURE 6. HB TO VSS OPERATING CURRENT vs FREQUENCY

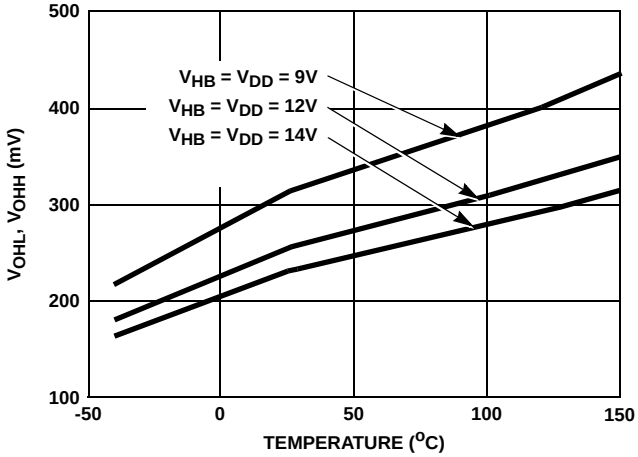


FIGURE 7. HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

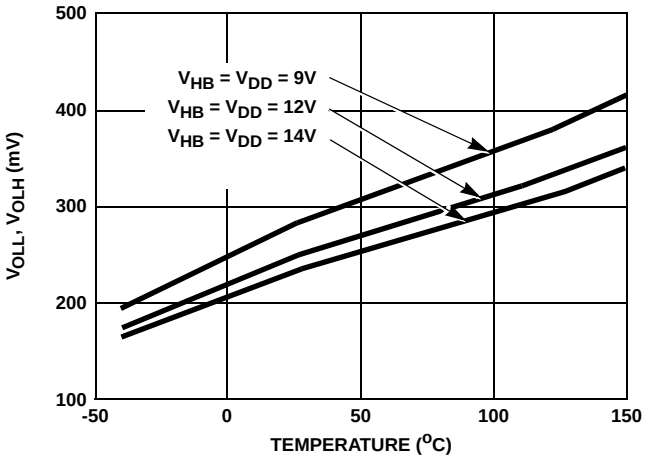


FIGURE 8. LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

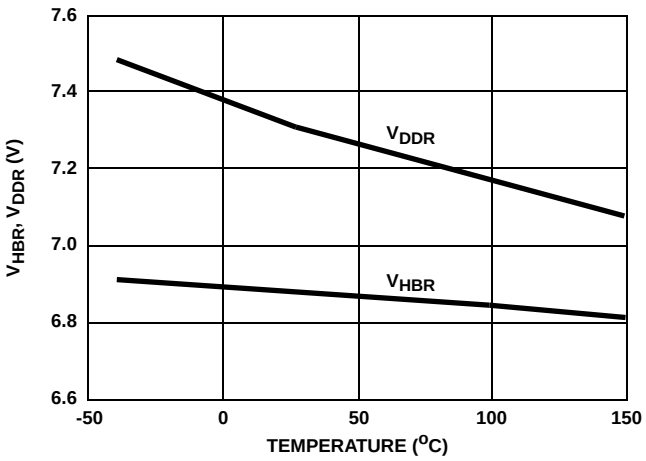


FIGURE 9. UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

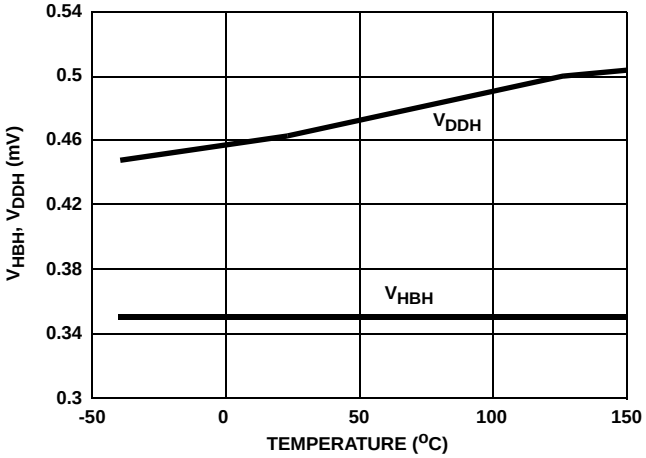


FIGURE 10. UNDERVOLTAGE LOCKOUT HYSTERESIS vs TEMPERATURE

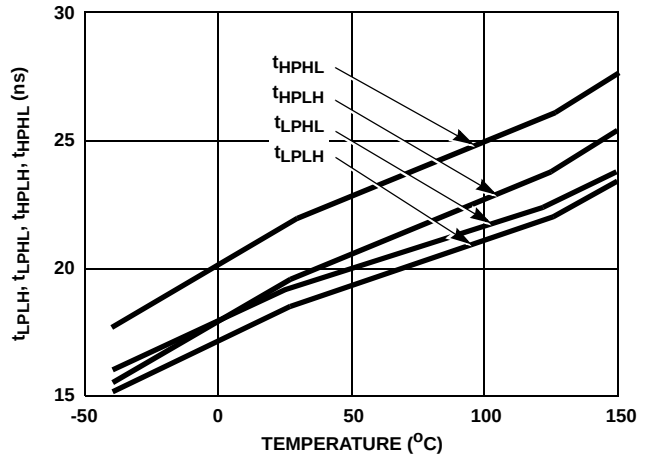


FIGURE 11. PROPAGATION DELAYS vs TEMPERATURE

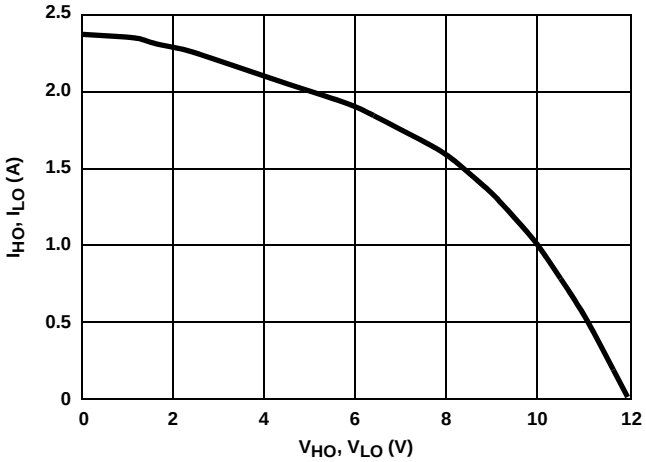


FIGURE 12. PEAK PULLUP CURRENT vs OUTPUT VOLTAGE

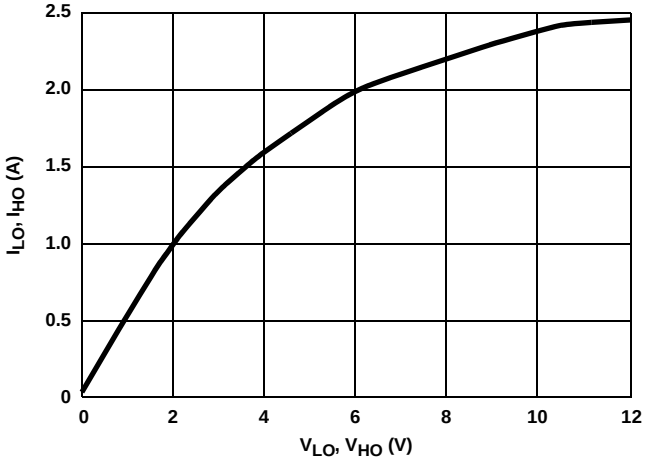


FIGURE 13. PEAK PULLDOWN CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

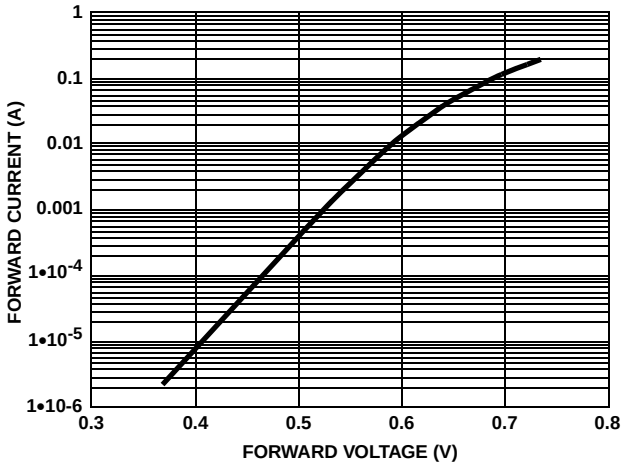


FIGURE 14. BOOTSTRAP DIODE I-V CHARACTERISTICS

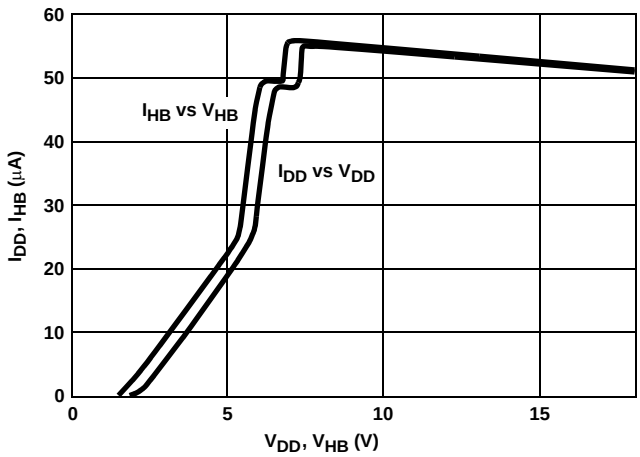


FIGURE 15. QUIESCENT CURRENT vs VOLTAGE

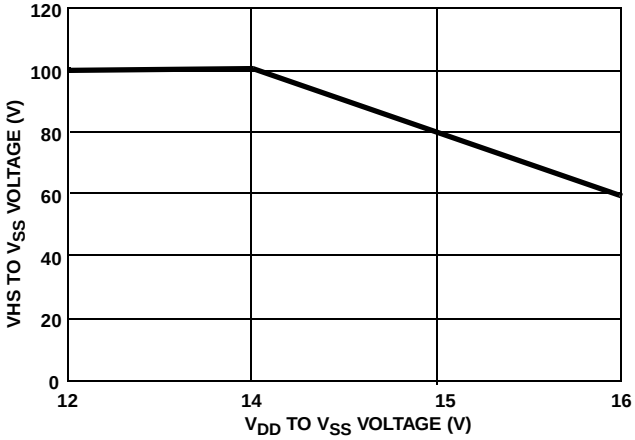
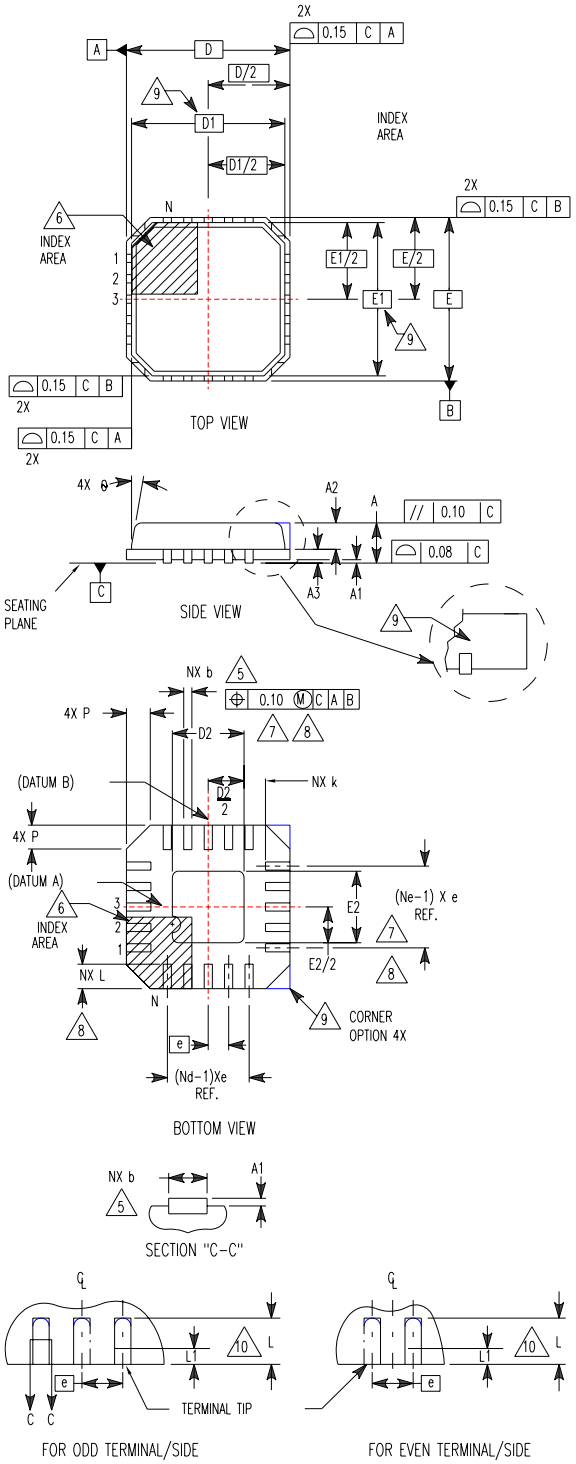


FIGURE 16. VHS VOLTAGE vs V_{DD} VOLTAGE

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.5x5

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHB ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.28	0.33	0.40	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.55	2.70	2.85	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.55	2.70	2.85	7, 8
e		0.80 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne	4	4		3
P	-	-	0.60	9
θ	-	-	12	9

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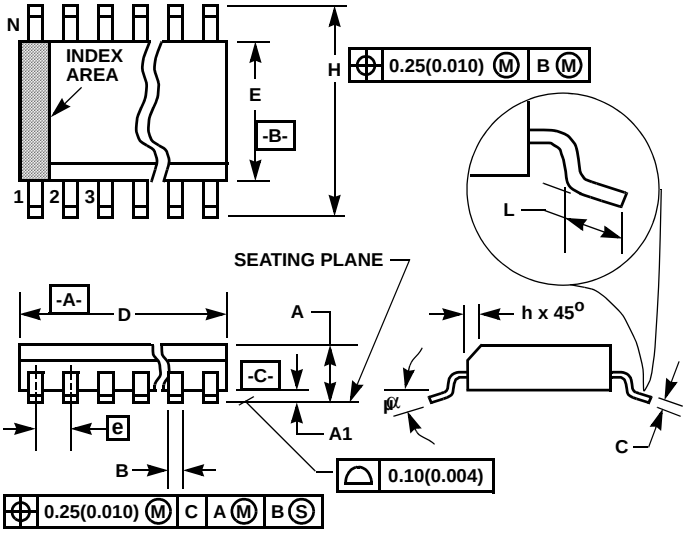
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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