

16 Channel High Voltage Analog Switch with Bleed Resistors

Features

- ❑ HVC MOS technology for high performance
- ❑ 220V operating conditions
- ❑ Output On-resistance typically 22Ω
- ❑ Integrated bleed resistors on the outputs
- ❑ 5.0V and 12.0V CMOS logic compatibility
- ❑ Very low quiescent power dissipation -10 μ A
- ❑ -45dB min off isolation at 7.5MHz
- ❑ Low parasitic capacitance
- ❑ Excellent noise immunity
- ❑ Flexible operating supply voltages

Applications

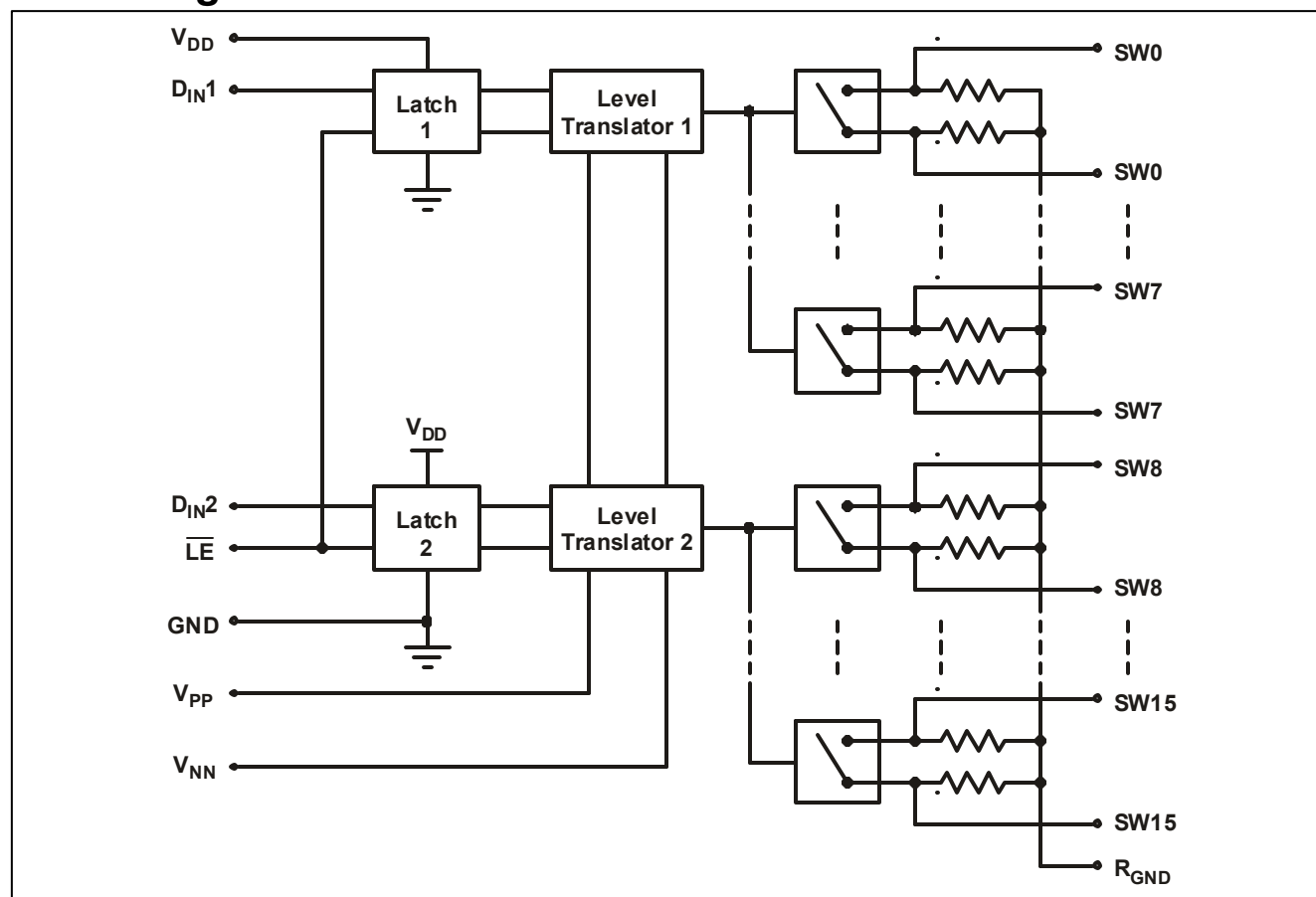
- ❑ Medical ultrasound imaging
- ❑ Piezoelectric transducer drivers

Description

The Supertex HV238 is a 220V 16-channel high voltage analog switch integrated circuit (IC) with output bleed resistors (R_{INT}). The output switches are configured as 2 sets of 8 single pole single throw analog switches. It is intended to be used in applications requiring high voltage switching controlled by low voltage control signals such as ultrasound imaging.

The 2 sets of 8 analog switches are controlled by 2 input logic controls, D_{IN1} and D_{IN2} . A logic high on D_{IN1} will turn ON switches 0 to 7 and a logic high on D_{IN2} will turn ON switches 8 to 15. The bleed resistors help significantly reduce voltage built up on capacitive loads such as piezoelectric transducers connected to the outputs.

Block Diagram



Ordering Information

Device	Package Options
	48 Lead TQFP
HV238	HV238FG

Absolute Maximum Ratings*

V_{DD} Logic supply	-0.5V to +15V
V_{PP} - V_{NN} differential supply	225V
V_{PP} Positive supply	-0.5V to V_{NN} +225V
V_{NN} Negative supply	+0.5V to -225V
Logic input voltage	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation	48 lead TQFP 1.0W

**Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.*

Operating Conditions*

Symbol	Parameter	Value
V_{PP}	Positive high voltage supply	50V to 110V
V_{NN}	Negative high voltage supply	-10V to V_{PP} -220V
V_{DD}	Logic power supply voltage	4.75V to 12.6V
V_{IH}	High level input voltage	V_{DD} -1.0V to V_{DD}
V_{IL}	Low level input voltage	0V to 1.0V
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air temperature	0°C to 70°C

*** Notes:**

- 1 Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
- 2 V_{SIG} must be within V_{NN} and V_{PP} or floating during power up/down transition.
- 3 Rise and fall times of power supplies V_{DD} , V_{PP} , and V_{NN} should not be less than 1.0msec.

Truth Table

D_{IN2}	D_{IN1}	LE bar	SW0 to SW7	SW8 to SW15
L	L	L	OFF	OFF
L	H	L	ON	OFF
H	L	L	OFF	ON
H	H	L	ON	ON
X	X	H	Hold Previous State	

Electrical Characteristics

DC Characteristics *(over recommended operating conditions unless otherwise noted)*

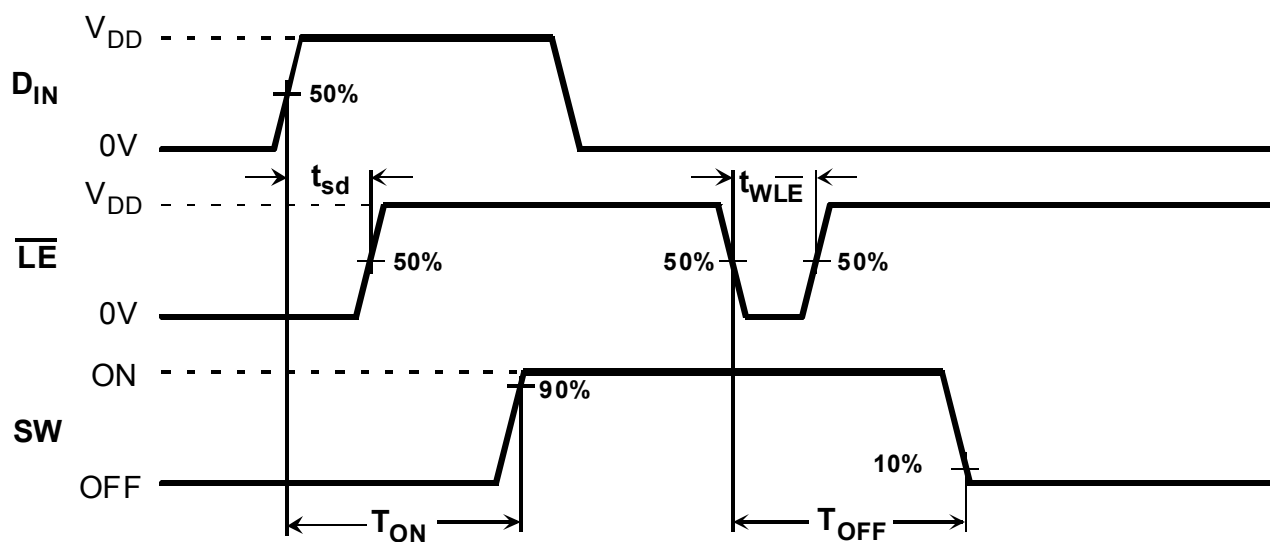
Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
R _{ONS}	Small Signal Switch On-Resistance		30		26	32		40	Ω	V _{SIG} =0V, I _{SIG} =5mA, V _{PP} =50V, V _{NN} =-170V
			25		22	27		35		V _{SIG} =0V, I _{SIG} =200mA, V _{PP} =50V, V _{NN} =-170V
			15		22	27		30		V _{SIG} =0V, I _{SIG} =5mA, V _{PP} =110V, V _{NN} =-110V
			20		18	22		25		V _{SIG} =0V, I _{SIG} =200mA, V _{PP} =110V, V _{NN} =-110V
ΔR _{ONS}	Small Signal Switch On-Resistance Matching		20		5.0	20		20	%	V _{SIG} =0V, I _{SIG} =5mA, V _{PP} =110V, V _{NN} =-110V
R _{ONL}	Large Signal Switch On-Resistance				15				Ω	V _{SIG} =0V, I _{SIG} =1.0A
R _{INT}	Output Switch Shunt Resistance			20	35	50			KΩ	Output Switch to R _{GND} I _{RINT} = 0.5mA
I _{SOL}	Switch Off Leakage per Switch		5.0		1.0	10		15	μA	V _{SIG} = V _{PP} -10V and V _{NN} =+10V
	DC offset Switch off		300		100	300		300	mV	No Load
	DC offset Switch on		500		100	500		500	mV	No Load
I _{PPQ}	Quiescent V _{PP} supply current				10	50			μA	All switches off
I _{NNQ}	Quiescent V _{NN} supply current				-10	-50			μA	All switches off
I _{PPQ}	Quiescent V _{PP} supply current				10	50			μA	All switches on, I _{SW} =5mA
I _{NNQ}	Quiescent V _{NN} supply current				-10	-50			μA	All switches on, I _{SW} =5mA
	Switch output peak current		3.0		3.0	2.0		2.0	A	V _{SIG} duty cycle < 0.1%
f _{SW}	Output switch frequency					50			kHz	Duty cycle=50%
I _{PP}	Average V _{PP} supply current		6.5			8.8		10	mA	V _{PP} =50V, V _{NN} =-170V, All Switches turning ON and OFF at 50kHz
I _{NN}	Average V _{NN} supply current		8.1			-8.8		-10		
I _{PP}	Average V _{PP} supply current		-8.1			6.3		6.9	mA	V _{PP} =110V, V _{NN} =-110V, All Switches turning ON and OFF at 50kHz
I _{NN}	Average V _{NN} supply current		5.0			-6.3		-6.9		
I _{DDQ}	Quiescent V _{DD} supply current		10			10		10	μA	All logic inputs are static
I _{DD}	Average V _{DD} supply current		2.0			2.0		2.0	mA	D _{IN1} = D _{IN2} =3MHz, LE bar =high
C _{IN}	Logic input capacitance		10			10		10	pF	

Electrical Characteristics

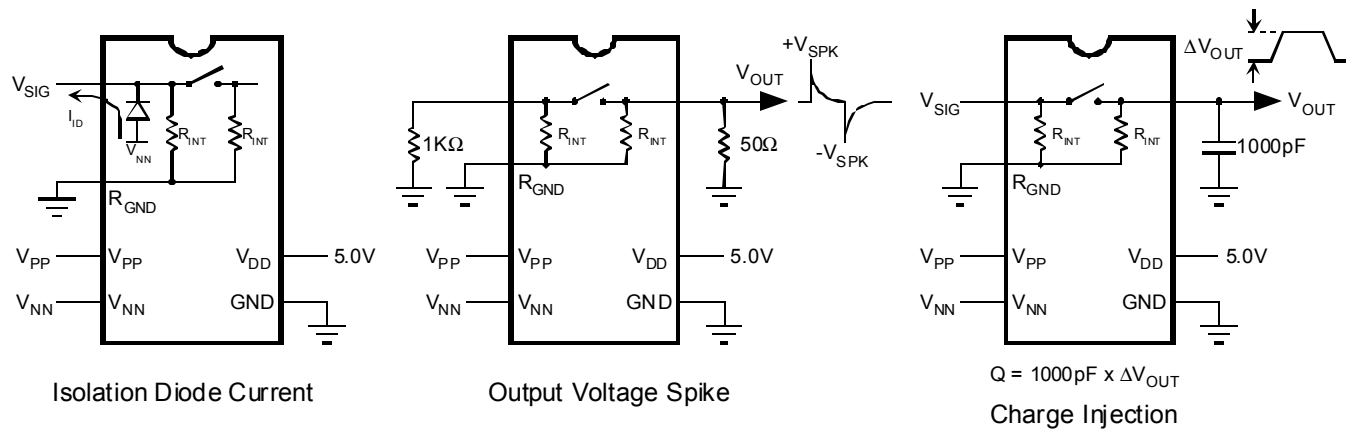
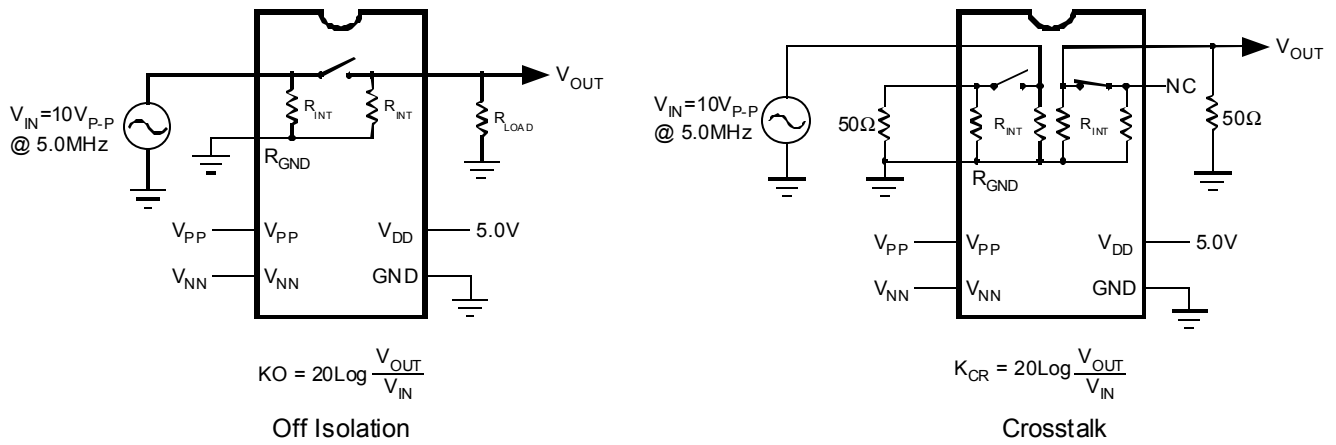
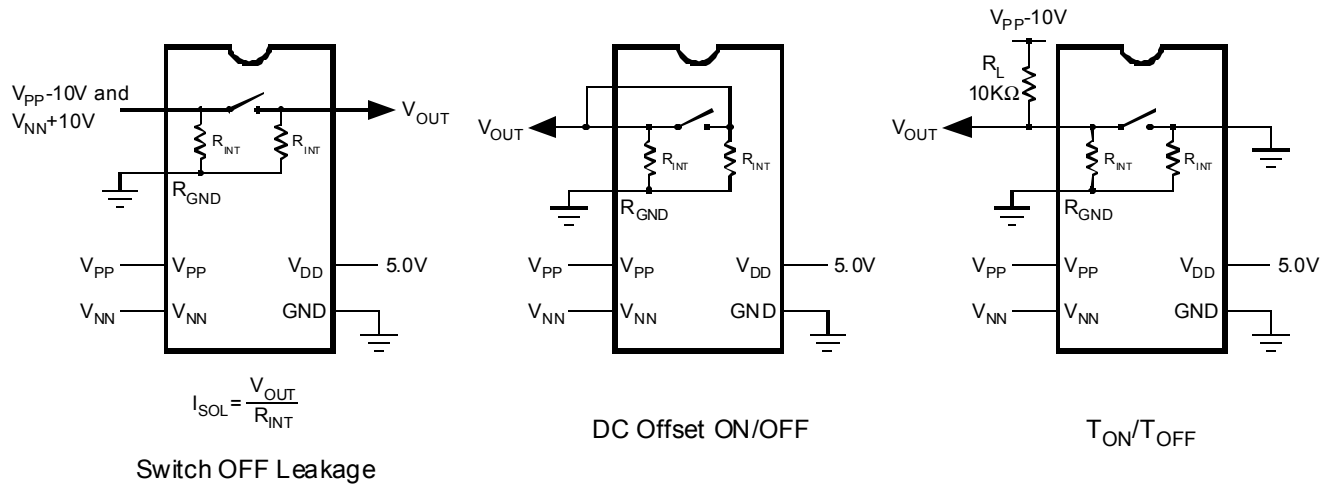
AC Characteristics (over recommended operating conditions unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{WLE}	Time Width of LE bar	150		150			150		ns	
t_{WDIN}	Time Width of D_{IN}	150		150			150		ns	
t_{SD}	Set Up Time Before LE bar Rises	150		150			150		ns	
T_{ON}	Turn On Time		2.0			2.0		2.0	μs	$V_{SIG}=V_{PP}-10V$, $R_{LOAD}=10K\Omega$
T_{OFF}	Turn Off Time		2.0			2.0		2.0	μs	$V_{SIG}=V_{PP}-10V$, $R_{LOAD}=10K\Omega$
dv/dt	Maximum V_{sig} Slew Rate		20			20		20	V/ns	
KO	Off Isolation	-30		-30	-33		-30		dB	$f=5MHz$, Load= $1K\Omega//15pF$
		-45		-45	-50		-45			$f=7.5MHz$, $R_{LOAD}=50\Omega$
K_{CR}	Switch Crosstalk	-45		-45			-45		dB	$f=5.0MHz$, $R_{LOAD}=50\Omega$
I_{ID}	Output Switch Isolation Diode Current		300			300		300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off Capacitance Switch to Gnd	5.0	17	5.0	12	17	5.0	17	pF	$V_{SIG}=0V$, $f=1.0MHz$
$C_{SG(ON)}$	On Capacitance Switch to Gnd	25	50	25	38	50	25	50	pF	$V_{SIG}=0V$, $f=1.0MHz$
$+V_{SPK}$	Output Voltage Spike				4.0				V	$R_{LOAD}=50\Omega$
$-V_{SPK}$					-4.0					

Logic Timing Diagram



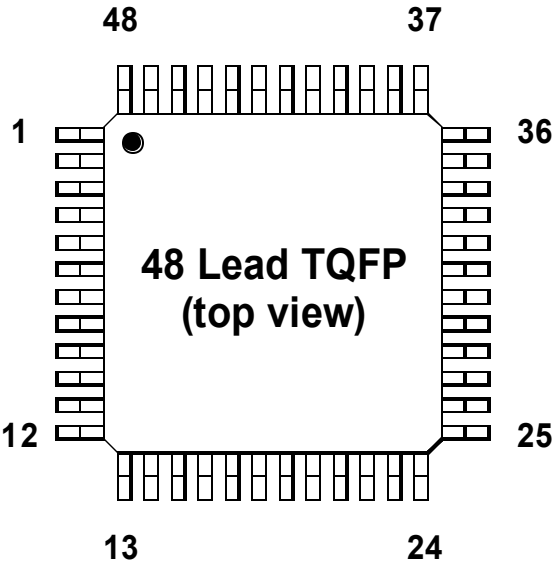
Test Circuits



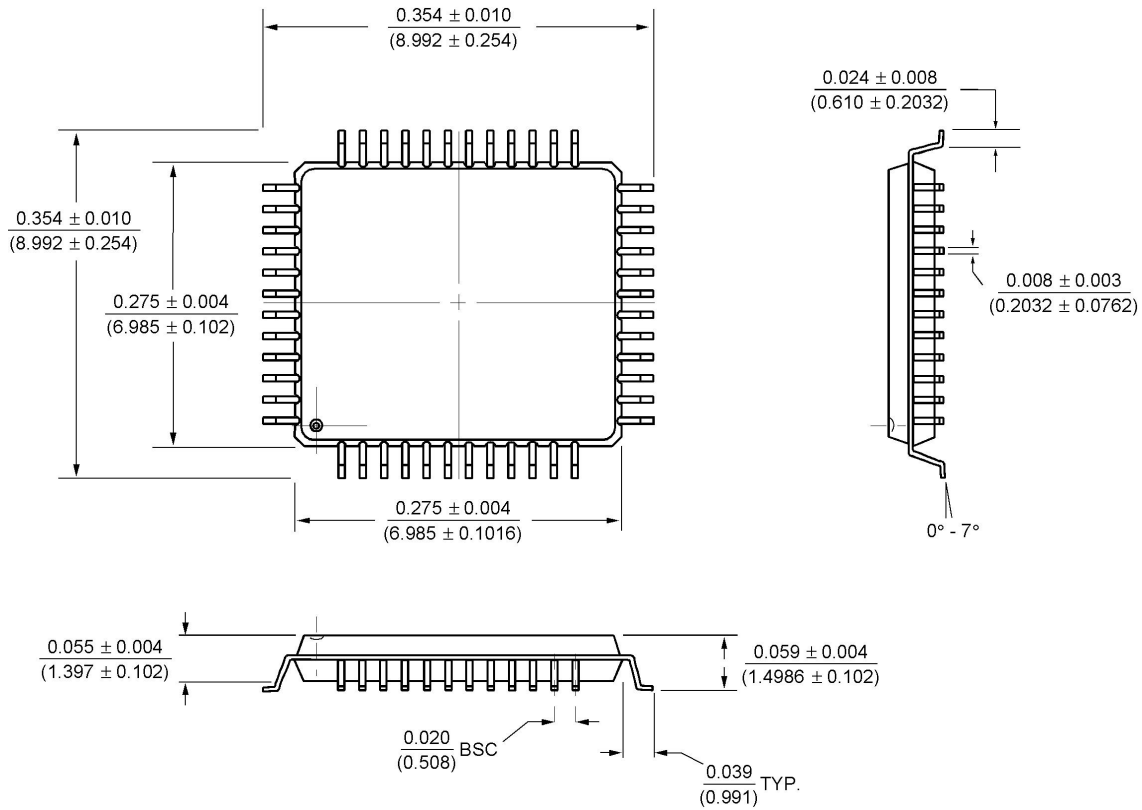
Pin Configurations

48 Lead TQFP

Pin	Function	Pin	Function
1	V _{NN}	25	SW10
2	N/C	26	SW10
3	V _{PP}	27	SW9
4	N/C	28	SW9
5	D _{IN1}	29	SW8
6	LE bar	30	SW8
7	D _{IN2}	31	SW7
8	N/C	32	SW7
9	N/C	33	SW6
10	V _{DD}	34	SW6
11	GND	35	SW5
12	N/C	36	SW5
13	R _{GND}	37	SW4
14	SW15	38	N/C
15	SW15	39	SW4
16	SW14	40	N/C
17	SW14	41	SW3
18	SW13	42	SW3
19	SW13	43	SW2
20	SW12	44	SW2
21	SW12	45	SW1
22	SW11	46	SW1
23	SW11	47	SW0
24	N/C	48	SW0



48-Lead TQFP Package Dimension



Measurement Legend = $\frac{\text{Dimensions in Inches}}{(\text{Dimensions in Millimeters})}$

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