8 MHz, 64-Channel Serial To Parallel Converter With Push-Pull Outputs

Ordering Information

Device	Package Options			
	80 Lead Quad Ceramic Gullwing	**80 Lead Quad Plastic Gullwing**	**80 Lead Quad Ceramic Gullwing** (MIL-STD-883 Processed*)	**Die**
HV57908	HV57908DG	HV57908PG	RBHV57908DG	HV57908X

*For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- ❏ Processed with HVCMOS® technology
- ❏ 5V CMOS logic
- ❏ Output voltages up to 80V
- ❏ Low power level shifting
- ❏ 8MHz data rate
- ❏ Latched data outputs
- ❏ Forward and reverse shifting options (DIR pin)
- ❏ Diode to V_{PP} allows efficient power recovery
- ❏ Outputs may be hot switched
- ❏ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.5V to +7.5V
Output voltage, V_{PP}		-0.5V to +90V
Logic input levels		-0.3V to V_{DD} +0.3V
Ground current[2]		1.5A
Continuous total power dissipation[3]	Plastic Ceramic	1200mW 1900mW
Operating temperature range	Plastic Ceramic	-40°C to 85°C -55°C to 125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to GND.
2. Limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 19mW/°C for ceramic.

General Description

The HV579 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for electroluminescent displays. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capability such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

The device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to GND, and CW shifting when connected to V_{DD}. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HV_{OUT} 64). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift registers to the latches occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latches is stored when $\overline{LE}$ is low.

Electrical Characteristics (over recommended operating conditions unless noted, T_A=-40°C to +85°C)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	$V_{DD} = V_{DD}$ max f_{CLK} = 8MHz
I_{PP}	High voltage supply current			100	µA	Outputs high
				100	µA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current			100	µA	All $V_{IN} = V_{DD}$
V_{OH}	High-level output	HV_{OUT}	65		V	I_O= -15mA, V_{PP} = 80V
		Data out	V_{DD} - 0.5		V	I_O= -100µA
V_{OL}	Low-level output	HV_{OUT}		7	V	I_O = 12mA, V_{PP} = 80V
		Data out		0.5	V	I_O= 100µA
I_{IH}	High-level logic input current			1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V
V_{OC}	High voltage clamp diode			1	V	I_{OC} = 1mA

AC Characteristics (T_A = 85°C max. Logic signal inputs and Data inputs have t_r, $t_f \leq$ 5ns [10% and 90% points])

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_{WL},t_{WH}	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	10		ns	
t_H	Data hold time after clock rises	15		ns	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}		500	ns	C_L = 15pF
t_{DHL}	Delay time clock to data high to low		70	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		70	ns	C_L = 15pF
t_{DLE}*	Delay time clock to $\overline{LE}$ low to high	25		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	25		ns	
t_{SLE}	$\overline{LE}$ set-up time before clock rises	0		ns	

* t_{DLE} is not required but is recommended to produce stable HV outputs and thus minimize power dissipation and current spikes (allows internal SR output to stabilize).

Recommended Operating Conditions

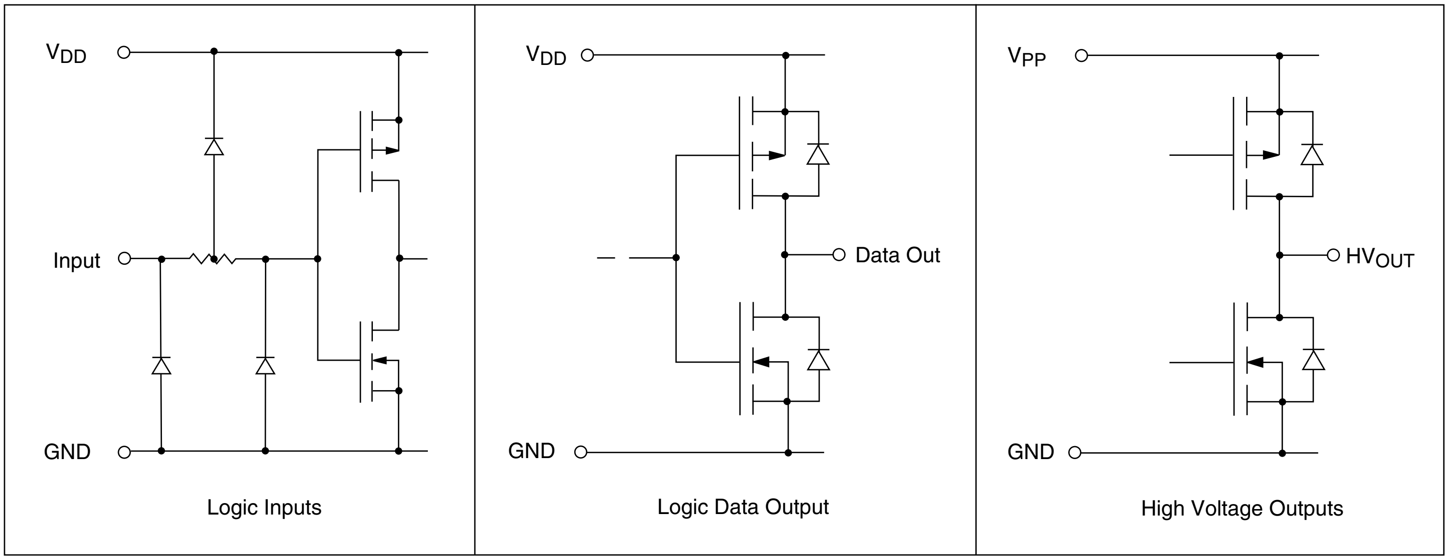
Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		4.5	5.5	V
V_{PP}	Output voltage		8	80	V
V_{IH}	High-level input voltage		V_{DD} -0.5		V
V_{IL}	Low-level input voltage		0	0.5	V
f_{CLK}	Clock frequency			8	MHz
T_A	Operating free-air temperature	Plastic	-40	+85	°C
		Ceramic	-55	+125	

Note: Power-up sequence should be the following:

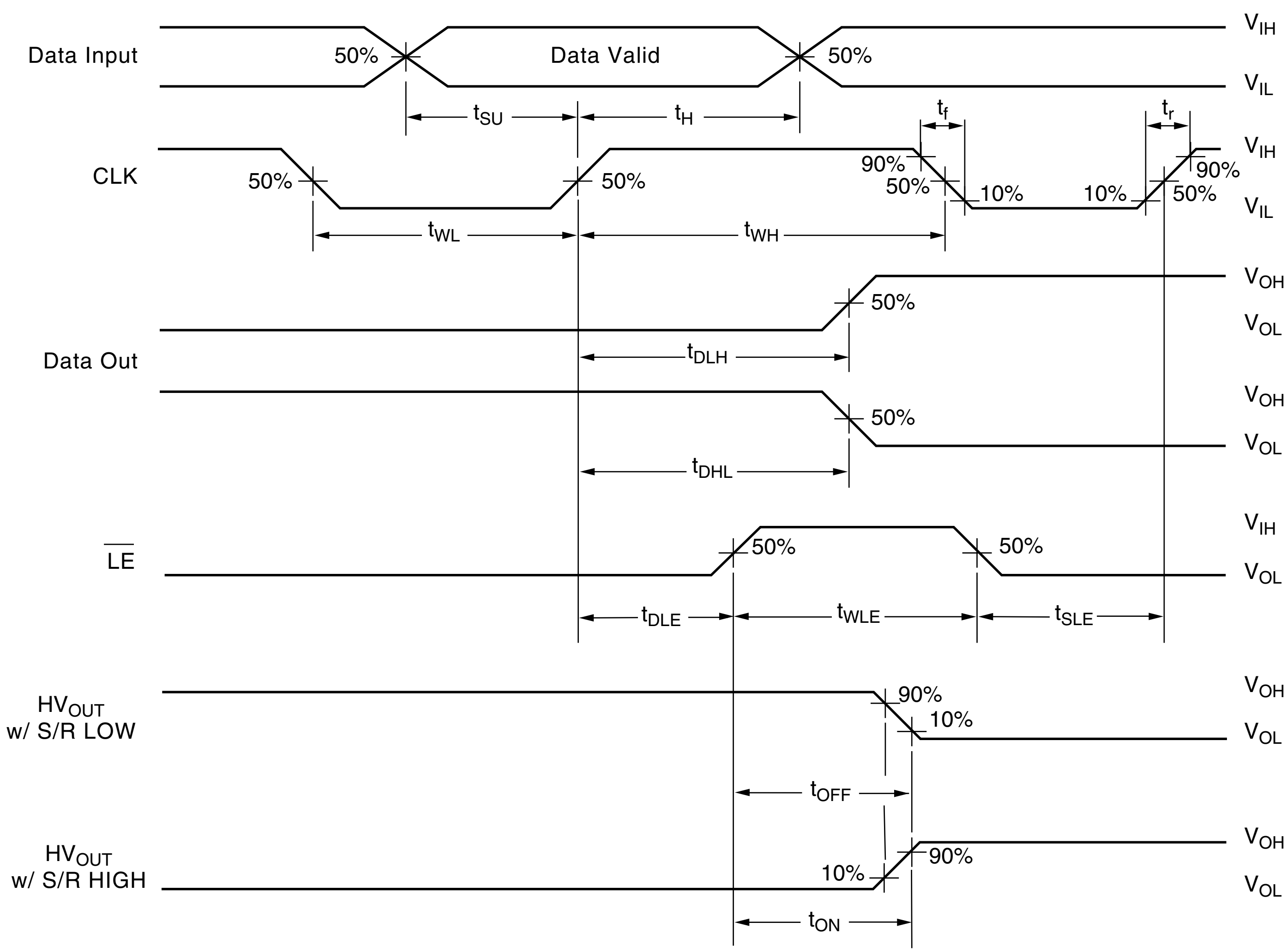
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.
5. The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

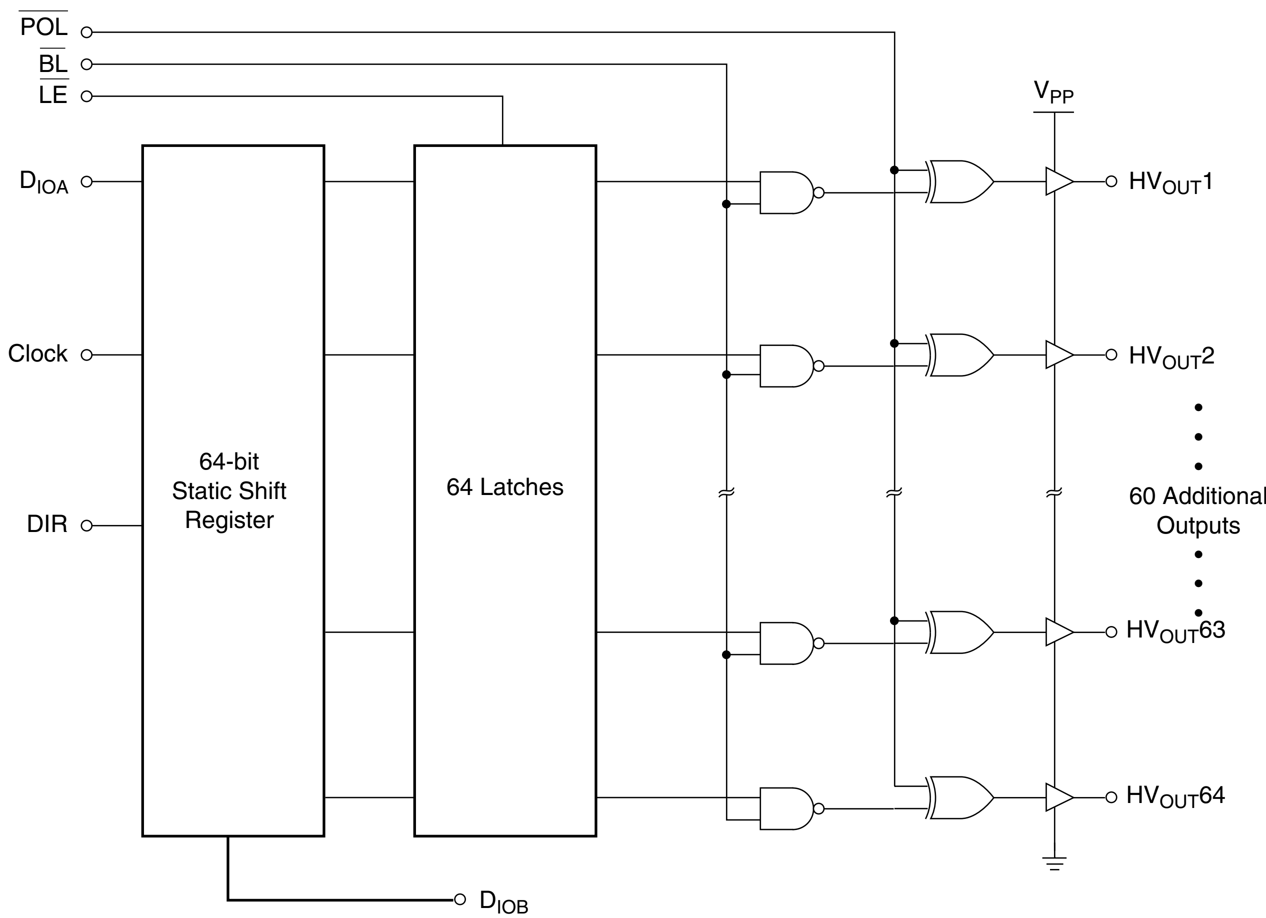
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	**Shift Reg**	**HV Outputs**	**Data Out**
All O/P High	X	X	X	L	L	X		H	
All O/P Low	X	X	X	L	H	X		L	
O/P Normal	X	X	X	H	H	X		No inversion	
O/P Inverted	X	X	X	H	L	X		Inversion	
Data Falls Through (Latches Transparent)	L	↑	H	H	H	X	L	L	
	H	↑	H	H	H	X	H	H	
	L	↑	H	H	L	X	L	H	
	H	↑	H	H	L	X	H	L	
Data Stored	X	X	L	H	H	X	*	Stored Data	
Latches Loaded	X	X	L	H	L	X	*	Inversion of Stored Data	
I/O Relation	D_{IOA}	↑	X	X	X	H	$Q_n \rightarrow Q_{n+1}$	-	D_{IOB}
	D_{IOB}	↑	X	X	X	L	$Q_n \rightarrow Q_{n-1}$	-	D_{IOA}

Note: * = dependent on previous stage's state.

Pin Configurations

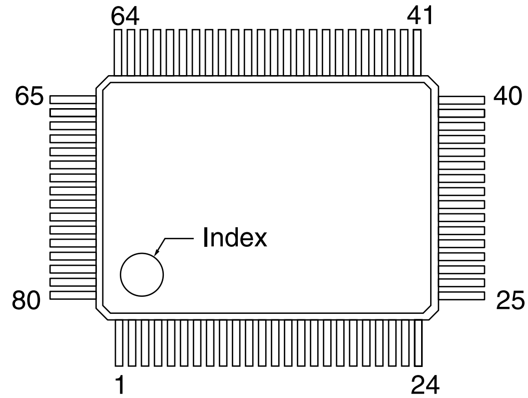
HV579

80-pin Gullwing

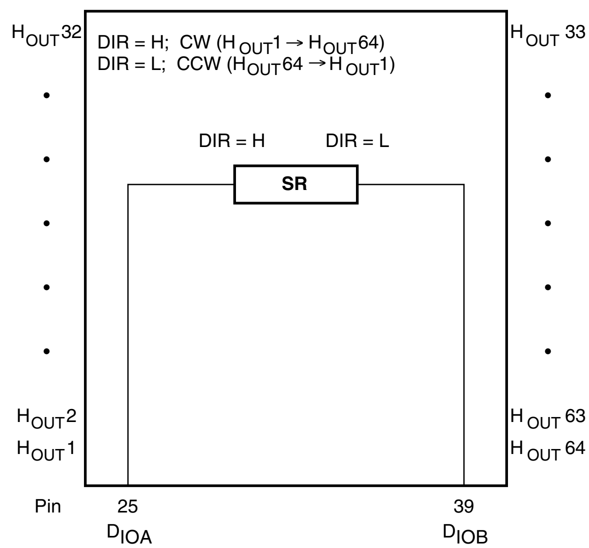
Pin	Function	Pin	Function
1	HV_{OUT} 24/41	41	HV_{OUT} 64/1
2	HV_{OUT} 23/42	42	HV_{OUT} 63/2
3	HV_{OUT} 22/43	43	HV_{OUT} 62/3
4	HV_{OUT} 21/44	44	HV_{OUT} 61/4
5	HV_{OUT} 20/45	45	HV_{OUT} 60/5
6	HV_{OUT} 19/46	46	HV_{OUT} 59/6
7	HV_{OUT} 18/47	47	HV_{OUT} 58/7
8	HV_{OUT} 17/48	48	HV_{OUT} 57/8
9	HV_{OUT} 16/49	49	HV_{OUT} 56/9
10	HV_{OUT} 15/50	50	HV_{OUT} 55/10
11	HV_{OUT} 14/51	51	HV_{OUT} 54/11
12	HV_{OUT} 13/52	52	HV_{OUT} 53/12
13	HV_{OUT} 12/53	53	HV_{OUT} 52/13
14	HV_{OUT} 11/54	54	HV_{OUT} 51/14
15	HV_{OUT} 10/55	55	HV_{OUT} 50/15
16	HV_{OUT} 9/56	56	HV_{OUT} 49/16
17	HV_{OUT} 8/57	57	HV_{OUT} 48/17
18	HV_{OUT} 7/58	58	HV_{OUT} 47/18
19	HV_{OUT} 6/59	59	HV_{OUT} 46/19
20	HV_{OUT} 5/60	60	HV_{OUT} 45/20
21	HV_{OUT} 4/61	61	HV_{OUT} 44/21
22	HV_{OUT} 3/62	62	HV_{OUT} 43/22
23	HV_{OUT} 2/63	63	HV_{OUT} 42/23
24	HV_{OUT} 1/64	64	HV_{OUT} 41/24
25	D_{IOA}	65	HV_{OUT} 40/25
26	N/C	66	HV_{OUT} 39/26
27	N/C	67	HV_{OUT} 38/27
28	N/C	68	HV_{OUT} 37/28
29	$\overline{LE}$	69	HV_{OUT} 36/29
30	CLK	70	HV_{OUT} 35/30
31	$\overline{BL}$	71	HV_{OUT} 34/31
32	V_{DD}	72	HV_{OUT} 33/32
33	DIR	73	HV_{OUT} 32/33
34	GND	74	HV_{OUT} 31/34
35	$\overline{POL}$	75	HV_{OUT} 30/35
36	N/C	76	HV_{OUT} 29/36
37	N/C	77	HV_{OUT} 28/37
38	N/C	78	HV_{OUT} 27/38
39	D_{IOB}	79	HV_{OUT} 26/39
40	V_{PP}	80	HV_{OUT} 25/40

Note:
Pin designation for DIR = H/L.
Example: For DIR = H, pin 41 is HV_{OUT} 64.
For DIR = L, pin 41 is HV_{OUT} 1.

Package Outline



top view
80-pin Gullwing Package



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