Preliminary

8-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs, POL, Hi-Z, and Short Detect

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Option
		24 Lead SOW
HV513	250V	HV513WG

Features

- ❑ HVCMOS® technology
- ❑ Operating voltage of 250V
- ❑ Shift register speed 8MHz @ V_{DD}=5V
- ❑ 8 latch data outputs
- ❑ Output polarity and blanking
- ❑ CMOS compatible inputs
- ❑ Output short circuit detect
- ❑ Output high-Z control

Applications

- ❑ Piezoelectric transducer driver
- ❑ Weaving applications

General Description

The device consists of an 8-bit shift register, 8 latches, and control logic to perform polarity select and blanking of the outputs. Data is shifted through the shift register on the low to high transition of the clock. A data output buffer is provided for cascading devices. Operation of the shift register is not affected by the $\overline{LE}$, $\overline{BL}$, $\overline{POL}$, or the $\overline{HI\text{-}Z}$ control inputs. Transfer of data from the shift register to the latch occurs when $\overline{LE}$ is high. The data in the latch is stored when $\overline{LE}$ goes low. A $\overline{HI\text{-}Z}$ pin is provided to set all the outputs in a high-Z state.

All outputs have a short circuit detection circuit that is activated when the voltage drop across any output transistor is excessive. Under normal operation, this output will briefly pulse low during output transistions; see Short Circuit Timing Diagram for details.

All outputs have break-before-make circuitry to reduce cross-over current during output state changes.

The $\overline{POL}$, $\overline{BL}$, $\overline{LE}$, and $\overline{HIZ}$ inputs have an internal pull up resistor.

Absolute Maximum Ratings*

Supply Voltage, V_{DD}	-0.5V to 6V
Supply Voltage, V_{PP}	V_{DD} to 270V
Logic input levels	-0.5V to V_{DD}+0.5V
Ground current	0.3A
High voltage supply current	0.25A
Continuous total power dissipation	750mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C +150°C

* All voltages are referenced to device ground.

DC Electrical Characteristics (Over operating supply voltages unless otherwise noted, T_A=25°C)

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
I_{DD}	V_{DD} supply current				4	mA	f_{CLK}=8MHz, $\overline{LE}$=LOW
I_{DDQ}	Quiescent V_{DD} supply current				0.1	mA	All V_{IN}= V_{DD}
					2.0		All V_{IN}=0V
I_{PP}	V_{PP} supply current				1.0	mA	V_{PP}=250V, f_{OUT}=300Hz, no load
I_{PPQ}	Quiescent V_{PP} supply current				100	µA	V_{PP}=250V, outputs static
V_{IH}	High-level input voltage		V_{DD} –0.9V		V_{DD}	V	
V_{IL}	Low-level input voltage		0		0.9	V	
I_{IH}	High-level logic input current				10	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current				-10	µA	D_{IN} and CLK, V_{IL}=0V
					-350		$\overline{POL}$, $\overline{BL}$, $\overline{LE}$, and $\overline{HIZ}$, V_{IL}=0V
V_{OH}	High-level output	HV_{OUT}	V_{PP} –60V			V	IHV_{OUT}=-20mA, V_{PP}=200V
		Data out	V_{DD} –0.5V				I_{DOUT}=-0.1mA
V_{OL}	Low-level output	HV_{OUT}			60	V	IHV_{OUT}=20mA
		Data out			0.5		I_{DOUT}=0.1mA
V_{SH}	Short voltage, output high			10		V	
V_{SL}	Short voltage, output low			10		V	

AC Electrical Characteristics (Over operating supply voltages unless otherwise noted, T_A=25°C)

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
f_{CLK}	Clock frequency	0		8	MHz	
t_{WL} , t_{WH}	Clock width high and low	50			ns	
t_{SU}	Data setup time before clock rises	35			ns	
t_H	Data hold time after clock rises	30			ns	
t_{WLE}	Width of latch enable pulse	80			ns	
t_{DLE}	$\overline{LE}$ delay time after rising edge of clock	35			ns	
t_{SLE}	$\overline{LE}$ setup time before rising edge of clock	40			ns	
$t_{R,}$ t_F	Rise/fall time of HV_{OUT}			1000	µs	C_L=100nF, V_{PP}=200V
				1		C_L=40pF, V_{PP}=200V
$t_{d\ ON/OFF}$	Delay time for output to start rise/fall			500	ns	
t_{DHL}	Delay time clock to D_{OUT} high to low			90	ns	C_L=15pF
t_{DLH}	Delay time clock to D_{OUT} low to high			90	ns	C_L=15pF
t_{SD}	Output short circuit detection			500	ns	Short to output fall of $\overline{SHORT}$, C_L=15pF
t_{SC}	Output short circuit clear			1000	ns	Short clear to output rise of $\overline{SHORT}$
t_{HI-Z}	Delay to HiZ			500	ns	

Note: Logic inputs have 5ns rise and fall times.

Recommended Operating Conditions

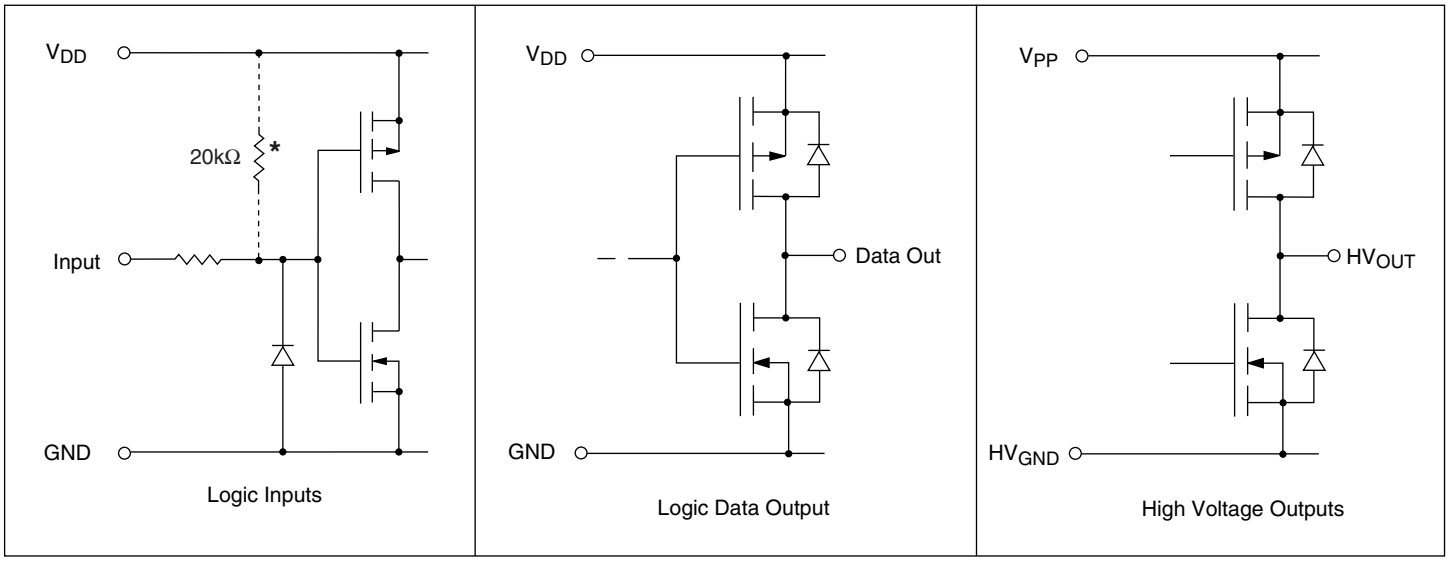
Symbol	Parameters	Min	Typ	Max	Unit	Conditions
f_{OUT}	Output switching frequency (SOA limited)		300		Hz	C_L=50nF, V_{PP}=200V
V_{DD}	Logic supply voltage	4.5	5.0	5.5	V	
V_{PP}	High voltage supply	50		250	V	

Notes:

1. Below minimum V_{PP} the output may not switch.
2. Power-up sequence should be the following:
    1. Connect ground.
    2. Apply V_{DD}.
    3. Set all inputs to a known state.
    4. Apply V_{PP}.
    5. The V_{PP} should not drop below V_{DD} or float during operation.

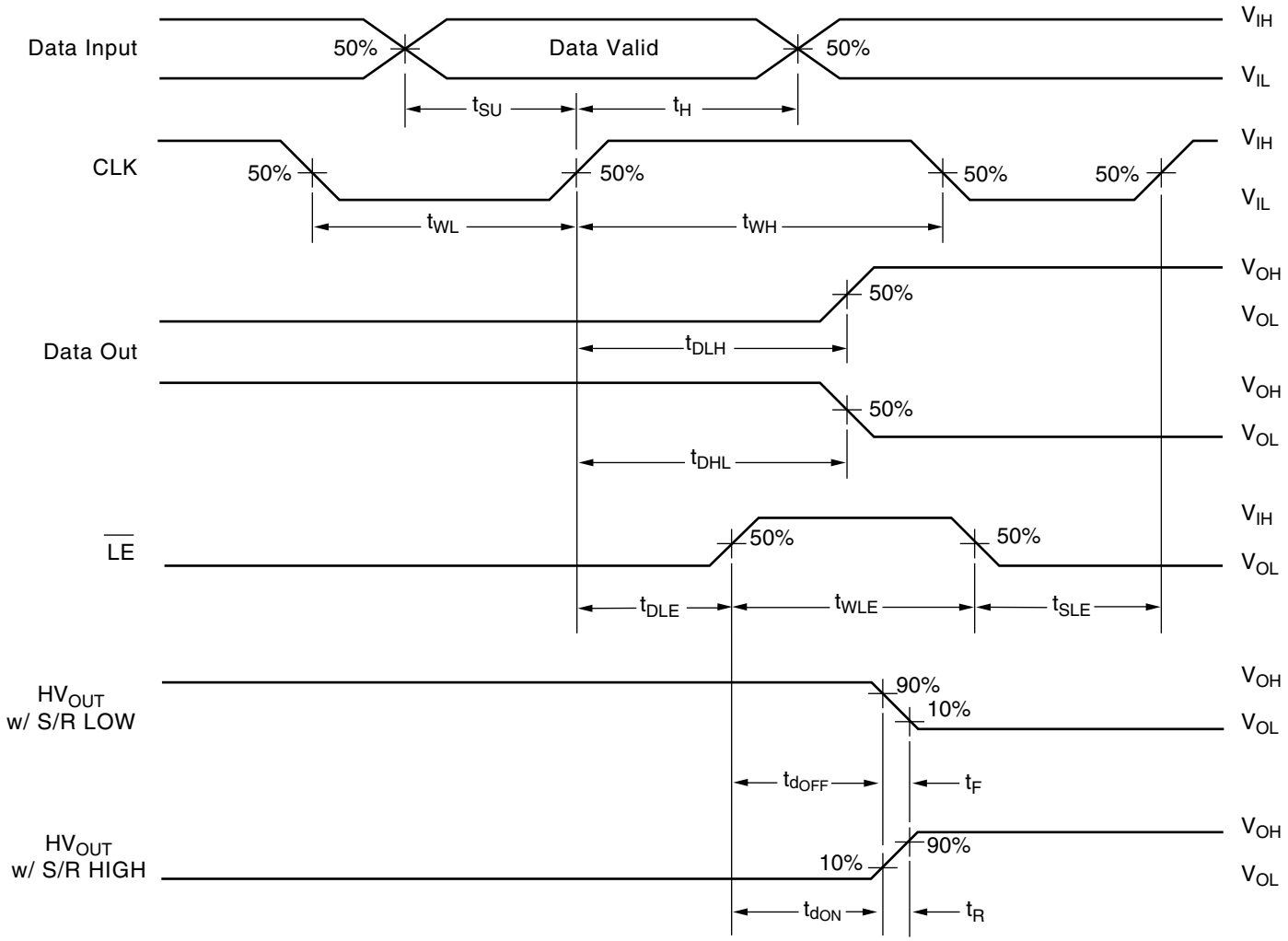
Power-down sequence should be the reverse of the above.

Input and Output Equivalent Circuits

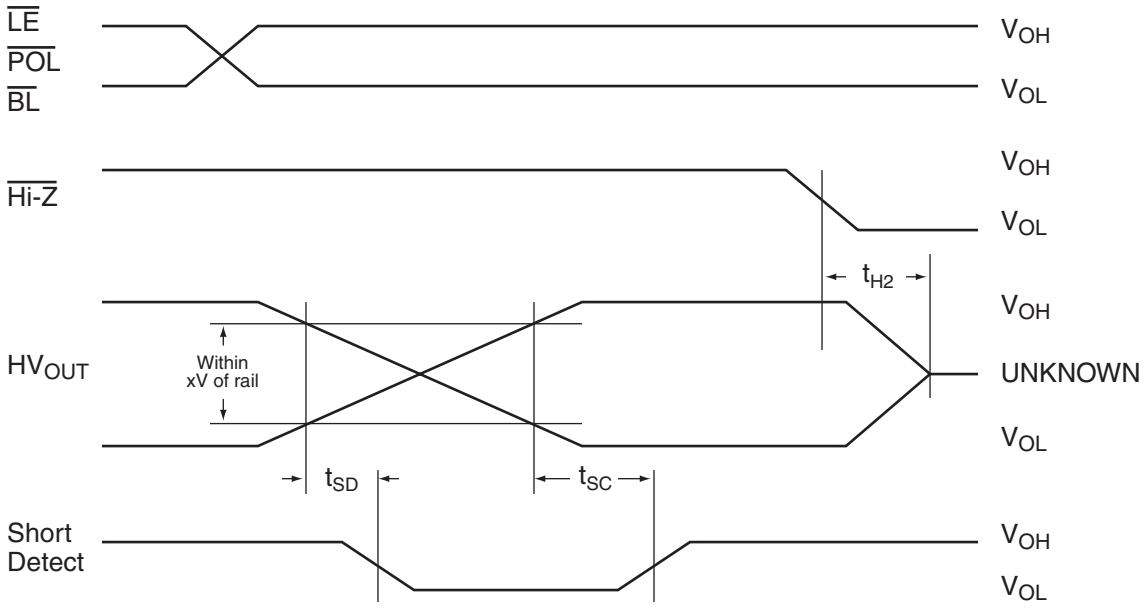


* $\overline{POL}$, $\overline{BL}$, $\overline{LE}$, and $\overline{HI\text{-}Z}$

Switching Waveforms

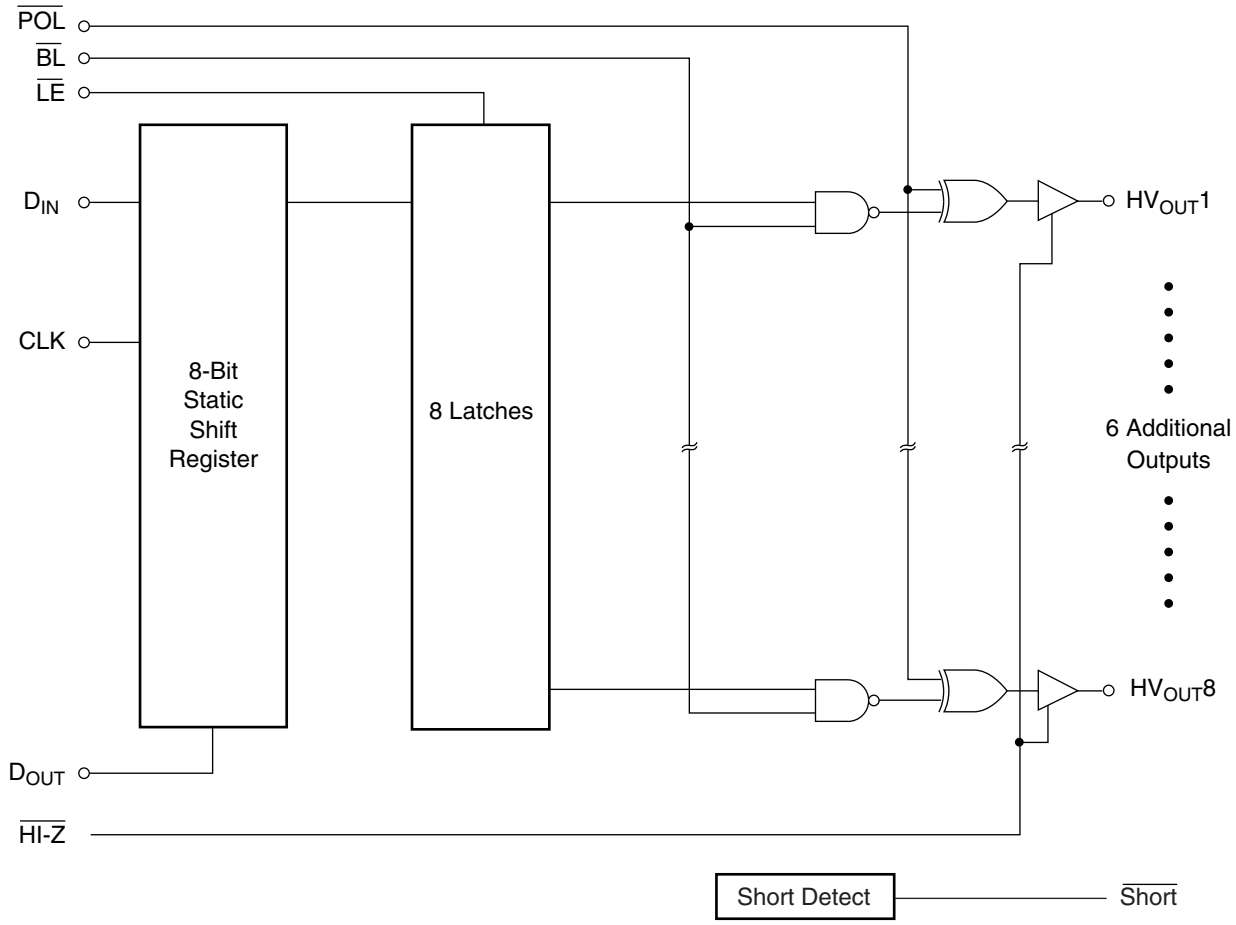


Short Circuit Detect Detail Timing (HV513)



Note: If the output is not within 5V to 10V of the desired output state, the SHORT signal goes LOW.

Functional Block Diagram



$\overline{POL}$, $\overline{BL}$, $\overline{LE}$, and $\overline{HI\text{-}Z}$ have internal 20kΩ pull-up resistors.

Function Table

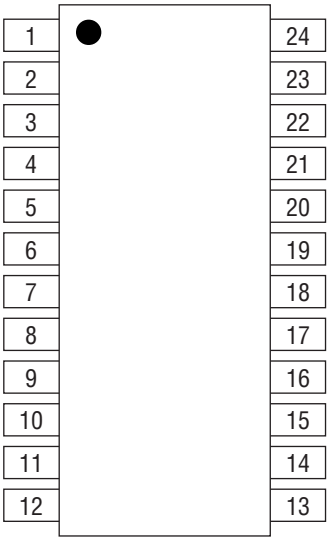
Function	Inputs					HV Outputs
	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	$\overline{HI\text{-}Z}$	
Clock data in	↑	L	H	H	H	previous state
Transparent	X	H	H	H	H	follows shift register outputs
Hold	X	L	H	H	H	holds previous state
Invert	X	X	H	L	H	logical inversion of latch outputs
All on	X	X	L	L	H	All high
All off	X	X	L	H	H	All low
High-Z	X	X	X	X	L	Hi-Z

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition

Pin Configuration

Pin	Function
1	N/C
2	V_{DD}
3	D_{OUT}
4	$\overline{BL}$
5	$\overline{POL}$
6	CLK
7	$\overline{LE}$
8	$\overline{SHORT}$
9	$\overline{HI\text{-}Z}$
10	D_{IN}
11	LGND
12	N/C
13	HVGND
14	HVGND
15	$HV_{out}1$
16	$HV_{out}2$
17	$HV_{out}3$
18	$HV_{out}4$
19	$HV_{out}5$
20	$HV_{out}6$
21	$HV_{out}7$
22	$HV_{out}8$
23	V_{PP}
24	V_{PP}

Package Outline



24-Lead SOW Package (WG)
(Wide Body)

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