



PRODUCT NUMBER:_____HML1010_____

DESCRIPTION:____L128 ELEMENT LINEAR IMAGE SENSOR____

ISSUE DATE: _____07/21/1993_____

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*THIS SPECIFICATION ARE SUBJECT TO BE CHANGED
WITHOUT NOTICE.

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HML1010

L128 ELEMENTS LINEAR IMAGE SENSOR

GENERAL DESCRIPTION

◆The HML1010 is a low dark current and high sensitive linear image sensor with 128 elements of sensor.
The sensor size is $32\mu\text{m} \times 28\mu\text{m}$ on $32\mu\text{m}$ pitch and the isolation of sensor is $2\mu\text{m}$. The device is operated by 12V power supply and 5V pulse of clock.
The package is 12 pin cerdip which is made by high quality ceramic sealing with optical glass_window.

APPLICATIONS

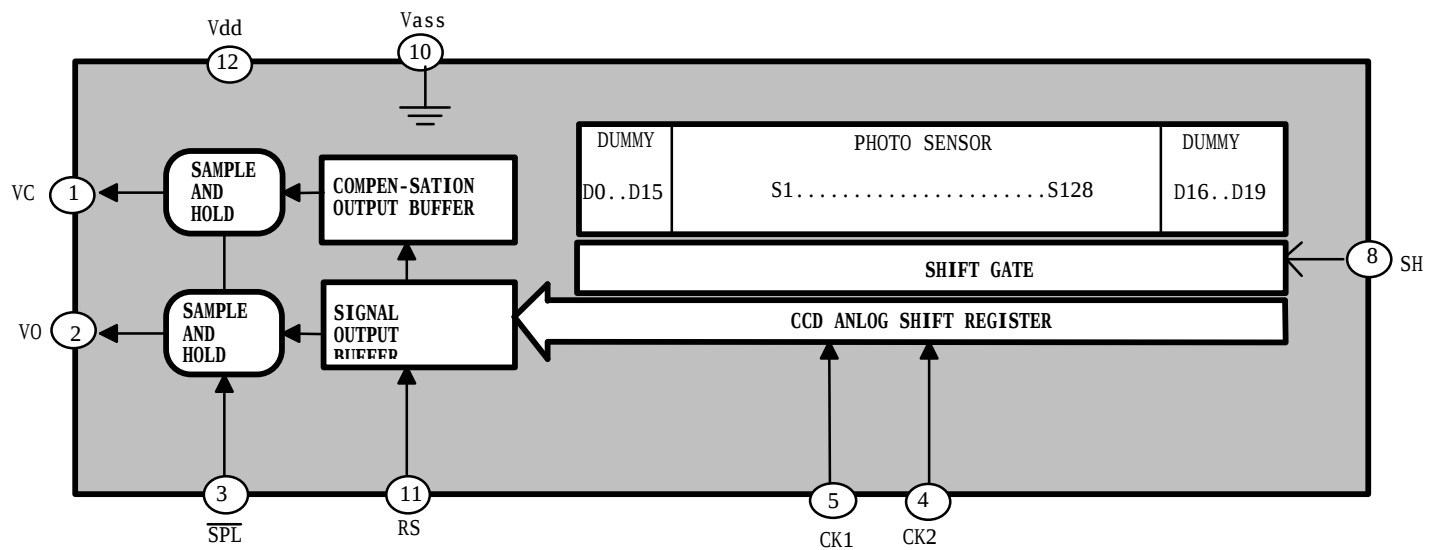
- ◆ OCR .
- ◆ Pen scanner.
- ◆ Camera auto-focus.
- ◆ E-O application.



FEATURES

- ◆ 128' 1 elements of image sensor.
- ◆ sensor size $32\text{mm} \times 28\text{mm}$ on 32mm pitch .
- ◆ operation frequency(typical) : 1MHZ.
- ◆ responsivity : $25 \text{ V}/(\text{lux} \cdot \text{sec})$
- ◆ 2 phase clocking.
- ◆ 12V DC power, 5V pulse clocking.
- ◆ Peak wavelength spectral response : 570nm.

CIRCUIT DIAGRAM



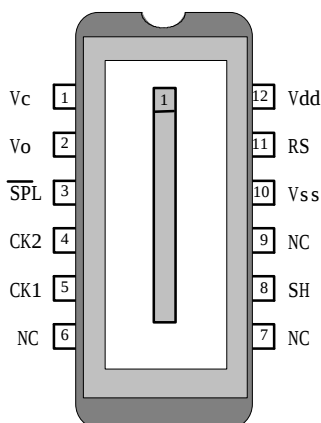
- 1 -



HML1010

L128 ELEMENTS LINEAR IMAGE SENSOR

PIN ASSIGNMENT



PIN DESCRIPTION

Name	Pin	I/O	Description
Vc	1	O	Compensation output
Vo	2	O	Signal output
SPL	3	I	Sample and hold clock
CK2	4	I	Clock phase 1
CK1	5	I	Clock phase 2
NC	6, 7, 9	I	Reset gate
SH	8	I	Shift gate
Vss	10	I	Analog ground
RS	11	I	Digital ground
Vdd	12	I	DC power supply

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating		
	Min	Max	Unit
Operating temperature	-25	+60	°C
Storage temperature	-40	+80	°C
Operating humidity	35%	80%	at 40°C
Storage humidity	20%	90%	at 40°C
Clock pulse voltage	-0.2	Vdd	V
Shift pulse voltage	-0.2	Vdd	V
Reset pulse voltage	-0.2	Vdd	V
Power supply voltage	-0.2	+13	V



HML1010

L128 ELEMENTS LINEAR IMAGE SENSOR

OPTICAL /ELECTRICAL CHARACTERISTICS

Temperature=25°C, Vdd=12V, CK1(CK2, RS, SH)=5V pulse, $f_{CK}=0.25\text{MHz}$, $f_{RS}=0.5\text{MHz}$, Tint =10ms
 ,Load resistance=100K Ω , Light source = 3200°K halogen lamp +CM500(infrared IR cutoff filter)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Responsivity	R	---	25	---	$\frac{\text{V}}{\text{lx} \cdot \text{sec}}$	
Dynamic range	DR	---	1500	---		1
Saturation Voltage	Vsat	1.2	1.5	---	V	2
Saturation exposure	SE	---	0.06	---	$\text{lx} \cdot \text{sec}$	2
Total transfer efficiency	TTE	92	96	---	%	
Output impedance	Z	---	---	1000	Ω	
DC power dissipation	P	---	---	100	mW	
Photorespons non-uniformity	PRNU1	---	---	10	%	3
Photorespons non-uniformity	PRNU2	---	---	10	%	3
Dark signal voltage	DS	---	1	5	mV	5
Dark signal non-uniformity	DSNU	---	---	5	mV	6
Output DC level	Vo	4.5	---	6.6	V	7
Compensation DC level	Vc	4.5	---	6.6	V	7
DC mismatch voltage	MDC	---	---	300	mV	7

NOTE:

1:Dynamic range (DR):

Dynamic range is defined as

$$DR = \frac{V_{SAT}}{DS}$$

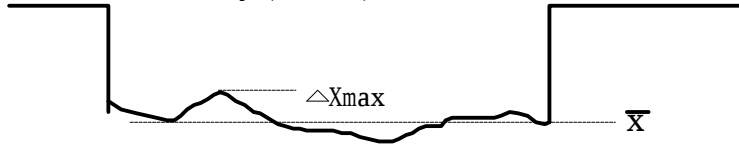
* DS is proportional to Tint (integration time)

2:Saturation voltage (Vsat) and Saturation exposure(SE):

Vsat is defined as the minimum saturation output voltage of all effective pixels.

And the exposure is defined as saturation exposure SE.

3: Photorespons nonuniformity (PRNU):



PRNU1 is defined as $PRNU1 = \frac{\Delta X_{\max}}{\bar{X}} \times 100\%$

$\bar{X}$ is average of total output signal ,

$\Delta X_{\max}$ is the maximum deviation from $\bar{X}$

PRNU2 is defined as $PRNU2 = \frac{\Delta X_{\text{next}}}{\bar{X}} \times 100\%$

ΔX_{next} is maximum difference of next pixel

4: Register Imbalance (RI):

RI is defined as follows

$$RI = \frac{\sum_{n=1}^{2159} |X_n - X_{n+1}|}{2159 \times \bar{X}} \times 100\%$$

Where X_n and X_{n+1} are output signal of each pixel .

$\bar{X}$ is average of total output signal.

5: Dark signal voltage (DS):

Dark signal is defined as average dark signal voltage of all effective pixels under room temperature 25°C, and integration time 10ms.

6: Dark signal nonuniformity (DSNU):

The DSNU is defined as the different dark voltage between the peak voltage and average voltage under room temperature 25°C and integration time 10ms.

peak dark signal



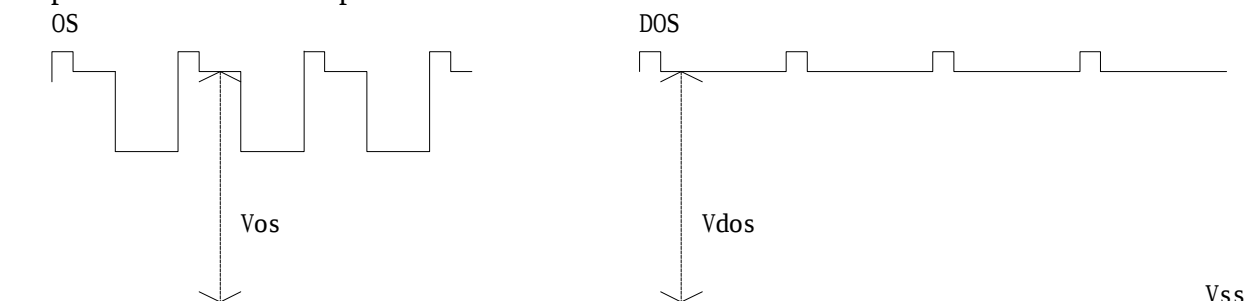


HML1010

L128 ELEMENTS LINEAR IMAGE SENSOR

7: Output DC level (V_o):

Output DC level and Compensation DC level are defined as





HML1010

L128 ELEMENTS LINEAR IMAGE SENSOR

OPERATING CONDITION

Characteristic		Symbol	Min	Typ	Max	Unit
Clock pulse voltage	H-level	CK1,CK2	4.5	5.0	Vdd	V
	L-level	CK1,CK2	-0.5	0	0.5	V
Shift pulse voltage	H-level	SH	4.5	5.0	Vdd	V
	L-level		-0.5	0	0.5	V
Reset pulse voltage	H-level	RS	4.5	5.0	Vdd	V
	L-level		-0.5	0	0.5	V
Power supply voltage		Vdd	11.0	12.0	13.0	V

CLOCK CHARACTERISTICS

Temperature 25 °C

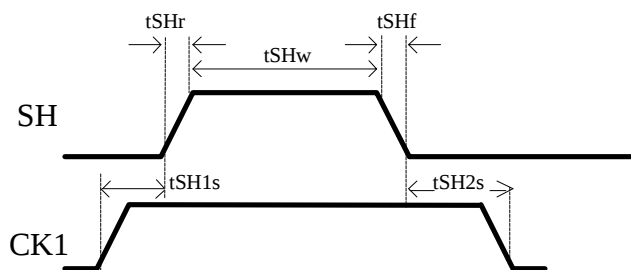
Parameter	Symbol	Min	Typ	Max	
Clock pulse frequency	CK1,CK2	0.1	1	2	MHZ
Reset pulse frequency	RS	0.1	1	2	MHZ
Clock capacitance	Cck1,Cck2	---	130	---	pF
Shift gate capacitance	C _{SH}	---	10	---	pF
Reset gate capacitance	C _{RS}	---	10	15	pF



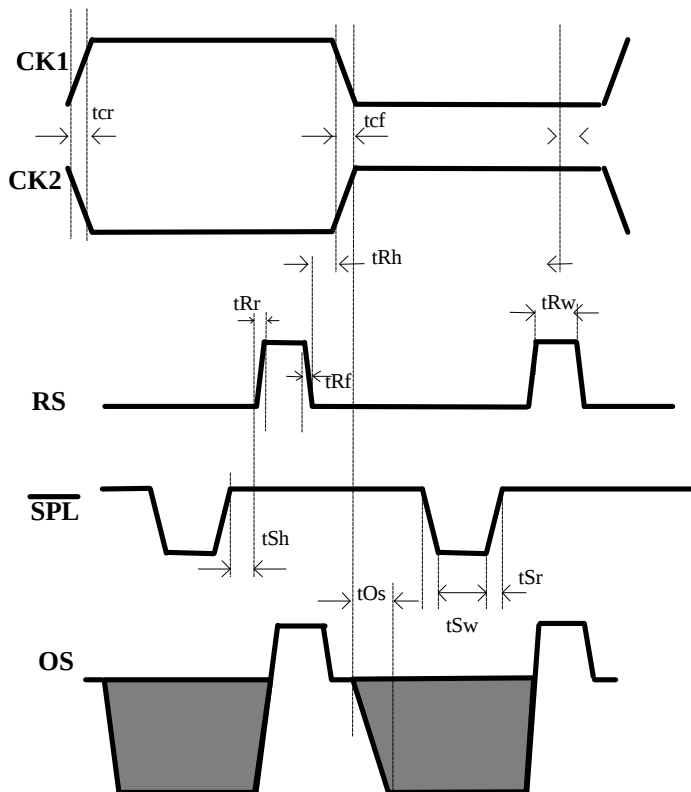
HML1010

L128 ELEMENTS LINEAR IMAGE SENSOR

Pulse Timing of SH and CK1



Pulse timing of CK1, CK2, RS and Vo



TIMING REQUIRMENT

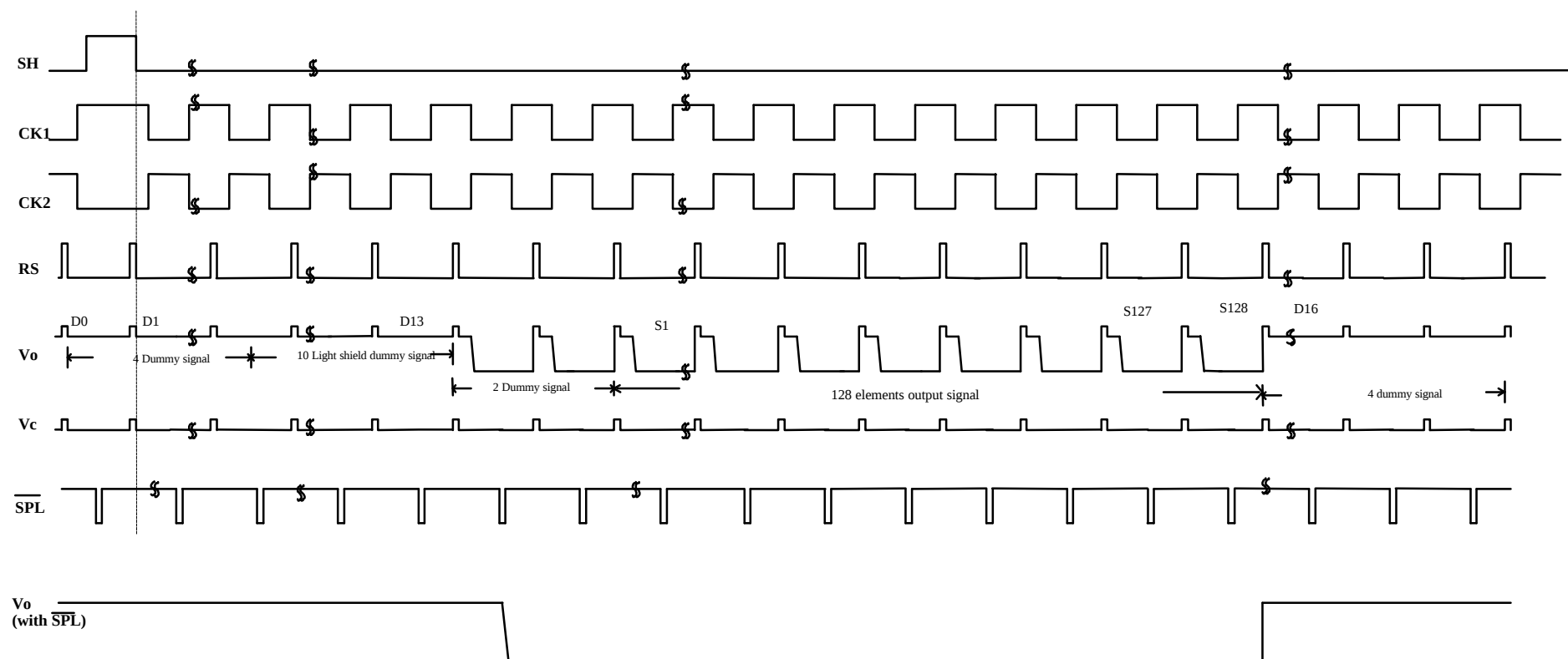
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Pulse timing of SH and CK	tSH1s, tSH2s	50	250	2000	ns
SH pulse rise time, fall time	tSHr, tSHf	0	50	---	ns
SH pulse width	tSHw	1	2	5	μs
CK1, CK2 pulse rise and fall time	tcr, tcf	0	100	---	ns
RS pulse rise and fall time	tRr, tRf	0	20	---	ns
RS, $\overline{\text{SPL}}$ pulse width	tRw, tSw	250	400	---	ns
Pulse time of CK1, CK2, RS	tRh	50	250	---	ns
Pulse time of RS, $\overline{\text{SPL}}$	tSh	50	100	---	ns
Video data delay time	tOs	---	150	450	ns



HML1010

L128 ELEMENTS LINEAR IMAGE SENSOR

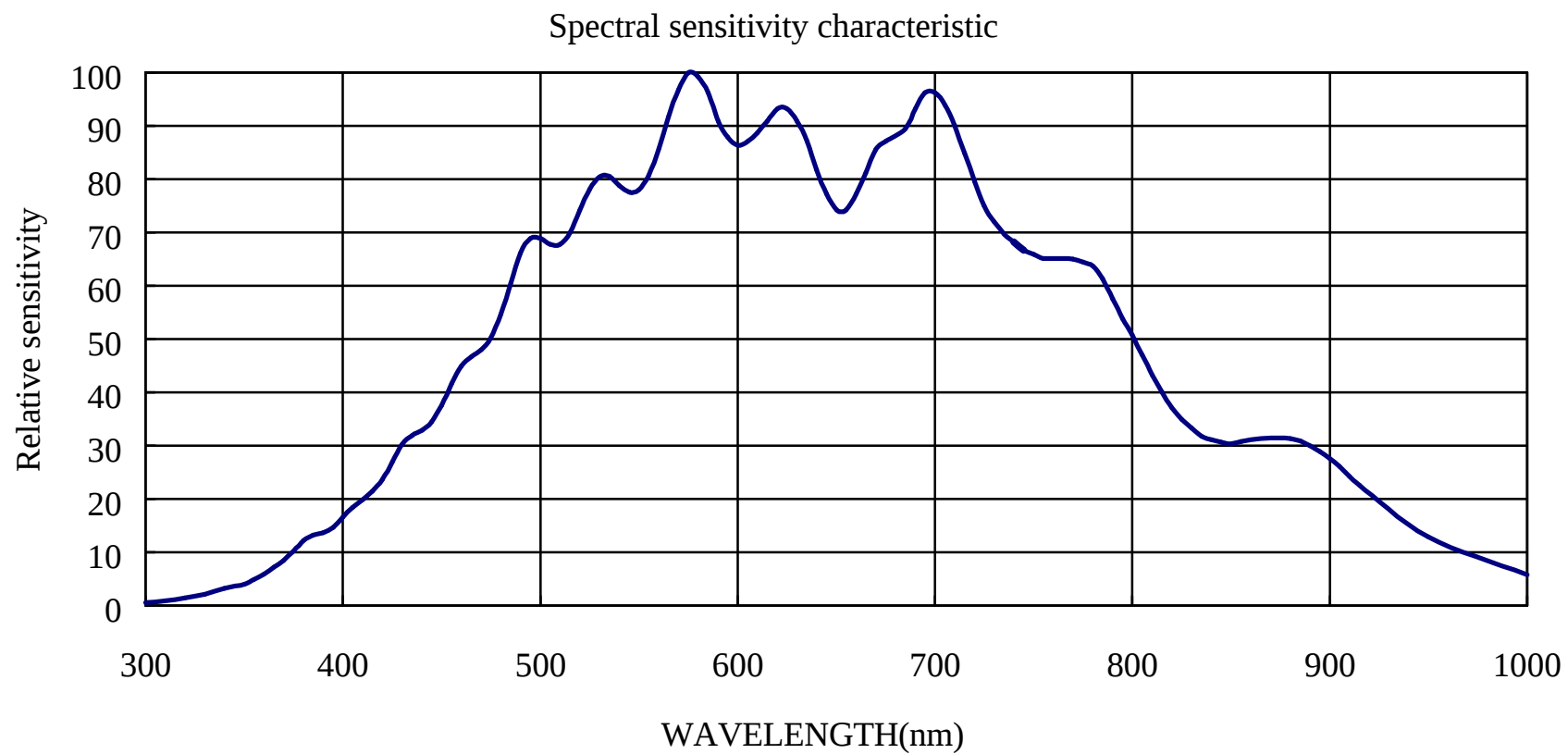
TIMING CHART





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L128 ELEMENTS LINEAR IMAGE SENSOR



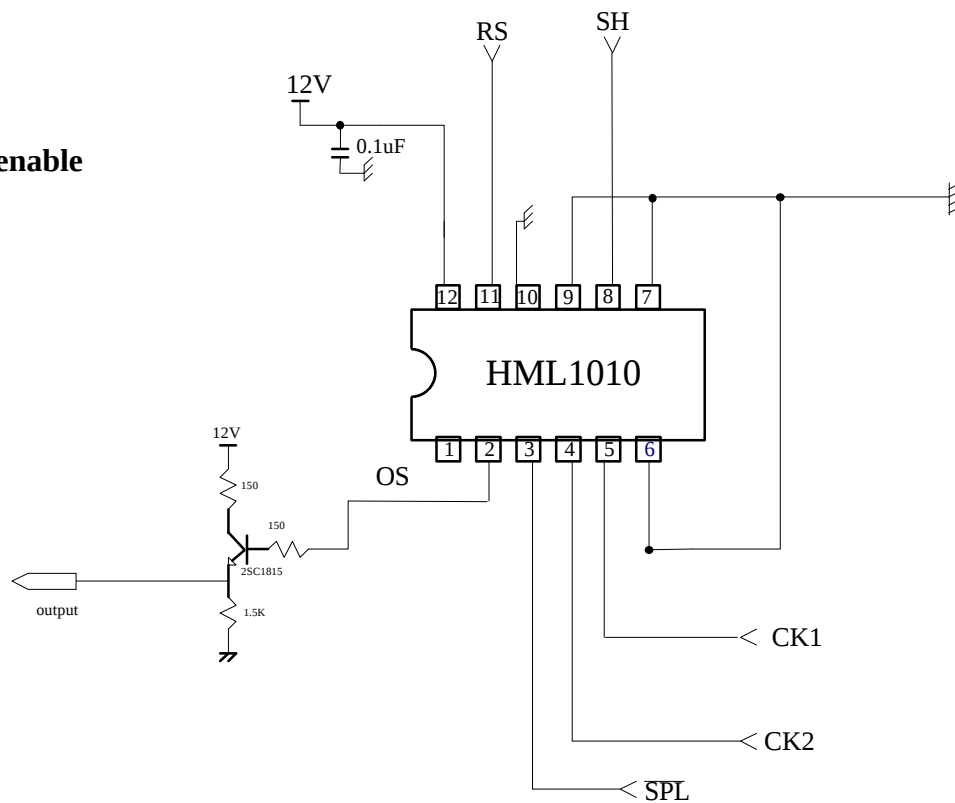


HML1010

L128 ELEMENTS LINEAR IMAGE SENSOR

APPLICATION CIRCUIT

Sample and hold circuit enable



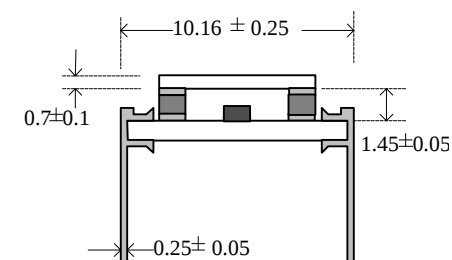
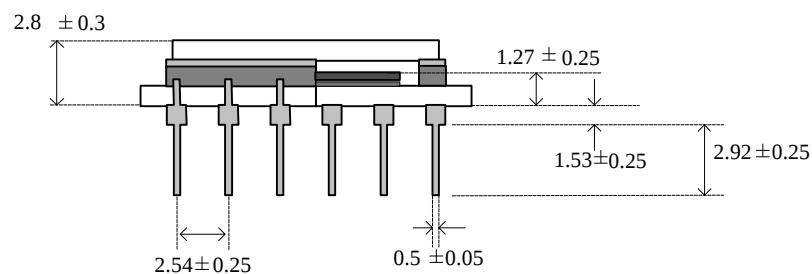
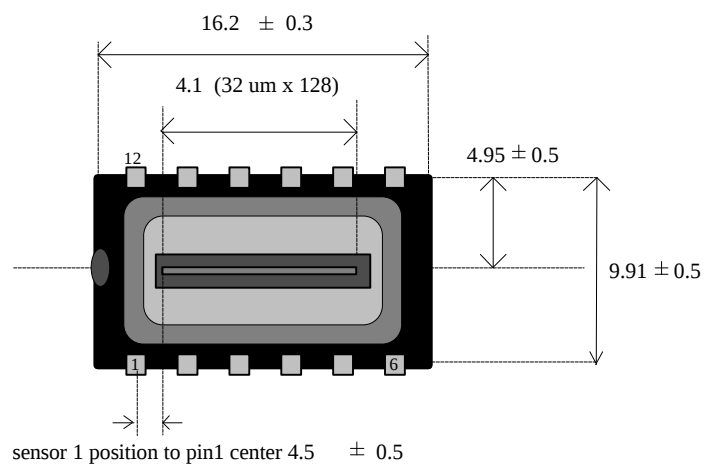


HML1010

L128 ELEMENTS LINEAR IMAGE SENSOR

PACKAGE OUTLINE

unit: mm



package structure

package material	ceramic
lead material	alloy with solder dip
glass refractive index	1.51
Background	black

