Honeywell

Aerospace Electronics

Advance Information

256K x 1 STATIC RAM—SOI

HX6156

FEATURES

RADIATION

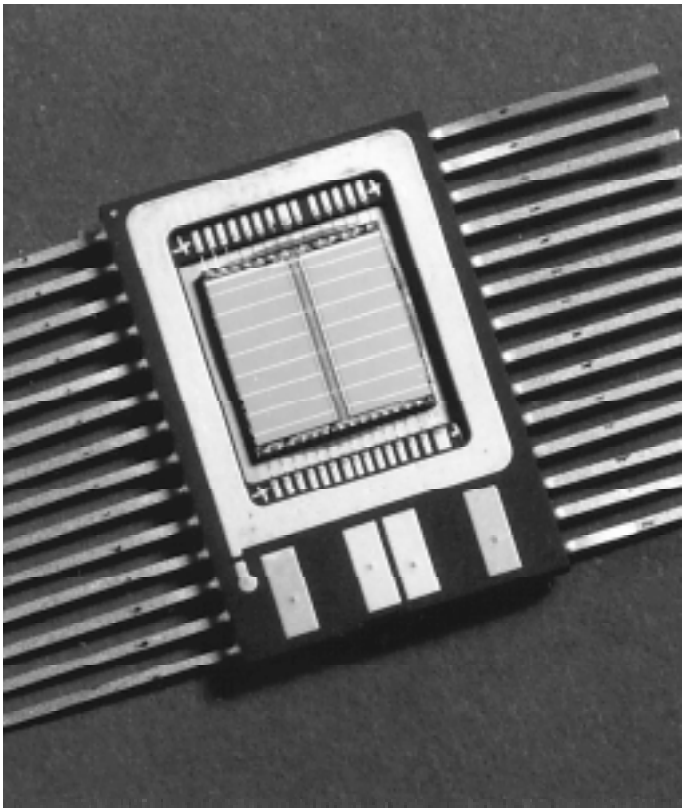
- Fabricated with RICMOS™ IV Silicon on Insulator (SOI) 0.75 µm Process (L_{eff} = 0.6 µm)
- Total Dose Hardness through $1x10^6$ rad(SiO_2)
- Neutron Hardness through $1x10^{14}$ cm^{-2}
- Dynamic and Static Transient Upset Hardness through $1x10^9$ rad(Si)/s
- Dose Rate Survivability through $1x10^{11}$ rad(Si)/s
- Soft Error Rate of $<1x10^{-10}$ upsets/bit-day in Geosynchronous Orbit

OTHER

- Fast Read/Write Cycle Times
  ≤ 15 ns (Typical)
  ≤ 25 ns (-55 to 125°C)
- Asynchronous Operation
- CMOS or TTL Compatible I/O
- Single 5 V ± 10% Power Supply
- Packaging Options
  – 24-Lead Flat Pack (0.540 in. x 0.600 in.)
  – 28-LeadFlat Pack (0.500 in. x 0.720 in.)

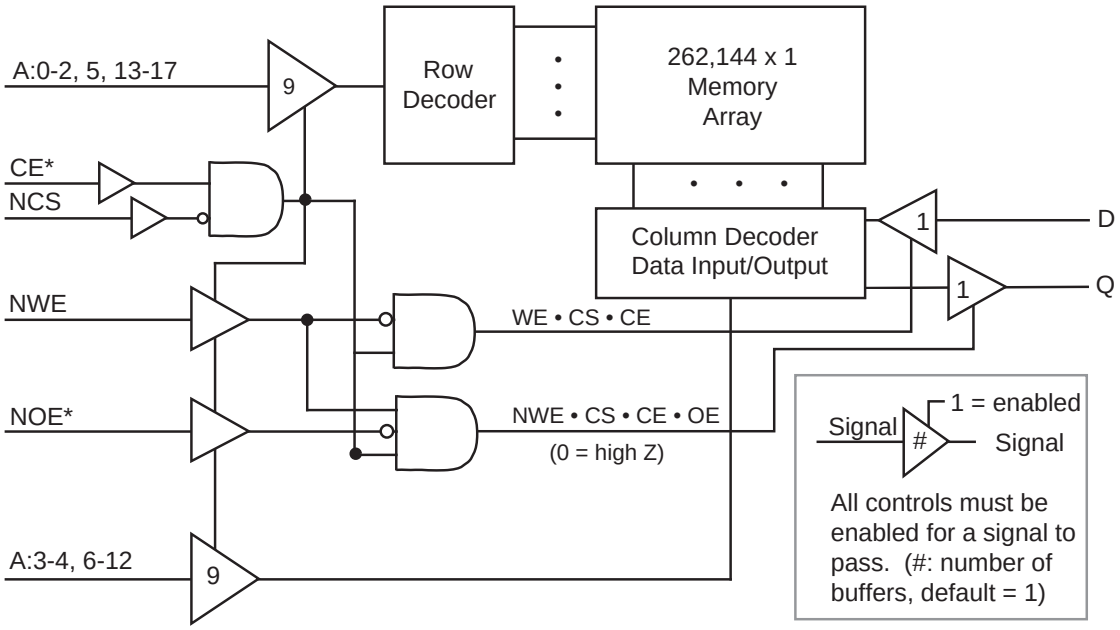
GENERAL DESCRIPTION

The 256K x 1 Radiation Hardened Static RAM is a high performance 262,144 word x 1-bit static random access memory with industry-standard functionality. It is fabricated with Honeywell's radiation hardened technology, and is designed for use in systems operating in radiation environments. The RAM operates over the full military temperature range and requires only a single 5 V ± 10% power supply. The RAM is available with either TTL or CMOS compatible I/O. Power consumption is typically less than 15 mW/MHz in operation, and less than 5 mW when de-selected. The RAM read operation is fully asynchronous, with an associated typical access time of 15 ns at 5 V.



Honeywell's enhanced SOI RICMOS™ IV (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques. The RICMOS™ IV process is a 5-volt, SIMOX CMOS technology with a 150 Å gate oxide and a minimum drawn feature size of 0.75 µm (0.6 µm effective gate length—L_{eff}). Additional features include tungsten via plugs, Honeywell's proprietary SHARP planarization process, and a lightly doped drain (LDD) structure for improved short channel reliability. A 7 transistor (7T) memory cell is used for superior single event upset hardening, while three layer metal power bussing and the low collection volume SIMOX substrate provide improved dose rate hardening.

FUNCTIONAL DIAGRAM



SIGNAL DEFINITIONS

A: 0-17	Address input pins which select a particular bit within the memory array.
NCS	Negative chip select, when at a low level allows normal read or write operation. When at a high level NCS forces the SRAM to a precharge condition, holds the data output driver in a high impedance state and disables all input buffers except CE. If this signal is not used it must be connected to VSS.
NWE	Negative write enable, when at a low level activates a write operation and holds the data output driver in a high impedance state. When at a high level NWE allows normal read operation.
NOE*	Negative output enable, when at a high level holds the data output driver in a high impedance state. When at a low level, the data output driver state is defined by NCS, NWE and CE. If this signal is not used it must be connected to VSS.
CE*	Chip enable, when at a high level allows normal operation. When at a low level CE forces the SRAM to a precharge condition, holds the data output driver in a high impedance state and disables all the input buffers except the NCS input buffer. If this signal is not used it must be connected to VDD.
D	Data input pin during a write operation. Remains in the high impedance state during a read operation.
Q	Data output pin during a read operation. Remains in the high impedance state during a write operation.

TRUTH TABLE

NCS	CE*	NWE	NOE*	MODE	D	Q
L	H	H	L	Read	X	Data Out
L	H	L	X	Write	Data In	High Z
H	X	XX	XX	Deselected	XX	High Z
X	L	XX	XX	Disabled	XX	High Z

Notes:
X: VI=VIH or VIL
XX: VSS≤VI≤VDD
NOE=H: High Z output state maintained for NCS=X, CE=X, NWE=X

*Available in 28-pin package only.

RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose

The SRAM will meet all stated functional and electrical specifications over the entire operating temperature range after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and T =125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 keV X-ray and Co60 radiation sources. Transistor gate threshold shift correlations have been made between 10 keV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The SRAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse up to the transient dose rate upset specification, when applied under recommended operating conditions.

To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation is ≤10%), it is suggested that stiffening capacitance be placed on or near the package VDD and VSS, with a maximum inductance between the package (chip) and stiffening capacitance of 0.7 nH per part. If there are no operate-through or valid stored data requirements, typical circuit board mounted de-coupling capacitors are recommended.

The SRAM will meet any functional or electrical specification after exposure to a radiation pulse up to the transient dose rate survivability specification, when applied under recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The SRAM will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

The SRAM has an extremely low Soft Error Rate (SER) as specified in the table below. This hardness level is defined by the Adams 90% worst case cosmic ray environment. The low SER is achieved by the use of a unique 7-transistor memory cell and the oxide isolation of the SOI substrate.

Latchup

The SRAM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SIMOX substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures. Sufficient transistor body tie connections to the p- and n-channel substrates are made to ensure no source/drain snapback occurs.

RADIATION HARDNESS RATINGS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	$\geq 1x10^6$	rad(SiO_2)	T_A=25°C
Transient Dose Rate Upset	$\geq 1x10^9$	rad(Si)/s	Pulse width ≤1 µs
Transient Dose Rate Survivability	$\geq 1x10^{11}$	rad(Si)/s	Pulse width ≤50 ns, X-ray, VDD=6.0 V, T_A=25°C
Soft Error Rate (SER)	$<1x10^{-10}$	upsets/bit-day	T_A=125°C, Adams 90% worst case environment
Neutron Fluence	$\geq 1x10^{14}$	N/cm^2	1 MeV equivalent energy, Unbiased, T_A=25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.
(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, TA=-55°C to 125°C.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Rating Min	Rating Max	Units
VDD	Positive Supply Voltage (2)		-0.5	6.5	V
VPIN	Voltage on Any Pin (2)		-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)		-65	150	°C
TSOLDER	Soldering Temperature • Time			270•5	°C•s
PD	Total Package Power Dissipation (3)			2.5	W
IOUT	DC or Average Output Current			25	mA
VPROT	ESD Input Protection Voltage (4)		2000		V
ΘJC	Thermal Resistance (Jct-to-Case)	24 FP		2	°C/W
		28 FP		2	
TJ	Junction Temperature			175	°C

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) RAM power dissipation (IDDSB + IDDOP) plus RAM output driver power dissipation due to external loading must not exceed this specification.
(4) Class 2 electrostatic discharge (ESD) input protection. Tested per MIL-STD-883, Method 3015 by DESC certified lab.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description Min	Description Typ	Description Max	Units
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TA	Ambient Temperature	-55	25	125	°C
VPIN	Voltage on Any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

Symbol	Parameter	Typical (1)	Worst Case Min	Worst Case Max	Units	Test Conditions
CI	Input Capacitance	5		7	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance	7		9	pF	VIO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial design characterization only.

DATA RETENTION CHARACTERISTICS

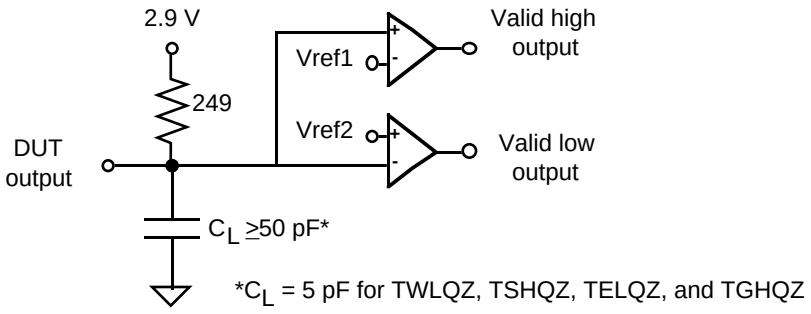
Symbol	Parameter	Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions
VDR	Data Retention Voltage		2.5		V	NCS=VDR VI=VDR or VSS
IDR	Data Retention Current			500	µA	NCS=VDD=VDR VI=VDR or VSS

(1) Typical operating conditions: TA= 25°C, pre-radiation.
(2) Worst case operating conditions: TA= -55°C to +125°C, post total dose at 25°C.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions
IDDSB1	Static Supply Current				1.5	mA	VIH=VDD, IO=0 VIL=VSS, f=0MHz
IDDSBMF	Standby Supply Current - Deselected				1.5	mA	NCS=VDD, IO=0, f=40 MHz
IDDOPW	Dynamic Supply Current, Selected (Write)				4.0	mA	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS (3)
IDDOPR	Dynamic Supply Current, Selected (Read)				4.0	mA	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS (3)
II	Input Leakage Current			-5	+5	µA	VSS≤VI≤VDD
IOZ	Output Leakage Current			-10	+10	µA	VSS≤VIO≤VDD Output=high Z
VIL	Low-Level Input Voltage	CMOS TTL	1.7		0.3xVDD 0.8	V V	March Pattern VDD = 4.5V
VIH	High-Level Input Voltage	CMOS TTL	3.2	0.7xVDD 2.2		V V	March Pattern VDD = 5.5V
VOL	Low-Level Output Voltage		0.3 0.005		0.4 0.05	V V	VDD = 4.5V, IOL = 10 mA (CMOS) = 8 mA (TTL) VDD = 4.5V, IOL = 200 µA
VOH	High-Level Output Voltage		4.3 4.5	4.2 VDD-0.05		V V	VDD = 4.5V, IOH = -5 mA VDD = 4.5V, IOH = -200 µA

(1) Typical operating conditions: VDD= 5.0 V,TA=25°C, pre-radiation.
(2) Worst case operating conditions: VDD=4.5 V to 5.5 V, TA=-55°C to +125°C, post total dose at 25°C.
(3) All inputs switching. DC average current.

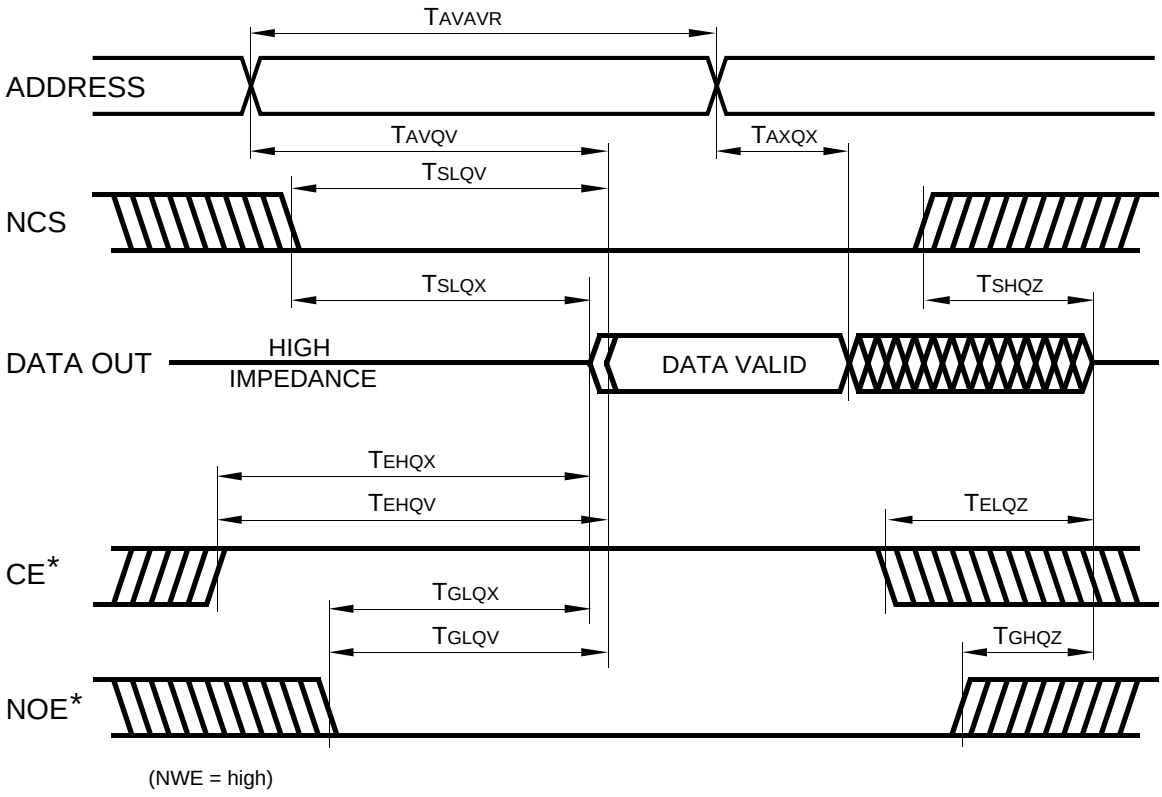


Tester Equivalent Load Circuit

READ CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) -55 to 125°C Min	Worst Case (3) -55 to 125°C Max	Units
TAVAVR	Address Read Cycle Time		25		ns
TAVQV	Address Access Time			25	ns
TAXQX	Address Change to Output Invalid Time		3		ns
TSLQV	Chip Select Access Time			25	ns
TSLQX	Chip Select Output Enable Time		5		ns
TSHQZ	Chip Select Output Disable Time			10	ns
TEHQV	Chip Enable Access Time (4)			25	ns
TEHQX	Chip Enable Output Enable Time (4)		5		ns
TELQZ	Chip Enable Output Disable Time (4)			10	ns
TGLQV	Output Enable Access Time			9	ns
TGLQX	Output Enable Output Enable Time		0		ns
TGHQZ	Output Enable Output Disable Time			9	ns

(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V (CMOS), VIL/VIH=0V/3V (TTL), input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading $C_L \geq 50$ pF, or equivalent capacitive output loading C_L=5 pF for TSHQZ, TELQZ TGHQZ. For C_L >50 pF, derate access times by 0.02 ns/pF (typical).
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55 to 125°C, post total dose at 25°C.
(4) Chip Enable (CE) pin only available with 28-lead FP.

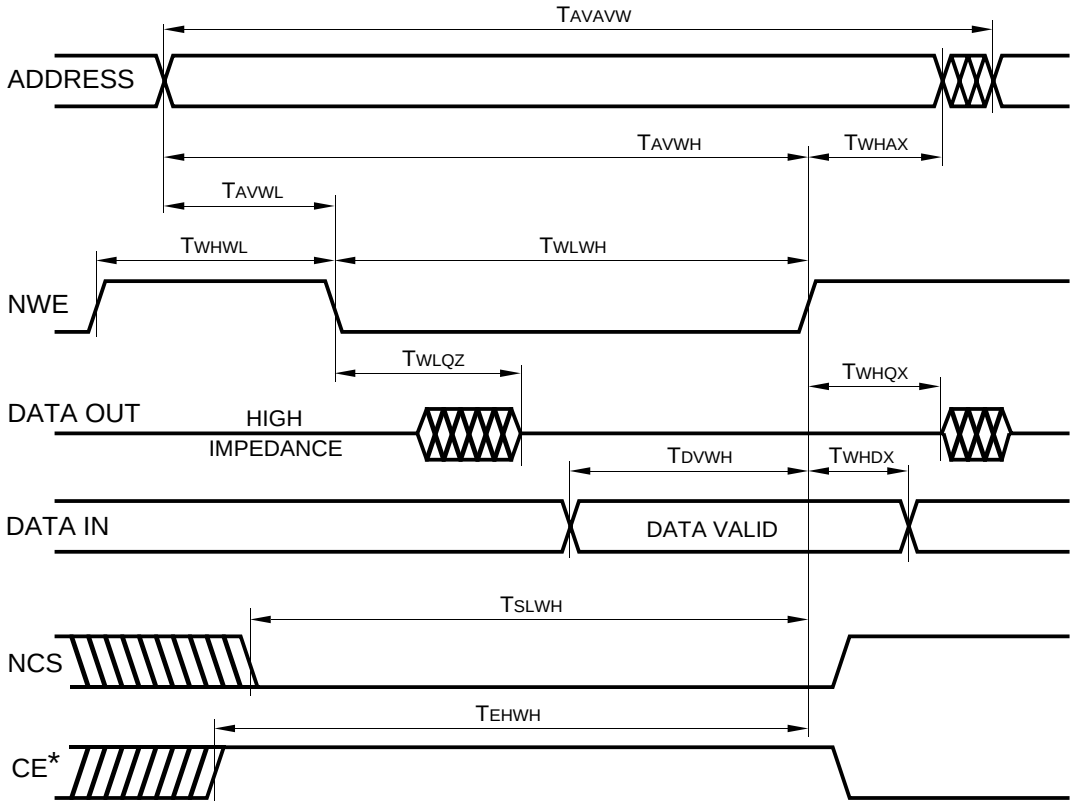


*Only available in 28-lead package.

WRITE CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3)		Units
			Min	Max	
TAVAVW	Write Cycle Time (4)		25		ns
TWLWH	Write Enable Write Pulse Width		20		ns
TSLWH	Chip Select to End of Write Time		20		ns
TDVWH	Data Valid to End of Write Time		15		ns
TAVWH	Address Valid to End of Write Time		20		ns
TWHDX	Data Hold Time after End of Write Time		0		ns
TAVWL	Address Valid Setup to Start of Write Time		0		ns
TWHAX	Address Valid Hold after End of Write Time		0		ns
TWLQZ	Write Enable to Output Disable Time		0	9	ns
TWHQX	Write Disable to Output Enable Time		5		ns
TWHWL	Write Disable to Write Enable Pulse Width(5)		5		ns
TEHWH	Chip Enable to End of Write Time (6)		20		ns

(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V (CMOS), VIL/VIH=0V/3V (TTL), input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading ≥50 pF, or equivalent capacitive load of 5 pF for TWLQZ.
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55 to 125°C, post total dose at 25°C.
(4) TAVAV = TWLWH + TWHWL
(5) Guaranteed but not tested.
(6) Chip Enable (CE) pin only available with 28-lead FP.



*Only available in 28-lead package.

DYNAMIC ELECTRICAL CHARACTERISTICS

Read Cycle

The RAM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select (NCS), or chip enable (CE) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and chip enable and write enable (NWE) must be high. The output driver can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and with CE held continuously high, and toggling the addresses.

For an address activated read cycle, NCS must be valid prior to, coincident with or within (TAVQV minus TSLQV) time following edge transition(s). CE must be valid a minimum of (TEHQV minimums TAVQV) time prior to the activating address edge transitions(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAV. When the RAM is operated at the minimum address activated read cycle time, the data output will remain valid on the RAM I/O until TAXQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses must be valid at least (TAVQV minus TSLQV) time prior to the enabling NCS edge transition. CE must be valid a minimum of (TEHQV minus TSLQV) time prior to the enabling NCS edge transition. Address or CE edge transitions can occur later than the specified setup times to NCS, however, the valid data access time will be delayed. Any address edge transition, which occurs during the time when NCS is low, will initiate a new read access, and the data output will not become valid until TAVQV time following the address edge transition. The data output will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

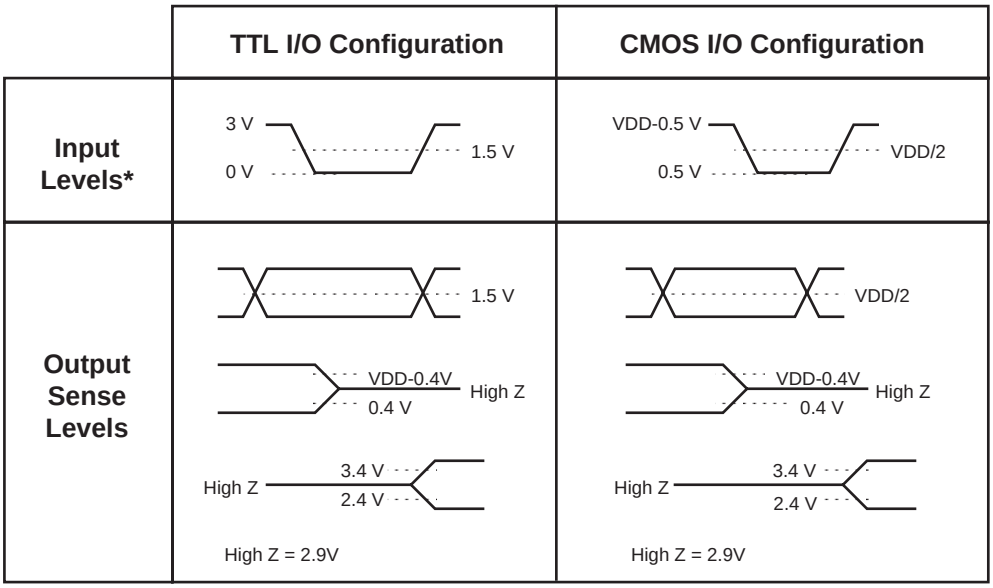
To control a read cycle with CE, all addresses and NCS must be valid prior to or coincident with the enabling CE edge transition. Address or NCS edge transitions can occur later than the specified setup times to CE; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when CE is high will initiate a new read access, and data output will not become valid until TAVQV time following the address edge transition. The data output will enter a high impedance state TELQZ time following a disabling CE edge transition.

Write Cycle

The write operation is synchronous with respect to the address bits, and control is governed by write enable (NWE), chip select (NCS), or chip enable (CE) edge transitions (refer to Write Cycle timing diagrams). To perform a write operation, both NWE and NCS must be low, and CE must be high. The ouput driver can be controlled independently by the output enable (NOE) signal. Consecutive write cycles can be performed with NWE or NCS held continuously low, or CE held continuously high. At least one of the control signals must transition to the opposite state between consecutive write operations.

To write data into the RAM, NWE and NCS must be held low and CE must be held high for at least TWLWH/TSLSH/TEHEL time. Any amount of edge skew between the signals can be tolerated, and any one of the control signals can initiate or terminate the write operation. For consecutive write operations, write pulses must be separated by the minimum specified TWHWL/TSHSL/TELEH time. Address inputs must be valid at least TAVWL/TAVSL/TAVEH time before the enabling NWE/NCS/CE edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of TDVWH/TDVSH/TDVEL, and an address valid to end of write time of TAVWH/TAVSH/TAVEL also must be provided for during the write operation. Hold times for address inputs and data input with respect to the disabling NWE/NCS/CE edge transition must be a minimum of TWHAX/TSHAX/TELAX time and TWHDX/TSHDX/TELDX time, respectively. The minimum write cycle time is TAVAV.

TESTER AC TIMING CHARACTERISTICS



* Input rise and fall times <1 ns/V

QUALITY AND RADIATION HARDNESS ASSURANCE

Honeywell maintains a high level of product integrity through process control, utilizing statistical process control, a complete “Total Quality Assurance System,” a computer data base process performance tracking system, and a radiation-hardness assurance strategy.

The radiation hardness assurance strategy starts with a technology that is resistant to the effects of radiation. Radiation hardness is assured on every wafer by irradiating test structures as well as SRAM product, and then monitoring key parameters which are sensitive to ionizing radiation. Conventional MIL-STD-883 TM 5005 Group E testing, which includes total dose exposure with Cobalt 60, may also be performed as required. This Total Quality approach ensures our customers of a reliable product by engineering in reliability, starting with process development and continuing through product qualification and screening.

SCREENING LEVELS

Honeywell offers several levels of device screening to meet your system needs. “Engineering Devices” are available with limited performance and screening for breadboarding and/or evaluation testing. Hi-Rel Level B and S devices undergo additional screening per the requirements of MIL-STD-883. As a QML supplier, Honeywell also offers QML Class Q and V devices per MIL-PRF-38535 and are available per the applicable Standard Microcircuit Drawing (SMD). QML devices offer ease of procurement by eliminating the need to create detailed specifications and offer benefits of improved quality and cost savings through standardization.

RELIABILITY

Honeywell understands the stringent reliability requirements for space and defense systems and has extensive experience in reliability testing on programs of this nature. This experience is derived from comprehensive testing of VLSI processes. Reliability attributes of the RICMOS™ process were characterized by testing specially designed irradiated and non-irradiated test structures from which specific failure mechanisms were evaluated. These specific mechanisms included, but were not limited to, hot carriers, electromigration and time dependent dielectric breakdown. This data was then used to make changes to the design models and process to ensure more reliable products.

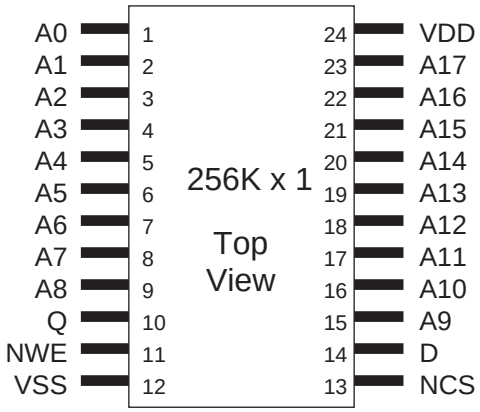
In addition, the reliability of the RICMOS™ process and product in a military environment was monitored by testing irradiated and non-irradiated circuits in accelerated dynamic life test conditions. Packages are qualified for product use after undergoing Groups B & D testing as outlined in MIL-STD-883, TM 5005, Class S. The product is qualified by following a screening and testing flow to meet the customer’s requirements. Quality conformance testing is performed as an option on all production lots to ensure the ongoing reliability of the product.

PACKAGING

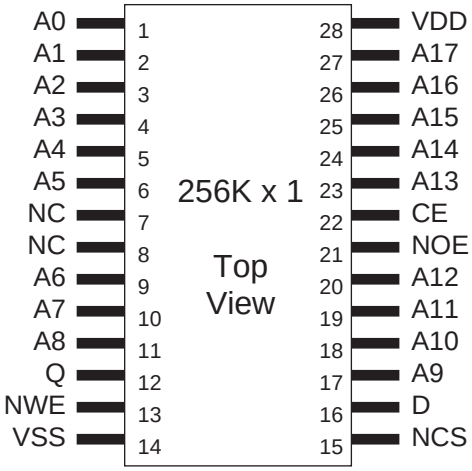
The 256K x 1 SRAM is offered in a custom 24-lead and 28-lead flat pack. These packages are constructed of multi-layer ceramic (Al_2O_3) and contain internal power and ground planes. All NC pins must be connected to either VDD, VSS or an active driver to prevent charge buildup in the radiation environment.

Optional capacitors can be mounted to the package by the user to maximize supply noise decoupling and increase board packing density. The capacitors attach electrically to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment.

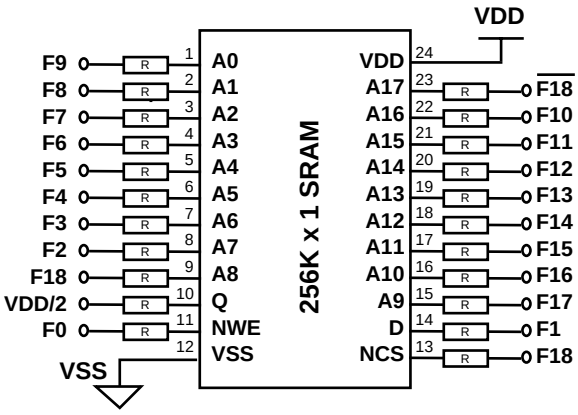
24-LEAD FP PINOUT



28-LEAD FP PINOUT

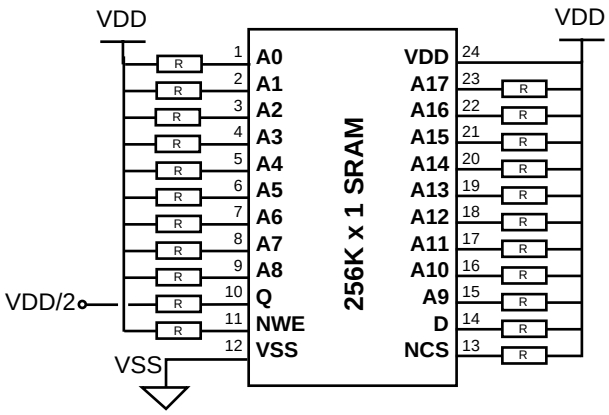


DYNAMIC BURN-IN DIAGRAM



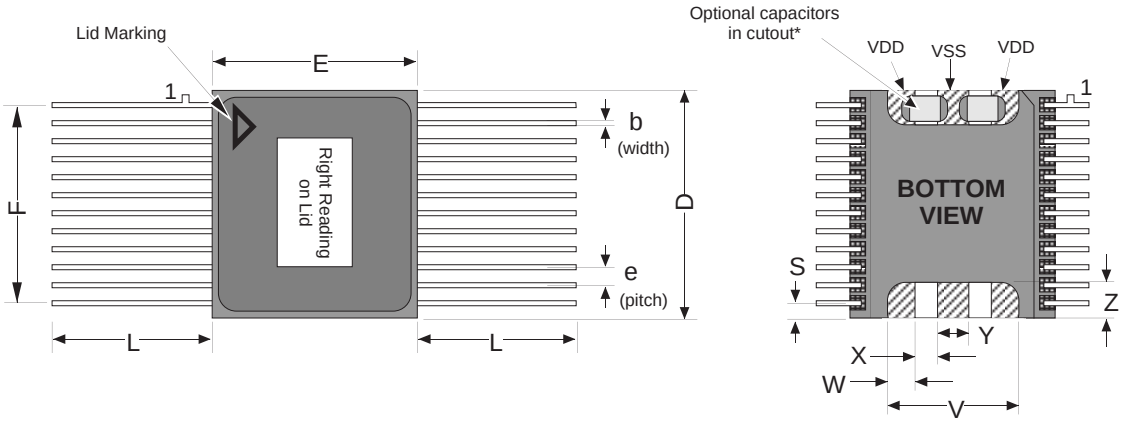
VDD = 5.6V, R≤10KΩ, VIH = VDD, VIL = VSS
Ambient Temperature ≥ 125°C, F0 ≥ 100 KHz Sq Wave
Frequency of F1 = F0/2, F2 = F0/4, F3 = F0/8, etc.

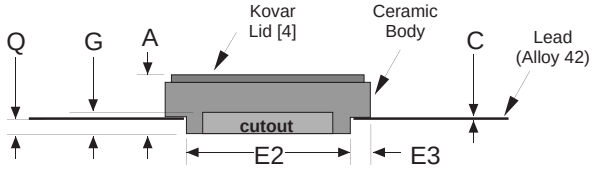
STATIC BURN-IN DIAGRAM



VDD = 5.5V, R ≤ 10 KΩ
Ambient Temperature ≥ 125°C

24-LEAD FLAT PACK



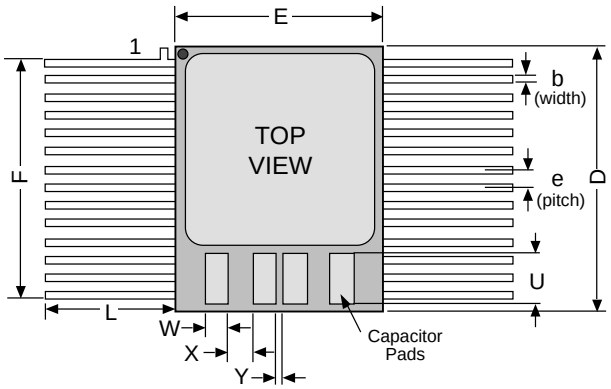


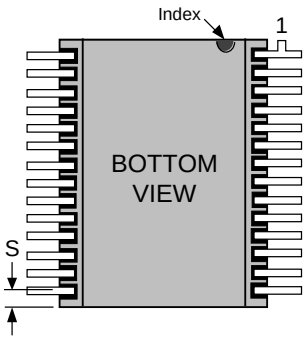
All dimensions in inches

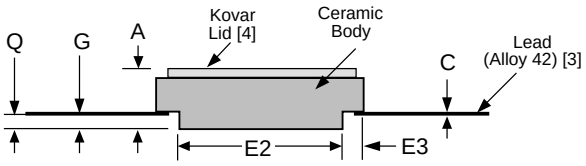
A	0.150 ± 0.015	**G**	0.050 ± 0.005
b	0.015 ± 0.002	**L**	0.376 min [3]
C	0.003 to 0.006	**Q**	0.026 to 0.045
D	0.600 ± 0.007	**S**	0.025 ± 0.010
e	0.050 ± 0.005 [1]	**V**	0.300 ref
E	0.540 ± 0.007	**W**	0.050 ref
E2	0.450 ± 0.007	**X**	0.030 ref
E3	0.030 min	**Y**	0.100 ref
F	0.550 ± 0.005 [2]	**Z**	0.080 ref

[1] Tolerances are non-accumulative
[2] Where lead is brazed to package
[3] Parts delivered with leads unformed
[4] Lid is connected to VSS

28-LEAD FLAT PACK





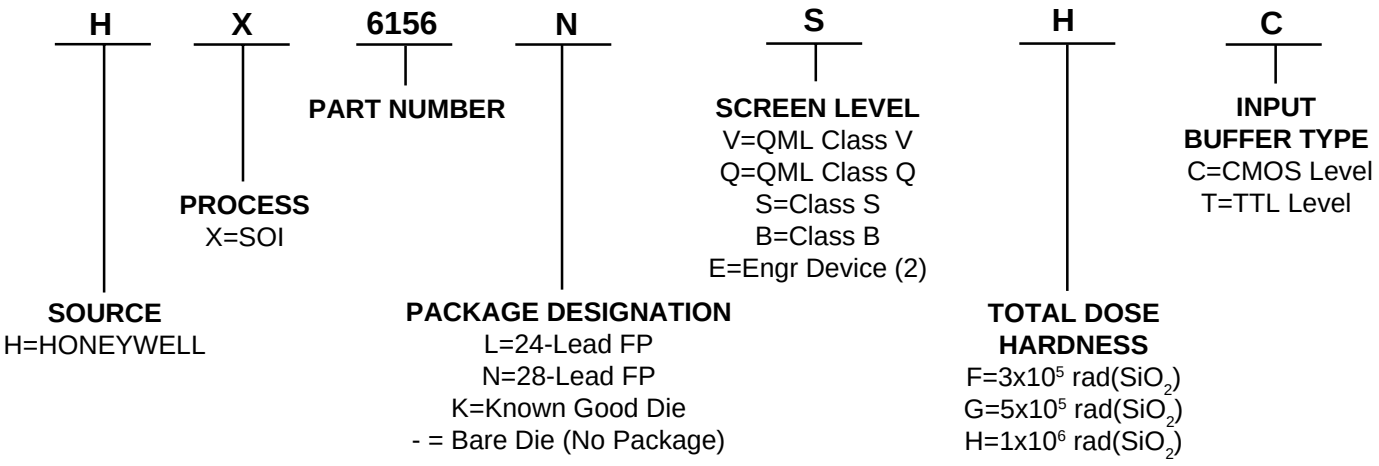


All dimensions in inches

A	0.105 ± 0.015
b	0.017 ± 0.002
C	0.003 to 0.006
D	0.720 ± 0.008
e	0.050 ± 0.005 [1]
E	0.500 ± 0.007
E2	0.380 ± 0.008
E3	0.060 ref
F	0.650 ± 0.005 [2]
G	0.035 ± 0.004
L	0.295 min [3]
Q	0.026 to 0.045
S	0.045 ± 0.010
U	0.130 ref
W	0.050 ref
X	0.075 ref
Y	0.010 ref

[1] BSC – Basic lead spacing between centers
[2] Where lead is brazed to package
[3] Parts delivered with leads unformed
[4] Lid connected to VSS

ORDERING INFORMATION (1)



(1) Orders may be faxed to 612-954-2051. Please contact our Customer Logistics Department at 612-954-2888 for further information.

(2) Engineering Device description: Parameters are tested from -55 to 125°C, 24 hr burn-in, no radiation guaranteed.

Contact Factory with other needs.

To learn more about Honeywell Solid State Electronics Center, visit our web site at http://www.ssec.honeywell.com

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