
HG73C Series

μCBIC - embedded H8/300H, H8S, SH-1, & SH-3
ASIC Product Brief

HITACHI

Description

The HG73C Series is a family of cell-based integrated circuits (CBICs) implemented in advanced 0.35-μm CMOS process technology featuring 3.3 V and 2.0 V core operation. Process-optimized libraries are available to support high-performance and low-power design requirements. Besides the low-voltage interface support for 3.3 V and 2.0V I/Os, the HG73C Series also provides support for standard 5V I/Os. Focusing on high density routing the HG73C can achieve a maximum of 3,000,000 useable gates. Three metal layers are standard with optional fourth and fifth layers available for clock, power, ground and signal distribution. Compilers for Single Port and Dual Port RAM, ROM, and Datapath provide necessary building blocks for ASIC designers, and a variety of analog modules including ADCs, DACs, video RAMDAC, and high frequency PLL allow designers to realize a single chip with both digital and analog functions.

The HG73C Series also includes Hitachi's μCBIC solution, which is a CBIC with an embedded/controller core. The cores available are Hitachi's 16-bit H8/300H, and H8S, and SuperH RISC engine cores including SH-1 controllers and SH-3 processors. Hitachi supports these cores with a comprehensive design and programming solution that includes the controller/processor core, simulation models, emulation support and software suite. The widely available emulators, compilers, and OS currently used for the the high volume standard controller and processor devices are fully compatible with the embedded cores. With processing performance ranging from several MIPS to 60 MIPS, Hitachi's μCBIC supports a broad range of application and system requirements with a highly integrated single chip solution.

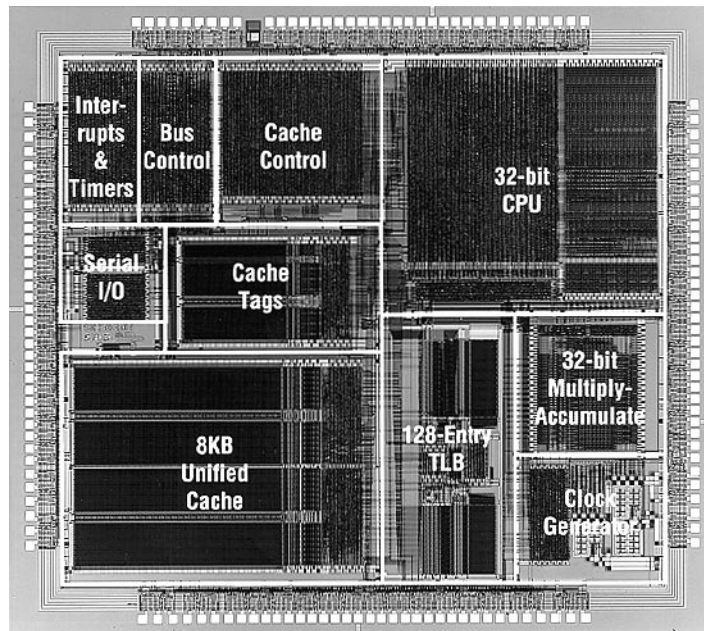
The design tools, based on popular, CAE tools, support a complete design environment capable of the seamless development of CBIC and μCBIC designs from logic simulation to final layout. Post-layout simulation takes full account of delay-driven components by factoring wiring RC parasitics and waveform ramp parameters into the simulation. The automated fault diagnostics and boundary scan design functions facilitate design-for-testability. Also, the application of automated clock-tree generation techniques greatly adds to the reduction of clock skew. The HG73C Series supports extensive libraries for core cells (internal cells) and I/O cells for the more popular CAE tools.

HG73C Series

Features

HG73C Series Cell-Based ICs for the Real System Solution

- Maximum Usable Gate Count:
 - 3,000,000 usable gates
- Raw Gate Density:
 - 18,600 gates/mm²
- Compileable Microcontroller cores:



- H8/300H, H8S, and SuperH-1
- High Performance Microprocessor core:
 - SH-3
- Analog Modules:
 - ADCs, DACs, RAMDAC, and PLL
- Ultra-High-Speed Operation:
 - Supports maximum clock frequency in excess of 150 MHz

Internal Gates	200 ps, Standard load, 2-input power
NAND gate, V _{cc} = 3.3V	
Input Buffers	300 ps, Standard load
Output Buffers	1300 ps, CL = 15 pF
- Low Power Dissipation:
 - 0.23 μ W/Gate \forall MHz, V_{cc}=3.3V
- Process Technology:
 - 0.35 μ m CMOS, 3 to 5 layer metalization
 - Process parameter-optimized with high-performance or low-power dissipation libraries

HG73C Series

- Core Power:
 - $3.3V \pm 0.3V$, $2.0V \pm 0.2V$
- I/O Interface:
 - $5.0V \pm 0.5V$, $3.3V \pm 0.3V$, $2.0V \pm 0.2V$
- Versatile Compilers:
 - Single Port RAM, Dual Port RAM, ROM, and Datapath
- Abundant I/O Cell Libraries:
 - GTL, PECL, CMOS, TTL and PCI interface libraries.
- Design-for-Testability:
 - Hitachi's auto-diagnostic (shift-scan) functions facilitates automated test circuit insertion and auto-generation of high fault-coverage test vectors. Support is also available for JTAG boundary scan (IEEE 1149.1)



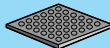

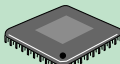
CBIC/ μ CBIC (μ CBIC contains an embedded microprocessor)

Part No.	Feature Size	Leff	Core Power	I/O Power	Metal Layers	Max. Usable Gates	Max. Gate Density (Typical)	Processor Available
HG71C	0.8 μ m	0.7 μ m	3.3/5.0V	3.3/5.0V	2, 3	300K Gates	4.1K Gates (~2.2K Gates)	H8/300H
HG72C	0.6 μ m	0.55 μ m	3.3/5.0V	3.3/5.0V	2, 3	600K Gates	7.2K Gates (~4K Gates)	H8/300H, SH-1
HG73C	0.4 μ m	0.35 μ m	2.0/3.3V	2.0/3.3/5.0V	3, 4, 5	3M Gates	18.9K Gates (~10K Gates)	H8/300H, H8S SH-1, SH-3
HG74C	0.25 μ m	0.2 μ m	1.8/2.5V	1.8/2.5/3.3/5.0V	3, 4, 5	6M Gates	39.2K Gates (~20K Gates)	SH-4

Embedded DRAM

Part No.	Feature Size	Leff	Core Power	I/O Power	Metal Layers	Max. Usable Gates (w/out DRAM)	Max. Gate Density (Typical)	Max. DRAM (w/o gates)	DRAM Density (w/overhead)	Processor Available
HG73M	0.28 μ m	0.35 μ m	3.3/5.0V	3.3/5.0V	3, 4, 5	3M Gates	18.9K Gates (~10K Gates)	140Mbit	50KBytes/mm 2	H8/300H, H8S, SH-1, SH-3

HG73C Series

Type	Item	Package Outline	Package Pin Count					
			0	100	200	300	400	600
Surface Mounting Type	QFP Quad Flat Plastic Package		64 80 100 136 160 168 208 240 256 296 304 344 384					
	LQFP Low-Profile Quad Flat Package		64 144 176					
	TOFP Thin Quad Flat Plastic Package		80 100 120					
	HQFP Heatspreader-enhanced Quad Flat Package		80 100 136 160 208					
	PLCC Plastic Leaded Chip Carrier		44 68 84					
	BGA Ball Grid Array		P-BGA 256 352 S-BGA 352 432 600 P-BGA 352 480 672					
	CSP Chip Scale Packaging		F I/O CSP 112 144 160 F/O CSP 184 216 264					
Pin Insertion Type	PGA Ceramic Pin Grid Array		135 179 240 257 299 401 600					

LEGEND:

- In Mass Production
- Under Development

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