HG72C Series

µCBIC - embedded SH-1 RISC
ASIC Product Brief

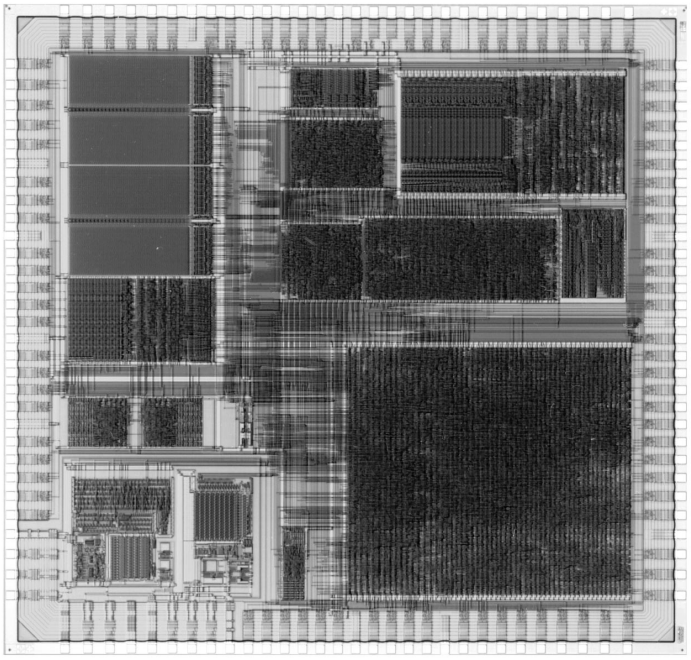
HITACHI

Description

The HG72C Series is a family of cell-based integrated circuits (CBICs) implemented in advanced 0.6µm CMOS process technology featuring 5.0 V and 3.3 V low-voltage core operation. Process-optimized libraries are available to support high performance and low-power design requirements. Besides the low-voltage interface support for 3.3 V I/Os, the HG72C Series also provides support for standard 5V I/Os. Focusing on high density routing the HG72C can achieve a maximum of 500,000 usable gates. Two and three layer metalizations are available. Compilers for Single Port and Dual Port RAM, ROM, and Datapath provide necessary building blocks for ASIC designers, and a variety of analog modules including ADCs, DACs, and high frequency PLL allow designers to realize a single chip with both digital and analog functions.

The HG72C Series includes Hitachi's µCBIC solution, which is a CBIC with an embedded Hitachi SuperH RISC SH-1 microcontroller core. The SH-1 microcontroller is capable of 20MHz performance and is compileable such that the peripheral modules and memories may be added or deleted to customize performance and functionality to match design requirements. The SuperH-1 microcontroller core is fully supported with a comprehensive design and programming solution that includes the microcontroller core, simulation models, emulation support and software suite. The widely available emulators, compilers, and OS currently used for the the high volume standard devices are fully compatible with the embedded core. With 20 MIPS performance, Hitachi's SH-1 µCBIC supports a broad range of consumer and embedded applications with a highly integrated, cost effective, single chip solution.

The design tools, based on popular CAE tools, support a complete design environment capable of the seamless development of CBIC and µCBIC designs from logic simulation to final layout. Post-layout simulation takes full account of delay-driven components by factoring wiring RC parasitics and waveform ramp parameters into the simulation. The automated fault diagnostics and boundary scan design functions facilitate design-for-testability. Also, the application of automated clock-tree generation techniques greatly adds to the reduction of clock skew. The HG72C Series supports extensive libraries for core cells (internal cells) and I/O cells for the more popular CAE tools.



HG72C Die Photo

Features

HG72C Series Cell-Based ICs for the System Solutions

- Maximum Usable Gate Count:
  — 500,000 usable gates
- Raw Gate Density:
  — 4,000 gates/mm2
- Compileable Microcontroller core:
  — 32 bit SH-1 RISC
- Analog Modules:
  — ADCs, DACs, and PLL

CBIC/µCBIC (µCBIC contains an embedded microprocessor)

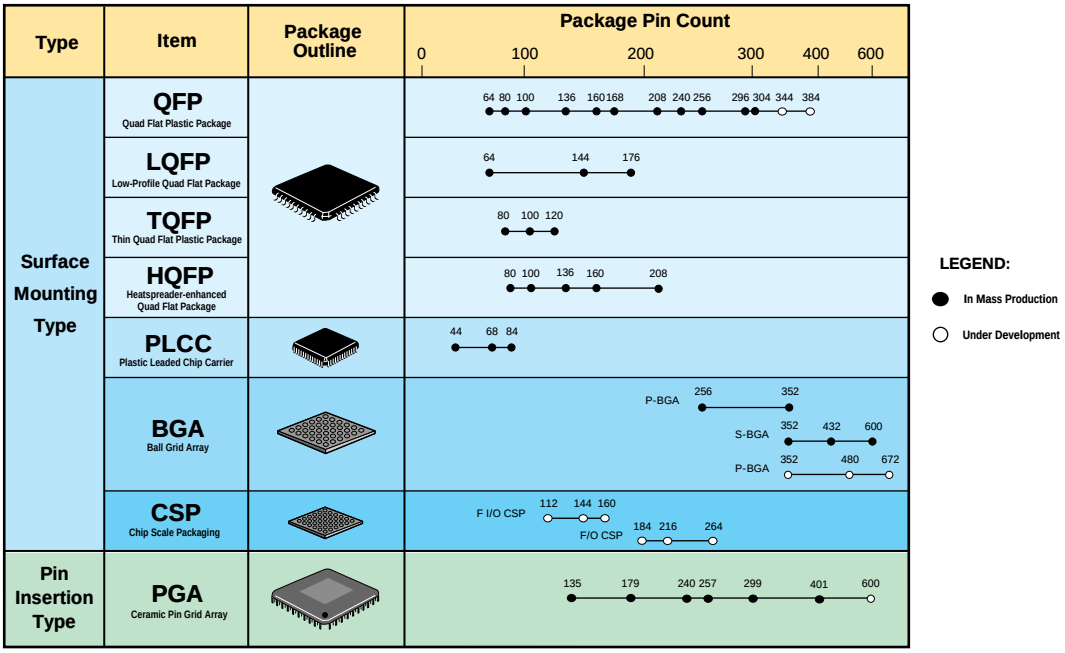
Part No.	Feature Size	Leff	Core Power	I/O Power	Metal Layers	Max. Usable Gates	Max. Gate Density (Typical)	Processor Available
HG71C	0.8µm	0.7µm	3.3/5.0V	3.3/5.0V	2, 3	300K Gates	4.1K Gates (~2.2K Gates)	H8/300H
HG72C	0.6µm	0.55µm	3.3/5.0V	3.3/5.0V	2, 3	600K Gates	7.2K Gates (~4K Gates)	H8/300H, SH-1
HG73C	0.4µm	0.35µm	2.0/3.3V	2.0/3.3/5.0V	3, 4, 5	3M Gates	18.9K Gates (~10K Gates)	H8/300H, H8S SH-1, SH-3
HG74C	0.25µm	0.2µm	1.8/2.5V	1.8/2.5/ 3.3/5.0V	3, 4, 5	6M Gates	39.2K Gates (~20K Gates)	SH-4

Embedded DRAM

Part No.	Feature Size	L eff	Core Power	I/O Power	Metal Layers	Max. Usable Gates (w/out DRAM)	Max. Gate Density (Typical)	Max. DRAM (w/o gates)	DRAM Density (w/overhead)	Processor Available
HG73M	0.28µm	0.35µm	3.3/5.0V	3.3/5.0V	3, 4, 5	3M Gates	18.9K Gates (~10K Gates)	140Mbit	50KBytes/ mm2	H8/300H, H8S, SH-1, SH-3

HG72C Series

ASIC Packaging Guide



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