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1. General Description

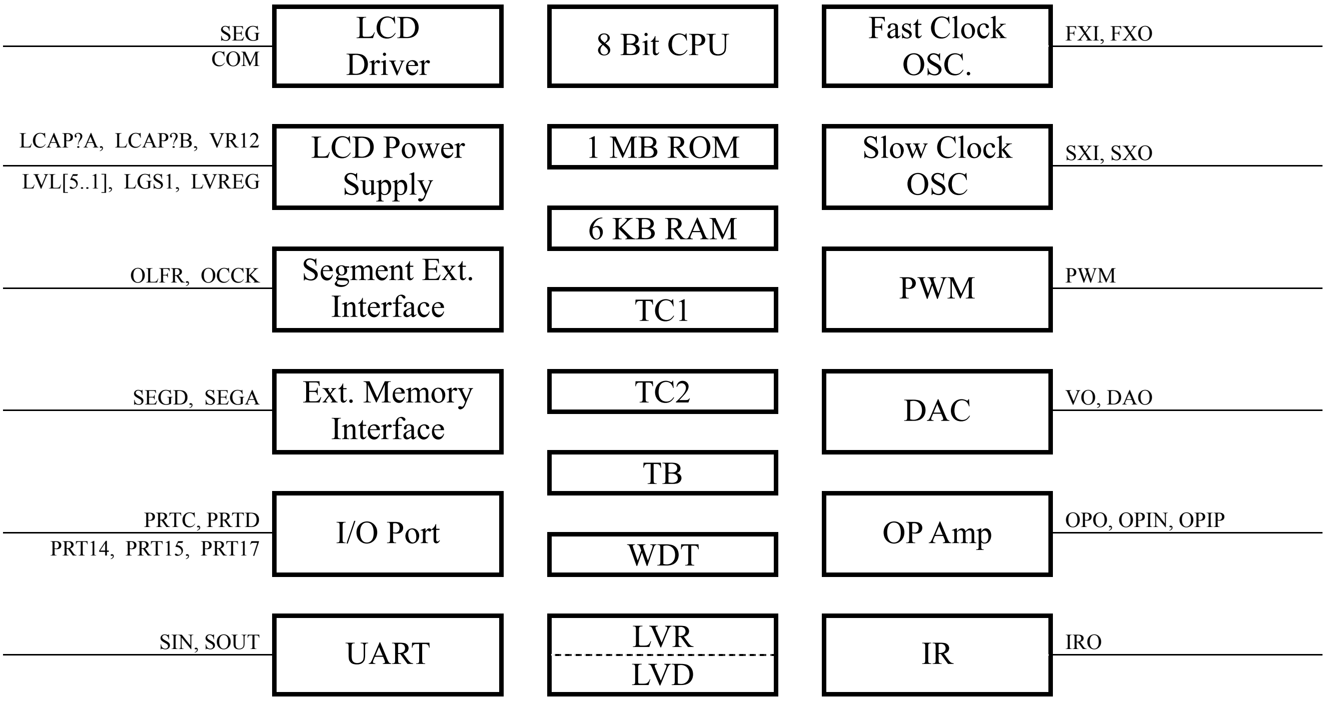
HE84G770 is a member of 8-bit Micro-controller series developed by King Billion Electronics. External address and data buses are provided to access external memory. This chip has 6400 pixel, 16 gray-scale LCD driver built-in with 4 different configurations, and up to 36-bit general purpose I/O ports. The built-in OP comparator can be used with light, voice, temperature and humility sensor or used to detect the battery low. The 8-bit current-type D/A converter and PWM driver output provides the complete speech output solutions. The 1M bytes ROM and 6K bytes RAM can be used for the storage of large speech data, image and text, etc. An UART is included to provide the serial communication capability. IR output makes it suitable for remote control applications.

The instruction sets of HE80004H series is easy to learn and simple to use. There are only thirty-two instructions and four addressing modes. Most of instructions take only 3 oscillator clocks to complete. The performance and low power consumption make it suitable for battery-powered applications such as translator, data bank, educational toy, digital voice recorder, etc.

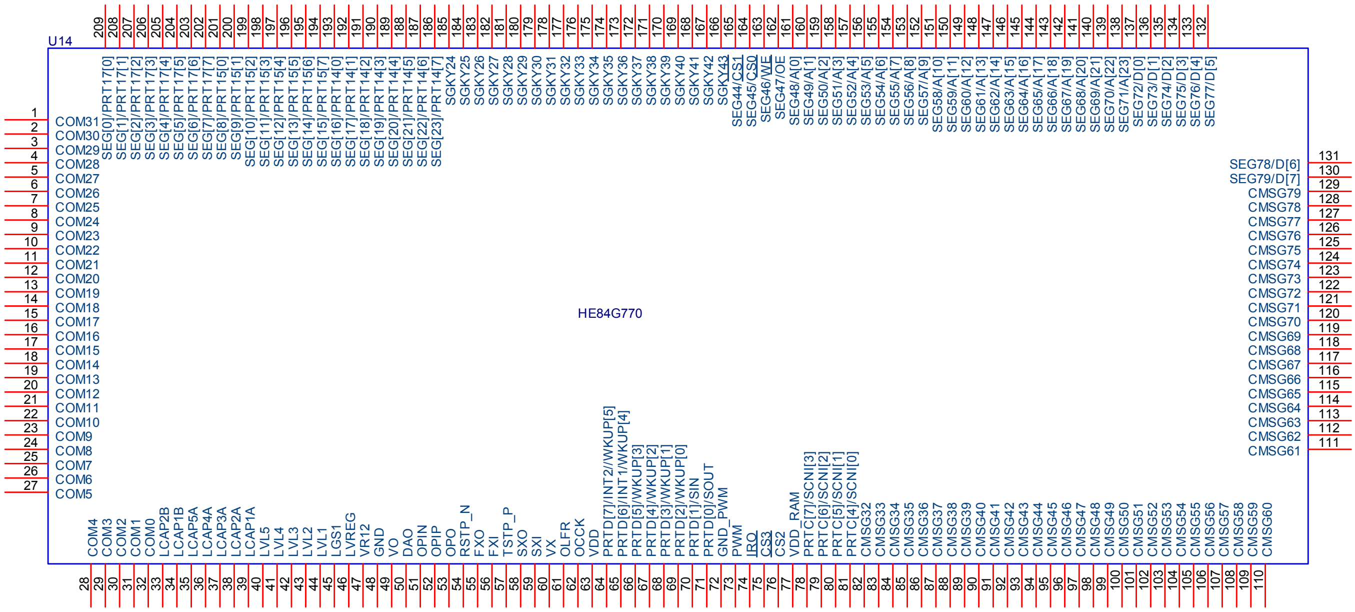
2. Features

- ✓ Operation Voltage: 2.4V ~ 3.6V
- ✓ Dual Clock System: Fast clock: 32768 Hz ~ 8 MHz
  Slow clock: 32768 Hz
- ✓ Four Operation Modes: Fast, Slow, Idle, Sleep modes.
- ✓ Internal ROM: 1M Bytes (512K Byte Program ROM, 512K Byte Data ROM)
- ✓ Internal RAM: 6K Bytes (Shared with LCD RAM).
- ✓ 6 ~ 36 bit Bi-directional general purpose I/O port with push-pull or open-Drain output type selectable for each I/O pin by mask option.
- ✓ Up to 6400 pixels with 16, 4 gray-scale or Black/White LCD driver.
- ✓ Segment extender interface with KDGS80.
- ✓ 4 LCD configurations: [32 × 128], [48 × 112], [64 × 96], [80 × 80].
- ✓ Built-in LCD power supply with input power regulator, voltage multiplier circuit and bias generating circuit.
- ✓ PWM output.
- ✓ 8-bit current-type DAC output.
- ✓ Built-in OP comparator.
- ✓ Built-in UART for serial communication.
- ✓ IR output.
- ✓ Low voltage reset: 2.2V
- ✓ Low voltage detection: 2.4V, 2.6V, 2.8V and 3.0V
- ✓ Built-in keyboard auto scan hardware for up to 4×20 key matrix (shared with LCD SEG pins) not only reduces the hardware cost, but also reduces the firmware effort.
- ✓ Watchdog timer.
- ✓ Two 16-bit timers and one time-base timer.
- ✓ Two external interrupts, three internal timer interrupts and one internal UART interrupt.
- ✓ Instruction set: 32 instructions, 4 addressing modes.

3. Functional Block Diagram



4. Pin Description



Pin Name	I/O	Description
COM[31..0]	O	LCD COMMON Driver pads.
LCAP2B	O	Charge Pump Capacitor Pin.
LCAP1B	O	Charge Pump Capacitor Pin.
LCAP5A	O	Charge Pump Capacitor Pin.
LCAP4A	O	Charge Pump Capacitor Pin.
LCAP3A	O	Charge Pump Capacitor Pin.
LCAP2A	O	Charge Pump Capacitor Pin.

Pin Name	I/O	Description
LCAP1A	O	Charge Pump Capacitor Pin.
LVL5	P	LCD Bias Voltage 5.
LVL4	P	LCD Bias Voltage 4
LVL3	P	LCD Bias Voltage 3
LVL2	P	LCD Bias Voltage 2
LVL1	P	LCD Bias Voltage 1.
LGS1	I	Regulator Voltage Setting
LVREG	O	Voltage Regulator Output. VDD is regulated to generate LVREG, which is in turns pumped to LVL5. Adjust resistor between LGS1 and LVREG to set LVREG voltage.
VR12	I	Charge Pump Input. The buffered output of the fine-adjusted VREG.
GND	P	Power Ground Input.
VO	O	DAC Output.
DAO	O	Alternate output of DAC.
OPIN	I	Inverting input of OP Amp.
OPIP	I	Non-inverting input of OP Amp.
OPO	O	Output of OP Amp.
RSTP_N	I	System Reset Input Pin. Level trigger, active low on this pin will put the chip in reset state.
FXO, FXI	O, B	External fast clock pin. Two types of oscillator can be selected by MO_FXTAL (‘0’ for RC type and ‘1’ for crystal type). For RC type oscillator, one resistor needs to be connected between FXI and GND. For crystal oscillator, one crystal needs to be placed between FXI and FXO. Please refer to application for details.
TSTP_P	I	Test input pin. Please bond this pad and reserve a test point on PCB for debugging. But for improving ESD, please connect this point with zero Ohm resistor to GND.
SXO, SXI	O, I	External slow clock pins. Slow clock is clock source for LCD display, TIMER1, Time-Base and other internal blocks. Both crystal and RC oscillator are provided. The slow clock type can be selected by mask option MO_SXTAL. Choose ‘0’ for RC type and ‘1’ for crystal oscillator.
VX	I	Input pin for x32 PLL circuit. Connect to external resistor and capacitors as shown in application circuit.
OLFR	O	LCD frame signal for interfacing with LCD segment extender KDGS80.
OCCK	O	LCD data load pin for interfacing with LCD segment extender KDGS80.
VDD	P	Positive power Input. A 0.1 µF decoupling capacitors should be placed as close to IC VDD and GND pads as possible for best decoupling effect.
PRTD[7..2] PRTD[1]/SIN PRTD[0]/SOUT	B	8-bit bi-directional I/O port D. The output type of I/O pad can also be selected by mask option MO_DPP[7..0] (‘1’ for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, ‘1’ must be outputted before reading the pin. PRTD[7..2] can be used as wake-up pins. PRTD[7..6] can be as external interrupt sources. PRTD[1] shares pad with UART Receiver SIN pin. PRTD[0] shares pad with UART transmitter SOUT pin.
GND_PWM	O	Dedicated Ground for PWM output.
PWM	O	The PWM output can drive speaker or buzzer directly. Set the bit2 of VOC register as one to turn on PWM. Using VDD & PWM to drive output device.
IRO	O	The Infrared output.
PRTC[7..4]/ SCNI[3..0]	B	4-bit bi-directional I/O port C. The output type of I/O pad can also be selected by mask option MO_CPP[7..4] (‘1’ for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, ‘1’ must be outputted before reading the pin. PRTC[7..4] is shared with Key Scan Dedicated Input SCNI[3..0]. The Key Scan function can be disabled by clearing MO_LCDKEY mask option to ‘0’.
VDD_RAM	P	Dedicated power input for RAM
CMSG[32..79]	O	COM[32..79] pads are shared with SEG[127..80] outputs. The functions of the pads to be

Pin Name	I/O	Description
		COM drivers or SEG drivers can be selected by mask option MO_COM[1..0]. Please refer to LCD driver configuration for details.
SEG[79..72]/ D[7..0]	O	LCD segment SEG[79..72] outputs share pads with data bus D[7..0] of external memory.
SEG[71..48]/ A[23..0]	O	LCD segment SEG[71..48] outputs share pads with address bus A[23..0] of external memory.
OE/SEG[47]	O	Output Enable control of external memory shares pad with SEG[47]. The function of the pin is selected by mask option MO_ EXMEM. When used as Output Enable control pin, this pin control the tri-state buffer of external memory data bus.
WE/SEG[46]	O	Write Enable 0 of external memory shares pad with SEG[46]. The function of the pin is selected by mask option MO_ EXMEM. When used as Write Enable control pin, this pin controls Write Enable input of the external memory device.
CS0/SEG[45]	O	Chip Enable 0 of external memory shares pad with SEG[45]. The function of the pin is selected by mask option MO_ EXMEM. When used as Chip Enable control pin, this pin select or de-select the external memory device based on the address been accessed.
CS1/SEG[44]	O	Chip Enable 1 of external memory shares pad with SEG[44]. The function of the pin is selected by mask option MO_ EXMEM. When used as Chip Enable control pin, this pin select or de-select the external memory device based on the address been accessed.
CS2	O	Chip Enable 2 of external memory. This pin select or de-select the external memory device based on the address been accessed.
CS3	O	Chip Enable 3 of external memory. This pin select or de-select the external memory device based on the address been accessed.
SGKY[43..24]	O	LCD segments share pads with key scan out SCNO[19..0]. The key scan function of these pins can be disabled by mask option clearing MO_LCDKEY to ‘0’, then SGKY[43..24] function as LCD segment driver only. Setting MO_LCDKEY to ‘1’ will turn on the key scan function.
PRT14[7..0]/ SEG[23..16]	B/ O	8 bits bi-directional I/O port 14 are shared with LCD segment pads SEG[23..16]. The function of the pad can be selected individually by mask options MO_LIO14[7..0]. (‘1’ for LCD and ‘0’ for I/O). The output type of I/O pad can also be selected by mask option MO_14PP[7..0] (1 for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, “1” must be outputted before reading.
PRT15[7..0]/ SEG[15..8]	B/ O	8 bits bi-directional I/O port 15 are shared with LCD segment pads SEG[15..8]. The function of the pad can be selected individually by mask options MO_LIO15[7..0]. (‘1’ for LCD and ‘0’ for I/O). The output type of I/O pad can also be selected by mask option MO_15PP[7..0] (1 for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, “1” must be outputted before reading.
PRT17[7..0]/ SEG[7..0]	B/ O	8 bits bi-directional I/O port 17 are shared with LCD segment pads SEG[7..0]. The function of the pad can be selected individually by mask options MO_LIO17[7..0]. (‘1’ for LCD and ‘0’ for I/O). The output type of I/O pad can also be selected by mask option MO_17PP[7..0] (1 for push-pull and ‘0’ for open-drain). As the output structure of I/O pad does not contain tri-state buffer. When using the I/O as input, “1” must be outputted before reading.

5. ROM Map Configurations

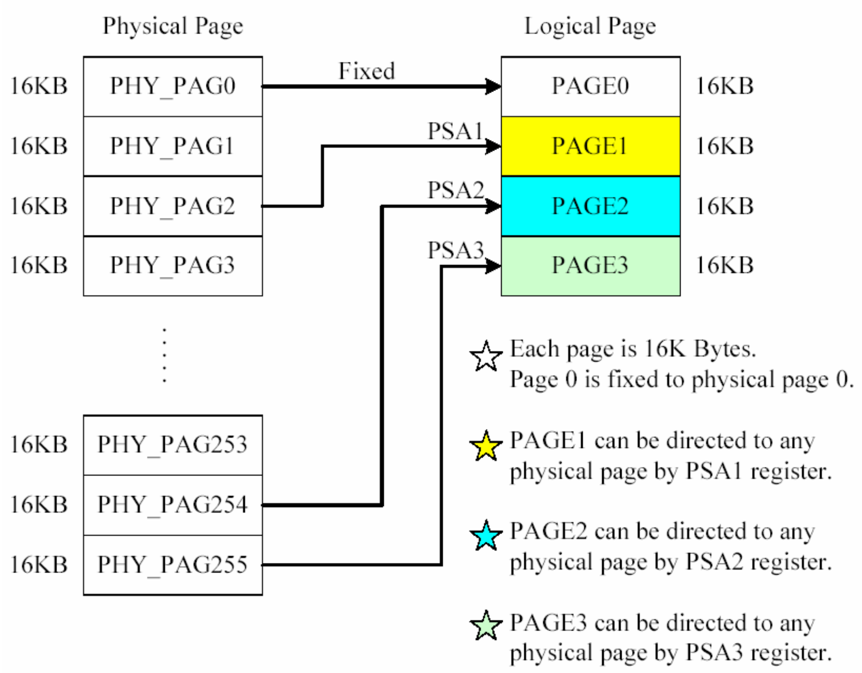
The chip has built-in 1M bytes internal ROM including 512K bytes program ROM and 512K bytes data ROM. In addition, address and data buses are provided to access External ROM. The MCU can access up to 4 MB Program ROM and up to 16 MB Data space through external buses. The SEG[79..72], SEG[71..44] pads are used as either data and address buses for external ROM or LCD segment driver pads depending on the mask option MO_EXMEM. When the external ROM mask option is selected, the MCU will retrieve the instructions and data from external ROM through the address and data buses and the SEG[79..44] will not be LCD segment signals.

The bit 14 ~ 15 bit of 16-bit logical program address can be mapped to any one of 256 pages through mapping registers PSA1, PSA2, PSA3. As logical page 0 can not be moved and is always physical page 0, the PSA1 ~ PSA3 contain the physical page addresses of logical pages 1 ~ 3.

Logical Address															
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Page Addr.		A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

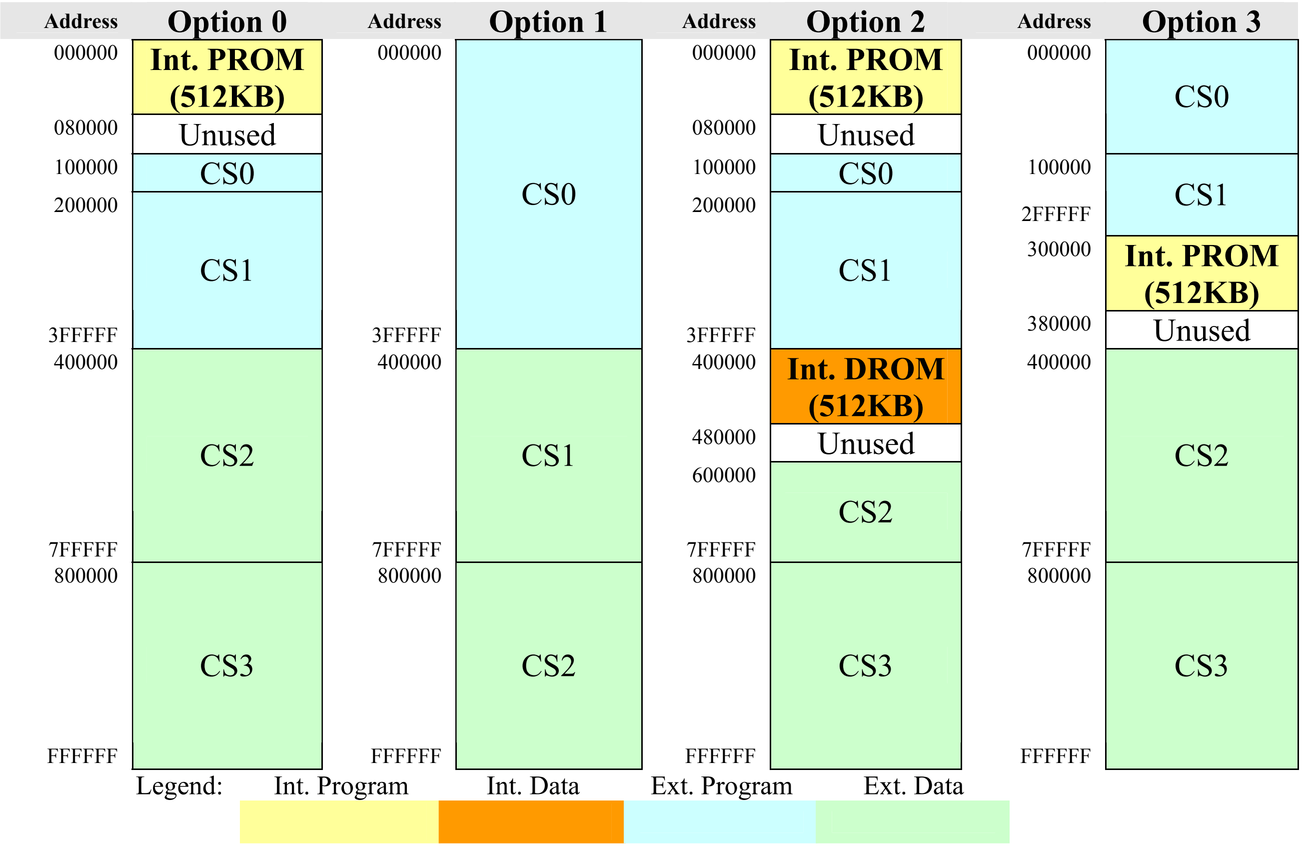
A[15..14]	**Logical Page**	**Physical Page Address**	**Physical Address**
00	0	0	00 A[13..0]
01	1	PSA1	PSA1+A[13..0]
10	2	PSA2	PSA2+A[13..0]
11	3	PSA3	PSA3+A[13..0]

Register	**Address**	**Type**	**Bits Definition**								**Reset**
PSA1	0x2C	R/W	A21	A20	A19	A18	A17	A16	A15	A14	0x01
PSA2	0x2D	R/W	A21	A20	A19	A18	A17	A16	A15	A14	0x02
PSA3	0x2E	R/W	A21	A20	A19	A18	A17	A16	A15	A14	0x03

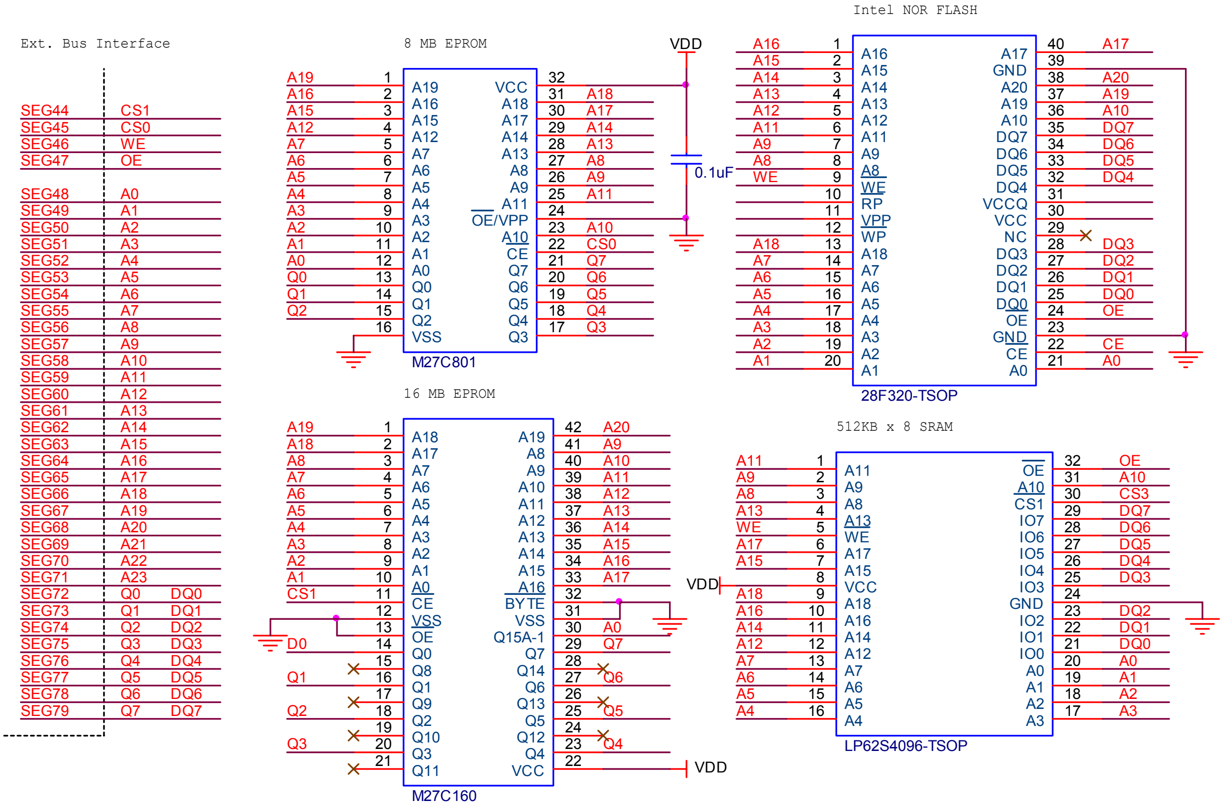


There are four configurations for external memory as determined by mask option MO_PMODE. For example, when option 0 is selected, 512 KB of internal ROM will occupy the address range from 0x000000 ~ 0x07FFFF of memory space, while CS1 controls external memory device whose address ranges from 0x200000 to 3FFFFF, etc. If the Option 1 is selected, the internal program/data ROM will be skipped and the external ROM will be active by CS0~2.

MO_ PMODE [1..0]	Configuration
00	Option 0
01	Option 1
10	Option 2
11	Option 3



Note: Option2 shall be selected when the internal "Data ROM" is used.



6. External RAM/Flash Memory

The external memory devices can be mask ROM, static RAM, or NOR type FLASH memory. Most NOR type FLASH memory and RAM can be used as external storage for both program and data, so program can be downloaded to external memory devices for future execution. However, there are some limitations. When the data is to be written to external devices, the loader must reside in internal program space. In other words, the loader program must be in internal ROM. When download is completed, the program in the external memory can be run.

The data written to external memory devices is through a command interface composed of AC, EXMC and EXMD registers for setting up the memory addresses, switching memory buses, generating read/write pulse, read/write memory contents, etc. When writing finishes, external memory can be switched back the external address and data bus for CPU to fetch data and instructions.

Writing to address registers is through a common register AC. Writing to AC will write data to ACL, ACH, and then ACP in cyclic order. The sequence will be reset by an access to EXMD register. Therefore, it is advisable to make a dummy read to EXMD register before writing to AC, so that the first write will be made to ACL.

AC	Mode	Description	Reset Value
ACL	R/W	Address Counter Low for AC7 ~ AC0	“--------“
ACH	R/W	Address Counter High for AC15 ~ AC8	“--------“
ACP	R/W	Address Counter Page for AC23 ~ AC16	“--------“

ACL: Lowest Significant Byte of Address Counter.

ACH: 2nd Byte of Address Counter.

ACP: Most Significant Byte of Address Counter.

Register	Mode	Description								Reset Value
EXMC	W	-	-	-	-	-	DNLD	RD	WR	“-----011”

DNLD: Switch the bus to download bus.

RD: Read pulse control.

WR: Write pulse control.

After address setup, the data can be written to address device through EXMD register. Program must generate the required write pulse by firmware. The address counter AC will automatically increment with each read/write access.

Register	Type	Description								Reset Value
EXMD	R/W	D7	D6	D5	D4	D3	D2	D1	D0	“--------“

The procedure for downloading data from I/O or any other sources, i.e. command mode ROM device is as follows:

1. Switch the external memory to download bus by setting the DNLD bit of EXMC register.

2. Make a dummy read to EXMD register to reset the AC pointer.
3. Set up the address for transferring data by first writing to ACL, and then ACH and ACP with the first 3 writes to register.
4. Start writing to addressed device by first writing 1 byte of data to EXMD register, clear WR bit of CMD register and set it again, the AC will increment with each write pulse.
5. To read addressed device, clear RD bit of EXMC register, read EXMD register and set RD bit again. The AC will also increment with each read pulse. Read back for verification is optional. Please note that read back can also be made through external address and data bus when the bus is switched back to program bus.
6. Switch back to normal bus for program execution and data access by clearing the DNLD bit of EXMC register.

Please note that NOR FLASH memory from different manufacturers such as Intel, AMD, SST, etc. requires various command sequence to set up. Programmer still needs to follow the respective specifications of the vendors.

7. LCD Display RAM Map

The gray-scale LCD driver can be configured to be a 16 gray-scale, 4 gray-scales or black and white display by mask option MO_GRAY_MODE.

MO_GRAY_MODE[1..0]	Gray levels
00	16
01	4
10	2 (B/W)
11	2 (B/W)

For 4 gray-scale displays, 2-bit of RAM is required for each pixel and 4 bit for 16 gray-scale display, 1-bit for black and white display. For different LCD configuration, the LCD display RAM is arranged differently. The following figure shows one byte of RAM in different LCD configurations:

0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Black/White	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0
4 Gray scales	SEG3		SEG2		SEG1		SEG0	
16 Gray scales	SEG1				SEG0			

The 16 Gray Scale register GRAY0 ~ GRAYF is the mapping register between the levels selected in RAM and the real gray scale. In other words, if the content of GRAY0 is 0x03, when value of a certain pixel is 0, the displayed effect will correspond to actual gray level 3. The 16 gray scale display use all 16 registers GRAY0 ~ GRAYF to select among 32 available gray levels to correspond to level 0 ~ 15, while

4 gray scale display utilizes registers GRAY0 ~ GRAY3 to select among 32 gray levels to correspond to level 0 ~ 3. Thus user can pick the gray levels which give the best and most linear effect.

16 Gray-scale registers share a common register address GRAY16. When writing is made to the register, it will step down to next register in order. The writing sequence can be reset by clearing bit 5 of LCDC register.

GRAY16	Field					
Seq.	Bit4	Bit3	Bit2	Bit1	Bit0	Reset
1	GRAY0					0x00
2	GRAY1					0x02
3	GRAY2					0x04
4	GRAY3					0x06
5	GRAY4					0x08
6	GRAY5					0x0A
7	GRAY6					0x0C
8	GRAY7					0x0E
9	GRAY8					0x10
10	GRAY9					0x12
11	GRAYA					0x14
12	GRAYB					0x16
13	GRAYC					0x18
14	GRAYD					0x1A
15	GRAYE					0x1C
16	GRAYF					0x1E

8. LCD driver configurations

There are 4 LCD configurations selectable by mask option MO_COM[1:0] for this chip. The function of CMSG[79..32] in each configuration is listed in the following table.

MO_COM[1:0]	**Configuration COM x SEG**	**CMSG[79..64] Function**	**CMSG[63..48] Function**	**CMSG[47..32] Function**
00	32 x 128	SEG[80..95]	SEG[96..111]	SEG[112..127]
01	48 x 112	SEG[80..95]	SEG[96..111]	COM[47..32]
10	64 x 96	SEG[80..95]	COM[63..48]	COM[47..32]
11	80 x 80	COM[79..64]	COM[63..48]	COM[47..32]

COMXSEG	32X128	48X112	64X96	80X80
CMSG32	SEG127	COM32	COM32	COM32
CMSG33	SEG126	COM33	COM33	COM33
CMSG34	SEG125	COM34	COM34	COM34
CMSG35	SEG124	COM35	COM35	COM35
CMSG36	SEG123	COM36	COM36	COM36
CMSG37	SEG122	COM37	COM37	COM37
CMSG38	SEG121	COM38	COM38	COM38
CMSG39	SEG120	COM39	COM39	COM39
CMSG40	SEG119	COM40	COM40	COM40
CMSG41	SEG118	COM41	COM41	COM41
CMSG42	SEG117	COM42	COM42	COM42
CMSG43	SEG116	COM43	COM43	COM43
CMSG44	SEG115	COM44	COM44	COM44
CMSG45	SEG114	COM45	COM45	COM45
CMSG46	SEG113	COM46	COM46	COM46
CMSG47	SEG112	COM47	COM47	COM47
CMSG48	SEG111	SEG111	COM48	COM48
CMSG49	SEG110	SEG110	COM49	COM49
CMSG50	SEG109	SEG109	COM50	COM50
CMSG51	SEG108	SEG108	COM51	COM51
CMSG52	SEG107	SEG107	COM52	COM52
CMSG53	SEG106	SEG106	COM53	COM53
CMSG54	SEG105	SEG105	COM54	COM54
CMSG55	SEG104	SEG104	COM55	COM55
CMSG56	SEG103	SEG103	COM56	COM56
CMSG57	SEG102	SEG102	COM57	COM57
CMSG58	SEG101	SEG101	COM58	COM58
CMSG59	SEG100	SEG100	COM59	COM59
CMSG60	SEG99	SEG99	COM60	COM60
CMSG61	SEG98	SEG98	COM61	COM61
CMSG62	SEG97	SEG97	COM62	COM62
CMSG63	SEG96	SEG96	COM63	COM63
CMSG64	SEG95	SEG95	SEG95	COM64
CMSG65	SEG94	SEG94	SEG94	COM65
CMSG66	SEG93	SEG93	SEG93	COM66
CMSG67	SEG92	SEG92	SEG92	COM67
CMSG68	SEG91	SEG91	SEG91	COM68
CMSG69	SEG90	SEG90	SEG90	COM69
CMSG70	SEG89	SEG89	SEG89	COM70
CMSG71	SEG88	SEG88	SEG88	COM71
CMSG72	SEG87	SEG87	SEG87	COM72
CMSG73	SEG86	SEG86	SEG86	COM73
CMSG74	SEG85	SEG85	SEG85	COM74
CMSG75	SEG84	SEG84	SEG84	COM75
CMSG76	SEG83	SEG83	SEG83	COM76
CMSG77	SEG82	SEG82	SEG82	COM77
CMSG78	SEG81	SEG81	SEG81	COM78
CMSG79	SEG80	SEG80	SEG80	COM79

Since there are four LCD driver configurations available for selection by mask option, the RAM map of LCD drivers is listed below for all configurations. Any unused RAM as marked with '*' sign can be used as general purposed RAM by application programs.

8.1. 16 Gray Scale LCD Display RAM Map

<table>
<tr><th></th><th></th><th colspan="2">32x128</th><th colspan="2">48x112</th><th colspan="2">64x96</th><th colspan="2">80x80</th><th></th></tr>
<tr><td>Page</td><td></td><td>F</td><td>0</td><td>F</td><td>0</td><td>F</td><td>0</td><td>F</td><td>0</td><td></td></tr>
<tr><td>1</td><td>00</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td rowspan="4">COM0</td></tr>
<tr><td></td><td>10</td><td colspan="2">S63 ~ S32</td><td colspan="2">S63 ~ S32</td><td colspan="2">S63 ~ S32</td><td colspan="2">S63 ~ S32</td></tr>
<tr><td></td><td>20</td><td colspan="2">S95 ~ S64</td><td colspan="2">S95 ~ S64</td><td colspan="2">S95 ~ S64</td><td>*</td><td>S80 ~ S64</td></tr>
<tr><td></td><td>30</td><td colspan="2">S127 ~ S96</td><td>*</td><td>S112 ~ S96</td><td colspan="2">*</td><td colspan="2">*</td></tr>
<tr><td></td><td>40</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td rowspan="4">COM1</td></tr>
<tr><td></td><td>50</td><td colspan="2">S63 ~ S32</td><td colspan="2">S63 ~ S32</td><td colspan="2">S63 ~ S32</td><td colspan="2">S63 ~ S32</td></tr>
<tr><td></td><td>60</td><td colspan="2">S95 ~ S64</td><td colspan="2">S95 ~ S64</td><td colspan="2">S95 ~ S64</td><td>*</td><td>S80 ~ S64</td></tr>
<tr><td></td><td>70</td><td colspan="2">S127 ~ S96</td><td>*</td><td>S112 ~ S96</td><td colspan="2">*</td><td colspan="2">*</td></tr>
<tr><td></td><td>80</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td rowspan="4">COM2</td></tr>
<tr><td></td><td>90</td><td colspan="2">S63 ~ S32</td><td colspan="2">S63 ~ S32</td><td colspan="2">S63 ~ S32</td><td colspan="2">S63 ~ S32</td></tr>
<tr><td></td><td>A0</td><td colspan="2">S95 ~ S64</td><td colspan="2">S95 ~ S64</td><td colspan="2">S95 ~ S64</td><td>*</td><td>S80 ~ S64</td></tr>
<tr><td></td><td>B0</td><td colspan="2">S127 ~ S96</td><td>*</td><td>S112 ~ S96</td><td colspan="2">*</td><td colspan="2">*</td></tr>
<tr><td></td><td>C0</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td colspan="2">S31 ~ S00</td><td>COM3</td></tr>
</table>

		32x128	48x112		64x96	80x80		
Page		F 0	F	0	F 0	F	0	
	D0	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0	S127 ~ S96	*	S112 ~ S96	*	*		
2	00	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM4
	10	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	20	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30	S127 ~ S96	*	S112 ~ S96	*	*		
	40	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM5
	50	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70	S127 ~ S96	*	S112 ~ S96	*	*		
	80	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM6
	90	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	B0	S127 ~ S96	*	S112 ~ S96	*	*		
	C0	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM7
	D0	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0	S127 ~ S96	*	S112 ~ S96	*	*		
3	00	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM8
	10	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	20	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30	S127 ~ S96	*	S112 ~ S96	*	*		
	00	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM9
	50	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70	S127 ~ S96	*	S112 ~ S96	*	*		
	80	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM10
	90	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	B0	S127 ~ S96	*	S112 ~ S96	*	*		
	C0	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM11
	D0	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0	S127 ~ S96	*	S112 ~ S96	*	*		
4	00	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM12
	10	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	20	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30	S127 ~ S96	*	S112 ~ S96	*	*		
	40	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM13
	50	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70	S127 ~ S96	*	S112 ~ S96	*	*		
	80	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM14
	90	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	B0	S127 ~ S96	*	S112 ~ S96	*	*		
	C0	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM15
	D0	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0	S127 ~ S96	*	S112 ~ S96	*	*		
5	00	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM16
	10	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	20	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30	S127 ~ S96	*	S112 ~ S96	*	*		

		32x128	48x112		64x96	80x80		
Page		F 0	F	0	F 0	F	0	
	40	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM17
	50	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70	S127 ~ S96	*	S112 ~ S96	*	*		
	80	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM18
	90	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	B0	S127 ~ S96	*	S112 ~ S96	*	*		
	C0	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM19
	D0	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0	S127 ~ S96	*	S112 ~ S96	*	*		
6	00	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM20
	10	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	20	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30	S127 ~ S96	*	S112 ~ S96	*	*		
	40	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM21
	50	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70	S127 ~ S96	*	S112 ~ S96	*	*		
	80	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM22
	90	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	B0	S127 ~ S96	*	S112 ~ S96	*	*		
	C0	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM23
	D0	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0	S127 ~ S96	*	S112 ~ S96	*	*		
7	00	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM24
	10	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	20	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30	S127 ~ S96	*	S112 ~ S96	*	*		
	40	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM25
	50	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70	S127 ~ S96	*	S112 ~ S96	*	*		
	80	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM26
	90	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	B0	S127 ~ S96	*	S112 ~ S96	*	*		
	C0	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM27
	D0	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0	S127 ~ S96	*	S112 ~ S96	*	*		
8	00	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM28
	10	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	20	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30	S127 ~ S96	*	S112 ~ S96	*	*		
	40	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM29
	50	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70	S127 ~ S96	*	S112 ~ S96	*	*		
	80	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM30
	90	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	

		32x128	48x112		64x96	80x80		
Page		F 0	F	0	F 0	F	0	
	B0	S127 ~ S96	*	S112 ~ S96	*	*		
	C0	S31 ~ S00	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM31
	D0	S63 ~ S32	S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0	S95 ~ S64	S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0	S127 ~ S96	*	S112 ~ S96	*	*		
9	00	*	S31 ~ S00		S31 ~ S00	S31 ~ S00		COM32
	10		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	20		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30		*	S112 ~ S96	*	*		
	40		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM33
	50		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70		*	S112 ~ S96	*	*		
	80		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM34
	90		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0		S95 ~ S64		S95 ~ S64		S80 ~ S64	
	B0		*	S112 ~ S96	*	*		
	C0		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM35
	D0		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0		*	S112 ~ S96	*	*		
A	00		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM36
	10		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	20		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30		*	S112 ~ S96	*	*		
	40		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM37
	50		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70		*	S112 ~ S96	*	*		
	80		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM38
	90		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	B0		*	S112 ~ S96	*	*		
	C0		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM39
	D0		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0		*	S112 ~ S96	*	*		
B	00		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM40
	10		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	20		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30		*	S112 ~ S96	*	*		
	40		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM41
	50		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70		*	S112 ~ S96	*	*		
	80		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM42
	90		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	B0		*	S112 ~ S96	*	*		
	C0		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM43
	D0		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0		*	S112 ~ S96	*	*		
C	00		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM44
	10		S63 ~ S32		S63 ~ S32	S63 ~ S32		

		32x128	48x112		64x96	80x80		
Page		F 0	F	0	F 0	F	0	
	20		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	30		*	S112 ~ S96	*	*		
	40		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM45
	50		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	60		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	70		*	S112 ~ S96	*	*		
	80		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM46
	90		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	A0		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	B0		*	S112 ~ S96	*	*		
	C0		S31 ~ S00		S31 ~ S00	S31 ~ S00		COM47
	D0		S63 ~ S32		S63 ~ S32	S63 ~ S32		
	E0		S95 ~ S64		S95 ~ S64	*	S80 ~ S64	
	F0		*	S112 ~ S96	*	*		
D	00		*		S31 ~ S00	S31 ~ S00		COM48
	10				S63 ~ S32	S63 ~ S32		
	20				S95 ~ S64	*	S80 ~ S64	
	30				*	*		
	40				S31 ~ S00	S31 ~ S00		COM49
	50				S63 ~ S32	S63 ~ S32		
	60				S95 ~ S64	*	S80 ~ S64	
	70				*	*		
	80				S31 ~ S00	S31 ~ S00		COM50
	90				S63 ~ S32	S63 ~ S32		
	A0				S95 ~ S64	*	S80 ~ S64	
	B0				*	*		
	C0				S31 ~ S00	S31 ~ S00		COM51
	D0				S63 ~ S32	S63 ~ S32		
	E0				S95 ~ S64	*	S80 ~ S64	
	F0				*	*		
E	00				S31 ~ S00	S31 ~ S00		COM52
	10				S63 ~ S32	S63 ~ S32		
	20				S95 ~ S64	*	S80 ~ S64	
	30				*	*		
	40				S31 ~ S00	S31 ~ S00		COM53
	50				S63 ~ S32	S63 ~ S32		
	60				S95 ~ S64	*	S80 ~ S64	
	70				*	*		
	80				S31 ~ S00	S31 ~ S00		COM54
	90				S63 ~ S32	S63 ~ S32		
	A0				S95 ~ S64	*	S80 ~ S64	
	B0				*	*		
	C0				S31 ~ S00	S31 ~ S00		COM55
	D0				S63 ~ S32	S63 ~ S32		
	E0				S95 ~ S64	*	S80 ~ S64	
	F0				*	*		
F	00				S31 ~ S00	S31 ~ S00		COM56
	10				S63 ~ S32	S63 ~ S32		
	20				S95 ~ S64	*	S80 ~ S64	
	30				*	*		
	40				S31 ~ S00	S31 ~ S00		COM57
	50				S63 ~ S32	S63 ~ S32		
	60				S95 ~ S64	*	S80 ~ S64	
	70				*	*		
	80				S31 ~ S00	S31 ~ S00		COM58

		32x128	48x112	64x96	80x80		
Page		F 0	F 0	F 0	F 0		
	90			S63 ~ S32	S63 ~ S32		
	A0			S95 ~ S64	*	S80 ~ S64	
	B0			*	*		
	C0			S31 ~ S00	S31 ~ S00		COM59
	D0			S63 ~ S32	S63 ~ S32		
	E0			S95 ~ S64	*	S80 ~ S64	
	F0			*	*		
10	00			S31 ~ S00	S31 ~ S00		COM60
	10			S63 ~ S32	S63 ~ S32		
	20			S95 ~ S64	*	S80 ~ S64	
	30			*	*		
	40			S31 ~ S00	S31 ~ S00		COM61
	50			S63 ~ S32	S63 ~ S32		
	60			S95 ~ S64	*	S80 ~ S64	
	70			*	*		
	80			S31 ~ S00	S31 ~ S00		COM62
	90			S63 ~ S32	S63 ~ S32		
	A0			S95 ~ S64	*	S80 ~ S64	
	B0				*		
	C0			S31 ~ S00	S31 ~ S00		COM63
	D0			S63 ~ S32	S63 ~ S32		
	E0			S95 ~ S64	*	S80 ~ S64	
	F0			*	*		
11	00				S31 ~ S00		COM64
	10				S63 ~ S32		
	20				*	S80 ~ S64	
	30				*		
	40				S31 ~ S00		COM65
	50				S63 ~ S32		
	60				*	S80 ~ S64	
	70				*		
	80				S31 ~ S00		COM66
	90				S63 ~ S32		
	A0				*	S80 ~ S64	
	B0				*		
	C0				S31 ~ S00		COM67
	D0				S63 ~ S32		
	E0				*	S80 ~ S64	
	F0				*		
12	00				S31 ~ S00		COM68
	10				S63 ~ S32		
	20				*	S80 ~ S64	
	30				*		
	40				S31 ~ S00		COM69
	50				S63 ~ S32		
	60				*	S80 ~ S64	
	70				*		
	80				S31 ~ S00		COM70
	90				S63 ~ S32		
	A0				*	S80 ~ S64	
	B0				*		
	C0				S31 ~ S00		COM71
	D0				S63 ~ S32		
	E0				*	S80 ~ S64	
	F0				*		

		32x128	48x112	64x96	80x80		
Page		F 0	F 0	F 0	F	0	
13	00				S31 ~ S00		COM72
	10				S63 ~ S32		
	20				*	S80 ~ S64	
	30				*		
	40				S31 ~ S00		COM73
	50				S63 ~ S32		
	60				*	S80 ~ S64	
	70				*		
	80				S31 ~ S00		COM74
	90				S63 ~ S32		
	A0				*	S80 ~ S64	
	B0				*		
	C0				S31 ~ S00		COM75
	D0				S63 ~ S32		
	E0				*	S80 ~ S64	
	F0				*		
14	00				S31 ~ S00		COM76
	10				S63 ~ S32		
	20				*	S80 ~ S64	
	30						
	40				S31 ~ S00		COM77
	50				S63 ~ S32		
	60				*	S80 ~ S64	
	70				*		
	80				S31 ~ S00		COM78
	90				S63 ~ S32		
	A0				*	S80 ~ S64	
	B0				*		
	C0				S31 ~ S00		COM79
	D0				S63 ~ S32		
	E0				*	S80 ~ S64	
	F0				*		

8.2. 4 Gray Scale LCD Display RAM Map

Page		32x128	48x112		64x96		80x80		
		F 0	F	0	F	0	F	0	
1	00	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM0
	10	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	20	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM1
	30	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	40	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM2
	50	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	60	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM3
	70	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	80	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM4
	90	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	A0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM5
	B0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	C0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM6
	D0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	E0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM7
	F0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	

Page		32x128	48x112		64x96		80x80		
		F 0	F	0	F	0	F	0	
2	00	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM8
	10	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	20	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM9
	30	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	40	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM10
	50	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	60	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM11
	70	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	80	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM12
	90	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	A0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM13
	B0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	C0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM14
	D0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	E0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM15
	F0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
3	00	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM16
	10	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	20	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM17
	30	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	40	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM18
	50	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	60	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM19
	70	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	80	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM20
	90	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	A0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM21
	B0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	C0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM22
	D0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	E0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM23
	F0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
4	00	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM24
	10	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	20	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM25
	30	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	40	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM26
	50	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	60	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM27
	70	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	80	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM28
	90	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	A0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM29
	B0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	C0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM30
	D0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	E0	S63 ~ S00	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM31
	F0	S127 ~ S64	*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
5	00	*	S63 ~ S00		S63 ~ S00		S63 ~ S00		COM32
	10		*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	20		S63 ~ S00		S63 ~ S00		S63 ~ S00		COM33
	30		*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	40		S63 ~ S00		S63 ~ S00		S63 ~ S00		COM34
	50		*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	60		S63 ~ S00		S63 ~ S00		S63 ~ S00		COM35

Page		32x128		48x112		64x96		80x80		
		F	0	F	0	F	0	F	0	
	70			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	80			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM36
	90			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	A0			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM37
	B0			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	C0			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM38
	D0			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	E0			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM39
	F0			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
6	00			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM40
	10			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	20			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM41
	30			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	40			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM42
	50			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	60			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM43
	70			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	80			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM44
	90			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	A0			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM45
	B0			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	C0			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM46
	D0			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
	E0			S63 ~ S00		S63 ~ S00		S63 ~ S00		COM47
	F0			*	S112~ S64	*	S96 ~ S64	*	S80~ S64	
7	00			*		S63 ~ S00		S63 ~ S00		COM48
	10					*	S96 ~ S64	*	S80~ S64	
	20					S63 ~ S00		S63 ~ S00		COM49
	30					*	S96 ~ S64	*	S80~ S64	
	40					S63 ~ S00		S63 ~ S00		COM50
	50					*	S96 ~ S64	*	S80~ S64	
	60					S63 ~ S00		S63 ~ S00		COM51
	70					*	S96 ~ S64	*	S80~ S64	
	80					S63 ~ S00		S63 ~ S00		COM52
	90					*	S96 ~ S64	*	S80~ S64	
	A0					S63 ~ S00		S63 ~ S00		COM53
	B0					*	S96 ~ S64	*	S80~ S64	
	C0					S63 ~ S00		S63 ~ S00		COM54
	D0					*	S96 ~ S64	*	S80~ S64	
	E0					S63 ~ S00		S63 ~ S00		COM55
	F0					*	S96 ~ S64	*	S80~ S64	
8	00					S63 ~ S00		S63 ~ S00		COM56
	10					*	S96 ~ S64	*	S80~ S64	
	20					S63 ~ S00		S63 ~ S00		COM57
	30					*	S96 ~ S64	*	S80~ S64	
	40					S63 ~ S00		S63 ~ S00		COM58
	50					*	S96 ~ S64	*	S80~ S64	
	60					S63 ~ S00		S63 ~ S00		COM59
	70					*	S96 ~ S64	*	S80~ S64	
	80					S63 ~ S00		S63 ~ S00		COM60
	90					*	S96 ~ S64	*	S80~ S64	
	A0					S63 ~ S00		S63 ~ S00		COM61
	B0					*	S96 ~ S64	*	S80~ S64	
	C0					S63 ~ S00		S63 ~ S00		COM62
	D0					*	S96 ~ S64	*	S80~ S64	

Page		32x128		48x112		64x96		80x80		
		F	0	F	0	F	0	F	0	
	E0					S63 ~ S00		S63 ~ S00		COM63
	F0					*	S96 ~ S64	*	S80~ S64	
9	00					*		S63 ~ S00		COM64
	10							*	S80~ S64	
	20							S63 ~ S00		COM65
	30							*	S80~ S64	
	40							S63 ~ S00		COM66
	50							*	S80~ S64	
	60							S63 ~ S00		COM67
	70							*	S80~ S64	
	80							S63 ~ S00		COM68
	90							*	S80~ S64	
	A0							S63 ~ S00		COM69
	B0							*	S80~ S64	
	C0							S63 ~ S00		COM70
	D0							*	S80~ S64	
	E0							S63 ~ S00		COM71
	F0							*	S80~ S64	
A	00							S63 ~ S00		COM72
	10							*	S80~ S64	
	20							S63 ~ S00		COM73
	30							*	S80~ S64	
	40							S63 ~ S00		COM74
	50							*	S80~ S64	
	60							S63 ~ S00		COM75
	70							*	S80~ S64	
	80							S63 ~ S00		COM76
	90							*	S80~ S64	
	A0							S63 ~ S00		COM77
	B0							*	S80~ S64	
	C0							S63 ~ S00		COM78
	D0							*	S80~ S64	
	E0							S63 ~ S00		COM79
	F0							*	S80~ S64	

8.3. Black and White LCD Display RAM Map

Page		32x128		48x112		64x96		80x80		
		F	0	F	0	F	0	F	0	
0	00	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM0
	10	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM1
	20	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM2
	30	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM3
	40	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM4
	50	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM5
	60	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM6
	70	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM7
	80	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM8
	90	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM9
	A0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM10
	B0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM11
	C0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM12
	D0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM13

Page		32x128		48x112		64x96		80x80		
		F	0	F	0	F	0	F	0	
	E0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM14
	F0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM15
1	00	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM16
	10	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM17
	20	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM18
	30	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM19
	40	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM20
	50	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM21
	60	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM22
	70	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM23
	80	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM24
	90	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM25
	A0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM26
	B0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM27
	C0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM28
	D0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM29
	E0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM30
	F0	S127 ~ S00		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM31
2	00	*		*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM32
	10			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM33
	20			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM34
	30			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM35
	40			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM36
	50			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM37
	60			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM38
	70			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM39
	80			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM40
	90			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM41
	A0			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM42
	B0			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM43
	C0			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM44
	D0			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM45
	E0			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM46
	F0			*	S111 ~ S00	*	S95 ~ S00	*	S79 ~ S00	COM47
3	00			*		*	S95 ~ S00	*	S79 ~ S00	COM48
	10					*	S95 ~ S00	*	S79 ~ S00	COM49
	20					*	S95 ~ S00	*	S79 ~ S00	COM50
	30					*	S95 ~ S00	*	S79 ~ S00	COM51
	40					*	S95 ~ S00	*	S79 ~ S00	COM52
	50					*	S95 ~ S00	*	S79 ~ S00	COM53
	60					*	S95 ~ S00	*	S79 ~ S00	COM54
	70					*	S95 ~ S00	*	S79 ~ S00	COM55
	80					*	S95 ~ S00	*	S79 ~ S00	COM56
	90					*	S95 ~ S00	*	S79 ~ S00	COM57
	A0					*	S95 ~ S00	*	S79 ~ S00	COM58
	B0					*	S95 ~ S00	*	S79 ~ S00	COM59
	C0					*	S95 ~ S00	*	S79 ~ S00	COM60
	D0					*	S95 ~ S00	*	S79 ~ S00	COM61
	E0					*	S95 ~ S00	*	S79 ~ S00	COM62
	F0					*	S95 ~ S00	*	S79 ~ S00	COM63
4	00					*		*	S79 ~ S00	COM64
	10							*	S79 ~ S00	COM65
	20							*	S79 ~ S00	COM66
	30							*	S79 ~ S00	COM67
	40							*	S79 ~ S00	COM68

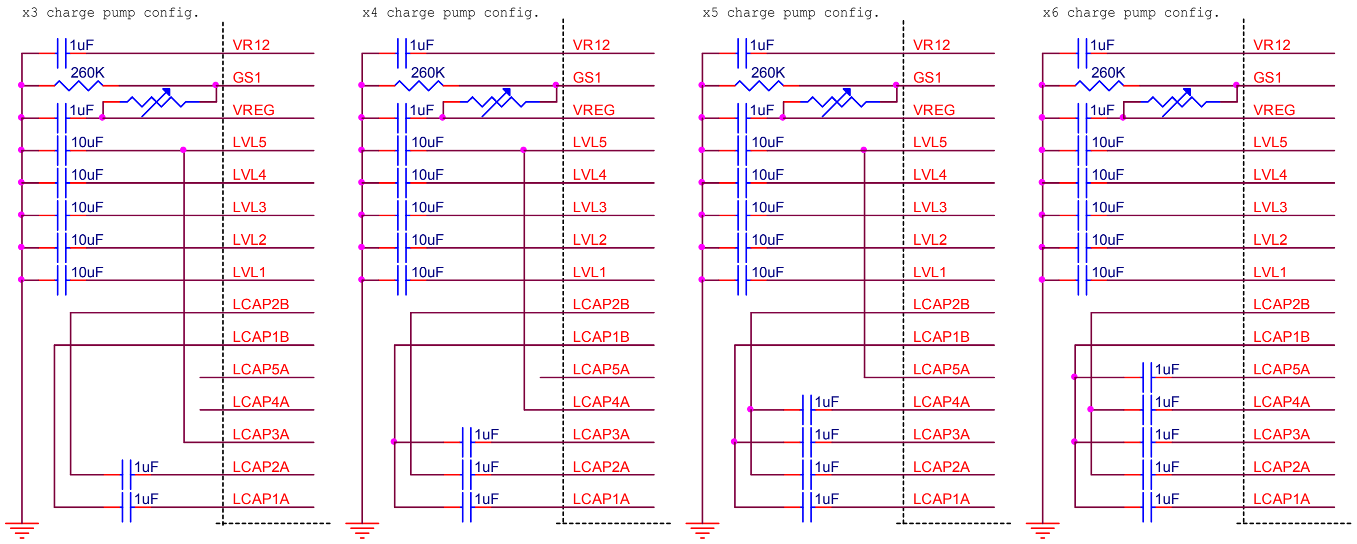
Page		32x128		48x112		64x96		80x80		
		F	0	F	0	F	0	F	0	
	50							*	S79 ~ S00	COM69
	60							*	S79 ~ S00	COM70
	70							*	S79 ~ S00	COM71
	80							*	S79 ~ S00	COM72
	90							*	S79 ~ S00	COM73
	A0							*	S79 ~ S00	COM74
	B0							*	S79 ~ S00	COM75
	C0							*	S79 ~ S00	COM76
	D0							*	S79 ~ S00	COM77
	E0							*	S79 ~ S00	COM78
	F0							*	S79 ~ S00	COM79

9. LCD Power Supply

The built-in LCD power supply is equipped with input voltage regulator, voltage multiplier and bias voltage generating circuit with active buffer instead of passive resistor voltage dividing network. The input voltage is regulated to LVREG using the internally generated LVAG as reference voltage. LVREG can be adjusted by resistors between LGS1 and LVREG.

LVREG adjustment guideline: First, the level of LVREG must be at least 0.4 volt lower than VDD at all time, even at the end of battery life, for the regulator to function properly. For example, if the VDD is expected to drop to 2.2 volts when battery is low, then the level of LVREG can only be set at 1.8 volts max. With this constraint, it is advisable to set the level of LVREG as high as possible and use less charge pump stages to save power. For example, to pump the 2 volts to 12 volts requires 6 charge pump stages; to pump the 2.4 volts to 12 volts requires only 5 charge pump stages which consumes less power. So it is recommended not to adjust the LVREG to an unnecessary low level.

Voltage charge pump: The LVREG is then multiplied by 3, 4, 5, or 6 times, depending on external capacitors configurations as shown below, to generate LVL5. Please note that LVL5 must be lower than 12 volts to prevent chip from break-down. The capacitance of capacitors connected to LVL1~5 shall be increased in an appropriate amount based on the LCD panel size. For small size LCD panel, the 10uF capacitors are enough, but 22uF capacitors may be necessary for large LCD size application.



The internal reference voltage has built-in temperature compensation to make up the reference voltage deviation due to the temperature variation. Four temperature coefficients are available for selection by mask option MO_TC. It's used to compensate the LCD display feature in the range of room temperature to low temperature. User shall set the MO_TC value based on the LCD feature and operation environment. If the MO_TC is set to "11", the LCD power voltage will have 0.33% decrease when the temperature increases one degree.

MO_TC	Temp. Coef.
00	-0.0 %/°C
01	-0.16 %/°C
10	-0.22 %/°C
11	-0.33 %/°C

Heavy LCD load: The bias voltages LVL1 ~ LVL5 for LCD driver are generated from internal bias network and buffered with active drive to provide greater bias driving strength. Usually larger LCD panel needs more power to drive. Four driving capabilities, which can be selected by mask option, are provided to suit the needs of application. Please note that high driving capability will cause the power consumption to be increased.

MO_LOAD	Driving Current
00	Low
01	Medium
10	Medium high
11	High

External LCD power supply: If the maximal driving option is still inadequate for applications, user may choose to use the external LCD power supply. In that case, there are still several options:

First, use the internal regulator and charge pump circuit to generate the high voltage, but use external bias network to generate and supply the bias voltage level LVL1 ~ LVL5. In this case, the buffered active drive for internal bias needs to be turned off to avoid confliction with external bias circuit and DC current drain.

The second option is to turn off internal charge pump circuit, and use external DC-to-DC circuit to generate high voltage and use internal bias network and buffer active drive to generate bias voltages.

The third option is to turn off internal regulator, charge pump circuit, and bias buffer circuit and use external circuit to generate the high voltage and bias voltage. The individual circuit can be turned on or off by the appropriate bit in LCDC and LCDPS registers and MO_PUMPE mask option.

Configuration	MO_PUMPE	BUFE	Internal Charge pump	Internal Bias Buffer
External charge-pump/External bias circuit	0	0	×	×
External charge-pump/Internal bias circuit	0	1	×	✓
Internal charge-pump/ External bias circuit	1	0	✓	×
Internal charge-pump/Internal bias circuit	1	1	✓	✓

Address	NAME	Field								Mode	RESET
0FH	LCDC	-	-	CLR_GP	Reserved			BLANK	LCDE	W	--1x xx10
24H	LCDPS	-	-	-	-	-	POWDN	PAcc	BUFE	R/W	---- -100

Field	Value	Function
POWDN	0	LCD power system enabled.
	1	LCD power system disabled.
PAcc	0	Internal Charge-pump doesn't accelerate to charge the capacitor.
	1	Internal Charge-pump accelerates to charge the capacitor.
BUFE	0	Disable internal bias network buffer
	1	Enable internal bias network buffer
CLR_GP	0	Reset GRAY palette register pointer by write '0' to CLR_P bit.
	1	No effect on GRAY palette register pointer
BLANK	0	normal display
	1	LCD display blanked. The COM signals of LCD driver output inactive levels (LVL4 and LVL1) while SEG signals output normal display patterns.
LCDE	0	LCD driver disabled, LCD driver has no output signal and LVL1 ~ LVL5 is pulled up to VDD
	1	LCD driver master control enabled

Bias Setting: Different duties require different bias settings. There is some theoretical correspondence between the Duty and Bias Setting. However, it is better to use it as starting point and adjust it with real LCD panel connected to it to determine the final setting. The theoretic relationship between the duty and bias setting is as the following table: However, the actual bias setting should be determined based on the best visual effect given when the target LCD panel is connected.

Duty Cycle	Normal Bias Setting
32 duty	1/7
48 duty	1/8
64 duty	1/9
80 duty	1/10

The bias setting is made by mask option MO_LBSR[1..0].

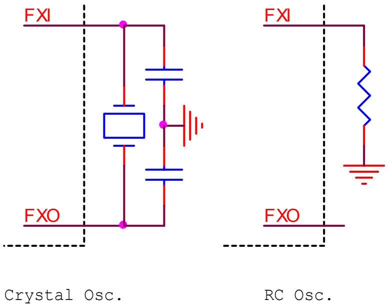
MO_LBSR[1..0]	Bias Setting
00	1/7
01	1/8
10	1/9
11	1/10

Please note that LCD driver must be turned off before the IC goes into sleep mode. That means user must clear the bit 0 of LCDC to turn off LCD driving circuit before setting bit6 of OP1 to enter sleep mode. Large current might happen if the procedure is not followed. Please note that LCD driver uses slow clock as clock source. The LCD display will not display normally if it works in Fast clock only mode because the LCD refresh action is too fast. The LCD power system shall be enabled by set POWDN to '1' before the LCD display is enabled. In order to accelerate the capacitor charging, the "PAcc" bit shall be set when the LCD power system is initialized and then "PAcc" can be cleared when the LCD power system is stable.

10. Oscillators

The MCU is equipped with two clock sources with a variety of selections on the types of oscillators to choose from. The system designer can select oscillator types based on the cost target, timing accuracy requirements etc. Crystal, Resonator or the RC oscillator can be used as fast clock source, components should be placed as close to the pins as possible. The type of oscillator used is selected by mask option MO_FXTAL.

MO_FXTAL	Fast clock type
0	RC Oscillator.
1	Crystal Oscillator.



The RC oscillator has a built-in capacitor. An external resistor is needed to connect from FXI to GND to determine the oscillation frequency. The capacitance of internal RC oscillator is selected by mask option MO_RCAP[2..0].

MO_RCAP[2:0]	Internal RC Cap. (pF)
000	2
001	4
010	7
011	14
100	20
101	40
110	50
111	60

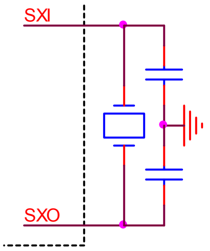
The following table shows the combinations of R and C, and the resulting frequency. Please note that oscillation frequency in the table only represents oscillation frequencies of certain samples. The actual oscillation frequency may vary up to ±15% from lot to lot due to process parameter variations. User must take this into consideration when using this chip in applications.

Ring Oscillator Frequency Table

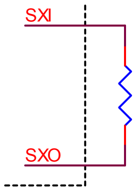
R (KΩ) \ C	40	20	14	7	4	2	
30.20	0.8	1.5	2.0	3.0	4.0	5.0	MHz
19.92	1.2	2.2	2.8	4.4	5.6	7.0	MHz
9.98	2.3	4.0	5.1	7.5	-	-	MHz

Two types of oscillator, crystal and RC, can be used as slow clock selectable by mask option MO_SXTAL. If used time keeping function or other applications that required the accurate timing, crystal oscillator is recommended. If the timing accuracy is not important, then RC type oscillator can be used to reduce cost.

MO_SXTAL	Slow clock type
0	R/C oscillator
1	Crystal oscillator



Crystal Osc.



RC Osc.

With two clock sources available, the system can switch among operation modes of Normal, Slow, Idle, and Sleep modes by the setting of OP1 and OP2 registers as shown in tables below to suit the needs of application such as high speed or low power, etc.

OP1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	DRDY	STOP	SLOW	INTE	T2E	T1E	Z	C
Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	-	-

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	-	-	0	-	-	-	-

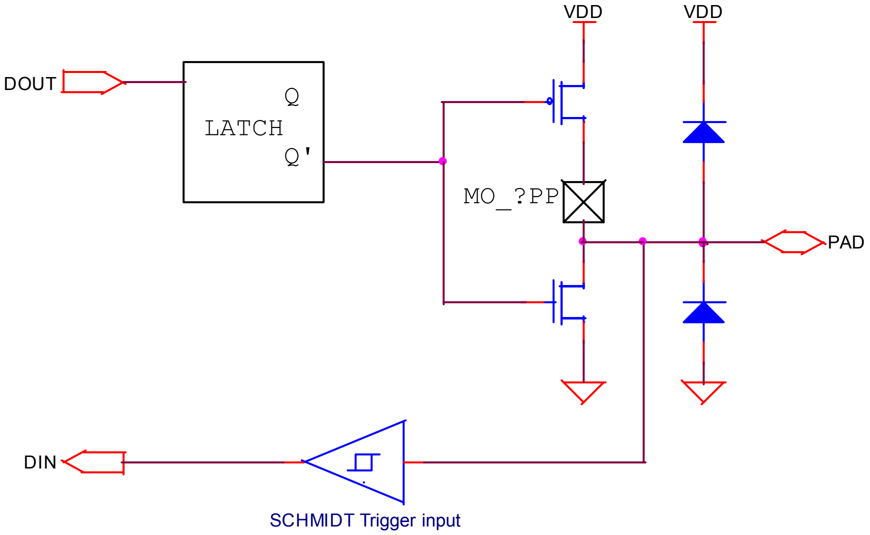
If the dual clock mode is used, the LCD display, Timer1 and Timer Base will derive its clock source from slow clock while the other blocks will operate with the fast clock.

11. General Purpose I/O

There are two dedicated general purpose I/O ports, PRTC[7..4] and PRTD, while the PRT14, PRT15 and PRT17 are multiplexed with LCD segment driver pins. All the I/O Ports are bi-directional and of nontri-state output structure. The output has weak sourcing (50 μA) and stronger sinking (1 mA) capability and each can be configured as push-pull or open-drain output structure individually by mask option.

When the I/O port is used as input, the weakly high sourcing can be used as weakly pull-up. Open drain can be used if the pull-up is not required and let the external driver to drive the pin. Please note that a floating pad could cause more power consumption since the noise could interfere with the circuit and cause the input to toggle. A '1' needs to be written to port first before reading the input data from the I/O pin. If the PMOS is used as pull-up, care should be taken to avoid the constant power drain by DC path between pull-up and external circuit.

The input port has built-in Schmidt trigger to prevent it from chattering. Hysteresis level of Schmidt trigger is 1/3 VDD.



As pads of PRT14, PRT15 and PRT17 are shared with LCD segment driver, the function of the pad is determined by mask options. Following table is the setting for MO_LIO?[...] and MO_?PP[...] and others related to LCD display setting and pin assignment features.

MO_LIO?[…]	MO_?PP[...]	I/O Port	LCD Pin
0	0	Open-drain output	--
0	1	Push-pull output	--
1	0	--	xx
1	1	--	LCD Display

--: Function not available.

xx: Displayable, but may have abnormal leakage current, do not use.

12. Key Scan Circuit

The built-in 4x20 hardware keyboard scan circuit helps to reduce the pin counts where application requires large key matrix and high LCD pixel count as well as the firmware effort. As key-scan pins are shared with LCD segment and PRTC4 ~ PRTC7 pins, it is advisable to put resistors between segment pins and key matrix to avoid shorting the segment pins when two or more keys in the same row are pressed simultaneously. Two key can be detected simultaneously and the first detected key code is stored in KEY0 register and the second in KEY1 register respectively. The key code for each key location is listed in the following table.

Key Loc	SCNI0	SCNI1	SCNI2	SCNI3
SCNO0	0x80	0xA0	0xC0	0xE0
SCNO1	0x81	0xA1	0xC1	0xE1
SCNO2	0x82	0xA2	0xC2	0xE2
SCNO3	0x83	0xA3	0xC3	0xE3
SCNO4	0x84	0xA4	0xC4	0xE4
SCNO5	0x85	0xA5	0xC5	0xE5
SCNO6	0x86	0xA6	0xC6	0xE6
SCNO7	0x87	0xA7	0xC7	0xE7
SCNO8	0x88	0xA8	0xC8	0xE8
SCNO9	0x89	0xA9	0xC9	0xE9
SCNO10	0x8A	0xAA	0xCA	0xEA
SCNO11	0x8B	0xAB	0xCB	0xEB
SCNO12	0x8C	0xAC	0xCC	0xEC
SCNO13	0x8D	0xAD	0xCD	0xED
SCNO14	0x8E	0xAE	0xCE	0xEE
SCNO15	0x8F	0xAF	0xCF	0xEF
SCNO16	0x90	0xB0	0xD0	0xF0
SCNO17	0x91	0xB1	0xD1	0xF1
SCNO18	0x92	0xB2	0xD2	0xF2
SCNO19	0x93	0xB3	0xD3	0xF3

KEY0	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x22	R	Row Index		Column Index				

KEY1	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x23	-	Row Index		Column Index				

The bit 7 of KEY0 and KEY1 is repeat indicator when the same key is scanned for the second time, the R bit will be cleared to indicate the key is not released yet.

The key-scan function can be turned on/off by mask option MO_LCDKEY.

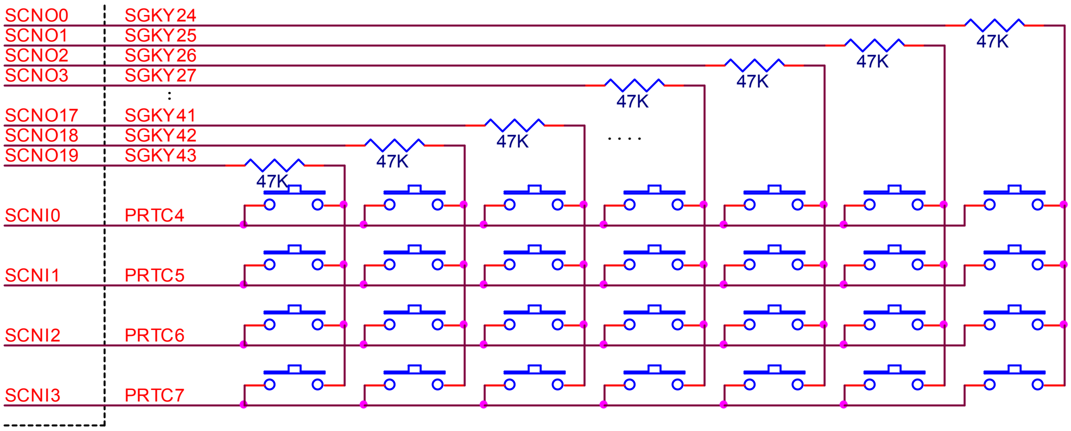
MO_LCDKEY	SGKY[43..24] Function
0	as SEG only
1	as SEG as well as KEY_SCAN

The pulse width of key-scan signal can be selected by mask options MO_SNCK[1:0].

MO_SNCK[1..0]	Key Scan Pulse Width
00	0.5 SCK
01	1.0 SCK
10	1.5 SCK
11	2.0 SCK

The strength of key-scan signal can also be selected by mask options MO_SCDRV[1:0].

MO_SCDRV[1..0]	Key Scan Signal Strength
00	weakest
01	weak
10	strong
11	strongest

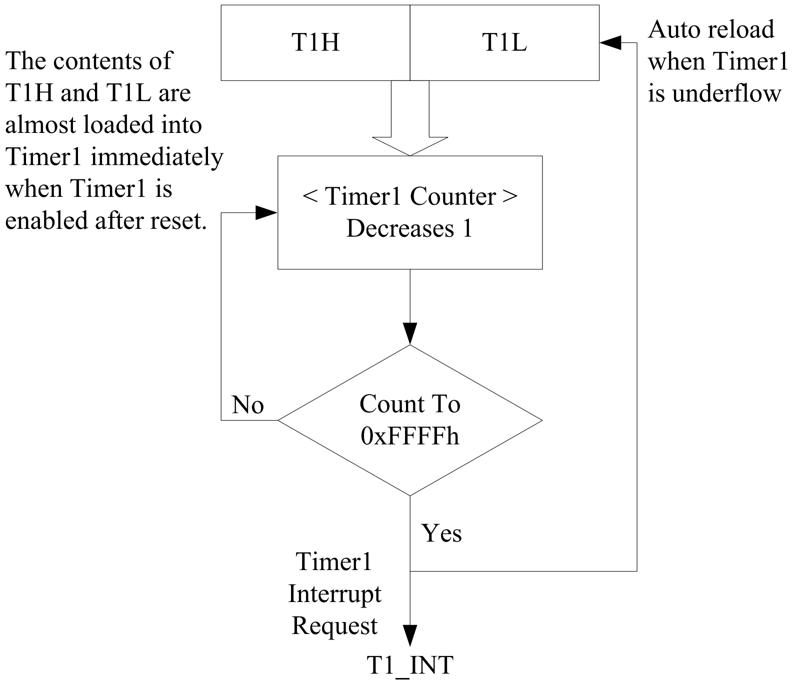


13. Timer1

The Timer1 consists of two 8-bit write-only preload registers T1H and T1L and 16-bit down counter. If Timer1 is enabled, the counter will decrement by one with each incoming clock pulse. Timer1 interrupt will be generated when the counter underflows - counts down to FFFFH. And the counter will be automatically reloaded with the value of T1H and T1L.

The clock source of Timer1 is derived from slow clock "SCK" at dual clock or slow clock only mode. And it comes from the fast clock "FCK" at fast clock only mode.

Please note that the interrupt is generated when counter counts from 0000H to FFFFH. If the value of T1H and T1L is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this moment, interrupt will be generated immediately and value of T1H and T1L will be loaded since it counts to FFFFH. So the T1H and T1L value should be set before enabling Timer1.



The Timer1 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC1_IER	2	R/W	0: TC1 interrupt is disabled. (default) 1: TC1 interrupt is enabled.
T1L	0x03	T1L[7:0]	7~0	W	Low byte of TC1 pre-load value
T1H	0x04	T1H[7:0]	7~0	W	High byte of TC1 pre-load value
OP1	0x09	TC1E	2	R/W	0: TC1 is disabled. (default) 1: TC1 is enabled.

14. Timer2

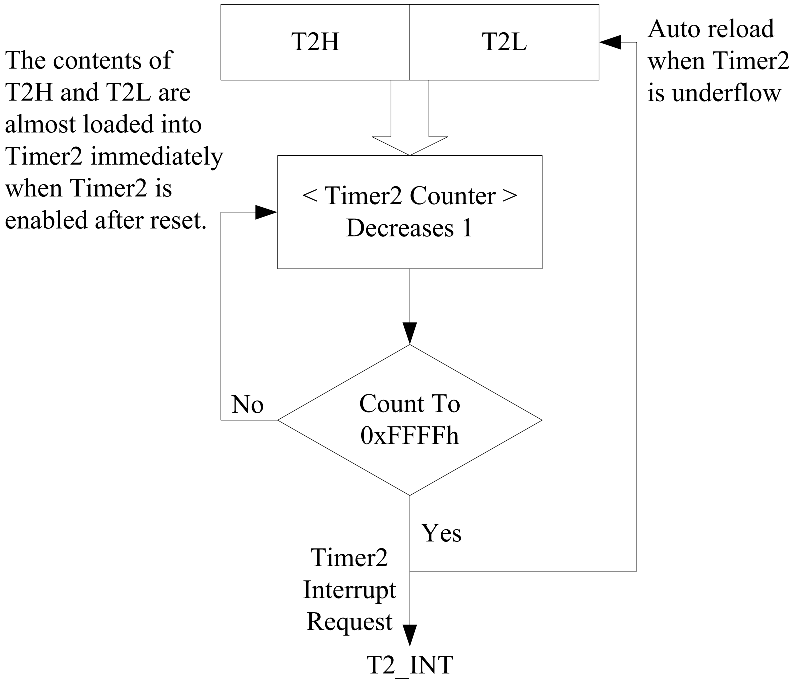
Timer2 is similar in structure to Timer1 except that clock source of Timer2 comes from the system clock "Fsys"/1.5. The system clock "Fsys" varies depending on the operation modes of the MCU.

The Timer2 consists of two 8-bit write-only preload registers T2H and T2L and 16-bit down counter. If Timer2 is enabled, counter will decrement by one with each incoming clock pulse. Timer2 interrupt will be generated when the counter underflows - counts down to FFFFH. And it will be automatically reloaded with the value of T2H and T2L.

Please note that the interrupt signal is generated when counter counts from 0000H to FFFFH. If the value of counter is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this time, the interrupt will be generated immediately and value of T2H and T2L will be loaded since the counter counts to FFFFH. So the T2H and T2L value should be set before enabling Timer2.

The Timer2 related control registers are list as below:

Register	Address	Field	Bit Position	Mode	Description
IER	0x02	TC2_IER	1	R/W	0: TC2 interrupt is disabled. (default) 1: TC2 interrupt is enabled.
T2L	0x05	T2L[7:0]	7~0	W	Low byte of TC2 pre-load value
T2H	0x06	T2H[7:0]	7~0	W	High byte of TC2 pre-load value
OP1	0x09	TC2E	3	R/W	0: TC2 is disabled. (default) 1: TC2 is enabled.



15. Time Base

The TB timer is used to generate time-out interrupt at fixed period. The time-out frequency of TB is determined by dividing slow clock with a factor selected in OP2[3..0]. TBE (Time Base Enable) bit controls enable or disable of the circuit.

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	-	-	0	-	-	-	-

TBE	Function
0	Disable Time Base
1	Enable Time Base

For example, if the slow clock is 32768 Hz, then the interrupt frequency is as shown in following table.

TBS[3..0]	Interrupt Frequency
0000	16.384 KHz
0001	8.192 KHz
0010	4.096 KHz
0011	2.048 KHz
0100	1.024 KHz
0101	512 Hz
0110	256 Hz
0111	128 Hz
1000	64 Hz
1001	32 Hz
1010	16 Hz
1011	8 Hz
1100	4 Hz
1101	2 Hz
1110	1 Hz
1111	0.5 Hz

16. Watch Dog Timer

Watch Dog Timer (WDT) is designed to reset system automatically and prevents system dead lock caused by abnormal hardware activities or program execution. The WDT needs to be enabled in Mask Option.

MO_WDTE	Function
0	WDT disable
1	WDT enable

Using the WDT function, the “CLRWDT” instruction needs to be executed in every possible program path when the program runs normally in order to clears the WDT counter before it overflows, so that the program can operate normally. When abnormal conditions happen to cause the MCU to divert from normal path, the WDT counter will not be cleared and reset signal will be generated to reset the system.

The WDT clock source is the same as TC1 (Timer1 clock), and the WDT reset signal is generated when the counter had counted 32768 clock. The WDT can function in Normal, Slow and Idle Mode. However, WDT will not function during Sleep Mode (as the TC1 clock has stopped).

17. Voice Output

There are 7 or 8 bits DAC/PWM voice output available for user. The 7 bits DAC/PWM output format and configuration are the same as the previous IC of HE80004H series. The 8 bits DAC/PWM format and configuration are new designed and controlled by the VOC and PWMC registers. The selection of 7/8 bits DAC/PWM output is by mask option **MO_8BVOC.**

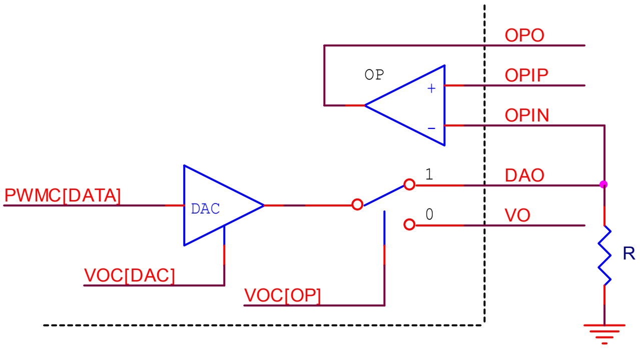
MO_8BVOC	Function
0	7-bit DAC/PWM output
1	8-bit DAC/PWM output

8-Bit DAC/PWM Output:

The Digital-to-Analog converter converts the 8-bit unsigned speech data which is written into PWMC data register to proportional current output.

PWMC	address	Reset	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Field	0x0E	--	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

There are two output paths for the DAC. Either VO or DAO can be selected as output port of DAC by VOC register when it is enabled. The VO output is primarily intended for speech generation, although it is not necessary so, while the DAO output path can be used in conjunction with built-in OP comparator to function as an Analog-to-Digital Converter as required in applications such as speech recording, speech recognition or sensor interfaces.

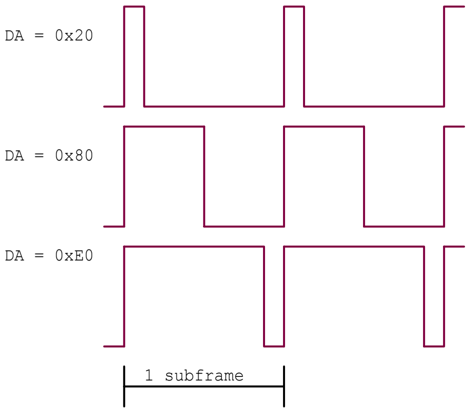


The DAC is enabled by DAC bit of VOC register. When DAC is enabled, the DAC output path can be selected to output to DAO or VO pin by OP bit of VOC register.

VOC	address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	0x13	-	PWM O/P driver			PWME	PWM	DAC	OP
Reset			0	0	0	0	0	0	0

Bit	Name	Value	Function description
VOC[3]	PWME	1	PWM Output Driver Enable
		0	PWM Output Driver Disable
VOC[2]	PWM	1	PWM Module Enable
		0	PWM Module Disable
VOC[1]	DAC	1	Digital-to-Analog Converter Enable
		0	Digital-to-Analog Converter Disable
VOC[0]	OP	1	DAC output to DAO pin
		0	DAC output to VO pin

The pulse-width modulator (PWM) converts 8-bit unsigned speech data which is written into PWMC data register to proportional duty cycle of PWM output. PWM module shares the same digital input register PWMC with Digit-to-Analog Converter. So PWM and DA output can exist at the same time. When PWM circuit is enabled, it generates signal with duty ratio in proportion to the value of PWMC register.



The PWM bit of VOC controls the enable/disable of the PWM circuit and output driver. When PWM bit of VOC is ‘0’, PWME bit and output drivers are both cleared. To use PWM as voice output, PWM bit has to be set to ‘1’ first, then set PWME bit and enable output driver by setting the driver number. If PWM bit is disabled and enabled again, the setting for driver and PWME bit will be clear.

The Fast Clock is gated through PWME bit of VOC register to provide the clock source of PWM circuit when it is enabled. As PWM needs higher frequency to operate, it cannot generate correct PWM signal in Slow clock only mode.

When the program enters into sleep mode or idle mode, it will automatically turn off all voice outputs by clearing VOC[6:0] to ”0000000”. To activate voice output again when returning to normal mode, the VOC register needs to be set again.

The PWM output volume can be adjusted by command register VOC[6..4]. The bit 6 and 5 control 2 time driver, while bit 4 controls 1 time driver, thus it has 5 levels of driver output. By turning on/off the internal drivers, the sound level of PWM output can be turned up and down. Please note that this adjustment apply only to PWM, but not DA output.

PWM output driver selection

VOC[6..4]	Number of Driver
000	off
001	1
010	2
011	3
100	2
101	3
110	4
111	5

7-Bit DAC/PWM Output:

The 7-bit DAC/PWM voice generator is another scenario and the definitions of PWMC and VOC registers are different from the 8-bit DAC/PWM format. These registers are different from the 8-bit architecture and described as following.

The 7-bit voice output is controlled by PWMC and VOC register, and the PWMC is a command/data register which is determined by PWMC[7] bit. The **VOC** is a three bit voice control register in the 7-bit mode.

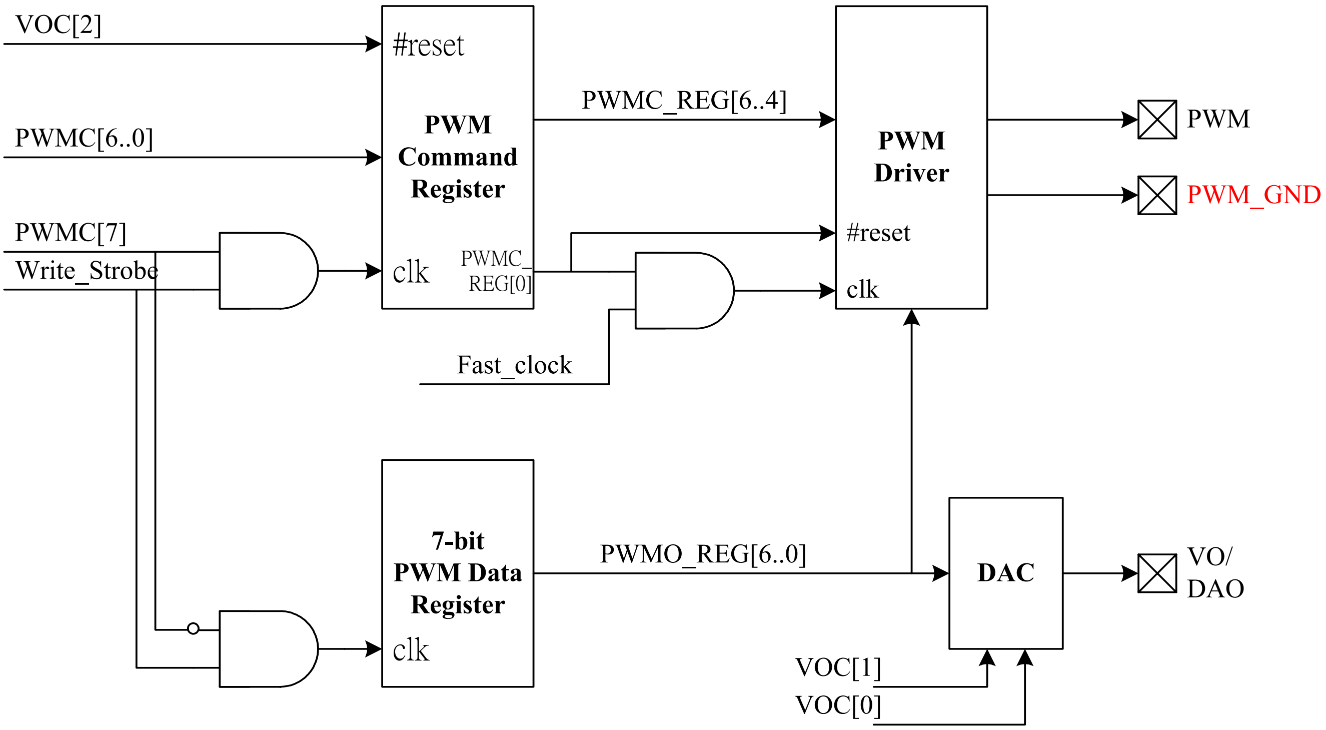
VOC	address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	0x13	-	-	-	-	-	PWM	DAC	OP
Reset	-	-	-	-	-	-	0	0	0

PWM: ‘1’ PWM output enabled; ‘0’ PWM output disabled.
DAC: ‘1’ DAC enabled; ‘0’ DAC disabled.
OP: ‘1’ DAC uses DAO pin as output pin; ‘0’ DAC uses VO pin as output pin.

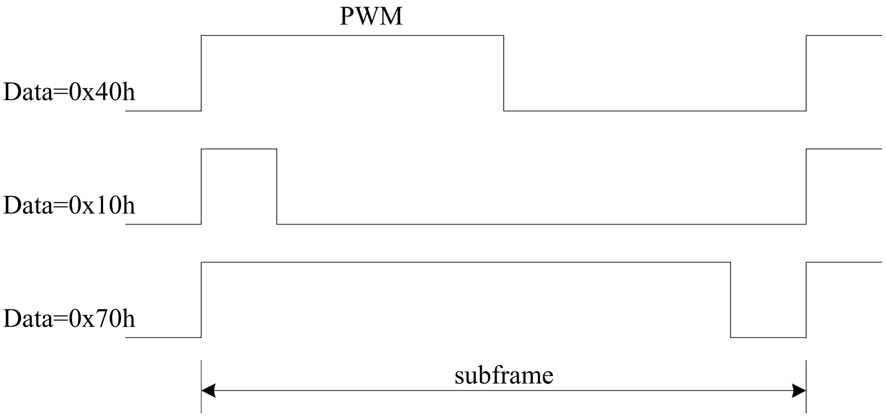
PWMC register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA & PWM Data	0	DA and PWM output value						
Control	1	PWM O/P driver			Reserved			PWME

When users write data into the PWMC register, the PWMC[7] bit will determines the data written into PWM command register or 7-bit data register and the data register is also sent to the DA converter shown as the below diagram. The definitions of “PWME” bit and “PWM O/P driver” bits are the same as VOC register definition of 8-bit output mode.

7-bit Voice Output Architecture

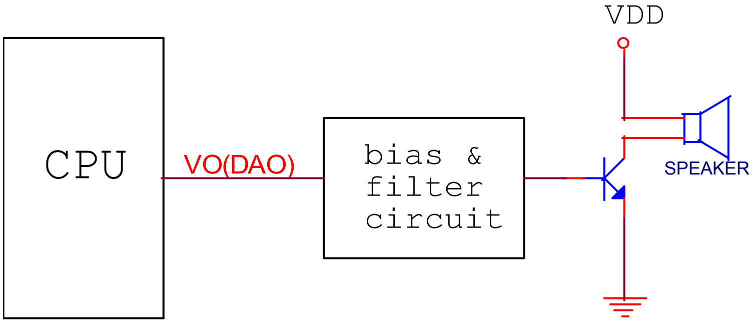


The fast clock is used to provide as PWM driver time base, and user shall set the PWMC[7]='1' and VOC[2]='1' to enable the PWM output. When the system enters into sleep or idle mode, it will automatically turn off the voice device by clearing VOC[2:0] to "000". In order to activate voice output again when the system returns and enter into normal mode, the related bits of VOC register need to be set again.



When the DAC is used as sound generator, the bias & filter circuit is used for bias voltage setting and waveform filter regulation and the DAC is output to the VO (Voice Output) pin and please see application notes for detailed calculation example and application. The driving capability of DAC is shown below.

	Condition	Min.	Typ.	Max.	Unit
VO/DAO	V_{DD}=3V;VO=0~2V;Data=7Fh	2.5	3		mA


VDD
CPU
VO(DAO)
bias &
filter
circuit
SPEAKER

18. Low Voltage Detection/Reset

The low voltage detection is used to detect low battery or low power condition. There are 4 options on the detection level selectable by mask option MO_DLVL. The low voltage detection circuit can be turned off by clearing LVDE bit, and the status of supply power can be read out at bit LVDO of LVDC register (extension register 0x17h).

MO_DLVL	**Detection voltage**
00	2.4 volts
01	2.6 volts
10	2.8 volts
11	3.0 volts

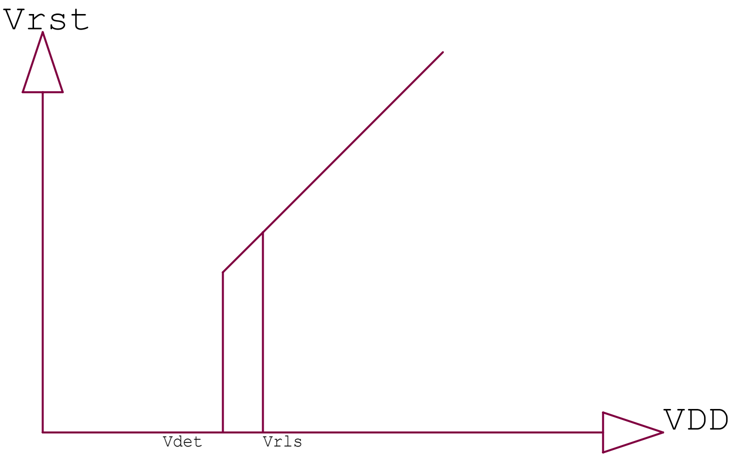
LVDC	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Field	LVDO	-	-	-	-	-	-	LVDE
Mode	R	-	-	-	-	-	-	W
Reset	-	-	-	-	-	-	-	0

LVDO: ‘0’ → Battery level low; ‘1’ → Battery level high
LVDE: ‘0’ → Disable voltage Detection, ‘1’ → Enable voltage Detection

Low voltage reset circuit prevents the CPU from operating below its physical limit. When the supply voltage drops below V_{DET} (2.2Volt), the CPU will be held in reset state until the supply voltage rises to V_{RLS}. Then CPU will be released from reset state. V_{RLS} will be higher than V_{DET} by 5% to provide hysteresis and prevent CPU from bouncing back and forth between reset and operating state. The low voltage reset function can be enabled or disabled by mask option MO_LVRE.

MO_LVRE	**Function**
0	Disable LVR
1	Enable LVR

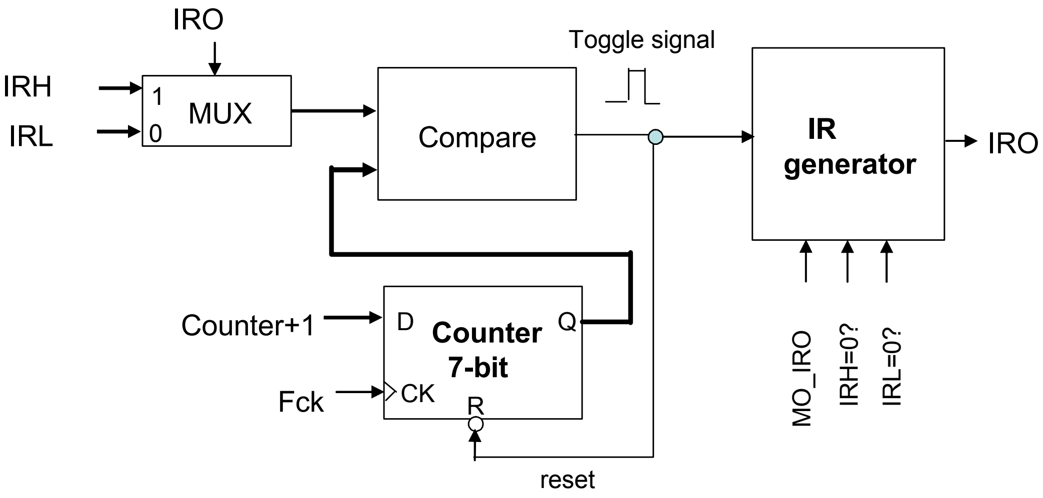
The voltage detection circuit is temperature compensated to prevent the detection voltage from drifting with temperature variation.



19. Infrared output

To achieve an IR output with programmable frequency and duty cycle, two 7-bit registers are employed here. The IRH register represents the period (on FCK clock number) of output high, while IRL register represents the period of output low. With this mechanism, the output IR frequency is equal to FCK/(IRH+IRL), and the high duty cycle ratio is equal to IRH/(IRH+IRL). To make the IRO as output pin alone, either IRH or IRL can be set as 0. When IRH is 0, the IRO output is a DC low. On the contrary, if IRL is 0, the output is a DC high. Special care in hardware implementation is also taken according to the MO_IRO (mask option to determine the default state of the IRO) to avoid glitch when PWM output is disabled.

IRO



To avoid unexpected IR output, users should firstly load the content of IRH and IRL before turn on IR by set IROE bits to '1'.

The access of all the registers of IR is through the extension register. They are list as below:

Extension register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Mode	Reset value
0x15h	IRL	IROE	IR PWM LOW DURATION							R/W	0xxx xxxx
0x16h	IRH	-	IR PWM HIGH DURATION							W	-xxx xxxx

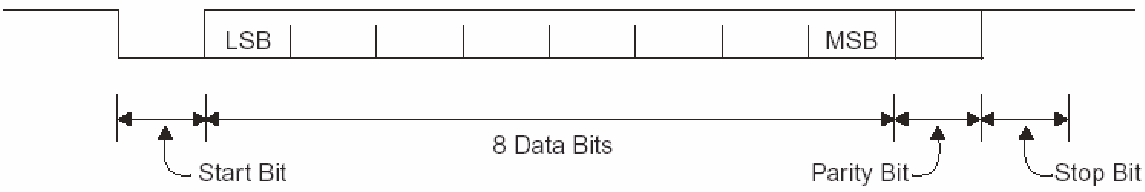
IROE: '0' → IR is disabled (default); '1' → IR is enabled.

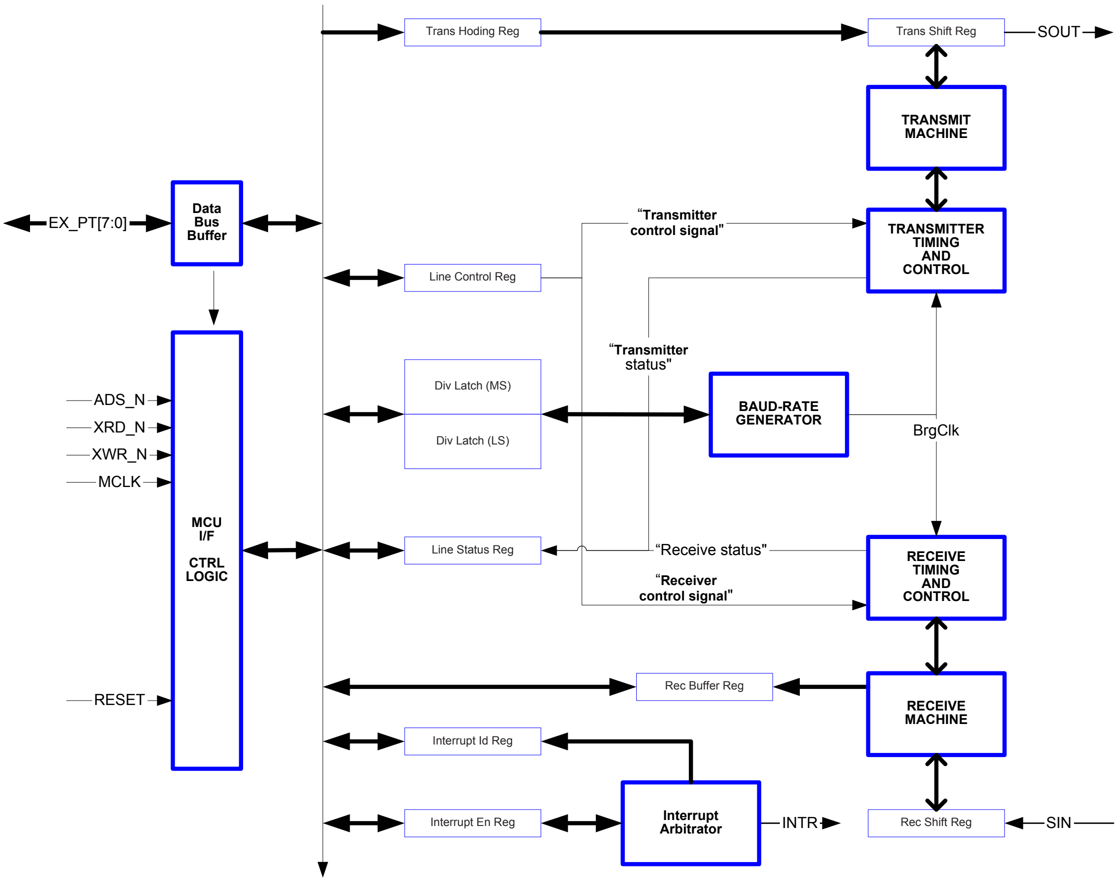
20. Universal Asynchronous Receiver/Transmitter

The UART (Universal Asynchronous Receiver/Transmitter) interface provides serial communication capabilities with other devices such as PC. Features include:

- ✓ Full duplex Asynchronous communication
- ✓ Programmable transmission rate with internal baud rate generator with selectable bit rates
- ✓ Double buffered Transmitter and Receiver.
- ✓ Programmable Data length (from 5 to 8 bits)
- ✓ Programmable stop bits (1, 1.5 or 2-stop bit) generation and detection
- ✓ Programmable parity type (odd, even or no parity)
- ✓ Error (parity, overrun and framing errors) detection
- ✓ Fully prioritized interrupt system control
- ✓ Line break generation and detection.

Example – 8-bit UART Frame Format: (1 Start Bit, 8 Data Bits, 1 Parity Bit, 1 Stop Bit)





20.1. Interface Registers

Addressable extension register used to interface with MCU

Address	Name	Function								Mode	RESET
00H	RBR	UART RECEIVER BUFFER								R	0000 0000
01H	THR	UART TRANSMITTER HOLDING REGISTER								R/W	0000 0000
02H	IEIR	0	RLSI	THRI	RBRI	0	ID2	ID1	ID0	R/W	0000 0000
03H	LCR	BRGE	SB	SP	EPS	PEN	STB	WLS1	WLS0	R/W	0000 0000
04H	BRL	UART LSB of Baud Rate Register								R/W	0000 0000
05H	BRH	UART MSB of Baud Rate Register								R/W	0000 0000
06H	LSR	0	TEMT	THRE	BI	FE	PE	OE	DR	R	0110 0000

IEIR: Interrupt enable/disable identification register.

LCR: Line control register.

LSR: Line status register.

20.2.Baud Rate Configuration Register

The BRH and BRL registers hold the upper and lower bytes of 16 bit baud rate divisor and which are readable/writable. The baud rate of UART is calculated as following:

$$BAUD\_RATE\_DIVISOR = \frac{FCK}{16 * BAUD\_RATE}, (FCK\text{: fast clock of system})$$

The contents of BRH and BRL are calculated by the following two formulas:

$$BRL = BAUD\_RATE\_DIVISOR \ \% \ 256$$

$$BRH = (BAUD\_RATE\_DIVISOR - BRL) / 256$$

The “%” symbol is the modulus operation (reminder of division). For example, if the FCK is 1.8432M Hz and the desired baud rate is 2400 baud, then

$$BAUD\_RATE\_DIVISOR = \frac{1843200}{16 * 2400} = 48$$

The BRL register shall be set to 0x30 and BRH set to 0x00. The setting of baud_rate_divisor is not updated until the BRH register is written. Thus user is strongly recommended to write BRL first, then BRH.

In order to obtain good communication quality, the same time base shall be used in the both sides of transmitting and receiving. The following table shows the most common baud rate setting used in the PC UART communication.

BRL and BRH: Baud Rate Control Registers

FCK(Hz)	Baud Rate (bps)	Divisor	BRL	BRH
1.8432M	50	2304	0x00	0x09
1.8432M	300	384	0x80	0x01
1.8432M	1200	96	0x60	0x00
1.8432M	2400	48	0x30	0x00
1.8432M	4800	24	0x18	0x00
1.8432M	9600	12	0x0C	0x00
1.8432M	19200	6	0x06	0x00
1.8432M	38400	3	0x03	0x00
1.8432M	57600	2	0x02	0x00
1.8432M	115200	1	0x01	0x00

20.3. Interrupt Enable, Identification Register

This high nibble of IEIR register allows to enable/disable interrupt generation by the UART, the low nibble ID[2..0] of IEIR register is used to identify the source of interrupts.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
0x02h	**IEIR**	0	RLSI	THRI	RBRI	0	ID2	ID1	ID0	“0000_0000”
		-	R/W	R/W	R/W	-	R	R	R	

RBRI: Receiver Buffer Register Interrupt (1 = Enable, 0 = Disable), related to ID[1] bit.
THRI: Transmitter Hold Register Interrupt (1 = Enable, 0 = Disable), related to ID[0] bit.
RLSI: Receiver Line Status Interrupt (1 = Enable, 0 = Disable), related to ID[2] bit.

The following table shows the related interrupt sources, user can read the ID[2:0] to retrieve what is the current highest priority of pending interrupts. The ID[2:0] bits will be cleared when user read the related registers. For example, when an interrupt happened and the content of ID[2:0] is "101", this means that LRS error and THR empty happen; user can read the LSR register to clear the ID[2] bit and ID[0] bit can also be cleared by reading the IEIR or writing data into THR register.

Level	IEIR Bit [2:0]	Source of Interrupt	Interrupt Reset Control
None	0 0 0	None	None
Highest	1 0 0	LSR error flags (OE/PE/FE/BI)	Reading LSR register to clear ID[2]
Second	0 1 0	LSR receiver data ready flag (DR)	Reading RBR register to clear ID[1]
Third	0 0 1	LSR flag THR Empty (THRE)	Reading IEIR register or Writing THR register to clear ID[0]

20.4.Line Control Register

The line control register allows user to configure the asynchronous data transfer format and set the UART function. Reading from the register is allowed to check the current settings of the communication.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRGE	SB	SP	EPS	PEN	STB	WLS1	WLS0

Name	Description
WLS[1..0]	**Word Length Select** "00": word length = 5 "01": word length = 6 "10": word length = 7 "11": word length = 8
STB	**Stop Bit Length** '0': Stop bit length = 1 '1': Stop bit length = 1.5 when WLS[1..0]="00", else Stop bit length = 2
[SP, EPS, PEN]	**Parity Selection** "xx0": No Parity "001": odd Parity "011": even Parity "101": Stick Parity 1 "111": Stick parity 0
SB	**Set Break** When enable the break control bit causes a break condition to be transmitted (SOUT is forced to a logic 0 state). This condition exists until disabled by resetting this bit to logic 0. '0': disable break; '1': enable break
BRGE	**Baud Rate Generator** '0': disable baud rate clock generator '1': enable baud rate clock generator

20.5.Line Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TEMT	THRE	BI	FE	PE	OE	DR

Name	Description
DR	**Receiver Data Ready** DR indicates status of RBR. It will be set to logic 1 when RBR data is valid and will be reset to logic 0 when RBR is empty. When line errors (OE/PE/FE/BI) happen, DR will also be set to logic 1 and RBR will be updated to reflect the Data bits portion of the frame.
OE	**Overrun Error** This bit will be set when the next character is transferred into RBR before the previous RBR data is read by the CPU. Even though DR will still be 1 when OE is set to logic 1, the previous frame data stored in RBR which is not read by the CPU is trashed and can‘t be recovered.
PE	**Parity Error** This bit will be set to logic 1 only when the Parity is enabled and the Parity bit is not at the logic state it should be. For Even Parity, the Parity bit should be 1 if an odd number of 1s in the Data bits is received; otherwise, the Parity bit should be 0. For Odd Parity, the Parity bit should be 1 if an even number of 1s in the Data bits is received; otherwise, the Parity bit should be 0. For Stick Parity '1', the Parity bit should be 1. For Stick Parity '0', the Parity bit should be 0.
FE	**Framing Error** FE will be reset to logic 0 whenever SIN is sampled high at the center of the first Stop bit, regardless of how many Stop bits the UART is configured to.
BI	**Break Interrupt** BI will be set to logic 1 whenever SIN is low for longer than the whole frame (the time of Start bit + Data bits + Parity bit + Stop bits), not at the SIN rising edge where Break is negated. If SIN is still low after BI is reset to logic 0 by reading LSR, BI will not be set to logic 1 again. Since Break is also a Framing error, FE will also be set to 1 when BI is set.
THRE	**THR Empty** THRE will be set to logic 1 whenever THR is empty which indicates that the transmitter is ready to accept new data to transmit.
TEMT	**Both THR and TSR are Empty** This bit will be set to logic 1 when THRE is set to 1 and the last Data bit in the TSR is shifted out through SOUT.

* The four error flags (OE, PE, FE and BI) of LSR will be reset to logic 0 after a LSR read.

Since the SIN and SOUT of UART pins are shared with PRTD[1..0], users can use the mask option to enable the UART function and select PRTD[1..0] function.

MO_UART	0	PRTD[1:0] = I/O Pin
	1	PRTD[1:0] = UART Pin

21. Extension Register Access

The extension registers can be accessed through the extension port control registers EXTAS and EXTDA. User can read/write the extension register easily and the control timing is generated by hardware automatically. The following code shows how to access the extension registers.

Read Extension Register:

```
LDA     #0x00h   ; load #0x00h data to A Register
STA     EXTAS    ; store A register data to the extension port address register.
LDA     EXTDA    ; store the extension register (0x00h) data to A Register.
```

Write Extension Register:

```
LDA     #0x03h   ; load #0x03h data to A Register
STA     EXTAS    ; store A register data to the extension port address register.
LDA     #0x18h   ; load #0x18h data to A Register
STA     EXTDA    ; store A register data to the extension port data register.
```

22. Summary of Registers and Mask Options

All the registers and mask options used in this chip are listed in the following tables.

Address	NAME	Field								Mode	RESET
00H	TPL	Table Pointer Low Byte								R/W	xxxx xxxx
01H	TPH	Table Pointer High Byte								R/W	xxxx xxxx
02H	IER	-	-	INT_EX	TB	INT1	T1	T2	INT2	R/W	--00 0000
03H	T1L	Timer 1 Low Byte								W	xxxx xxxx
04H	T1H	Timer 1 High Byte								W	xxxx xxxx
05H	T2L	Timer 2 Low Byte								W	xxxx xxxx
06H	T2H	Timer 2 High Byte								W	xxxx xxxx
07H	SP	Stack Pointer								R/W	1111 1111
08H	DP	RAM Pointer								R/W	xxxx xxxx
09H	OP1	DRDY	STOP	SLOW	INTE	T2E	T1E	Z	C	R/W	1000 00xx
0AH	OP2	IDLE	PNWK	TCWK	TBE	TBS[3..0]				R/W	0xx0 ----
0BH	PP	RAM Page Pointer								R/W	0000 0000
0CH	PRTC	PRTC[7]	PRTC[6]	PRTC[5]	PRTC[4]	**Reserved**				R/W	1111 ----
0DH	PRTD	I/O Port D								R/W	1111 1111
0EH	PWMC	PWM Data								W	0000 0000
0FH	LCDC	-	-	CLR_GP	Reserved			BLANK	LCDE	W	xx1x xx10
13H	VOC	-	PWM O/P driver			PWME	PWM	DAC	OP	R/W	x000 0000
14H	PRT14	I/O Port 14								R/W	1111 1111
15H	PRT15	I/O Port 15								R/W	1111 1111
16H	TPP	ROM Table Page Pointer								R/W	0000 0000
17H	PRT17	I/O Port 17								R/W	1111 1111
20H	EXTAS	Extension Port Address Register								R/W	xxxx xxxx
21H	EXTDA	Extension Port Data Register								R/W	xxxx xxxx
22H	KEYR0	R	RI[1]	RI[0]	CI[4]	CI[3]	CI[2]	CI[1]	CI[0]	R/W	xxxx xxxx
23H	KEYR1	0	RI[1]	RI[0]	CI[4]	CI[3]	CI[2]	CI[1]	CI[0]	R/W	xxxx xxxx

Address	NAME	Field								Mode	RESET
24H	LCDPS	-	-	-	-	-	POWDN	PAcc	BUFE	R/W	---- -100
2BH	GRAY16	32 to 16 Gray Level Palette Register								W	
	GRAY0	Gray Level 0 Mapping Register								W	xxx0 0000
	GRAY1	Gray Level 1 Mapping Register								W	xxx0 0010
	GRAY2	Gray Level 2 Mapping Register								W	xxx0 0100
	GRAY3	Gray Level 3 Mapping Register								W	xxx0 0110
	GRAY4	Gray Level 4 Mapping Register								W	xxx0 1000
	GRAY5	Gray Level 5 Mapping Register								W	xxx0 1010
	GRAY6	Gray Level 6 Mapping Register								W	xxx0 1100
	GRAY7	Gray Level 7 Mapping Register								W	xxx0 1110
	GRAY8	Gray Level 8 Mapping Register								W	xxx1 0000
	GRAY9	Gray Level 9 Mapping Register								W	xxx1 0010
	GRAYA	Gray Level A Mapping Register								W	xxx1 0100
	GRAYB	Gray Level B Mapping Register								W	xxx1 0110
	GRAYC	Gray Level C Mapping Register								W	xxx1 1000
	GRAYD	Gray Level D Mapping Register								W	xxx1 1010
	GRAYE	Gray Level E Mapping Register								W	xxx1 1100
	GRAYF	Gray Level F Mapping Register								W	xxx1 1110
2CH	PSA1	Physical Page Address Mapping Register for Logical Page 1								R/W	0000 0001
2DH	PSA2	Physical Page Address Mapping Register for Logical Page 2								R/W	0000 0010
2EH	PSA3	Physical Page Address Mapping Register for Logical Page 3								R/W	0000 0011
30H	AC	Download bus address counter								R/W	
	ACL	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	R/W	0000 0000
	ACH	AC15	AC14	AC13	AC12	AC11	AC10	AC9	AC8	R/W	0000 0000
	ACP	AC23	AC22	AC21	AC20	AC19	AC18	AC17	AC16	R/W	0000 0000
31H	EXMD	Download Bus Data Port								R/W	xxxx xxxx
32H	EXMC	-	-	-	-	-	WR	RD	DNLD	R/W	xxxx x011

Extension registers:

Address	Name	Function								Mode	RESET
00H	RBR	UART Receiver Buffer								R	0000 0000
01H	THR	UART Transmitter Holding Register								R/W	0000 0000
02H	IEIR	0	RLSI	THRI	RBRI	0	ID2	ID1	ID0	R/W	0000 0000
03H	LCR	BRGE	SB	SP	EPS	PEN	STB	WLS1	WLS0	R/W	0000 0000
04H	BRL	UART LSB of Baud Rate Register								R/W	0000 0000
05H	BRH	UART MSB of Baud Rate Register								R/W	0000 0000
06H	LSR	0	TEMT	THRE	BI	FE	PE	OE	DR	R	0110 0000
15H	IRL	IROE	IR PWM Low Duration							R/W	0xxx xxxx
16H	IRH	-	IR PWM High Duration							W	-xxx xxxx
17H	LDVC	LVDO	-	-	-	-	-	-	LVDE	R/W	x--- ---0

Mask Options:

NAME	Value	Description
MO_LVRE	0	Low Voltage Reset Disable
	1	Low Voltage Reset Enable
MO_FXTAL	0	R/C Oscillator Used for Fast Clock
	1	X'tal Oscillator Used for Fast Clock
MO_SXTAL	0	R/C Oscillator Used for Slow Clock
	1	X'tal Oscillator Used for Slow Clock
MO_FCK/SCKN	00	Slow Clock Only
	01	illegal

NAME	Value	Description
	10	Dual Clock
	11	Fast Clock Only
MO_WDTE	0	WDT Disable
	1	WDT Enable
MO_CPP[7:4]	0	Open-drain Output
	1	Push-pull Output
MO_DPP[7:0]	0	Open-drain Output
	1	Push-pull Output
MO_14PP[7:0]	0	Open-drain Output
	1	Push-pull Output
MO_15PP[7:0]	0	Open-drain Output
	1	Push-pull Output
MO_17PP[7:0]	0	Open-drain Output
	1	Push-pull Output
MO_LIO14[7:0]	0	PRT14 used as IO pin
	1	PRT14 used as LCD pin
MO_LIO15[7:0]	0	PRT15 used as IO pin
	1	PRT15 used as LCD pin
MO_LIO17[7:0]	0	PRT17 used as IO pin
	1	PRT17 used as LCD pin
MO_COM[1:0]	00	LCD Configuration = 32COM x 128SEG
	01	LCD Configuration = 48COM x 112SEG
	10	LCD Configuration = 64COM x 96SEG
	11	LCD Configuration = 80COM x 80SEG
MO_LBSR[1:0]	00	LCD Bias= 1/7
	01	LCD Bias= 1/8
	10	LCD Bias= 1/9
	11	LCD Bias= 1/10
MO_TC[1:0]	00	Temperature Coefficient of Regulator Voltage = -0.00 %/℃
	01	Temperature Coefficient of Regulator Voltage = -0.16 %/℃
	10	Temperature Coefficient of Regulator Voltage = -0.22 %/℃
	11	Temperature Coefficient of Regulator Voltage = -0.33 %/℃
MO_LOAD[1:0]	00	LCD driving current= "Low"
	01	LCD driving current= "Medium"
	10	LCD driving current= "Medium High"
	11	LCD driving current= "High"
MO_LCDKEY	0	LCD SGKY[43:24] Used as SEG only
	1	LCD SGKY[43:24] Used as SEG/KEY_SCAN
MO_SNCK[1:0]	00	Scan Pulse Width = 0.5 SCK
	01	Scan Pulse Width = 1.0 SCK
	10	Scan Pulse Width = 1.5 SCK
	11	Scan Pulse Width = 2.0 SCK
MO_SCDRV[1:0]	00	Strength of Key Scan = Weakest
	01	Strength of Key Scan = Weak
	10	Strength of Key Scan = Strong
	11	Strength of Key Scan = Strongest
MO_RCAP[2:0]	000	Capacitor Selection: C=2P => 4M Hz(R=30k)

NAME	**Value**	**Description**
	001	Capacitor Selection: C=4P => 4M Hz(R=17k)
	010	Capacitor Selection: C=7P => 4M Hz(R=11k)
	011	Capacitor Selection: C=14P => 1M Hz(R=25k)
	100	Capacitor Selection: C=20P => 1M Hz(R=18k)
	101	Capacitor Selection: C=40P => 500K Hz(R=19k)
	110	Capacitor Selection: C=50P => 500K Hz(R=15k)
	111	Capacitor Selection: C=60P => 500K Hz(R=13k)
MO_8BVOC	0	7 bit DAC/PWM Voice Output
	1	8 bit DAC/PWM Voice Output
MO_GRAY_MODE[1:0]	00	16 GRAY LEVEL
	01	4 GRAY LEVEL
	10	2 LEVEL(B/W)
	11	2 LEVEL(B/W)
MO_EXMEM	0	Internal MEMORY Used Only
	1	External MEMORY Used.
MO_DLVL[1:0]	00	Low Voltage Detection Level= 2.4V
	01	Low Voltage Detection Level= 2.6V
	10	Low Voltage Detection Level= 2.8V
	11	Low Voltage Detection Level= 3.0V
MO_IRO	0	Default State of the IRO After Reset: Low
	1	Default State of the IRO After Reset: High
MO_PMODE[1:0]	00	ROM MAP Configuration Option 0
	01	ROM MAP Configuration Option 1
	10	ROM MAP Configuration Option 2
	11	ROM MAP Configuration Option 3
MO_UART	0	PRTD[1:0] = I/O Pin
	1	PRTD[1:0] = UART Pin
MO_PUMPE	0	Disable Internal Charge-pump
	1	Enable Internal Charge-pump

23. Absolute Maximum Rating

Item	Symbol	Rating	Condition
Supply Voltage	V_{DD}	-0.5V ~ 4.0V	
Input Voltage	V_{IN}	-0.5V ~ V_{DD}+0.5V	
Output Voltage	V_O	-0.5V ~ V_{DD}+0.5V	
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

24. Recommended Operating Conditions

Item	Symbol	Rating	Condition
Supply Voltage	V_{DD}	2.4V ~ 3.6V	
Input Voltage	V_{IH}	0.9 V_{DD} ~ V_{DD}	
	V_{IL}	0.0V ~ 0.1V_{DD}	
Operating Frequency	$F_{MAX.}$	8M Hz	V_{DD} =3.0V
		6M Hz	V_{DD} =2.4V
Operating Temperature	T_{OP}	0°C ~ 70°C	
Storage Temperature	T_{ST}	-50°C ~ 100°C	

25. AC/DC Characteristics

Testing Condition : TEMP=25℃, VDD=3V±10%

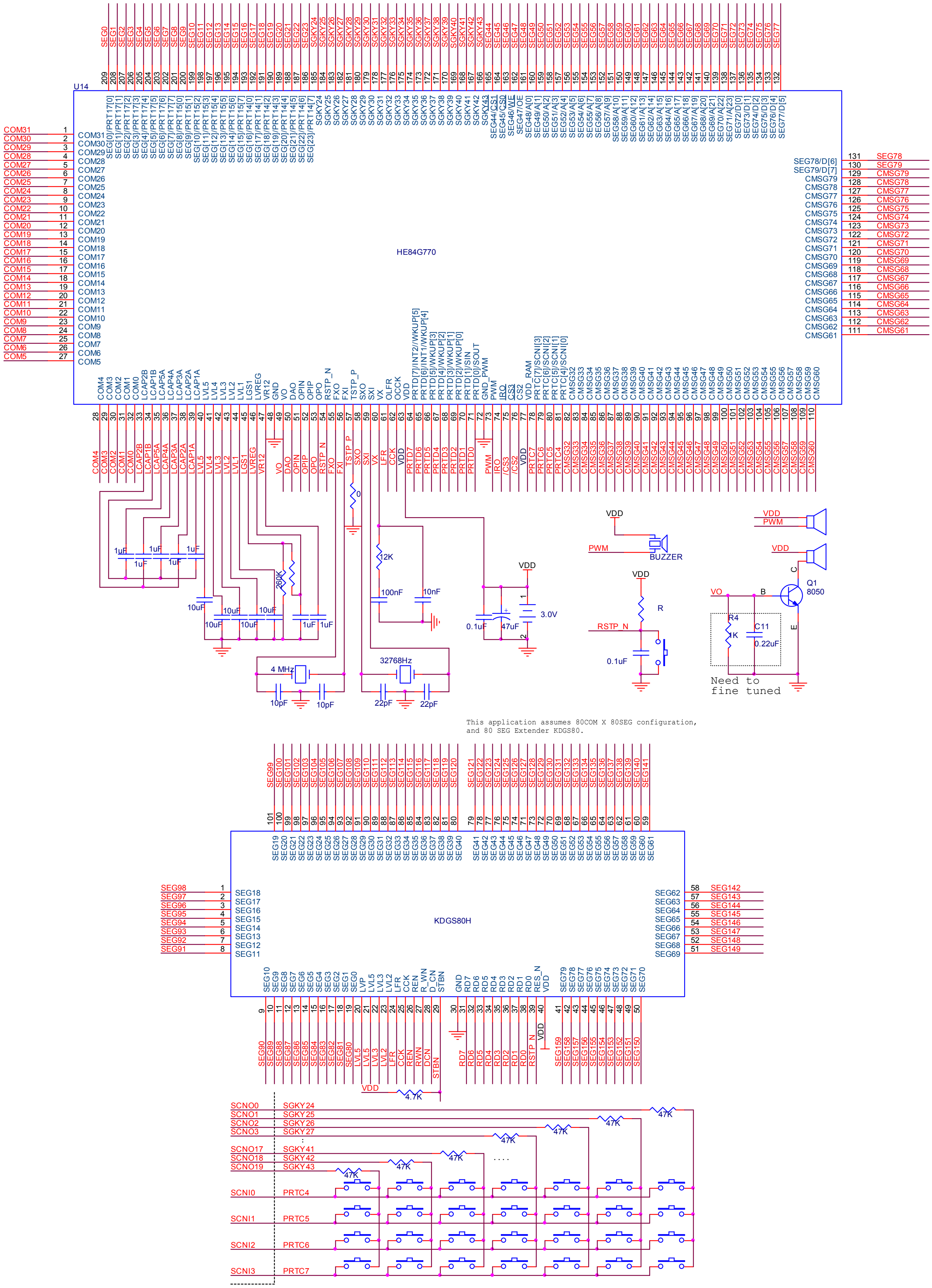
Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Power consumption						
NORMAL Mode Current	I_{FAST}		1	1.5	mA	2M external R/C fast clock
SLOW Mode Current	I_{SLOW}		15	25	µA	32768 Hz slow clock with LCD disabled
IDLE Mode Current	I_{IDLE}		10	20	µA	32768 Hz slow clock with LCD disabled
Sleep Mode Current	I_{SLEEP}			1	µA	LVR and LVD disable
Additional Current if LCD ON	I_{LCD}		200	220	µA	LV5=3×LVREG
			250	275		LV5=4×LVREG
			300	330		LV5=5×LVREG
I/O specification						
Input High Voltage	V_{IH}	0.8			V_{DD}	Input Pins
Input Low Voltage	V_{IL}			0.2	V_{DD}	Input Pins
Input Hysteresis Width	V_{HYS}		1/3		V_{DD}	I/O, RSTP_N Threshold = 2/3 VDD (Input from low to high), Threshold = 1/3 VDD (Input from high to low)
Output Source Current	I_{OH}	50			µA	Output drive high[*1], V_{OH}=2.0V
Output Sink Current	I_{OL1}	1.0			mA	Output drive low, V_{OL}=0.4V
Input Low Current	I_{IL1}		20		µA	RSTP_N, V_{IL} = GND, Pull high Internally
Input Low Current	I_{IL2}		100		µA	I/O, V_{IL}=GND, if pull high Internally by user
PWM and DAC						
PWM Output Current	I_{PWM}	10	14		mA	PWM[*2] With 32Ω Loading
		6	8		mA	With 64Ω Loading
		4	5		mA	With 100Ω Loading

DAC Output Current	I_{VO}	2.5	3		mA	VO, DAO@ V_{DD}=3V,VO=0~2V, Data =FF
Low voltage Reset						
LVR detection voltage	V_{DET}		2.2		Volts	
LVR release voltage	V_{RLS}		2.31		Volts	
IR Output Sink/Source Current	I_O		20		mA	V_{OL}=0.4V, V_{OH}=2.0V
LVR power consumption	I_{LVR}		10		µA	When LVR is enabled

Notes:

1. The “Output Source Current” specification is applicable only to the Push-Pull I/O type.
2. This Specification indicates only one PWM driving capability, and there are totally five built-in drivers, user can multiply the actual number of driver to get the total amount of current. (I_{PWM} x N; N=0, 1, 2, 3, 4, 5)

26. Application Circuit



This application assumes 80COM X 80SEG configuration, and 80 SEG Extender KDGS80.

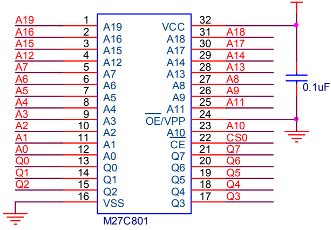
Note: Options for system configuration of LCD Display, Osc. and external memory.

COMXSEG	32X128	48X112	64X96	80X80
CMSG32	SEG127	COM32	COM32	COM32
CMSG33	SEG126	COM33	COM33	COM33
CMSG34	SEG125	COM34	COM34	COM34
CMSG35	SEG124	COM35	COM35	COM35
CMSG36	SEG123	COM36	COM36	COM36
CMSG37	SEG122	COM37	COM37	COM37
CMSG38	SEG121	COM38	COM38	COM38
CMSG39	SEG120	COM39	COM39	COM39
CMSG40	SEG119	COM40	COM40	COM40
CMSG41	SEG118	COM41	COM41	COM41
CMSG42	SEG117	COM42	COM42	COM42
CMSG43	SEG116	COM43	COM43	COM43
CMSG44	SEG115	COM44	COM44	COM44
CMSG45	SEG114	COM45	COM45	COM45
CMSG46	SEG113	COM46	COM46	COM46
CMSG47	SEG112	COM47	COM47	COM47
CMSG48	SEG111	SEG111	COM48	COM48
CMSG49	SEG110	SEG110	COM49	COM49
CMSG50	SEG109	SEG109	COM50	COM50
CMSG51	SEG108	SEG108	COM51	COM51
CMSG52	SEG107	SEG107	COM52	COM52
CMSG53	SEG106	SEG106	COM53	COM53
CMSG54	SEG105	SEG105	COM54	COM54
CMSG55	SEG104	SEG104	COM55	COM55
CMSG56	SEG103	SEG103	COM56	COM56
CMSG57	SEG102	SEG102	COM57	COM57
CMSG58	SEG101	SEG101	COM58	COM58
CMSG59	SEG100	SEG100	COM59	COM59
CMSG60	SEG99	SEG99	COM60	COM60
CMSG61	SEG98	SEG98	COM61	COM61
CMSG62	SEG97	SEG97	COM62	COM62
CMSG63	SEG96	SEG96	COM63	COM63
CMSG64	SEG95	SEG95	SEG95	COM64
CMSG65	SEG94	SEG94	SEG94	COM65
CMSG66	SEG93	SEG93	SEG93	COM66
CMSG67	SEG92	SEG92	SEG92	COM67
CMSG68	SEG91	SEG91	SEG91	COM68
CMSG69	SEG90	SEG90	SEG90	COM69
CMSG70	SEG89	SEG89	SEG89	COM70
CMSG71	SEG88	SEG88	SEG88	COM71
CMSG72	SEG87	SEG87	SEG87	COM72
CMSG73	SEG86	SEG86	SEG86	COM73
CMSG74	SEG85	SEG85	SEG85	COM74
CMSG75	SEG84	SEG84	SEG84	COM75
CMSG76	SEG83	SEG83	SEG83	COM76
CMSG77	SEG82	SEG82	SEG82	COM77
CMSG78	SEG81	SEG81	SEG81	COM78
CMSG79	SEG80	SEG80	SEG80	COM79

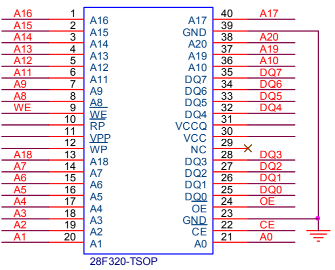
Ext. Bus Interface

SEG44	CS1	
SEG45	CS0	
SEG46	WE	
SEG47	OE	
SEG48	A0	
SEG49	A1	
SEG50	A2	
SEG51	A3	
SEG52	A4	
SEG53	A5	
SEG54	A6	
SEG55	A7	
SEG56	A8	
SEG57	A9	
SEG58	A10	
SEG59	A11	
SEG60	A12	
SEG61	A13	
SEG62	A14	
SEG63	A15	
SEG64	A16	
SEG65	A17	
SEG66	A18	
SEG67	A19	
SEG68	A20	
SEG69	A21	
SEG70	A22	
SEG71	A23	
SEG72	Q0	DQ0
SEG73	Q1	DQ1
SEG74	Q2	DQ2
SEG75	Q3	DQ3
SEG76	Q4	DQ4
SEG77	Q5	DQ5
SEG78	Q6	DQ6
SEG79	Q7	DQ7

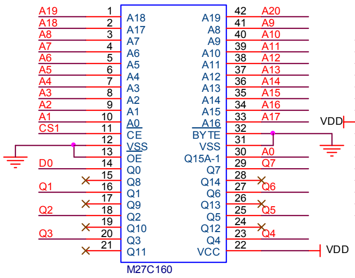
8 MB EPROM



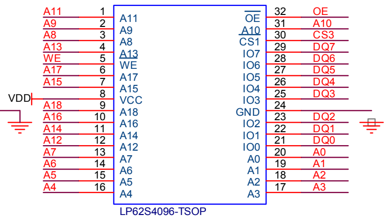
Intel NOR FLASH

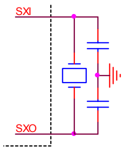


16 MB EPROM

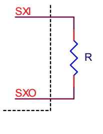


512KB x 8 SRAM

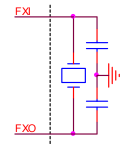




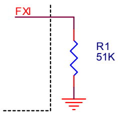
Crystal Osc.



RC Osc.

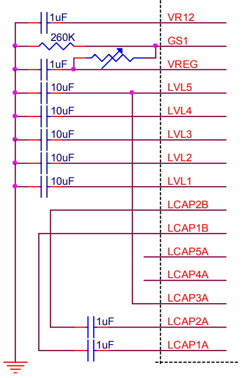


Crystal Osc.

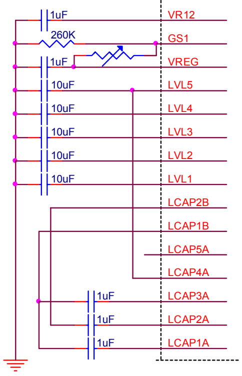


RC Osc.

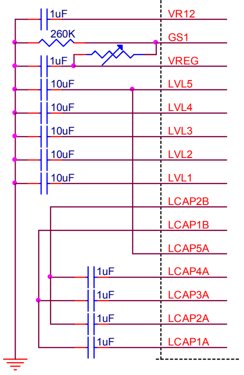
x3 charge pump config.



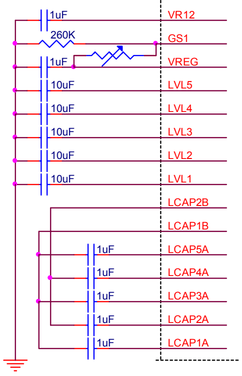
x4 charge pump config.



x5 charge pump config.



x6 charge pump config.



27. Important Note

1. Please note that ICE is different from IC which is your target chip. The ICE is a superset of HE80004H series IC, but each IC is a subset of ICE. Don't use any hardware resource that your target chip doesn't have them, especially RAM and register. KBIDS and compiler can't prevent user from using some hardware resources that don't exist in your target chip.
2. To access "Data ROM", users must update TPP first, TPH, and then TPL. Only follow this order, the pre-charge circuit of ROM will work correctly. The 5μs waiting is also necessary before LDV instruction is executed since Data ROM is a low speed ROM. User can't emulate this accessing process in ICE, so 5μs delay should be added by firmware.
3. Please bond the TSTP_P, RSTP_N and PRTD [7:0] with test points on PCB (can be soldered and probed) as you can, then some testing can be performed on PCB when it's necessary. The TSTP_P is suggested to connect to ground by a 0 ohm resistor. The following figure is an example (Testing point with through hole).
4. The LV5 must be lower than 12 Volt; otherwise the chip may be damaged.

28. Updated History

Version	Date	Revised History
V1.0	7/22/03	New Released
V1.1	10/31/03	1. Modify the 7-bit DAC block diagram 2. Change the product name from HE84G770H to HE84G770