



A. HE8P480 Introduction

HE8P480 is a member of 8-bit Micro-controller OTP series product developed by King Billion Electronics Ltd. This IC use OTP (One Time Programming) ROM, which can be written by the OTPWriter tool provided by King Billion. It provides fast verification, pilot-run product, and also provides more versatile application request to user. HE8P480 is a super-set of twenty-six IC body (**HE82006**、**HE82015**、**HE83006**、**HE83015**、**HE83120**、**HE83121**、**HE83122**、**HE83123**、**HE83124**、**HE83R123**、**HE83R125**、**HE83130**、**HE83131**、**HE83134**、**HE83135**、**HE83136**、**HE83137**、**HE83141**、**HE83R141**、**HE83142**、**HE83R142**、**HE83144**、**HE83145**、**HE83146**、**HE83147**、**HE83148**). If user wants to simulate any one of the twenty-six IC body, The OTPWriter tool will automatically restrict the hardware resource, such as ROM、RAM size, it is very convenient to use.

This IC has build-in LCD driver which have many configuration and can use Mask Option to select the configuration, such as **【1024 pixel LCD driver + 24 Bit I/O Port】**... **【128 pixel LCD driver + 56 Bit I/O Port】**. Build-in voltage regulator let LCD display stable when external battery voltage drop. The built-in OP operation amplifier can be used with (light、voice、temperature、humility) sensor and used as battery low detection. The 7-bit current-type D/A converter and PWM device provides the complete speech output mechanism.

The instruction set of HE8P160 are quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take 3 oscillator clocks (machine cycles). The processing power is enough to most of battery operation system.

B. HE8P480 Features

- Operation Voltage : 2.4V – 5.5V
- System Clock : DC ~ 8MHz @ 5.0V
DC ~ 4MHz @ 2.4V
- Internal ROM : 256K Bytes (64K Bytes Program ROM)
- Internal RAM : 4K Bytes.
- Dual Clock System : Normal (Fast) clock : 32.768K ~ 8MHz
- Slow clock : 32.768KHz
- Operation Mode : DUAL、FAST、SLOW、IDLE、SLEEP Mode.
- Build-in WDT (WATCH DOG TIMER) to prevent deadlock or abnormal condition..
- 16~32 bit Bi-directional I/O port. Mask Option can select PUSH-PULL or OPEN DRAIN output mode for each I/O pin. The I/O PRD [3:0] each has 5mA sink capability.
- Build-in **OP amplifier**. This OP operating range between **0 ~ (VDD-1)**, that is different from previous **OP comparator** operating range between 0.8~VDD, the user should notice this. Please set the operation range on **0.8 ~ (VDD-1)**, if user wants to design a circuit working both on HE8P480 and target IC.
- Build-in voltage regulator which provide LCD stable operating voltage.
- Contain a 7-bit Current-type D/A converter.



- Provides PWM output device. (Users can select with or without Rate Selection, connect with “VDD+PWM” or “PWMP+PWMN”)
- Two external interrupts and three internal timer interrupts.
- Two 16-bit timers and one Time Base timer.
- Instruction set : 32 instructions, 4 addressing mode. 9-bit DATA POINTER for RAM and 16-bit TABLE POINTER for ROM.



C. HE8P480 Body Mapping Table

BODY	PROM	DROM	RAM	FX	FRC	Fin	SX	SRC	CKmd	TC1	TC2	TB	PORT	PORT_LCD	COM	SEG	LDVD	LREG	PWM	PMD	VO	DAO	OP Amp	DTMF	WDT
HE82006	64kB	192kB	128B	Y	Y	-	-	-	F	Y	-	-	D	-	-	-	-	-	NEW	1	Y	-	-	-	Y
HE82015	64kB	64kB	128B	Y	Y	-	-	-	F	Y	-	-	D	-	-	-	-	-	NEW	1	Y	-	-	-	Y
HE83006	64kB	192kB	128B	Y	Y	Y	Y	Y	N	Y	Y	-	C,D,10	-	-	-	-	-	OLD	2	Y	Y	Y	-	Y
HE83015	64kB	64kB	128B	Y	Y	Y	Y	Y	N	Y	Y	-	C,D,10	-	-	-	-	-	OLD	2	Y	Y	Y	-	Y
HE83120	64kB	192kB	256B	Y	Y	Y	Y	Y	N	Y	Y	-	C[3:0],D	-	8	40	R5	-	OLD	2	Y	-	Y	-	Y
HE83121	64kB	64kB	256B	Y	Y	Y	Y	Y	N	Y	Y	-	C[3:0],D	-	8	40	R5	-	OLD	2	Y	-	Y	-	Y
HE83122	64kB	-	256B	Y	Y	Y	Y	Y	N	Y	Y	-	C[3:0],D	-	8	40	R5	-	OLD	2	Y	-	Y	-	Y
HR83123	64kB	-	256B	Y	Y	Y	Y	Y	N	Y	Y	-	D	-	8	40	R5	-	OLD	2	-	-	-	-	Y
HE83R123	64kB	-	256B	Y	Y	Y	Y	Y	N	Y	Y	-	D	11,14,15,17	8	40	C4	Y	OLD	2	-	-	-	-	Y
HE83124	64kB	192kB	256B	Y	Y	Y	Y	Y	N	Y	Y	-	D	-	8	40	R5	-	OLD	2	-	-	-	-	Y
HE83R125	64kB	64kB	256B	Y	Y	Y	Y	Y	N	Y	Y	-	D	11,14,15,17	8	40	C4	Y	OLD	2	-	-	-	-	Y
HE83130	64kB	-	256B	Y	Y	Y	Y	Y	N	Y	Y	-	C[3:0],D	-	16	40	R5	-	OLD	2	Y	-	Y	-	Y
HE83131	16kB	-	256B	Y	Y	Y	Y	Y	N	Y	Y	-	C[3:0],D	-	16	40	R5	-	OLD	2	Y	-	Y	-	Y
HE83134	64kB	192kB	256B	Y	Y	Y	Y	Y	N	Y	Y	-	C[3:0],D	14,15,17[7:4]	16	40	R5	-	OLD	2	Y	Y	Y	-	Y
HE83135	64kB	-	2kB	Y	Y	Y	Y	Y	N	Y	Y	-	C[3:0],D	-	16	40	R50	-	OLD	2	Y	-	Y	-	Y
HE83136	64kB	-	4kB	Y	Y	Y	Y	Y	N	Y	Y	-	C[3:0],D	-	16	40	R50	-	OLD	2	Y	-	Y	-	Y
HE83137	64kB	-	4kB	Y	Y	Y	Y	Y	N	Y	Y	-	C[3:0],D	14,15,17	16	40	R50	-	OLD	2	Y	Y	Y	-	Y
HE83141	64kB	64kB	256B	Y	Y	Y	Y	Y	N	Y	Y	Y	C,D	14	16	64	R5	-	OLD	2	Y	Y	Y	Y	Y



BODY	PROM	DROM	RAM	FX	FRC	Fin	SX	SRC	CKmd	TC1	TC2	TB	PORT	PORT_LCD	COM	SEG	LDVD	LREG	PWM	PMD	VO	DAO	OP Amp	DTMF	WDT
HE83R141	64kB	64kB	256B	Y	Y	-	Y	Y	N	Y	Y	Y	C,D	14	16	64	C5	Y	NEW	1	Y	Y	Y	Y	Y
HE83142	64kB	192kB	4kB	Y	Y	Y	Y	Y	N	Y	Y	Y	C,D	14	16	64	R5	-	OLD	2	Y	Y	Y	Y	Y
HE83R142	64kB	192kB	4kB	Y	Y	-	Y	Y	N	Y	Y	Y	C,D	14	16	64	C5	Y	NEW	1	Y	Y	Y	Y	Y
HE83144	64kB	-	256B	Y	Y	Y	Y	Y	N	Y	Y	Y	D	14,15	16	64	R50V	-	OLD	2	Y	-	-	-	-
HE83145	64kB	64kB	256B	Y	Y	Y	Y	Y	N	Y	Y	Y	D	14,15	16	64	R50V	-	OLD	2	Y	-	-	-	-
HE83146	64kB	128kB	256B	Y	Y	Y	Y	Y	N	Y	Y	Y	D	14,15	16	64	R50V	-	OLD	2	Y	-	-	-	-
HE83147	64kB	192kB	256B	Y	Y	Y	Y	Y	N	Y	Y	Y	D	14,15	16	64	R50V	-	OLD	2	Y	-	-	-	-
HE83148	64kB	192kB	2kB	Y	Y	Y	Y	Y	N	Y	Y	Y	D	14,15	16	64	R50V	-	OLD	2	Y	-	-	-	-
Mask Options	PROM	DROM [1:0]	RAM [1:0]	FXTAL	FOSCE	SXTAL	FCK/SCKN	TC1	TC2	TB	PRTCH, PRTCL, PRTD, PRT10	PRT10, PRT14, PRT15, PRT17H, PRT17L, PRTLCD	COM [1:0]	LPS[2:0]	PWM [1:0]	PMD	VO	DAO	OPAMP	DTMF	WDTE				

BODY : Sequence Code of Device Name

PROM : Program ROM

DROM : Data ROM

RAM : Internal SRAM

FX : Crystal Fast Clock

FRC : RC Fast Clock

Fin : OSC. Clock Input

SX : Crystal Slow Clock

SRC : RC Slow Clock

TC2 : Timer 2

TB : Time Base

PORT : Dedicated PORT Name

PORT_CLD : PORT Shared with LCD

COM : LCD Common Number

SEG : LCD Segment Number

LREG : LCD Regulator

PMD : PWM Architecture

VO : VO Output



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HE8P480
HE80000 SERIES

BODY	PROM	DROM	RAM	FX	FRC	Fin	SX	SRC	CKmd	TC1	TC2	TB	PORT	PORT_LCD	COM	SEG	LDVD	LREG	PWM	PMD	VO	DAO	OP Amp	DTMF	WDT
CKmd	: Clock Selection													DAO	: DAO Output										
TC1	: Timer 1													OP	: OP Amplifier										
														DTMF	: DTMF generator										

D. Pin Description

Pin Name	I/O	Function	Description
FXI	B	External fast clock pin. Connecting to crystal or RC to generate 32.768 kHz ~ 8MHz frequency.	Mask option setting : MO_FCK/SCKN= 00 → Slow Clock only 01 → Illegal 10 → Dual Clock 11 → Fast Clock only
FXO	O		
SXI	I	External slow clock pin. Connecting with 32768 Hz crystal or resistor as slow clock and providing clock source for LCD display, TIMER1, Time-Base and other internal blocks.	MO_FOSCE = 0 → Internal fast osc. = 1 → External fast osc. MO_FXTAL = 0 → RC osc. for fast clock = 1 → X'tal osc. for fast clock MO_SXTAL = 0 → RC for 32768 Hz clock = 1 → X'tal for 32768 Hz clock Use OP1 and OP2 to switch among different operation mode (NORMAL, SLOW, IDEL and SLEEP). In Dual Clock mode, the main system clock is still the Fast Clock. The 32768 Hz clock is for LCD and Timer 1 only.
SXO	O		
RSTP_N	I	system reset	Level trigger, active low. Except for using this pin, using mask option (MO_PORE=1) could enable IC build-in Power-on reset circuit. Besides, MO_WDTE can set Watch Dog Timer : MO_WDTE= 0 → Disable Watch Dog Timer = 1 → Enable Watch Dog Timer
TSTP_P	I	TEST PIN	Please bond this pin and add a test point on PCB for debugging. But for improving ESD, please connect this point with zero Ohm resistor to GND.
PRTC[7:0]/ PDATA[7:0]	B	Port C bi-directional I/O pin, or parallel program download mode when programming by parallel mode.	Mask options : MO_CPP[7..0] = 1 → Push-pull. = 0 → Open-drain. When use them as input (No tri-state structure), it must Output "1" before reading.
PRTD7/SDO	B	I/O port / WAKEUP / INT/ SDO: Series Data Output	8-pin bi-directional I/O port. PRTD[7..2] as wake-up pin, PRTD[7..6] as external interrupt pin, and Mask options :



Pin Name	I/O	Function	Description
PRTD6/SDI	B	I/O port / WAKEUP / INT/ SDI: Series Data Input	MO_DPP[7..0] = 1 → Push-pull. = 0 → Open-drain. When use them as input (No tri-state structure), it must Output “1” before reading. The PRTD are also used for OTP programming when setting the loader pin high to enter programming mode.
PRTD5/SCK	B	I/O port / WAKEUP / SCK: Series Clock	
PRTD4/D_C n	B	I/O port / WAKEUP / D_Cn: data or command	
PRTD3/R_W n	B	I/O port / WAKEUP / R_Wn: Read or Write	
PRTD2/P_Sn	B	I/O port / WAKEUP / P_Sn: Parallel or Series	
PRTD[1:0]	B	I/O port	Mask options : MO_10PP[7:0] = 1 → Push-pull. = 0 → Open-drain. When use them as input (No tri-state structure), it must Output “1” before reading.
PRT10[7:0]	B	Bi-directional I/O Port	
COM[15:0]	O	LCD COM Output	Please refer to LCD and RAM map
SEG[63:56]	B	SEG / IO Ports	These pins can be used as LCD segment driver or I/O ports. Please refer to Mask options Table for details.
SEG[55:48]	B	SEG / IO Ports	
SEG[47:40]	O	LCD segment	
SEG[39:36]	B	SEG / IO Ports	
SEG[35:32]	B	SEG / IO Ports	
SEG[31:28]	B	SEG / IO Ports	
SEG[27:24]	B	SEG / IO Ports	
SEG[23:20]	B	SEG / IO Ports	
SEG[19:16]	B	SEG / IO Ports	
SEG[15:8]	B	SEG / IO Ports	
SEG[7:0]	O	LCD segment	
LCDGS	B	LCD voltage control	Refer to Application circuit.
LCDVX	B	LCD voltage control	
LCDVTB	B	LCD voltage control	



Pin Name	I/O	Function	Description
LC4B	B	charge pump switch	
LC4A	B	charge pump switch	
LC3B	B	charge pump switch	
LC3A	B	charge pump switch	
LC2B	B	charge pump switch	
LC2A	B	charge pump switch	
LC1B	B	charge pump switch	
LC1A	B	charge pump switch	
LC2	B	charge pump switch2	
LC1	B	charge pump switch1	
LV5	B	charge pump V5(V4,V3)	
LV4	B	charge pump V4(V3,V2)	
LV3	B	charge pump V3(V2,V1)	
LV2	B	charge pump V2(V1)	
LV1	B	charge pump V1, regulator output	
LVF	B	regulator resistor feedback	
LR4	B	LCD resistor level 4	
LR3	B	LCD resistor level 3	
LR2	B	LCD resistor level 2	
LR1	B	LCD resistor level 1	
LR0	B	LCD resistor level 0	
LVG	B	LCD virtual GND	
PWM	O	The PWM output can drive speaker or buzzer directly.	Set Bit2 (PWM=1) of VOC register to turn on PWM.
GND_PWM	P	dedicated GND for PWM	Dedicated PWM ground which is separated with digital ground.
PWMP	O	The PWM positive output can drive	Set Bit2 (PWM=1) of VOC register to turn on PWM.



Pin Name	I/O	Function	Description
		speaker or buzzer directly.	
PWMN	O	The PWM negative output can drive speaker or buzzer directly.	Set Bit2 (PWM=1) of VOC register to turn on PWM.
VO	O	DAC voice output	Set Bit1 (DA=1) of VOC register to turn on VO.
DAO	O	DAC output	Digital to analog converter output
OPIP	I	Positive input of OP comparator	Set the bit0 (OP=1) of VOC register to turn on OP comparator.
OPIN	I	Negative input of OP comparator	The operating range between 0 ~ (VDD-1).
OPO	O	OPAMP output pin	
DTMFO	O	DTMF tone	This function can be turned on/off in DTMFC register. Refer to HE80000 series user's manual. Use Mask Option MO_DTMFSCK set clock source : MO_DTMFSCK= 0 → Clock Source=3.579545MHz = 1 → Clock Source=32768 Hz
MUTE	O	MUTE Output for Dialer	This function can be turned on/off in DTMFC register. Refer to HE80000 series user's manual.
SDO	O	SDO for Dialer Application	This function can be turned on/off in DTMFC register. Refer to HE80000 series user's manual.
KEYTONE	O	1024 Hz 50% Duty square wave	This function can be turned on/off in DTMFC register. Refer to HE80000 series user's manual.
LOADER	I	Define Loader Mode	Used by OTP writer to load program.
VDD	P	digital VDD	Add a 0.1 μ F capacitor as by-pass capacitor.
GND	P	digital GND	
VPP	P	OTP high voltage power	Apply 12V to write the OTP ROM, and 5V to normal operation



E. PIN Connection Comparison Table

NAME	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HR83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
FXI	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
FXO	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
SXI	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
SXO	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
RSTP_N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
TSTP_P	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PRTC[7:4]	float	float	Y	Y	float	float	float	float	float	float	float	float	float
PRTC[3:0]	float	float	Y	Y	Y	Y	Y	float	float	float	float	Y	Y
PRTD[7:6]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PRTD[5:4]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PRTD[3:2]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PRTD[1:0]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PRT10[7:0]	float	float	Y	Y	float	float	float	float	float	float	float	float	float
COM[15:12]	float	float	float	float	float	float	float	float	float	float	float	Y	Y
COM[11:8]	float	float	float	float	float	float	float	float	float	float	float	Y	Y
COM[7]	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[6]	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[5]	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[4]	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y



NAME	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HR83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
COM[3]	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[2]	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[1:0]	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y
SEG[63:56]	float	float	float	float	float	float	float	float	float	float	float	float	float
SEG[55:48]	float	float	float	float	float	float	float	float	float	float	float	float	float
SEG[47:40]	float	float	float	float	float	float	float	float	float	float	float	float	float
SEG[39:36]	float	float	float	float	Y	Y	Y	Y	Y/P17H	Y	Y/P17H	Y	Y
SEG[35:32]	float	float	float	float	Y	Y	Y	Y	Y/P17L	Y	Y/P17L	Y	Y
SEG[31:28]	float	float	float	float	Y	Y	Y	Y	Y/P15H	Y	Y/P15H	Y	Y
SEG[27:24]	float	float	float	float	Y	Y	Y	Y	Y/P15L	Y	Y/P15L	Y	Y
SEG[23:20]	float	float	float	float	Y	Y	Y	Y	Y/P14H	Y	Y/P14H	Y	Y
SEG[19:16]	float	float	float	float	Y	Y	Y	Y	Y/P14L	Y	Y/P14L	Y	Y
SEG[15:8]	float	float	float	float	Y	Y	Y	Y	Y/P11	Y	Y/P11	Y	Y
SEG[7:0]	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y
LCDGS	float	float	float	float	float	float	float	float	float	float	float	float	float
LCDVX	float	float	float	float	float	float	float	float	float	float	float	float	float
LCDVTB	float	float	float	float	float	float	float	float	float	float	float	float	float
LC4B	float	float	float	float	float	float	float	float	float	float	float	float	float
LC4A	float	float	float	float	float	float	float	float	float	float	float	float	float
LC3B	float	float	float	float	float	float	float	float	float	float	float	float	float
LC3A	float	float	float	float	float	float	float	float	float	float	float	float	float



NAME	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HR83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
LC2B	float	float	float	float	float	float	float	float	float	float	float	float	float
LC2A	float	float	float	float	float	float	float	float	float	float	float	float	float
LC1B	float	float	float	float	float	float	float	float	float	float	float	float	float
LC1A	float	float	float	float	float	float	float	float	float	float	float	float	float
LC2	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y
LC1	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y
LV5	float	float	float	float	Y(V3)	Y(V3)	Y(V3)	Y(V3)	Y(V4)	Y(V3)	Y(V4)	Y(V3)	Y(V3)
LV4	float	float	float	float	VDD(V2)	VDD(V2)	VDD(V2)	VDD(V2)	Y(V3)	VDD(V2)	T(V3)	VDD(V2)	VDD(V2)
LV3	float	float	float	float	Y(V1)	Y(V1)	Y(V1)	Y(V1)	Y(V2)	Y(V1)	TY(V2)	Y(V1)	Y(V1)
LV2	float	float	float	float	float	float	float	float	Y(V1)	float	Y(V1)	float	float
LV1	float	float	float	float	float	float	float	float	float	float	float	float	float
LVF	float	float	float	float	float	float	float	float	Y	float	Y	float	float
LR4	float	float	float	float	Y	Y	Y	Y	float	Y	float	Y	Y
LR3	float	float	float	float	Y	Y	Y	Y	float	Y	float	Y	Y
LR2	float	float	float	float	Y	Y	Y	Y	float	Y	float	Y	Y
LR1	float	float	float	float	Y	Y	Y	Y	float	Y	float	Y	Y
LR0	float	float	float	float	float	float	float	float	float	float	float	float	Y
LVG	float	float	float	float	Y	Y	Y	Y	float	Y	float	Y	Y
PWM	Y	Y	float	float	float	float	float	float	float	float	float	float	float
GND_PWM	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
PWMP	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y



NAME	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HR83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
PWMN	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
VO	Y	Y	Y	Y	Y	Y	Y	float	float	float	float	Y	Y
DAO	float	float	Y	Y	float	float	float	float	float	float	float	float	float
OPIP	float	float	Y	Y	Y	Y	Y	float	float	float	float	Y	Y
OPIN	float	float	Y	Y	Y	Y	Y	float	float	float	float	Y	Y
OPO	float	float	Y	Y	Y	Y	Y	float	float	float	float	Y	Y
DTMFO	float	float	float	float	float	float	float	float	float	float	float	float	float
MUTE	float	float	float	float	float	float	float	float	float	float	float	float	float
SDO	float	float	float	float	float	float	float	float	float	float	float	float	float
KEYTONE	float	float	float	float	float	float	float	float	float	float	float	float	float
LOADER	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
VPP	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y



NAME	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
FXI	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
FXO	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
SXI	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
SXO	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
RSTP_N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
TSTP_P	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PRTC[7:4]	float	float	float	float	Y	Y	Y	Y	float	float	float	float	float
PRTC[3:0]	Y	Y	Y	Y	Y	Y	Y	Y	float	float	float	float	float
PRTD[7:6]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PRTD[5:4]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PRTD[3:2]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PRTD[1:0]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
PRT10[7:0]	float	float	float	float	float	float	float	float	float	float	float	float	float
COM[15:12]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[11:8]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[7]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[6]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[5]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[4]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[3]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y



NAME	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
COM[2]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
COM[1:0]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
SEG[63:56]	float	float	float	float	Y/P14	Y/P14	Y/P14	Y/P14	Y/P15	Y/P15	Y/P15	Y/P15	Y/P15
SEG[55:48]	float	float	float	float	Y	Y	Y	Y	Y/P14	Y/P14	Y/P14	Y/P14	Y/P14
SEG[47:40]	float	float	float	float	Y	Y	Y	Y	Y	Y	Y	Y	Y
SEG[39:36]	Y/P17L	Y	Y	Y/P17H	Y	Y	Y	Y	Y	Y	Y	Y	Y
SEG[35:32]	Y/P15H	Y	Y	Y/P17L	Y	Y	Y	Y	Y	Y	Y	Y	Y
SEG[31:28]	Y/P15L	Y	Y	Y/P15H	Y	Y	Y	Y	Y	Y	Y	Y	Y
SEG[27:24]	Y/P14H	Y	Y	Y/P15L	Y	Y	Y	Y	Y	Y	Y	Y	Y
SEG[23:20]	Y/P14L	Y	Y	Y/P14H	Y	Y	Y	Y	Y	Y	Y	Y	Y
SEG[19:16]	Y	Y	Y	Y/P14L	Y	Y	Y	Y	Y	Y	Y	Y	Y
SEG[15:8]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
SEG[7:0]	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
LCDGS	float	float	float	float	float	Y	float	Y	float	float	float	float	float
LCDVX	float	float	float	float	float	Y	float	Y	float	float	float	float	float
LCDVTB	float	float	float	float	float	Y	float	Y	float	float	float	float	float
LC4B	float	float	float	float	float	Y	float	Y	float	float	float	float	float
LC4A	float	float	float	float	float	Y	float	Y	float	float	float	float	float
LC3B	float	float	float	float	float	Y	float	Y	float	float	float	float	float
LC3A	float	float	float	float	float	Y	float	Y	float	float	float	float	float
LC2B	float	float	float	float	float	Y	float	Y	float	float	float	float	float



NAME	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
LC2A	float	float	float	float	float	Y	float	Y	float	float	float	float	float
LC1B	float	float	float	float	float	Y	float	Y	float	float	float	float	float
LC1A	float	float	float	float	float	Y	float	Y	float	float	float	float	float
LC2	Y	Y	Y	Y	Y	float	Y	float	Y	Y	Y	Y	Y
LC1	Y	Y	Y	Y	Y	float	Y	float	Y	Y	Y	Y	Y
LV5	Y(V3)	Y(V3)	Y(V3)	Y(V3)	Y(V3)	Y(V5)	Y(V3)	Y(V5)	Y(V3)	Y(V3)	Y(V3)	Y(V3)	Y(V3)
LV4	VDD(V2)	VDD(V2)	VDD(V2)	VDD(V2)	VDD(V2)	Y(V4)	VDD(V2)	Y(V4)	Y(V2)	Y(V2)	Y(V2)	Y(V2)	Y(V2)
LV3	Y(V1)	Y(V1)	Y(V1)	Y(V1)	Y(V1)	Y(V3)	Y(V1)	Y(V3)	Y(V1)	Y(V1)	Y(V1)	Y(V1)	Y(V1)
LV2	float	float	float	float	float	Y(V2)	float	Y(V2)	float	float	float	float	float
LV1	float	float	float	float	float	Y(V1)	float	Y(V1)	float	float	float	float	float
LVF	float	float	float	float	float	float	float	float	float	float	float	float	float
LR4	Y	Y	Y	Y	Y	float	Y	float	Y	Y	Y	Y	Y
LR3	Y	Y	Y	Y	Y	float	Y	float	Y	Y	Y	Y	Y
LR2	Y	Y	Y	Y	Y	float	Y	float	Y	Y	Y	Y	Y
LR1	Y	Y	Y	Y	Y	float	Y	float	Y	Y	Y	Y	Y
LR0	float	Y	Y	Y	float	float	float	float	Y	Y	Y	Y	Y
LVG	Y	Y	Y	Y	Y	float	Y	float	Y	Y	Y	Y	Y
PWM	float	float	float	float	float	Y	float	Y	float	float	float	float	float
GND_PWM	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
PWMP	Y	Y	Y	Y	Y	float	Y	float	Y	Y	Y	Y	Y
PWMN	Y	Y	Y	Y	Y	float	Y	float	Y	Y	Y	Y	Y



NAME	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
VO	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
DAO	Y	Y	Y	Y	Y	Y	Y	Y	float	float	float	float	float
OPIP	Y	Y	Y	Y	Y	Y	Y	Y	float	float	float	float	float
OPIN	Y	Y	Y	Y	Y	Y	Y	Y	float	float	float	float	float
OPO	Y	Y	Y	Y	Y	Y	Y	Y	float	float	float	float	float
DTMFO	float	float	float	float	Y	Y	Y	Y	float	float	float	float	float
MUTE	float	float	float	float	Y	Y	Y	Y	float	float	float	float	float
SDO	float	float	float	float	Y	Y	Y	Y	float	float	float	float	float
KEYTONE	float	float	float	float	Y	Y	Y	Y	float	float	float	float	float
LOADER	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
VPP	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y



F. Mask Option Comparison Table

When use KB OTPWriter (include application software& hardware) to write data to OTP, user can select specific IC from software application and in the mean time, the KB OTPWriter will set the entire configuration automatically. The following table describes the related configuration setting, if user wants to use HE8P480 full function setting, please reference following setting. The KB OTPWriter can also output the configuration setting to a file (*.FUS) and this file can be used for mass production. The “user” in the table means the related item can be set by user.



NAME	VALUE	NOTE	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HE83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
MO_FOSCE	0	internal fast OSC	1	1	User	User	User	User	User	User	User	User	User	User	User
	1	external fast OSC													
MO_FXTAL	0	R/C osc. For fast clock	User	User	User	User	User	User	User	User	User	User	User	User	User
	1	X'tal osc. For fast clock													
MO_FRCL_S[2:0]	000	RFRC_I $\sim$ 500k	000	000	User	User	User	User	User	User	User	User	User	User	User
	001	RFRC_I $\sim$ 1M													
	010	RFRC_I $\sim$ 1.5M													
	011	RFRC_I $\sim$ 2M													
	100	RFRC_I $\sim$ 2.5M													
	101	RFRC_I $\sim$ 3M													
	110	RFRC_I $\sim$ 3.5M													
	111	RFRC_I $\sim$ 4M													
MO_SXTAL	0	R/C osc. For 32k clock	0	0	User	User	User	User	User	User	User	User	User	User	User
	1	X'tal osc. For 32k clock													
MO_FCK/SCKN	00	slow clock only	11	11	User	User	User	User	User	User	User	User	User	User	User
	01	illegal													
	10	dual clock													
	11	fast clock only													
MO_WDTE	0	WDT disable	User	User	User	User	User	User	User	User	User	User	User	User	User
	1	WDT enable													
MO_CPP[7:4]	0	open-drain output	1111	1111	User	User	1111	1111	1111	1111	1111	1111	1111	1111	1111



NAME	VALUE	NOTE	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HE83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
	1	push-pull output					(User)	(User)	(User)						
MO_CPP[3:0]	0	open-drain output	1111	1111	User	User	User	User	User	1111	1111	1111	1111	User	User
	1	push-pull output													
MO_DPP[7:0]	0	open-drain output	User	User	User	User	User	User	User	User	User	User	User	User	User
	1	push-pull output													
MO_10PP[7:0]	0	open-drain output	11111111	11111111	User	User	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
	1	push-pull output													
MO_11PP[7:0]	0	open-drain output	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	User	11111111	User	11111111	11111111
	1	push-pull output													
MO_14PP[7:0]	0	open-drain output	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	User	11111111	User	11111111	11111111
	1	push-pull output													
MO_15PP[7:0]	0	open-drain output	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	User	11111111	User	11111111	11111111
	1	push-pull output													
MO_17PP[7:4]	0	open-drain output	1111	1111	1111	1111	1111	1111	1111	1111	User	1111	User	1111	1111
	1	push-pull output													
MO_17PP[3:0]	0	open-drain output	1111	1111	1111	1111	1111	1111	1111	1111	User	1111	User	1111	1111
	1	push-pull output													
MO_DTMFSCK	0	DTMF clock source 3.58M Hz	0	0	0	0	0	0	0	0	0	0	0	0	0
	1	DTMF clock source 32768 Hz													
LCDR(fixed to 0)	0	LCD low resistance disable	1	1	1	1	User	User	User	User	1	User	1	User	User
	1	LCD low resistance enable													



NAME	VALUE	NOTE	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HE83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
LCDBS[2:0]	000	LCD bias R=30k	111	111	111	111	User	User	User	User	111	User	111	User	User
	001	LCD bias R=60k													
	010	LCD bias R=90k													
	011	LCD bias R=120k													
	100	LCD bias R=210k													
	101	LCD bias R=240k													
	110	LCD bias R=270k													
	111	LCD bias R=300k													
EM_TPP	0	TPP[23:16] == 00h	1	1	1	1	1	1	0	0	0	1	1	0	0
	1	TPP enable													
MO_LIOS15_8	0	IO pin	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	User	11111111	User	11111111	11111111
	1	LCD pin													
MO_LIOS19_16	0	IO pin	1111	1111	1111	1111	1111	1111	1111	1111	User	1111	User	1111	1111
	1	LCD pin													
MO_LIOS23_20	0	IO pin	1111	1111	1111	1111	1111	1111	1111	1111	User	1111	User	1111	1111
	1	LCD pin													
MO_LIOS27_24	0	IO pin	1111	1111	1111	1111	1111	1111	1111	1111	User	1111	User	1111	1111
	1	LCD pin													
MO_LIOS31_28	0	IO pin	1111	1111	1111	1111	1111	1111	1111	1111	User	1111	User	1111	1111
	1	LCD pin													
MO_LIOS35_32	0	IO pin	1111	1111	1111	1111	1111	1111	1111	1111	User	1111	User	1111	1111



NAME	VALUE	NOTE	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HE83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
	1	LCD pin													
MO_LIOS39_36	0	IO pin	1111	1111	1111	1111	1111	1111	1111	1111	User	1111	User	1111	1111
	1	LCD pin													
MO_LIOS55_48	0	IO pin	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
	1	LCD pin													
MO_LIOS63_56	0	IO pin	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
	1	LCD pin													
MO_S3920_Prt	0	SEG23-20 shared with P14L	1	1	1	1	1	1	1	1	1	1	1	1	1
		SEG27-24 shared with P14H													
		SEG31-28 shared with P15L													
		SEG35-32 shared with P15H													
		SEG39-36 shared with P17L													
	1	SEG23-20 shared with P14H													
		SEG27-24 shared with P15L													
		SEG31-28 shared with P15H													
		SEG35-32 shared with P17L													
		SEG39-36 shared with P17H													
MO_S6356_Prt	0	SEG63-56 shared with P14	1	1	1	1	1	1	1	1	1	1	1	1	1
	1	SEG63-56 shared with P15													
MO_LCD[1:0]	00	LCD not exist	00	00	00	00	01	01	01	01	01	01	01	10	10
	01	8 x 40													



NAME	VALUE	NOTE	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HE83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
	10	16 x 40													
	11	16 x 64													
LCDPS[1:0]	00	NO LCD power system	00	00	00	00	01	01	01	01	10	01	10	01	01
	01	R50V													
	10	C4													
	11	C5													
MO_LVRG	0	Regulator disabled	0	0	0	0	0	0	0	0	User	0	User	0	0
	1	Regulator enabled													
MO_PROTECTN	0	OTP read protect	User	User	User	User	User	User	User	User	User	User	User	User	User
	1	OTP not protect													
MO_OTPCMP	0	OTP read by Pre-charge	KB	KB	KB	KB	KB	KB	KB	KB	KB	KB	KB	KB	KB
	1	OTP read by current compare													
MO_PROM	0	PROM 16KB	1	1	1	1	1	1	1	1	1	1	1	1	0
	1	PROM 64KB													
MO_DROM[1:0]	00	NO DROM	11	01	11	01	11	01	00	00	00	11	01	00	00
	01	DROM 64KB													
	10	DROM 128KB													
	11	DROM 192KB													
MO_RAM[1:0]	00	RAM 128 byte	00	00	00	00	01	01	01	01	01	01	01	01	01
	01	RAM 256 byte													
	10	RAM 2K byte													



NAME	VALUE	NOTE	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HE83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
	11	RAM 4K byte													
MO_TC2	0	TC2 not exist	0	0	1	1	1	1	1	1	1	1	1	1	1
	1	TC2 exist													
MO_TB	0	TB not exist	0	0	0	0	0	0	0	0	0	0	0	0	0
	1	TB exist													
MO_PRT0C[1:0]	00	prt0C not exist	00	00	11	11	01	01	01	00	00	00	00	01	01
	01	only prt0C[3:0] exist													
	10	only prt0C[7:4] exist													
	11	prt0C exist													
MO_PRT10	0	prt10 not exist	0	0	1	1	0	0	0	0	0	0	0	0	0
	1	prt10 exist													
MO_PWM	0	PWMP/PWMN output	1	1	0	0	0	0	0	0	0	0	0	0	0
	1	PWM/GND_PWM output													
MO_PMD	0	2 drive pin	1	1	0	0	0	0	0	0	0	0	0	0	0
	1	1 drive pin													
MO_VO	0	DAC not exist	1	1	1	1	1	1	1	0	0	0	0	1	1
	1	DAC exist													
MO_DAO	0	DAO output not exist	0	0	1	1	0	0	0	0	0	0	0	0	0
	1	DAO output exist													
MO_OPAMP	0	OP Amp not exist	0	0	1	1	1	1	1	0	0	0	0	1	1
	1	OP Amp exist													



NAME	VALUE	NOTE	HE82006	HE82015	HE83006	HE83015	HE83120	HE83121	HE83122	HE83123	HE83R123	HE83124	HE83R125	HE83130	HE83131
MO_DTMF	0	DTMF not exist	0	0	0	0	0	0	0	0	0	0	0	0	0
	1	DTMF exist													



Mask Options Table 2

NAME	VALUE	NOTE	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
MO_FOSCE	0	internal fast OSC	User	User	User	User	User	1	User	1	User	User	User	User	User
	1	external fast OSC													
MO_FXTAL	0	R/C osc. For fast clock	User	User	User	User	User	User	User	User	User	User	User	User	User
	1	X'tal osc. For fast clock													
MO_FRCL_S[2:0]	000	RFRC_I $\approx$ 500k	User	User	User	User	User	000	User	000					
	001	RFRC_I $\approx$ 1M													
	010	RFRC_I $\approx$ 1.5M													
	011	RFRC_I $\approx$ 2M													
	100	RFRC_I $\approx$ 2.5M													
	101	RFRC_I $\approx$ 3M													
	110	RFRC_I $\approx$ 3.5M													
	111	RFRC_I $\approx$ 4M													
MO_SXTAL	0	R/C osc. For 32k clock	User	User	User	User	User	User	User	User	User	User	User	User	User
	1	X'tal osc. For 32k clock													
MO_FCK/SCKN	00	slow clock only	User	User	User	User	User	User	User	User	User	User	User	User	User
	01	illegal													
	10	dual clock													
	11	fast clock only													
MO_WDTE	0	WDT disable	User	User	User	User	User	User	User	User	0	0	0	0	0
	1	WDT enable													



NAME	VALUE	NOTE	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
MO_CPP[7:4]	0	open-drain output	1111	1111	1111	1111	User	User	User	User	1111	1111	1111	1111	1111
	1	push-pull output													
MO_CPP[3:0]	0	open-drain output	User	User	User	User	User	User	User	User	1111	1111	1111	1111	1111
	1	push-pull output													
MO_DPP[7:0]	0	open-drain output	User	User	User	User	User	User	User	User	User	User	User	User	User
	1	push-pull output													
MO_10PP[7:0]	0	open-drain output	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
	1	push-pull output													
MO_11PP[7:0]	0	open-drain output	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
	1	push-pull output													
MO_14PP[7:0]	0	open-drain output	User	11111111	11111111	User	User	User	User	User	User	User	User	User	User
	1	push-pull output													
MO_15PP[7:0]	0	open-drain output	User	11111111	11111111	User	11111111	11111111	11111111	11111111	User	User	User	User	User
	1	push-pull output													
MO_17PP[7:4]	0	open-drain output	User	1111	1111	User	1111	1111	1111	1111	1111	1111	1111	1111	1111
	1	push-pull output													
MO_17PP[3:0]	0	open-drain output	1111	1111	1111	User	1111	1111	1111	1111	1111	1111	1111	1111	1111
	1	push-pull output													
MO_DTMFSCK	0	DTMF clock source 3.58M Hz	0	0	0	0	User	User	User	User	0	0	0	0	0
	1	DTMF clock source 32768 Hz													
LCDR (fixed to 0)	0	LCD low resistance disable	User	User	User	User	User	1	User	1	User	User	User	User	User



NAME	VALUE	NOTE	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
	1	LCD low resistance enable													
LCDBS[2:0]	000	LCD bias R=30k	User	User	User	User	User	111	User	111	User	User	User	User	User
	001	LCD bias R=60k													
	010	LCD bias R=90k													
	011	LCD bias R=120k													
	100	LCD bias R=210k													
	101	LCD bias R=240k													
	110	LCD bias R=270k													
	111	LCD bias R=300k													
EM_TPP	0	TPP[23:16] == 00h	1	0	0	0	1	1	1	1	0	1	1	1	1
	1	TPP enable													
MO_LIOS15_8	0	IO pin	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
	1	LCD pin													
MO_LIOS19_16	0	IO pin	1111	1111	1111	User	1111	1111	1111	1111	1111	1111	1111	1111	1111
	1	LCD pin													
MO_LIOS23_20	0	IO pin	User	1111	1111	User	1111	1111	1111	1111	1111	1111	1111	1111	1111
	1	LCD pin													
MO_LIOS27_24	0	IO pin	User	1111	1111	User	1111	1111	1111	1111	1111	1111	1111	1111	1111
	1	LCD pin													
MO_LIOS31_28	0	IO pin	User	1111	1111	User	1111	1111	1111	1111	1111	1111	1111	1111	1111
	1	LCD pin													



NAME	VALUE	NOTE	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
MO_LIOS35_32	0	IO pin	User	1111	1111	User	1111	1111	1111	1111	1111	1111	1111	1111	1111
	1	LCD pin													
MO_LIOS39_36	0	IO pin	User	1111	1111	User	1111	1111	1111	1111	1111	1111	1111	1111	1111
	1	LCD pin													
MO_LIOS55_48	0	IO pin	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	User	User	User	User	User
	1	LCD pin													
MO_LIOS63_56	0	IO pin	11111111	11111111	11111111	11111111	User	User	User	User	User	User	User	User	User
	1	LCD pin													
MO_S3920_Prt	0	SEG23-20 shared with P14L	0	1	1	1	1	1	1	1	1	1	1	1	1
		SEG27-24 shared with P14H													
		SEG31-28 shared with P15L													
		SEG35-32 shared with P15H													
		SEG39-36 shared with P17L													
	1	SEG23-20 shared with P14H													
		SEG27-24 shared with P15L													
		SEG31-28 shared with P15H													
		SEG35-32 shared with P17L													
		SEG39-36 shared with P17H													
MO_S6356_Prt	0	SEG63-56 shared with P14	1	1	1	1	0	0	0	0	1	1	1	1	1
	1	SEG63-56 shared with P15													
MO_LCD[1:0]	00	LCD not exist	10	10	10	10	11	11	11	11	11	11	11	11	11



NAME	VALUE	NOTE	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
	01	8 x 40													
	10	16 x 40													
	11	16 x 64													
LCDPS[1:0]	00	NO LCD power system	01	01	01	01	01	11	01	11	01	01	01	01	01
	01	R50V													
	10	C4													
	11	C5													
MO_LVRG	0	Regulator disabled	0	0	0	0	0	1	0	1	0	0	0	0	0
	1	Regulator enabled													
MO_PROTECTN	0	OTP read protect	User	User	User	User	User	User	User	User	User	User	User	User	User
	1	OTP not protect													
MO_OTPCMP	0	OTP read by Pre-charge	KB	KB	KB	KB	KB	KB	KB	KB	KB	KB	KB	KB	KB
	1	OTP read by current compare													
MO_PROM	0	PROM 16KB	1	1	1	1	1	1	1	1	1	1	1	1	1
	1	PROM 64KB													
MO_DROM[1:0]	00	NO DROM	11	00	00	00	01	01	11	11	00	01	10	11	11
	01	DROM 64KB													
	10	DROM 128KB													
	11	DROM 192KB													
MO_RAM[1:0]	00	RAM 128 byte	01	10	11	11	01	01	11	11	01	01	01	01	10
	01	RAM 256 byte													



NAME	VALUE	NOTE	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
	10	RAM 2K byte													
	11	RAM 4K byte													
MO_TC2	0	TC2 not exist	1	1	1	1	1	1	1	1	1	1	1	1	1
	1	TC2 exist													
MO_TB	0	TB not exist	0	0	0	0	1	1	1	1	1	1	1	1	1
	1	TB exist													
MO_PRT0C[1:0]	00	prt0C not exist	01	01	01	01	11	11	11	11	00	00	00	00	00
	01	only prt0C[3:0] exist													
	10	only prt0C[7:4] exist													
	11	prt0C exist													
MO_PRT10	0	prt10 not exist	0	0	0	0	0	0	0	0	0	0	0	0	0
	1	prt10 exist													
MO_PWM	0	PWMP/PWMN output	0	0	0	0	0	1	0	1	0	0	0	0	0
	1	PWM/GND_PWM output													
MO_PMD	0	2 drive pin	0	0	0	0	0	1	0	1	0	0	0	0	0
	1	1 drive pin													
MO_VO	0	DAC not exist	1	1	1	1	1	1	1	1	1	1	1	1	1
	1	DAC exist													
MO_DAO	0	DAO output not exist	1	0	0	1	1	1	1	1	0	0	0	0	0
	1	DAO output exist													
MO_OPAMP	0	OP Amp not exist	1	1	1	1	1	1	1	1	0	0	0	0	0



NAME	VALUE	NOTE	HE83134	HE83135	HE83136	HE83137	HE83141	HE83R141	HE83142	HE83R142	HE83144	HE83145	HE83146	HE83147	HE83148
	1	OP Amp exist													
MO_DTMF	0	DTMF not exist	0	0	0	0	1	1	1	1	0	0	0	0	0
	1	DTMF exist													



F. LCD Display RAM MAP Table

LCD RAM MAP

		16COM x 64SEG		16COM x 40SEG		8COM x 40SEG	
RAM Address		7	0	7	0	7	0
	80	C0	C0	C0	C0		
		SEG7 ~ SEG0	SEG7 ~ SEG0	SEG7 ~ SEG0			
	90	C15	C15	C15	C15		
		SEG15 ~ SEG8	SEG15 ~ SEG8	SEG15 ~ SEG8			
	A0	C0	C0	C0	C0		
		SEG23 ~ SEG16	SEG23 ~ SEG16	SEG23 ~ SEG16			
	B0	C15	C15	C15	C15		
		SEG31 ~ SEG24	SEG31 ~ SEG24	SEG31 ~ SEG24			
	C0	C0	C0	C0	C0		
		SEG39 ~ SEG32	SEG39 ~ SEG32	SEG39 ~ SEG32			
	D0	C15	C15	C15	C15		
		SEG47 ~ SEG40					
	D8	C0	C0			C7	SEG7 ~ SEG0 C0
		SEG55 ~ SEG48				C7	SEG15 ~ SEG8 C0
	E0	C15	C15			C7	SEG23 ~ SEG16 C0
	E8	C0	C0			C7	SEG31 ~ SEG24 C0
	F0					C7	SEG39 ~ SEG32 C0
	F8	SEG63 ~ SEG56					

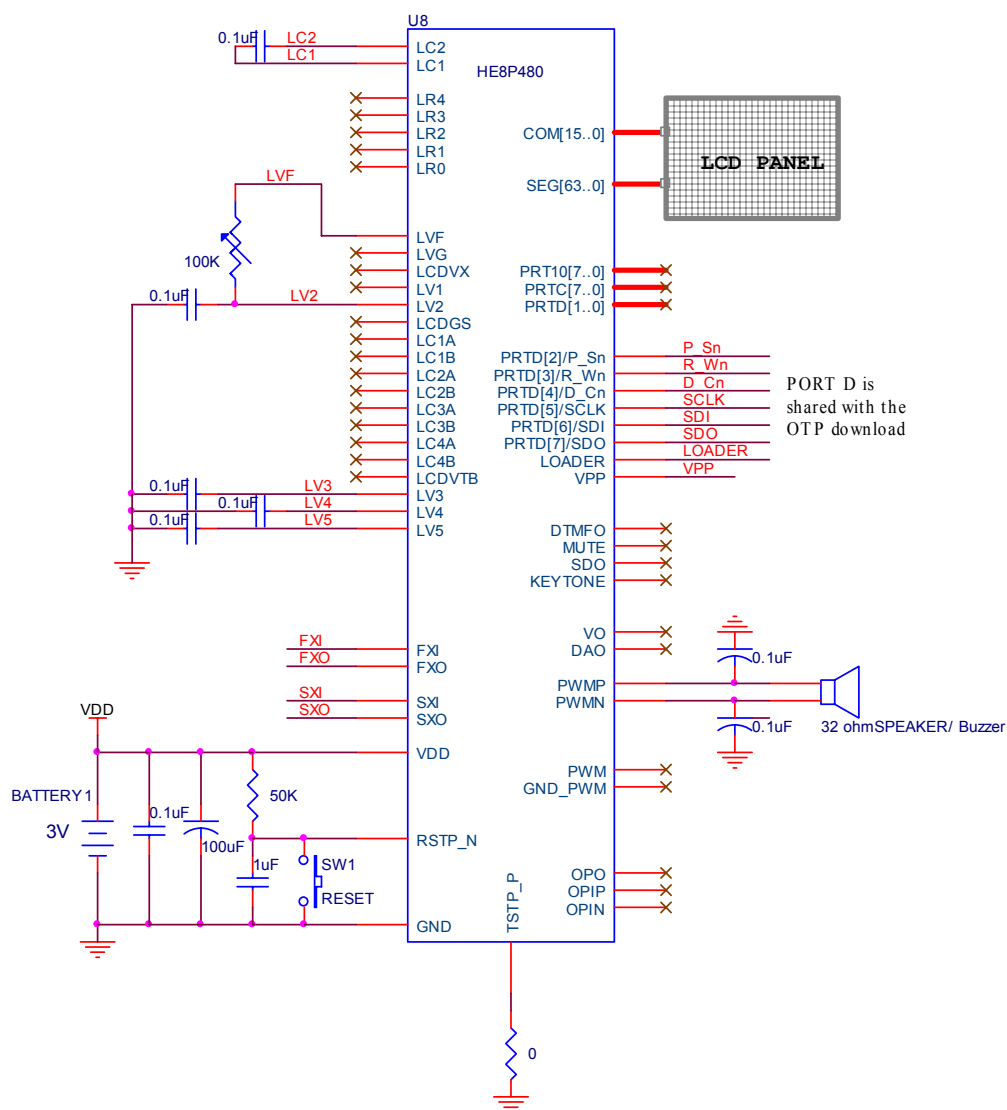


G. LCD Segments and I/O Map

SEG	63 ~ 60	59 ~ 56	55 ~ 52	51 ~ 48	47 ~ 44	43 ~ 40	39 ~ 36	35 ~ 32	31 ~ 28	27 ~ 24	23 ~ 20	19 ~ 16	15 ~ 12	11 ~ 8	7 ~ 4	3 ~ 0
HE83120							SEG39 ~ SEG0									
HE83121							SEG39 ~ SEG0									
HE83122							SEG39 ~ SEG0									
HR83123							SEG39 ~ SEG0									
HR83124							SEG39 ~ SEG0									
HE83R123							PRT17		PRT15		PRT14		PRT11		SEG7 ~ SEG0	
HE83R125							PRT17		PRT15		PRT14		PRT11		SEG7 ~ SEG0	
HE83130							SEG39 ~ SEG0									
HE83131							SEG39 ~ SEG0									
HE83134							PRT17L	PRT15		PRT14		SEG19 ~ SEG0				
HE83135							SEG39 ~ SEG0									
HE83136							SEG39 ~ SEG0									
HE83137							PRT17		PRT15		PRT14		SEG15 ~ SEG0			
HE83141	PRT14		SEG55 ~ SEG0													
HE83R141	PRT14		SEG55 ~ SEG0													
HE83142	PRT14		SEG55 ~ SEG0													
HE83R142	PRT14		SEG55 ~ SEG0													
HE83144	PRT15		PRT14		SEG48 ~ SEG0											
HE83145	PRT15		PRT14		SEG48 ~ SEG0											
HE83146	PRT15		PRT14		SEG48 ~ SEG0											
HE83147	PRT15		PRT14		SEG48 ~ SEG0											
HE83148	PRT15		PRT14		SEG48 ~ SEG0											

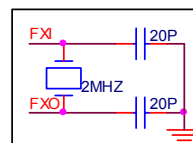
H. Application Circuit

Application circuit for HE83124, HE83R123 and HE83R125

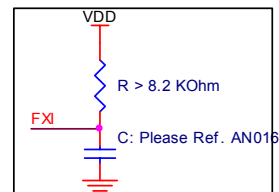


No External Parts is necessary if user adopt Internal Fast RC Clock

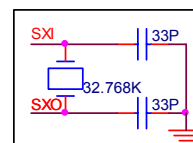
External Fast Clock:
Crystal osc.



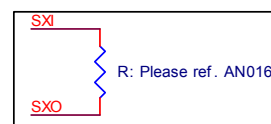
External Fast Clock:
RC osc.



External Slow Clock:
Crystal osc.



External Slow Clock:
RC osc.

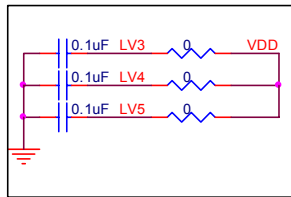


VDD	1		2	GND
VPP	3		4	LOADER
SDO	5		6	SDI
SCLK	7		8	D CN
R WN	9		10	P SN

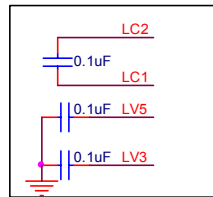
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Application circuit for HE83120, HE83121, HE83122, HE83123, HE83130, HE83131, HE83134, HE83135, HE83136, HE83137, HE83141, HE83R141, HE83142, HE83144, HE83145, HE83146, HE83147, HE83148

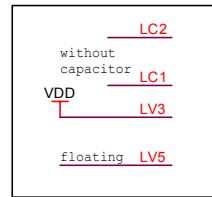
General design for different LCD Charge Pump



Three times Charge Pump is selected
LCD Max. Voltage=LV3=3/2*VDD

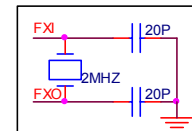


Three times Charge Pump is selected
LCD Max. Voltage=LV3=VDD

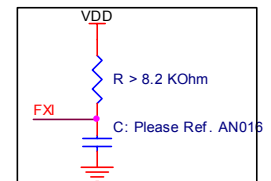


No External Parts is necessary if user adopt Internal Fast RC Clock

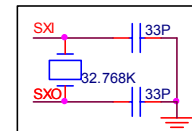
External Fast Clock: Crystal osc.



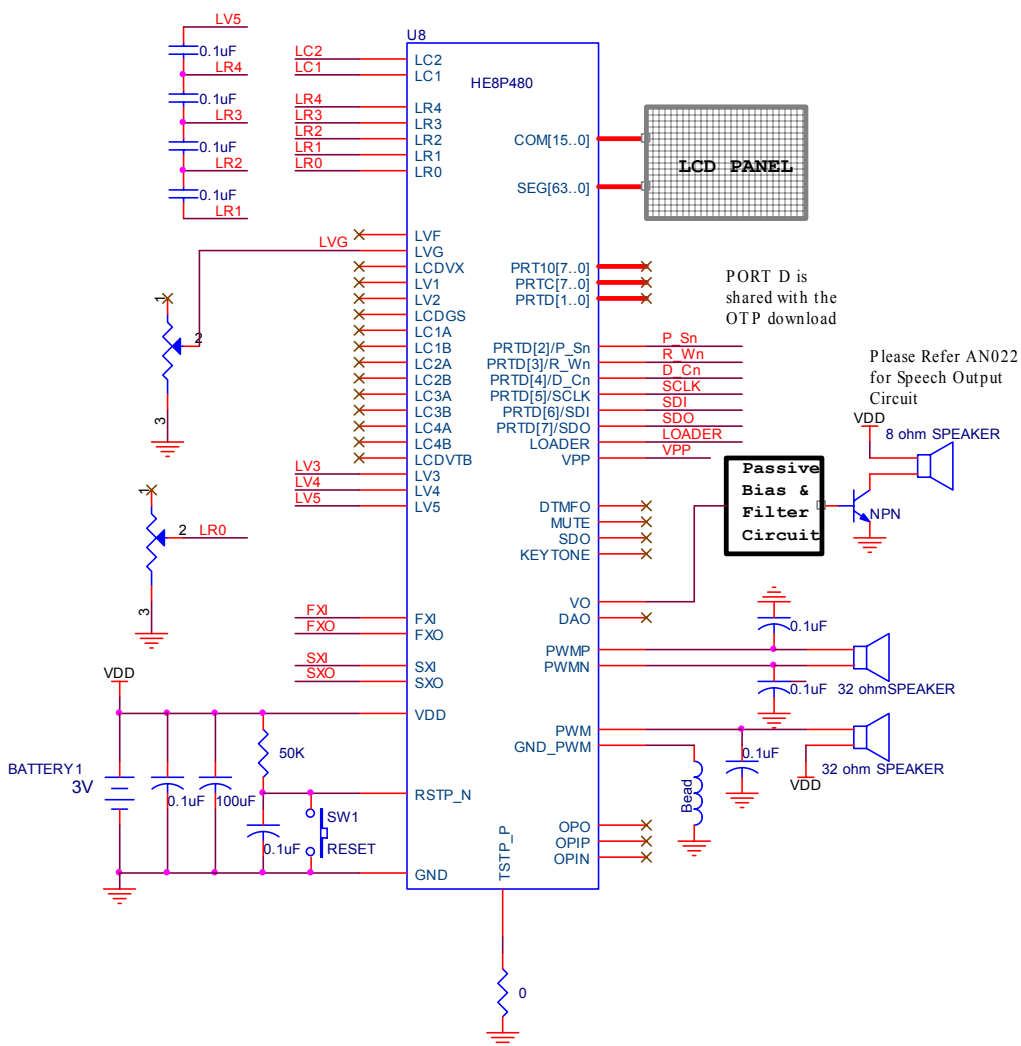
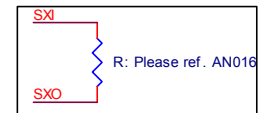
External Fast Clock: RC osc.



External Slow Clock: Crystal osc.



External Slow Clock: RC osc.

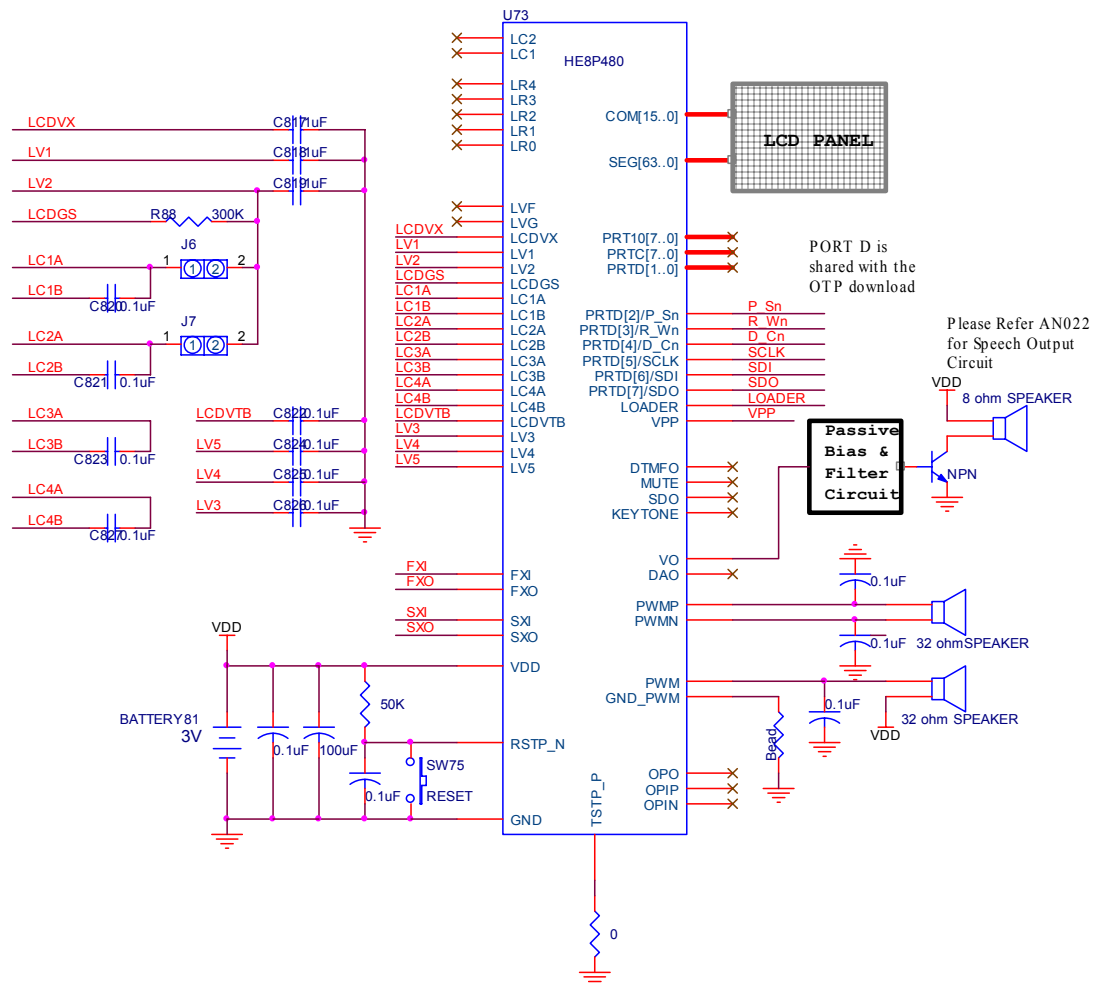


VDD (5V)	1	2	GND
VPP (12V)	3	4	LOADER
SDO	5	6	SDI
SCLK	7	8	D CN
R WN	9	10	P SN

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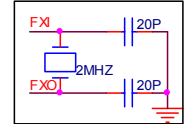


Application circuit for 4G LCD Driver

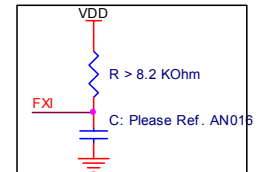


No External Parts is necessary if user adopt Internal Fast RC Clock

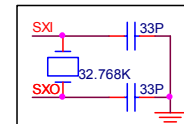
External Fast Clock: Crystal osc.



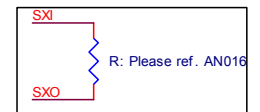
External Fast Clock: RC osc.



External Slow Clock: Crystal osc.



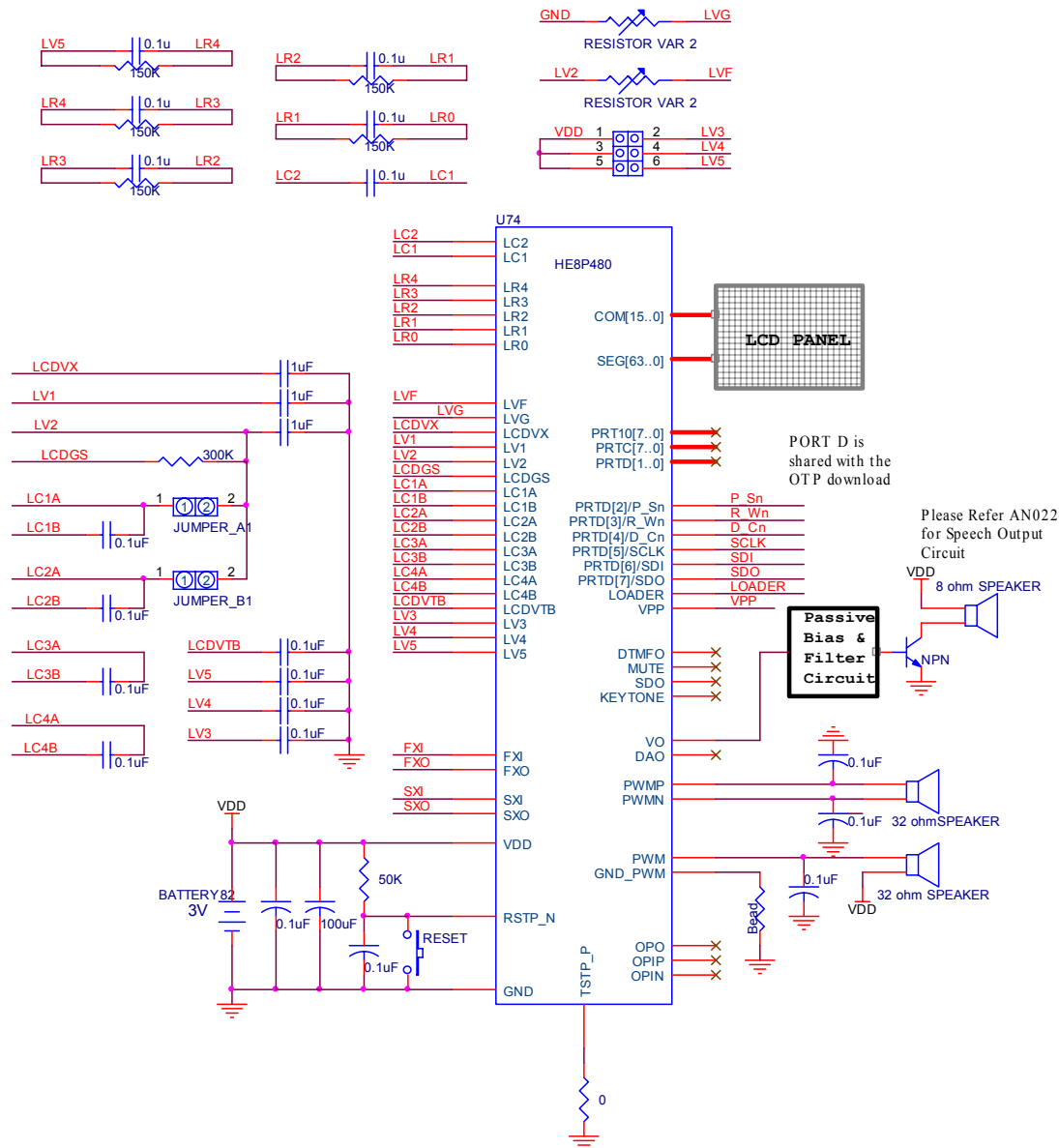
External Slow Clock: RC osc.



VDD (5V)	1	2	GND
VPP (12V)	3	4	LOADER
SDO	5	6	SDI
SCLK	7	8	D CN
R WN	9	10	P SN

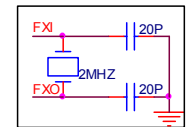
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Application circuit for general LCD design

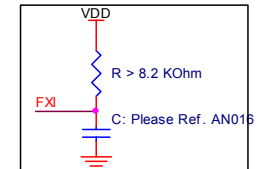


No External Parts is necessary if user adopt Internal Fast RC Clock

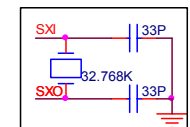
External Fast Clock: Crystal osc.



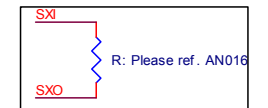
External Fast Clock: RC osc.



External Slow Clock: Crystal osc.



External Slow Clock: RC osc.

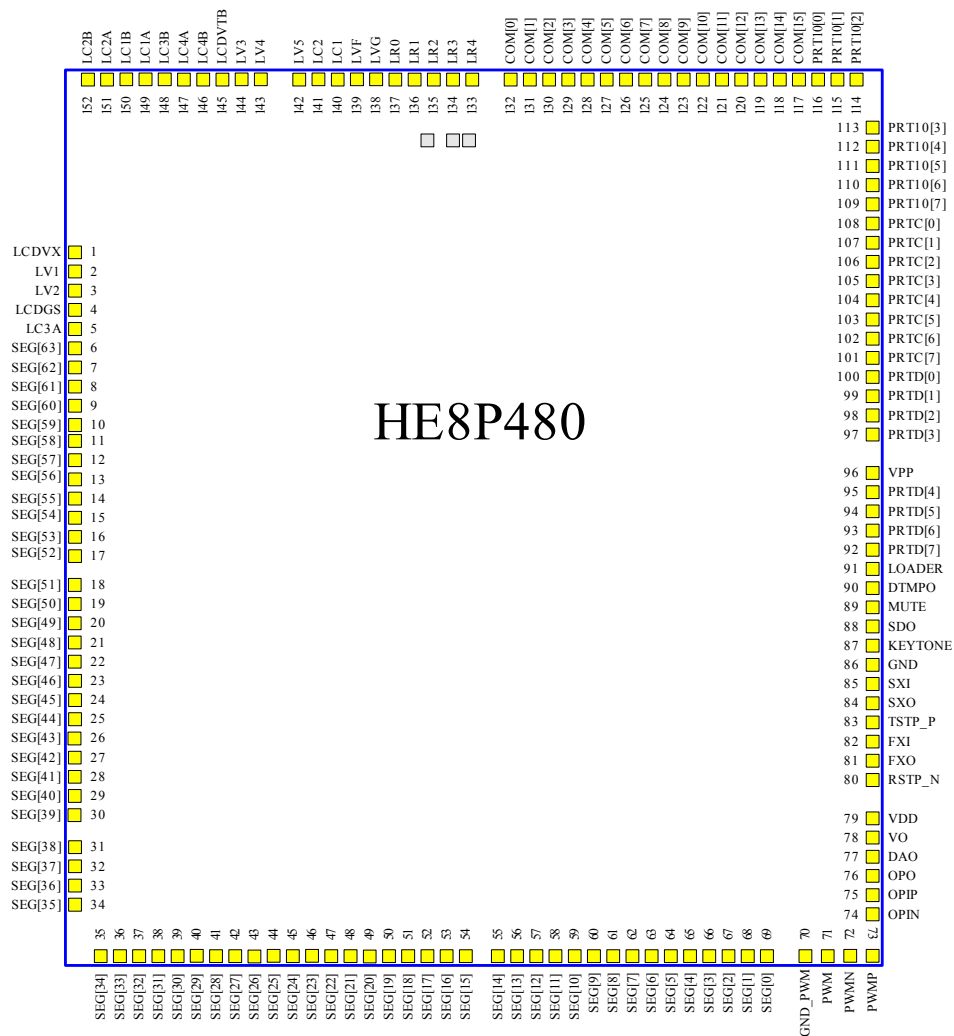


VDD (5V)	1	2	GND
VPP (12V)	3	4	LOADER
SDO	5	6	SDI
SCLK	7	8	D_CN
R_WN	9	10	P_SN

OTP Series Download



I. Pin Diagram





J. Bonding Pad Location

PIN No.	PIN Name	X Coordinate	Y Coordinate	PIN No.	PIN Name	X Coordinate	Y Coordinate
1	LCDVX	X=-2527.10	Y= 1833.95	77	DAO	X= 2528.80	Y=-2169.85
2	LV1	X=-2527.10	Y= 1715.90	78	VO	X= 2528.80	Y=-2054.85
3	LV2	X=-2527.10	Y= 1597.85	79	VDD	X= 2528.80	Y=-1936.80
4	LCDGS	X=-2527.10	Y= 1479.80	80	RSTP_N	X= 2528.80	Y=-1689.50
5	LC3A	X=-2527.10	Y= 1361.75	81	FXO	X= 2528.80	Y=-1571.45
6	SEG[63]	X=-2527.10	Y= 1246.75	82	FXI	X= 2528.80	Y=-1450.65
7	SEG[62]	X=-2527.10	Y= 1125.55	83	TSTP_P	X= 2528.80	Y=-1332.60
8	SEG[61]	X=-2527.10	Y= 1004.35	84	SXO	X= 2528.80	Y=-1214.55
9	SEG[60]	X=-2527.10	Y= 883.15	85	SXI	X= 2528.80	Y=-1096.50
10	SEG[59]	X=-2527.10	Y= 761.95	86	GND	X= 2528.80	Y= -978.45
11	SEG[58]	X=-2527.10	Y= 640.75	87	KEYTONE	X= 2528.80	Y= -857.65
12	SEG[57]	X=-2527.10	Y= 519.55	88	SDO	X= 2528.80	Y= -736.85
13	SEG[56]	X=-2527.10	Y= 398.35	89	MUTE	X= 2528.80	Y= -616.05
14	SEG[55]	X=-2527.10	Y= 277.15	90	DTMFO	X= 2528.80	Y= -498.00
15	SEG[54]	X=-2527.10	Y= 155.95	91	LOADER	X= 2528.80	Y= -379.95
16	SEG[53]	X=-2527.10	Y= 34.75	92	PRTD[7]	X= 2528.80	Y= -263.60
17	SEG[52]	X=-2527.10	Y= -215.70	93	PRTD[6]	X= 2528.80	Y= -141.35
18	SEG[51]	X=-2527.10	Y= -336.90	94	PRTD[5]	X= 2528.80	Y= -19.10
19	SEG[50]	X=-2527.10	Y= -458.10	95	PRTD[4]	X= 2528.80	Y= 103.15
20	SEG[49]	X=-2527.10	Y= -579.30	96	VPP	X= 2528.80	Y= 232.75
21	SEG[48]	X=-2527.10	Y= -700.50	97	PRTD[3]	X= 2528.80	Y= 490.15
22	SEG[47]	X=-2527.10	Y= -822.70	98	PRTD[2]	X= 2528.80	Y= 612.40
23	SEG[46]	X=-2527.10	Y= -943.90	99	PRTD[1]	X= 2528.80	Y= 734.65
24	SEG[45]	X=-2527.10	Y=-1063.00	100	PRTD[0]	X= 2528.80	Y= 856.90
25	SEG[44]	X=-2527.10	Y=-1182.10	101	PRTC[7]	X= 2528.80	Y= 979.15
26	SEG[43]	X=-2527.10	Y=-1301.20	102	PRTC[6]	X= 2528.80	Y= 1101.40
27	SEG[42]	X=-2527.10	Y=-1420.30	103	PRTC[5]	X= 2528.80	Y= 1223.65
28	SEG[41]	X=-2527.10	Y=-1539.40	104	PRTC[4]	X= 2528.80	Y= 1345.90
29	SEG[40]	X=-2527.10	Y=-1658.50	105	PRTC[3]	X= 2528.80	Y= 1468.15
30	SEG[39]	X=-2527.10	Y=-1903.75	106	PRTC[2]	X= 2528.80	Y= 1590.40

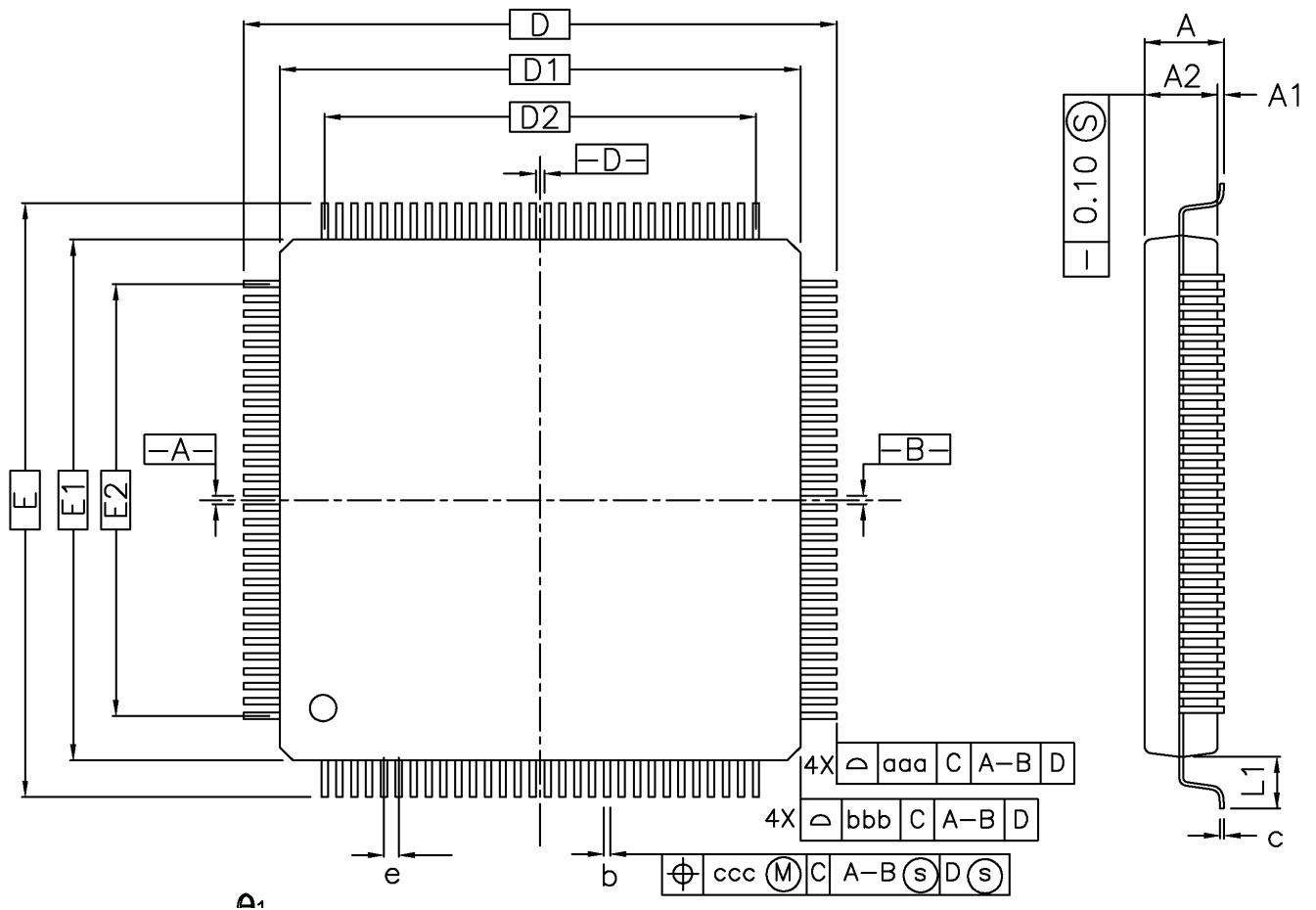


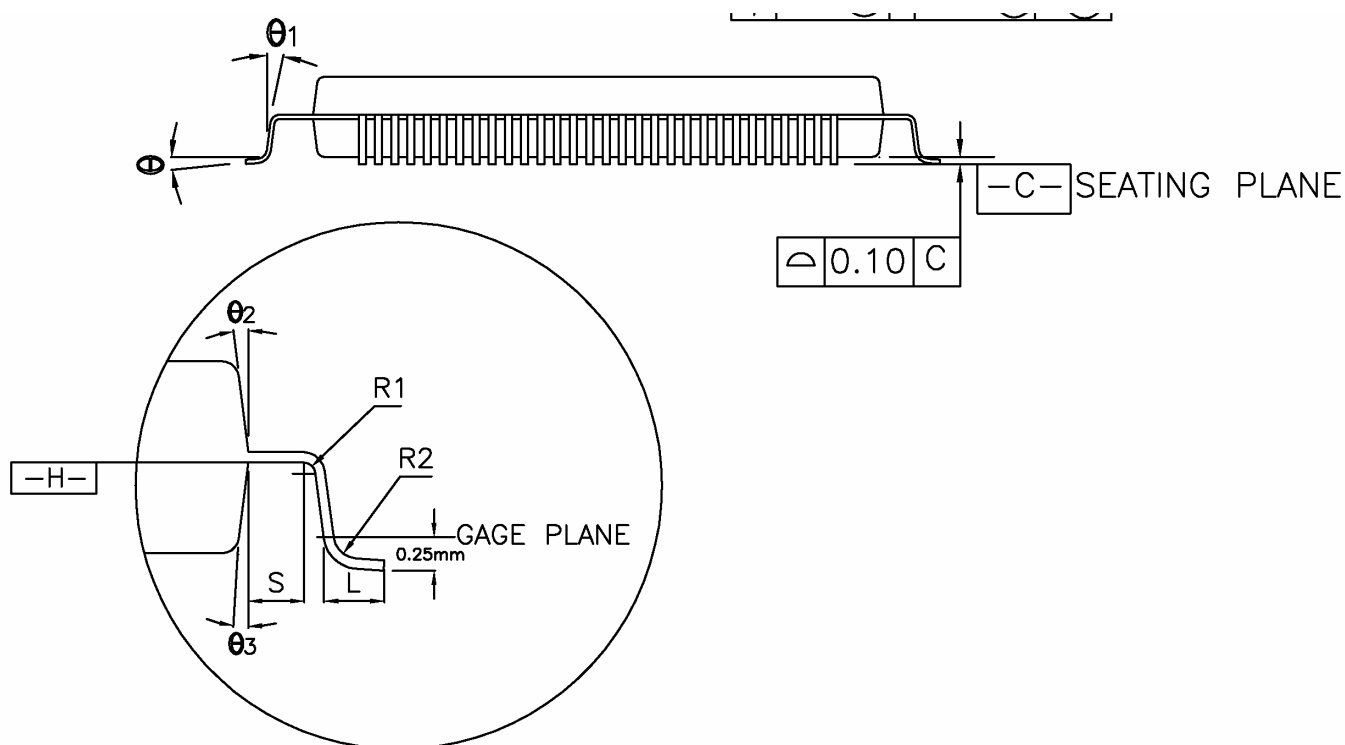
PIN No.	PIN Name	X Coordinate	Y Coordinate	PIN No.	PIN Name	X Coordinate	Y Coordinate
31	SEG[38]	X=-2527.10	Y=-2024.95	107	PRTC[1]	X= 2528.80	Y= 1712.65
32	SEG[37]	X=-2527.10	Y=-2146.15	108	PRTC[0]	X= 2528.80	Y= 1834.90
33	SEG[36]	X=-2527.10	Y=-2267.35	109	PRT10[7]	X= 2528.80	Y= 1961.60
34	SEG[35]	X=-2527.10	Y=-2388.55	110	PRT10[6]	X= 2528.80	Y= 2082.40
35	SEG[34]	X=-2413.90	Y=-2886.00	111	PRT10[5]	X= 2528.80	Y= 2203.20
36	SEG[33]	X=-2292.70	Y=-2886.00	112	PRT10[4]	X= 2528.80	Y= 2324.00
37	SEG[32]	X=-2171.50	Y=-2886.00	113	PRT10[3]	X= 2528.80	Y= 2444.80
38	SEG[31]	X=-2050.30	Y=-2886.00	114	PRT10[2]	X= 2356.15	Y= 2887.40
39	SEG[30]	X=-1929.10	Y=-2886.00	115	PRT10[1]	X= 2235.35	Y= 2887.40
40	SEG[29]	X=-1807.90	Y=-2886.00	116	PRT10[0]	X= 2114.55	Y= 2887.40
41	SEG[28]	X=-1686.70	Y=-2886.00	117	COM[15]	X= 1996.45	Y= 2887.40
42	SEG[27]	X=-1565.50	Y=-2886.00	118	COM[14]	X= 1877.35	Y= 2887.40
43	SEG[26]	X=-1444.30	Y=-2886.00	119	COM[13]	X= 1758.25	Y= 2887.40
44	SEG[25]	X=-1323.10	Y=-2886.00	120	COM[12]	X= 1639.15	Y= 2887.40
45	SEG[24]	X=-1201.90	Y=-2886.00	121	COM[11]	X= 1520.05	Y= 2887.40
46	SEG[23]	X=-1080.70	Y=-2886.00	122	COM[10]	X= 1400.95	Y= 2887.40
47	SEG[22]	X= -959.50	Y=-2886.00	123	COM[9]	X= 1281.85	Y= 2887.40
48	SEG[21]	X= -838.30	Y=-2886.00	124	COM[8]	X= 1162.75	Y= 2887.40
49	SEG[20]	X= -717.10	Y=-2886.00	125	COM[7]	X= 1043.65	Y= 2887.40
50	SEG[19]	X= -595.90	Y=-2886.00	126	COM[6]	X= 924.55	Y= 2887.40
51	SEG[18]	X= -474.70	Y=-2886.00	127	COM[5]	X= 805.45	Y= 2887.40
52	SEG[17]	X= -353.50	Y=-2886.00	128	COM[4]	X= 686.35	Y= 2887.40
53	SEG[16]	X= -232.30	Y=-2886.00	129	COM[3]	X= 567.25	Y= 2887.40
54	SEG[15]	X= -111.10	Y=-2886.00	130	COM[2]	X= 448.15	Y= 2887.40
55	SEG[14]	X= 139.35	Y=-2886.00	131	COM[1]	X= 329.05	Y= 2887.40
56	SEG[13]	X= 260.55	Y=-2886.00	132	COM[0]	X= 209.95	Y= 2887.40
57	SEG[12]	X= 381.75	Y=-2886.00	133	LR4	X= -38.35	Y= 2887.40
58	SEG[11]	X= 502.95	Y=-2886.00	134	LR3	X= -156.40	Y= 2887.40
59	SEG[10]	X= 624.15	Y=-2886.00	135	LR2	X= -274.45	Y= 2887.40
60	SEG[9]	X= 745.35	Y=-2886.00	136	LR1	X= -392.50	Y= 2887.40
61	SEG[8]	X= 866.55	Y=-2886.00	137	LR0	X= -510.55	Y= 2887.40
62	SEG[7]	X= 982.55	Y=-2886.00	138	LVG	X= -628.60	Y= 2887.40
63	SEG[6]	X= 1101.65	Y=-2886.00	139	LVF	X= -746.65	Y= 2887.40



PIN No.	PIN Name	X Coordinate	Y Coordinate	PIN No.	PIN Name	X Coordinate	Y Coordinate
64	SEG[5]	X= 1220.75	Y=-2886.00	140	LC1	X= -864.70	Y= 2887.40
65	SEG[4]	X= 1339.85	Y=-2886.00	141	LC2	X= -982.75	Y= 2887.40
66	SEG[3]	X= 1458.95	Y=-2886.00	142	LV5	X=-1100.80	Y= 2887.40
67	SEG[2]	X= 1578.05	Y=-2886.00	143	LV4	X=-1348.10	Y= 2887.40
68	SEG[1]	X= 1697.15	Y=-2886.00	144	LV3	X=-1466.15	Y= 2887.40
69	SEG[0]	X= 1816.25	Y=-2886.00	145	LCDVTB	X=-1584.20	Y= 2887.40
70	GND_PWM:G	X= 2101.25	Y=-2886.00	146	LC4B	X=-1702.25	Y= 2887.40
71	PWM	X= 2239.50	Y=-2886.00	147	LC4A	X=-1820.30	Y= 2887.40
72	PWMN	X= 2379.90	Y=-2886.00	148	LC3B	X=-1938.35	Y= 2887.40
73	PWMP	X= 2502.55	Y=-2886.00	149	LC1A	X=-2056.40	Y= 2887.40
74	OPIN	X= 2528.80	Y=-2520.95	150	LC1B	X=-2174.45	Y= 2887.40
75	OPIP	X= 2528.80	Y=-2402.90	151	LC2A	X=-2292.50	Y= 2887.40
76	OPO	X= 2528.80	Y=-2284.85	152	LC2B	X=-2410.55	Y= 2887.40

K. Package – QFP160





SYMBOL	MILLIMETER			INCH		
	MIN.	NOR.	MAX.	MIN.	NOR.	MAX.
A	--	--	4.07	--	--	0.160
A ₁	0.15	0.25	0.35	0.006	0.010	0.014
A ₂	3.17	3.32	3.67	0.125	0.131	0.144
D	31.90 BASIC			1.256 BASIC		
D ₁	28.00 BASIC			1.102 BASIC		
E	31.90 BASIC			1.256 BASIC		
E ₁	28.00 BASIC			1.102 BASIC		
R ₂	0.13	--	0.30	0.005	--	0.012
R ₁	0.13	--	0.30	0.005	--	--
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	--	--	0°	--	--
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L ₁	1.95 REF			0.077 REF		
S	0.40	--	--	0.016	--	--
b	0.22	0.30	0.38	0.009	0.012	0.015



e	0.65 BASIC	0.026 BASIC
D ₂	25.35	0.998
E ₂	25.35	0.998
TOLERANCES OF FORM AND POSITION		
aaa	0.25	0.010
bbb	0.20	0.008
ccc	0.13	0.005



Pins Definition of QFP 160 Package

PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name	PIN Number	PIN Name
1	N.C.	41	N.C.	81	OPIN	121	N.C.
2	N.C.	42	SEG[34]	82	OPIP	122	PRT10[2]
3	N.C.	43	SEG[33]	83	OPO	123	PRT10[1]
4	N.C.	44	SEG[32]	84	DAO	124	PRT10[0]
5	N.C.	45	SEG[31]	85	VO	125	COM[15]
6	N.C.	46	SEG[30]	86	VDD	126	COM[14]
7	LCDVX	47	SEG[29]	87	RSTP_N	127	COM[13]
8	LV1	48	SEG[28]	88	FXO	128	COM[12]
9	LV2	49	SEG[27]	89	FXI	129	COM[11]
10	LCDGS	50	SEG[26]	90	TSTP_P	130	COM[10]
11	LC3A	51	SEG[25]	91	SXO	131	COM[9]
12	SEG[63]	52	SEG[24]	92	SXI	132	COM[8]
13	SEG[62]	53	SEG[23]	93	GND	133	COM[7]
14	SEG[61]	54	SEG[22]	94	KEYTONE	134	COM[6]
15	SEG[60]	55	SEG[21]	95	SDO	135	COM[5]
16	SEG[59]	56	SEG[20]	96	MUTE	136	COM[4]
17	SEG[58]	57	SEG[19]	97	DTMFO	137	COM[3]
18	SEG[57]	58	SEG[18]	98	LOADER	138	COM[2]
19	SEG[56]	59	SEG[17]	99	PRTD[7]	139	COM[1]
20	SEG[55]	60	SEG[16]	100	PRTD[6]	140	COM[0]
21	SEG[54]	61	SEG[15]	101	PRTD[5]	141	LR4
22	SEG[53]	62	SEG[14]	102	PRTD[4]	142	LR3
23	SEG[52]	63	SEG[13]	103	VPP	143	LR2
24	SEG[51]	64	SEG[12]	104	PRTD[3]	144	LR1
25	SEG[50]	65	SEG[11]	105	PRTD[2]	145	LR0
26	SEG[49]	66	SEG[10]	106	PRTD[1]	146	LVG
27	SEG[48]	67	SEG[9]	107	PRTD[0]	147	LVF
28	SEG[47]	68	SEG[8]	108	PRTC[7]	148	LC1
29	SEG[46]	69	SEG[7]	109	PRTC[6]	149	LC2
30	SEG[45]	70	SEG[6]	110	PRTC[5]	150	LV5
31	SEG[44]	71	SEG[5]	111	PRTC[4]	151	LV4
32	SEG[43]	72	SEG[4]	112	PRTC[3]	152	LV3
33	SEG[42]	73	SEG[3]	113	PRTC[2]	153	LCDVTB
34	SEG[41]	74	SEG[2]	114	PRTC[1]	154	LC4B
35	SEG[40]	75	SEG[1]	115	PRTC[0]	155	LC4A
36	SEG[39]	76	SEG[0]	116	PRT10[7]	156	LC3B
37	SEG[38]	77	GND_PWM:G	117	PRT10[6]	157	LC1A
38	SEG[37]	78	PWM	118	PRT10[5]	158	LC1B
39	SEG[36]	79	PWMN	119	PRT10[4]	159	LC2A
40	SEG[35]	80	PWMP	120	PRT10[3]	160	LC2B

N.C. : No connection



L. DC/AC Characteristics

Absolute Maximum Rating

Item	Symbol	Rating	Condition
Supply Voltage	V_{dd}	$-0.5V \sim 8V$	
Input Voltage	V_{in}	$-0.5V \sim V_{dd}+0.5V$	
Output Voltage	V_o	$-0.5V \sim V_{dd}+0.5V$	
Operating Temperature	T_{op}	$0^{\circ}C \sim 70^{\circ}C$	
Storage Temperature	T_{st}	$-50^{\circ}C \sim 100^{\circ}C$	

Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	$2.4V \sim 5.5V$	
Input Voltage	V_{ih}	$0.9 V_{dd} \sim V_{dd}$	
	V_{il}	$0.0V \sim 0.1 V_{dd}$	
Operating Frequency	F_{max}	8 MHz	$V_{dd} = 5.0V$
		4 MHz	$V_{dd} = 2.4V$
Operating Temperature	T_{op}	$0^{\circ}C \sim 70^{\circ}C$	
Storage Temperature	T_{st}	$-50^{\circ}C \sim 100^{\circ}C$	



Testing condition: TEMP=25°C, VDD=3V±10%, GND=0V

SYM.	PARAMETER	ITEMS	CONDITION	MIN.	TYP.	MAX.	UNIT
I _{Fast}	NORMAL Mode Current	System	2M ext. R/C		0.75	1	mA
I _{Slow}	SLOW Mode Current	System	32.768K X'tal LCD Disable		6	9	μA
I _{Idle}	IDLE Mode Current	System	32.769K X'tal LCD Disable		4	7	μA
I _{LCD}	Extra Current if LCD ON	System	LCD Enable		2	3	μA
I _{Sleep}	Sleep Mode Current	System				1	μA
I _{PWM}	PWM Output Current	PWMP, PWMN*2	With 32Ω Loading	10	14		mA
			With 64Ω Loading	6	8		mA
			With 100Ω Loading	4	5		mA
I _{ovo}	DAC Output Current	VO	V _{DD} =3V; VO=0~2V, Data=7F	2.5	3		mA
V _{iH}	Input High Voltage	I/O pins		0.8V _{DD}			V
V _{iL}	Input Low Voltage	I/O pins				0.2V _{DD}	V
V _{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V _{DD} (input from low to high) Threshold=1/3V _{DD} (input from high to low)		1/3V _{DD}		V
I _{oH}	Output Drive Current	I/O pull-high*1	V _{oL} =2.0V	50			μA
I _{oL_1}	Output Sink Current	I/O pull-low*1	V _{oL} =0.4V	1.0			mA
I _{oL_2}	Output Sink Current	PRTD[3:0]	V _{oL} =0.4V	5.0			mA
I _{iL_1}	Input Low Current	RSTP_N	V _{iL} =GND, pull high Internally		20		μA
I _{iL_2}	Input Low Current	I/O	V _{iL} =GND, if pull high Internally by user		100		μA

Note: *1: Drive Current Specification ➔ for Push-Pull I/O port only

Sink Current Specification ➔ for both Push-Pull and Open-Drain I/O port.

*2: This Spec. bases on one driver only. There are five build-in drivers actually, so user can multiply the number of driver to obtain the necessary driver current to drive the speak.

(I_{PWM} * N; N=0, 1, 2, 3, 4, 5)



M. OTP Programming

User can use the EZ_writer to program the HE8P480 OTP ROM through the programming pins which are shared with I/O PRTD and the functions are described as below.

Pin Name	Function
VPP	Apply 12V to write the OTP ROM, and 5V to normal operation
LOADER	Used to program the OTP ROM
PRTD7/SDO	I/O port / WAKEUP / INT/ SDO: Series Data Output
PRTD6/SDI	I/O port / WAKEUP / INT/ SDI: Series Data Input
PRTD5/SCK	I/O port / WAKEUP / SCK: Series Clock
PRTD4/D_Cn	I/O port / WAKEUP /D_Cn: data or command
PRTD3/R_Wn	I/O port / WAKEUP /R_Wn: Read or Write
PRTD2/P_Sn	I/O port / WAKEUP /P_Sn: Parallel or Series

N. Application Note

When the HE8P480 is used to emulate the HE83R141 and HE83R142, the power consumption of HE8P480 will have about 100uA larger than the mask type HE83R141 and HE83R142 if the LCD display is turned on and the 1/5 bias + regulator are set in the mask option of HE8P480.

The HE8P480 can operate on 4MHz correctly only when the power supply is above 2.5V. and the mask type chip don't have this problem.



O. Updated Record

Version	Date	Original Content	New Content
1.0	2002/10/30	Original	
1.1	2002/11/07	Without LV3	Add a capacitor to LV3
1.11	2002/11/18	LVG and LR0	Remove the VDD which is tired to variable resistor.
1.12	2002/11/29		The SEG[15:8] of HE83R141 & HE83R142's exist
1.13	2003/03/26	HE83124 SEG and I/O configuration.	HE83124 don't have SEG and I/O sharing.
1.14	2003/05/07	Page 12, 17 for HE83131, HE83135,6	HE83131 with LR0 and HE83135,6 with DAO