HY29F040A

4 Megabit (512K x 8), 5 Volt-only, Flash Memory

KEY FEATURES

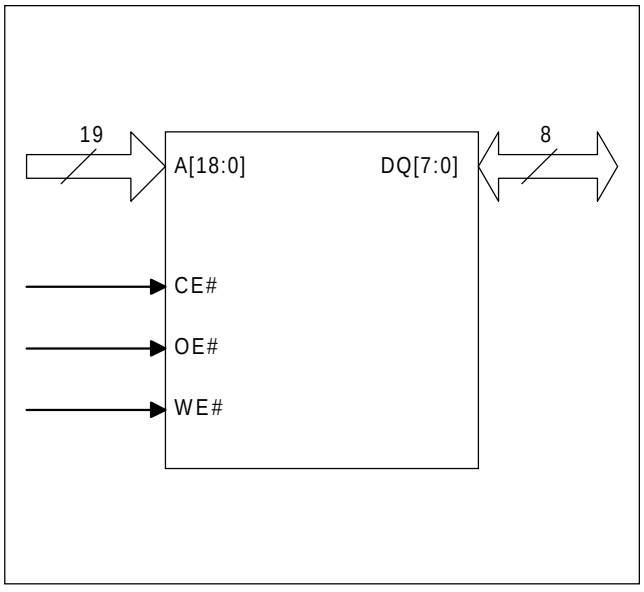
- **5 Volt Read, Program, and Erase**
  - Minimizes system-level power requirements
- **High Performance**
  - Access times as fast as 55 ns
- **Low Power Consumption**
  - 20 mA typical active read current
  - 30 mA typical program/erase current
  - 5 µA maximum CMOS standby current
- **Compatible with JEDEC Standards**
  - Package, pinout and command-set compatible with the single-supply Flash device standard
  - Provides superior inadvertent write protection
- **Sector Erase Architecture**
  - Eight equal size sectors of 64K bytes each
  - A command can erase any combination of sectors
  - Supports full chip erase
- **Erase Suspend/Resume**
  - Temporarily suspends a sector erase operation to allow data to be read from, or programmed into, any sector not being erased
- **Sector Protection**
  - Sectors may be locked to prevent program or erase operations within that sector
- **Automatic Erase Algorithm**
  - Erases a sector, any combination of sectors, or the entire chip
- **Automatic Programming Algorithm**
  - Programs and verifies data at a specified address
- **Fast Program and Erase Times**
  - Byte programming time: 7 µs typical
  - Sector erase time: 1.0 sec typical
  - Chip erase time: 8 sec typical
- **Data# Polling and Toggle Status Bits**
  - Provide software confirmation of completion of program or erase operations
- **Minimum 100,000 Program/Erase Cycles**
- **Space Efficient Packaging**
  - Available in industry-standard 32-pin TSOP and reverse TSOP and 32-pin PLCC packages

GENERAL DESCRIPTION

The HY29F040A is a 4 Megabit, 5 volt-only, CMOS Flash memory organized as 524,288 (512K) bytes of eight-bits each. The device is offered in industry-standard 32-pin TSOP and reverse TSOP and 32-pin PLCC packages.

The HY29F040A can be programmed and erased in-system with a single 5-volt V_{CC} supply. Internally generated and regulated voltages are provided for program and erase operations, so that the device does not require a high voltage power supply to perform those functions. The device can also be programmed in standard EPROM programmers. Access times as fast as 55 ns over the full operating voltage range of 5.0 volts ± 10% are offered for timing compatibility with the zero wait state requirements of high speed microprocessors.

LOGIC DIAGRAM



To eliminate bus contention, the HY29F040A has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device is compatible with the JEDEC single power-supply Flash command set standard. Commands are written to the command register using standard microprocessor write timings, from where they are routed to an internal state-machine that controls the erase and programming circuits. Device programming is performed a byte at a time by executing the four-cycle Program Command. This initiates an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

The HY29F040A's sector erase architecture allows any number of array sectors to be erased and reprogrammed without affecting the data contents of other sectors. Device erasure is initiated by executing the Erase Command. This initiates an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase cycles, the device automatically times the erase pulse widths and verifies proper cell margin.

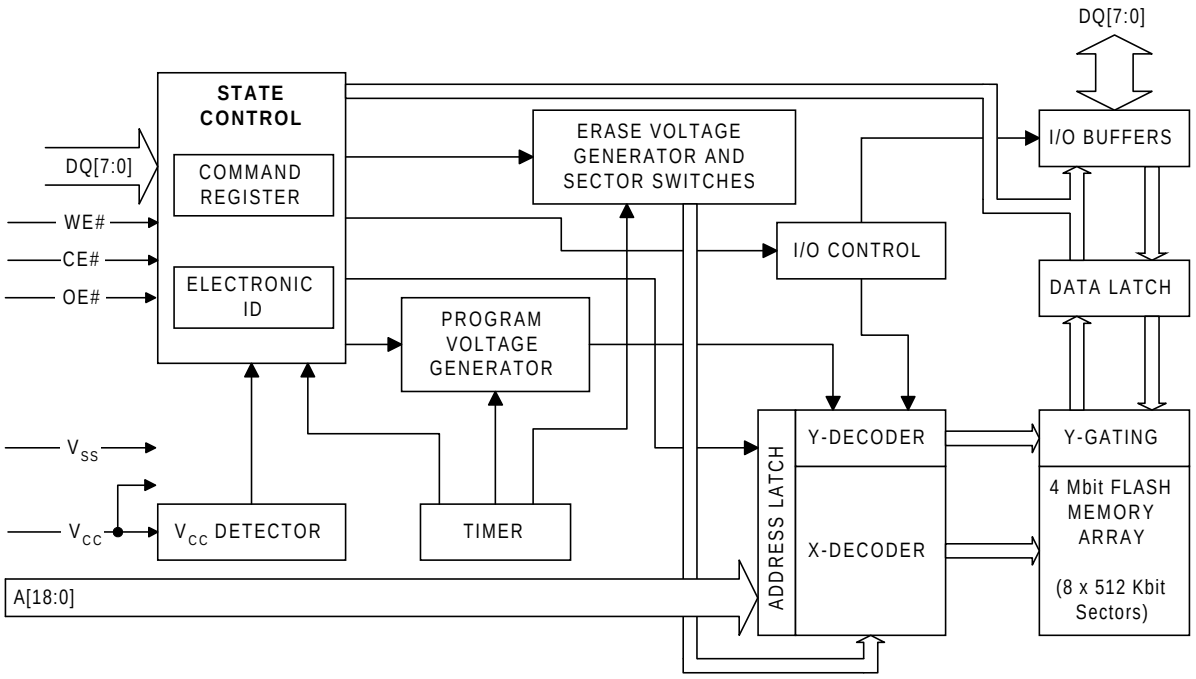
To protect data in the device from accidental or unauthorized attempts to program or erase the device while it is in the system (e.g., by a virus), the device has a Sector Protect function that hardware write protects selected sectors. The sector protect and unprotect features require high voltage and are typically enabled in a PROM programmer. .

Erase Suspend enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. The device is fully erased when shipped from the factory.

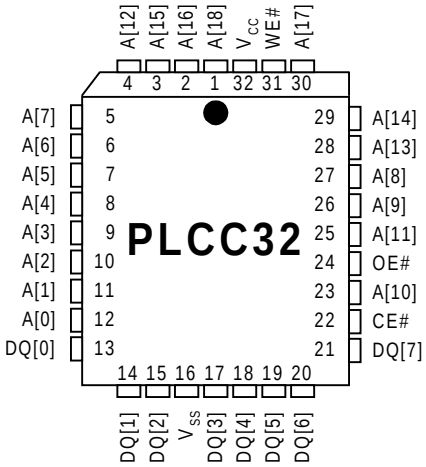
Addresses and data needed for the programming and erase operations are internally latched during write cycles, and the host system can detect completion of a program or erase operation by reading the DQ[7] (Data# Polling) and DQ[6] (toggle) status bits. Reading data from the device is similar to reading from SRAM or EPROM devices. Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions.

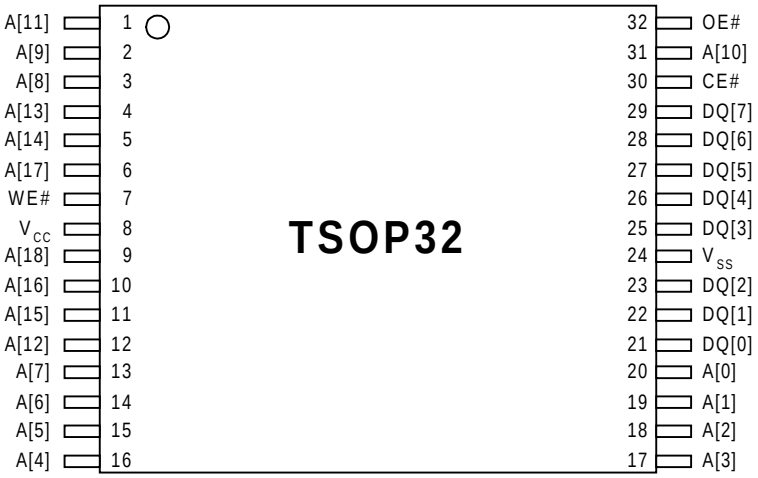
The host can place the device into the standby mode. Power consumption is greatly reduced in this mode.

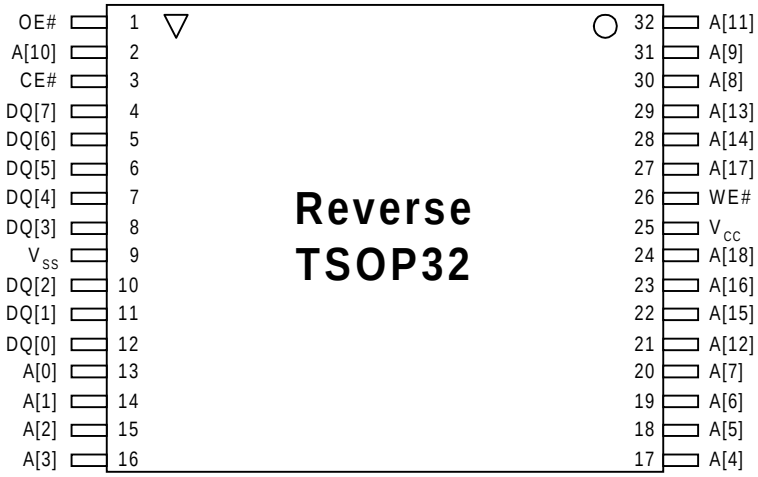
BLOCK DIAGRAM



PIN CONFIGURATIONS







CONVENTIONS

Unless otherwise noted, a positive logic (active High) convention is assumed throughout this document, whereby the presence at a pin of a higher, more positive voltage (nominally 5VDC) causes assertion of the signal. A '#' symbol following the signal name, e.g., WE#, indicates that the signal is asserted in a Low state (nominally 0 volts).

Whenever a signal is separated into numbered bits, e.g., DQ[7], DQ[6], ..., DQ[0], the family of bits may also be shown collectively, e.g., as DQ[7:0].

The designation 0xNNNN (N = 0, 1, 2, . . . , 9, A, . . . , E, F) indicates a number expressed in hexadecimal notation. The designation 0bXXXX indicates a number expressed in binary notation (X = 0, 1).

SIGNAL DESCRIPTIONS

Name	Type	Description
A[18:0]	Inputs	**Address, active High.** These nineteen inputs select one of 524,2886 512K) bytes within the array for read or write operations. A[18] is the MSB and A[0] is the LSB.
DQ[7:0]	Inputs/Outputs Tri-state	**Data Bus, active High**. These pins provide an 8-bit data path for read and write operations.
CE#	Input	**Chip Enable, active Low.** This input must be asserted to read data from or write data to the HY29F040A. When High, the data bus is tri-stated and the device is placed in the Standby mode.
OE#	Input	**Output Enable, active Low**. This input must be asserted for read operations and negated for write operations. When High, data outputs from the device are disabled and the data bus pins are placed in the high impedance state.
WE#	Input	**Write Enable, active Low.** Controls writing of commands or command sequences in order to program data or erase sectors of the memory array. A write operation takes place when WE# is asserted while CE# is Low and OE# is High.
V_{CC}	--	**5-volt power supply.**
V_{SS}	--	**Power and signal ground.**

Table 1. HY29F040A Memory Array Organization [1]

Sector	Sector Address			Address Range A[18:0]
	A[18]	A[17]	A[16]	
S0	0	0	0	0x00000 - 0x0FFFF
S1	0	0	1	0x10000 - 0x1FFFF
S2	0	1	0	0x20000 - 0x2FFFF
S3	0	1	1	0x30000 - 0x3FFFF
S4	1	0	0	0x40000 - 0x4FFFF
S5	1	0	1	0x50000 - 0x5FFFF
S6	1	1	0	0x60000 - 0x6FFFF
S7	1	1	1	0x70000 - 0x7FFFF

Notes:
1. All sectors are 64 KBytes in size.

MEMORY ARRAY ORGANIZATION

The 512 KByte Flash memory array is organized into eight 64 KByte blocks called *sectors* (S0, S1, . . . , S7). A sector is the smallest unit that can be erased. It is also the smallest unit that can be protected to prevent accidental or unauthorized erasure. See 'Bus Operations' and 'Command Definitions' sections of this document for additional information on these functions.

BUS OPERATIONS

Device bus operations are initiated through the internal command register, which consists of sets of latches that store the commands, along with the address and data information, if any, needed to execute the specific command. The command register itself does not occupy any addressable memory location. The contents of the command register serve as inputs to an internal state machine whose outputs control the operation of the device. Table 2 lists the normal bus operations, the inputs and control levels they require, and the resulting outputs. Certain bus operations require a high voltage on one or more device pins. Those are described in Table 3.

Read Operation

Data is read from the HY29F040A by using standard microprocessor read cycles while placing the address of the byte to be read on the device's address inputs, A[18:0]. The host system must drive the CE# and OE# inputs Low and drive WE# High for a valid read operation to take place. The device outputs the specified array data on DQ[7:0].

The HY29F040A is automatically set for reading array data after device power-up to ensure that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data, and the device remains enabled for read accesses until the command register contents are altered.

Table 2. HY29F040A Normal Bus Operations [1]

Operation	CE#	OE#	WE#	A[18:0]	DQ[7:0]
Read	L	L	H	A_{IN}	D_{OUT}
Write	L	H	L	A_{IN}	D_{IN}
Output Disable	L	H	H	X	High-Z
TTL Standby	H	X	X	X	High-Z
CMOS Standby	V_{CC} ± 0.5V	X	X	X	High-Z

Notes:
1. L = V_{IL}, H = V_{IH}, X = Don't Care, D_{OUT} = Data Out, D_{IN} = Data In. See DC Characteristics for voltage levels.

Table 3. HY29F040A Bus Operations Requiring High Voltage [1, 2]

Operation [3]	CE#	OE#	WE#	A[18:16]	A[9]	A[6]	A[1]	A[0]	DQ[7:0]
Sector Protect	L	V_{ID}	X	SA [4]	V_{ID}	X	X	X	X
Sector Unprotect	V_{ID}	V_{ID}	X	X	V_{ID}	X	X	X	X
Manufacturer Code	L	L	H	X	V_{ID}	L	L	L	Hynix = 0xAD
Device Code	L	L	H	X	V_{ID}	L	L	H	HY29F040A = 0xA4
Sector Protection Verification	L	L	H	SA [4]	V_{ID}	L	H	L	0x00 = Unprotected
									0x01 = Protected

Notes:
1. L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels.
2. Address bits not specified are Don't Care.
3. See text for additional information.
4. SA = sector address. See Table 1.

This device features an Erase Suspend mode. While in this mode, the host may read the array data from any sector of memory that is not marked for erasure. If the host attempts to read from an address within an erase-suspended sector, or while the device is performing an erase or byte program operation, the device outputs status data instead of array data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exceptions noted above. After completing an internal program or internal erase algorithm, the HY29F040A automatically returns to the read array data mode.

The host must issue the software reset command (see Command Definitions) to return a sector to the read array data mode if DQ[5] goes high during a program or erase cycle, or to return the device to the read array data mode while it is in the Electronic ID mode.

Write Operation

Certain operations, including programming data and erasing sectors of memory, require the host to write a command or command sequence to the HY29F040A. Writes to the device are performed by placing the byte address on the device's address inputs while the data to be written is input on DQ[7:0]. The host system must drive the CE# and WE# pins Low and drive OE# High for a valid write operation to take place. All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first.

The 'Device Commands' section of this document provides details on the specific device commands implemented in the HY29F040A.

Output Disable Operation

When the OE# input is at V_{IH}, output data from the device is disabled and the data bus pins are placed in the high impedance state.

Standby Operation

When the system is not reading from or writing to the HY29F040A, it can place the device in the Standby mode. In this mode, current consumption is greatly reduced, and the data bus outputs are placed in the high impedance state, independent of the OE# input.

The device enters the *CE# CMOS Standby* mode if the CE# pin is held at V_{CC} ± 0.5V. Note that this is a more restricted voltage range than V_{IH}. If CE# is held High (V_{IH}), but not within V_{CC} ± 0.5V, the device will be in the *CE# TTL Standby* mode, but the standby current will be greater.

The device requires standard access time (t_{CE}) for read access when the device is in the standby mode, before it is ready to read data. If the device is deselected during erasure or programming, it continues to draw active current until the operation is completed.

Sector Protect/Unprotect Operations

Hardware sector protection can be invoked to disable program and erase operations in any single sector or combination of sectors. This function is typically used to protect data in the device from unauthorized or accidental attempts to program or erase the device while it is in the system (e.g., by a virus) and is implemented using programming equipment. Sector unprotection re-enables the program and erase operations in previously protected sectors.

Table 1 identifies the eight sectors and the address range that each covers. The device is shipped with all sectors unprotected.

The sector protect/unprotect operations require a high voltage (V_{ID}) on address pin A[9] and the CE# and/or OE# control pins, as detailed in Table 3. When implementing these operations, note that V_{CC} must be applied to the device before applying V_{ID}, and that V_{ID} should be removed before removing V_{CC} from the device.

The flow chart in Figure 1 illustrates the procedure for protecting sectors, and timing specifications and waveforms are shown in the specifications section of this document. Verification of protection is accomplished as described in the Electronic ID Mode section and shown in the flow chart.

The procedure for sector unprotection is illustrated in the flow chart in Figure 2, and timing specifications and waveforms are given at the end of this document. *Note that to unprotect any sector, all unprotected sectors must first be protected prior to the first unprotect write cycle.*

Electronic ID Mode Operation

The Electronic ID mode provides manufacturer and device identification and sector protection verification through identifier codes output on DQ[7:0]. This mode is intended primarily for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. The Electronic ID information can also be obtained by the host through a command sequence, as described in the Device Commands section.

Operation in the Electronic ID mode requires V_{ID} on pin A[9], with additional requirements for obtaining specific data items as listed in Table 2:

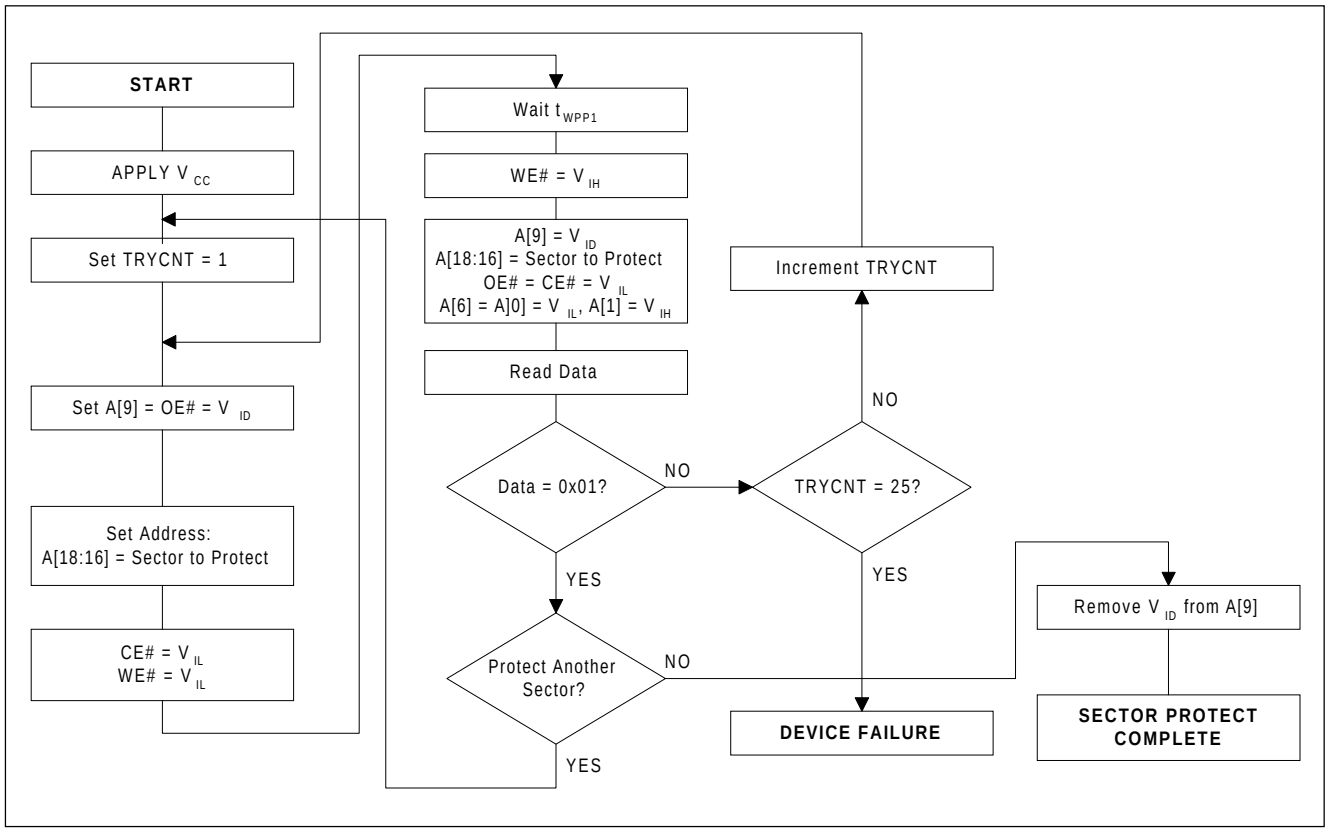


Figure 1. Sector Protect Procedure

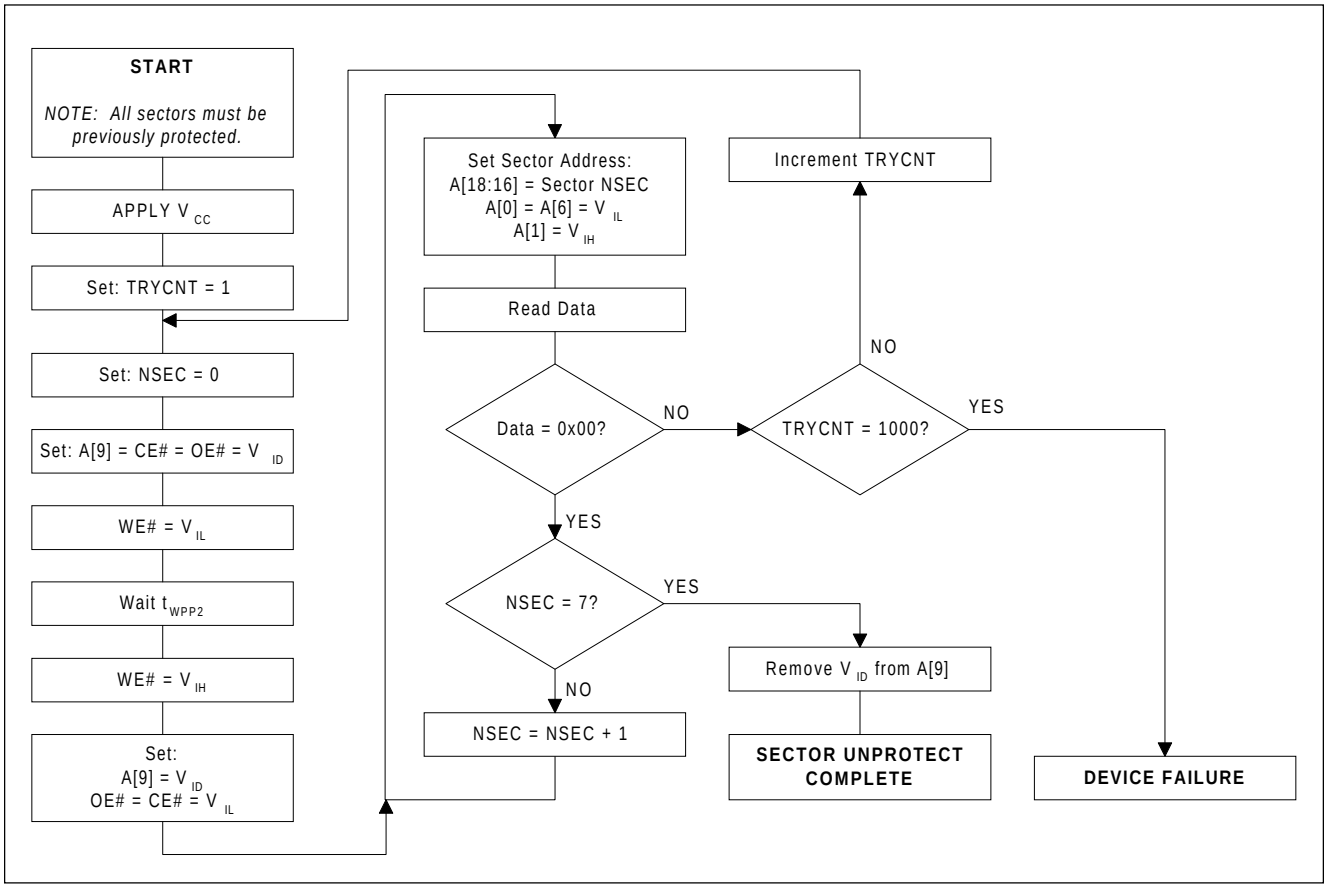


Figure 2. Sector Unprotect Procedure

- A read cycle at address 0xXXX00 retrieves the manufacturer code (Hynix = 0xAD).
- A read cycle at address 0xXXX01 returns the device code (HY29F040A = 0xA4).
- A read cycle containing a sector address (Table 1) in A[18:16] and the address 0x02 in A[7:0] returns 0x01 if that sector is protected, or 0x00 if it is unprotected.

DEVICE COMMANDS

Device operations are initiated by writing designated address and data *command sequences* into the device. A command sequence is composed of one, two or three of the following sub-segments: an *unlock cycle*, a *command cycle* and a *data cycle*. Table 4 summarizes the composition of the valid command sequences implemented in the HY29F040A, and these sequences are fully described in Table 5 and in the sections that follow.

Writing incorrect address and data values or writing them in the improper sequence resets the HY29F040A to the Read mode.

Table 4. Composition of Command Sequences

Command Sequence	Number of Bus Cycles		
	Unlock	Command	Data
Read/Reset 1	0	1	Note 1
Read/Reset 2	2	1	Note 1
Byte Program	2	1	1
Chip Erase	4	1	1
Sector Erase	4	1	1 (Note 2)
Erase Suspend	0	1	0
Erase Resume	0	1	0
Electronic ID	2	1	Note 3

Notes:
1. Any number of Flash array read cycles are permitted.
2. Additional data cycles may follow. See text.
3. Any number of Electronic ID read cycles are permitted.

Read/Reset 1, 2 Commands

The HY29F040A automatically enters the Read mode after device power-up and upon the completion of certain commands. Read/Reset commands are not required to retrieve data in these cases.

A Read/Reset command must be issued in order to read array data in the following cases:

- If the device is in the Electronic ID mode, a Read/ Reset command must be written to return to the Read mode. If the device was in the Erase Suspend mode when the device entered the Electronic ID mode, writing the Read/Reset command returns the device to the Erase Suspend mode.

  Note: When in the Electronic ID bus operation mode, the device returns to the Read mode when V_{ID} is removed from the A[9] pin. The Read/Reset command is not required in this case.

- If DQ[5] (Exceeded Time Limit) goes High during a program or erase operation, writing the Read/Reset command returns the sectors to the Read mode (or to the Erase Suspend mode if the device was in Erase Suspend).

The Read/Reset command may also be used to abort certain command sequences:

- In a Sector Erase or Chip Erase command sequence, the Read/Reset command may be written at any time before erasing actually begins, including, for the Sector Erase command, between the cycles that specify the sectors to be erased (see Sector Erase command description). This aborts the command and resets the device to the Read mode. Once erasure begins, however, the device ignores Read/Reset commands until the operation is complete.
- In a Program command sequence, the Read/Reset command may be written between the sequence cycles before programming actually begins. This aborts the command and resets the device to the Read mode, or to the Erase Suspend mode if the Program command sequence is written while the device is in the Erase Suspend mode. Once programming begins, however, the device ignores Read/Reset commands until the operation is complete.
- The Read/Reset command may be written between the cycles in an Electronic ID command sequence to abort that command. As described above, once in the Electronic ID mode, the Read/ Reset command *must* be written to return to the Read mode.

Table 5. HY29F040A Command Sequences

Command Sequence		Write Cycles	Bus Cycles [1, 2, 3] First Add	First Data	Second Add	Second Data	Third Add	Third Data	Fourth Add	Fourth Data	Fifth Add	Fifth Data	Sixth Add	Sixth Data
Read/Reset 1 [6, 8]		1	XXX	F0	RA	RD								
Reset/Reset 2 [7, 8]		3	555	AA	2AA	55	555	F0	RA	RD				
Byte Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend [4]		1	XXX	B0										
Erase Resume [5]		1	XXX	30										
Electronic ID [7]	Manufacturer Code	3	555	AA	2AA	55	555	90	X00	AD				
	Device Code								X01	A4				
	Sector Protect Verify								SPVA	STAT				

Legend:

X = Don't Care
RA = Memory address of data to be read
RD = Data read from location RA during the read operation
STAT = Sector protect status: 0x00 = unprotected, 0x01 = protected.
PA = Address of the data to be programmed
PD = Data to be programmed at address PA
SA = Sector address of sector to be erased (see Note 3 and Table 1).
SPVA = Address of the sector to be verified (see Note 3 and Table 1).

Notes:

1. All values are in hexadecimal.
2. All bus cycles are write operations unless otherwise noted.
3. Address is A[10:0] and A[18:11] are don't care except as follows:
   - For RA and PA, A[18:11] are the upper address bits of the byte to be read or programmed.
   - For SA, A[18:16] are the address of the sector to be erased and A[15:0] are don't care.
   - For SPVA, A[18:16] are the address of the sector to be verified, A[7:0] = 0x02, all other address bits are don't care.
4. The Erase Suspend command is valid only during a sector erase operation. The system may read and program in non-erasing sectors, or enter the Electronic ID mode, while in the Erase Suspend mode.
5. The Erase Resume command is valid only during the Erase Suspend mode.
6. The second bus cycle is a read cycle.
7. The fourth bus cycle is a read cycle.
8. Either command sequence is valid. The command is required only to return to the Read mode when the device is in the Electronic ID command mode or if DQ[5] goes High during a program or erase operation. It is not required for normal read operations.

Byte Program Command

The host processor programs the device a byte at a time by issuing the Program command sequence shown in Table 5. The sequence begins by writing two unlock cycles, followed by the Program setup command and, lastly, a data cycle specifying the program address and data. This initiates the Automatic Programming algorithm, which provides internally generated program pulses and verifies the programmed cell margin. The host is not required to provide further controls or timings during this operation. When the Automatic Programming algorithm is complete, the device returns to the Read mode. Several methods are provided to allow the host to determine the status of the programming operation, as described in the Write Operation Status section.

Commands written to the device during execution of the Automatic Programming algorithm are ignored.

Programming is allowed in any sequence. Only erase operations can convert a stored “0” to a “1”. Thus, a bit cannot be programmed from a “0” back to a “1”. Attempting to do so will set DQ[5] to “1”, and the Data# Polling algorithm will indicate that the operation was not successful. A Read/Reset command is required to exit this state, and a succeeding read will show that the data is still “0”.

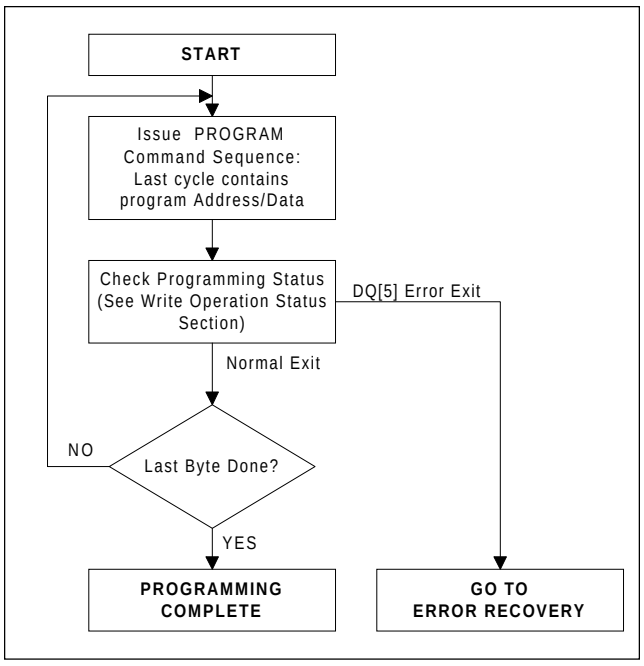


Figure 3. Programming Procedure

Figure 3 illustrates the procedure for the Program operation.

Chip Erase Command

The Chip Erase command sequence consists of two unlock cycles, followed by the erase command, two additional unlock cycles and then the chip erase data cycle. During chip erase, all sectors of the device are erased except protected sectors. The command sequence starts the Automatic Erase algorithm, which preprograms and verifies the entire memory, except for protected sector groups, for an all zero data pattern prior to electrical erase. The device then provides the required number of internally generated erase pulses and verifies cell erasure within the proper cell margins. The host system is not required to provide any controls or timings during these operations.

Commands written to the device during execution of the Automatic Erase algorithm are ignored.

When the Automatic Erase algorithm is finished, the device returns to the Read mode. Several methods are provided to allow the host to determine the status of the erase operation, as described in the Write Operation Status section.

Figure 4 illustrates the Chip Erase procedure.

Sector Erase Command

The Sector Erase command sequence consists of two unlock cycles, followed by the erase command, two additional unlock cycles and then the sector erase data cycle, which specifies which

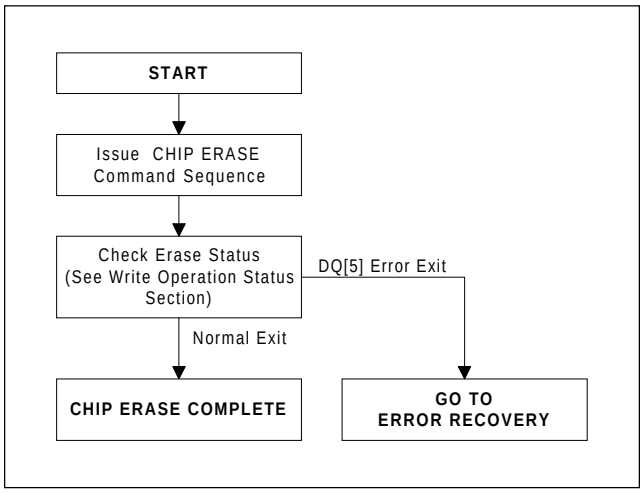


Figure 4. Chip Erase Procedure

sector is to be erased. As described later in this section, multiple sectors can be specified for erasure with a single command sequence. During sector erase, all specified sectors are erased sequentially. The data in sectors not specified for erasure, as well as the data in any sectors specified for erasure but located within protected sectors, is not affected by the sector erase operation.

The Sector Erase command sequence starts the Automatic Erase algorithm, which preprograms and verifies the specified unprotected sectors for an all zero data pattern prior to electrical erase. The device then provides the required number of internally generated erase pulses and verifies cell erasure within the proper cell margins. The host system is not required to provide any controls or timings during these operations.

After the sector erase data cycle (the sixth bus cycle) of the command sequence is issued, a sector erase time-out of 50 µs (typical), measured from the rising edge of the final WE# pulse in that bus cycle, begins. During this time, an additional sector erase data cycle, specifying the sector address of another sector to be erased, may be written into an internal sector erase buffer. This buffer may be loaded in any sequence, and the number of sectors specified may be from one sector to all sectors. The only restriction is that the time between these additional data cycles must be less than 50 µs, otherwise erasure may begin before the last data cycle is accepted. To ensure that all data cycles are accepted, it is recommended that host processor interrupts be disabled during the time that the additional cycles are being issued and then be re-enabled afterwards.

Note: The device is capable of accepting three ways of invoking Erase Commands for additional sectors during the time-out window. The preferred method, described above, is the sector erase data cycle after the initial six bus cycle command sequence. However, the device also accepts the following methods of specifying additional sectors during the sector erase time-out:

- Repeat the entire six-cycle command sequence, specifying the additional sector in the sixth cycle.
- Repeat the last three cycles of the six-cycle command sequence, specifying the additional sector in the third cycle.

If all sectors scheduled for erasing are protected, the device returns to reading array data after approximately 100 µs. If at least one selected sector is not protected, the erase operation erases the unprotected sectors, and ignores the command for the selected sectors that are protected.

The system can monitor DQ[3] to determine if the 50 µs sector erase time-out has expired, as described in the Write Operation Status section. If the time between additional sector erase data cycles can be insured to be less than the time-out, the system need not monitor DQ[3].

Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must then rewrite the command sequence, including any additional sector erase data cycles. Once the sector erase operation itself has begun, only the Erase Suspend command is valid. All other commands are ignored.

When the Automatic Erase algorithm terminates, the device returns to the Read mode. Several methods are provided to allow the host to determine the status of the erase operation, as described in the Write Operation Status section.

Figure 5 illustrates the Sector Erase procedure.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation to read data from, or program data in, any sector not being erased. The command causes the erase operation to be suspended in all sectors selected for erasure. This command is valid only during the sector erase operation, including during the 50 µs time-out period at the end of the initial command sequence and any subsequent sector erase data cycles, and is ignored if it is issued during chip erase or programming operations.

The HY29F040A requires a maximum of 20 µs to suspend the erase operation if the Erase Suspend command is issued during active sector erasure. However, if the command is written during the time-out, the time-out is terminated and the erase operation is suspended immediately. Any subsequent attempts to specify additional sectors for erasure by writing the sector erase data cycle (SA/0x30) will be interpreted as the Erase Resume command (XXX/0x30), which will cause the Automatic Erase algorithm to begin its operation. Note that any other command during the time-out will reset the device to the Read mode.

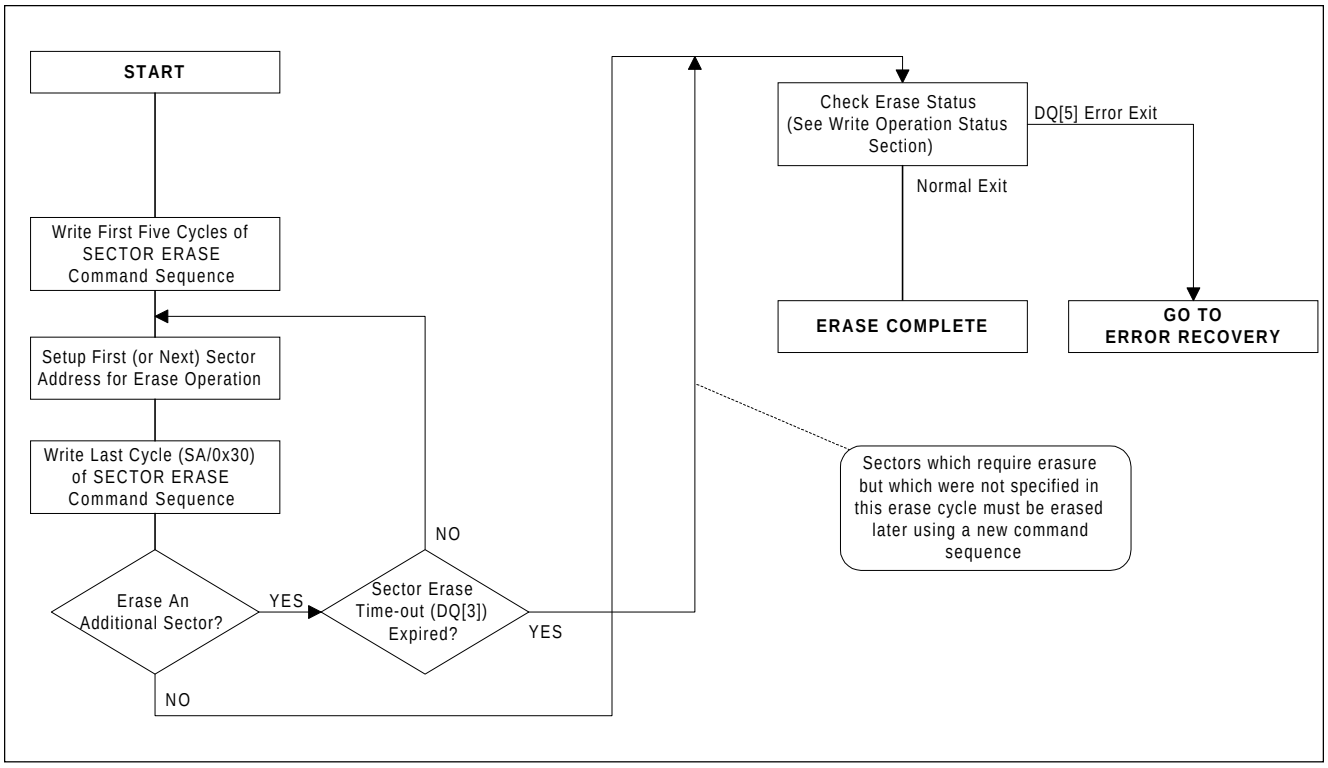


Figure 5. Sector Erase Procedure

Once the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ[7:0]. The host can use DQ[7], or DQ[6] and DQ[2] together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the host can initiate another programming operation (or read operation) within non-suspended sectors. The host can determine the status of a program operation during the erase-suspended state just as in the standard programming operation.

The system must write the Erase Resume command to exit the Erase Suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

The host may also write the Electronic ID command sequence when the device is in the Erase Suspend mode. The device allows reading Electronic ID codes even if the addresses used for the ID read cycles are within erasing sectors, since the codes are not stored in the memory array. When the device exits the Electronic ID mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See Electronic ID section for more information.

Electronic ID Command

The Electronic ID operation intended for use in programming equipment has been described previously. The host processor can also be obtain the same data by using the Electronic ID command sequence shown in Table 5. This method does not require V_{ID} on any pin. The Electronic ID command sequence may be invoked while the device is in the Read mode or the Erase Suspend mode, but is invalid while the device is actively programming or erasing.

The Electronic ID command sequence is initiated by writing two unlock cycles, followed by the Electronic ID command. The device then enters the Electronic ID mode, and:

- A read cycle at address 0xXXX00 retrieves the manufacturer code (Hynix = 0xAD).

- A read cycle at address 0xXXX01 returns the device code (HY29F040A = 0xA4).
- A read cycle containing a sector address (SA) in A[18:16] and the address 0x02 in A[7:0] returns 0x01 if that sector is protected, or 0x00 if it is unprotected.

The host system may read at any address any number of times, without initiating another command sequence. Thus, for example, the host may determine the protection status for all sectors by doing successive reads at address 0x02 while changing the SA in A[18:16] for each cycle.

The system must write the Reset command to exit the Electronic ID mode and return to the Read mode, or to the Erase Suspend mode if the device was in that mode when the command sequence was issued.

WRITE OPERATION STATUS

The HY29F040A provides a number of status bits to determine the status of a program or erase operation. These are contained in a status word that can be read from the device during the programming and erase operations. Table 6 summarizes the status indications and further detail is provided in the subsections that follow.

DQ[7] - Data# Polling

The Data# (“Data Bar”) Polling bit, DQ[7], indicates to the host system whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend mode. Data# Polling is valid after the rising edge of the final WE# pulse in the Program or Erase command sequence.

The system must do a read at the program address to obtain valid programming status information on this bit. While a programming operation is in progress, the device outputs the complement of the value programmed to DQ[7]. When the programming operation is complete, the device outputs the value programmed to DQ[7]. If a program operation is attempted within a protected sector, Data# Polling on DQ[7] is active for approximately 2 µs, then the device returns to reading array data.

The host must read at an address within any non-protected sector scheduled for erasure to obtain valid erase status information on DQ[7]. During an erase operation, Data# Polling produces a “0” on DQ[7]. When the erase operation is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ[7]. If all sectors selected for erasing are protected, Data# Polling on DQ[7] is active for approximately 100 µs, then the device returns to reading array data.

Table 6. Write and Erase Operation Status Summary

Mode	Operation	DQ[7] [1]	DQ[6]	DQ[5]	DQ[3]	DQ[2] [1]
Normal	Programming in progress	DQ[7]#	Toggle	0/1 [2]	N/A	N/A
	Programming completed	Data	Data [4]	Data	Data	Data
	Erase in progress	0	Toggle	0/1 [2]	1 [3]	Toggle
	Erase completed	1	Data [4]	Data	Data	Data [4]
Erase Suspend	Read within erase suspended sector	1	No toggle	0	N/A	Toggle
	Read within non-erase suspended sector	Data	Data	Data	Data	Data
	Programming in progress [5]	DQ[7]#	Toggle	0/1 [2]	N/A	N/A
	Programming completed [5]	Data	Data [4]	Data	Data	Data

Notes:
1. A valid address is required when reading status information. See text for additional information.
2. DQ[5] status switches to a ‘1’ when a program or erase operation exceeds the maximum timing limit.
3. A ‘1’ during sector erase indicates that the 50 µs timeout has expired and active erasure is in progress. DQ[3] is not applicable to the chip erase operation.
4. Equivalent to ‘No Toggle’ because data is obtained in this state.
5. Programming can be done only in a non-suspended sector (a sector not marked for erasure).

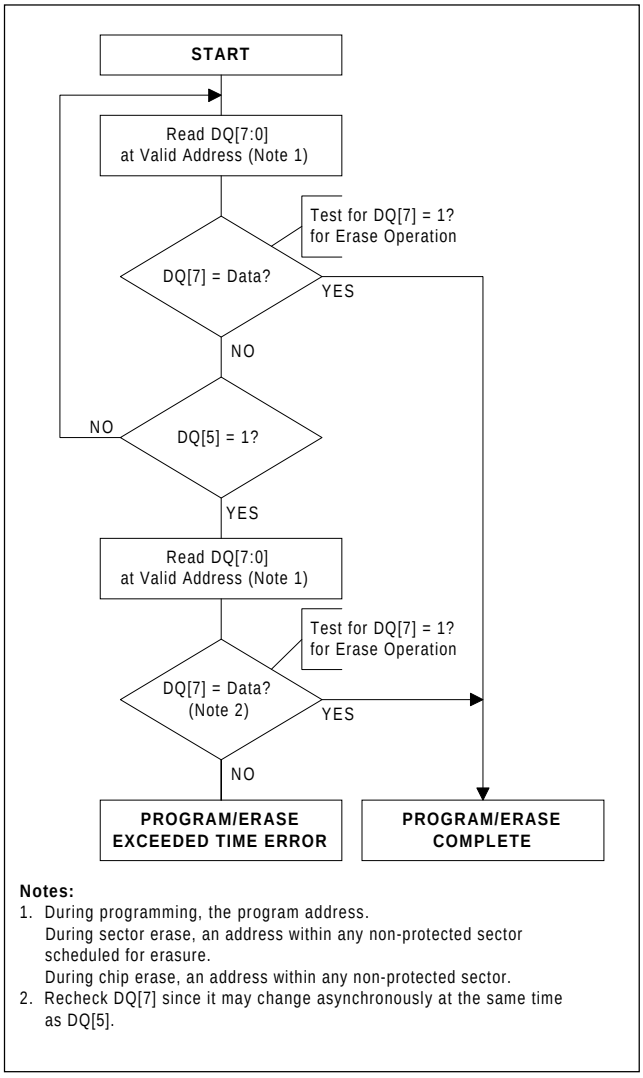
If at least one selected sector is not protected, the erase operation erases the unprotected sectors, and ignores the command for the selected sectors that are protected.

When the system detects that DQ[7] has changed from the complement to true data (or “0” to “1” for erase), it should do an additional read cycle to read valid data from DQ[7:0]. This is because DQ[7] may change asynchronously with respect to the other data bits while Output Enable (OE#) is asserted low.

Figure 6 illustrates the Data# Polling test algorithm.

DQ[6] - Toggle Bit I

Toggle Bit I on DQ[6] indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the program or erase command sequence, including during the sector erase time-out. The system may use either OE# or CE# to control the read cycles.



Notes:
1. During programming, the program address.
   During sector erase, an address within any non-protected sector scheduled for erasure.
   During chip erase, an address within any non-protected sector.
2. Recheck DQ[7] since it may change asynchronously at the same time as DQ[5].

Figure 6. Data# Polling Test Algorithm

Successive read cycles at any address during an Automatic Program algorithm operation (including programming while in Erase Suspend mode) cause DQ[6] to toggle. DQ[6] stops toggling when the operation is complete. If a program address falls within a protected sector, DQ[6] toggles for approximately 2 µs after the program command sequence is written, then returns to reading array data.

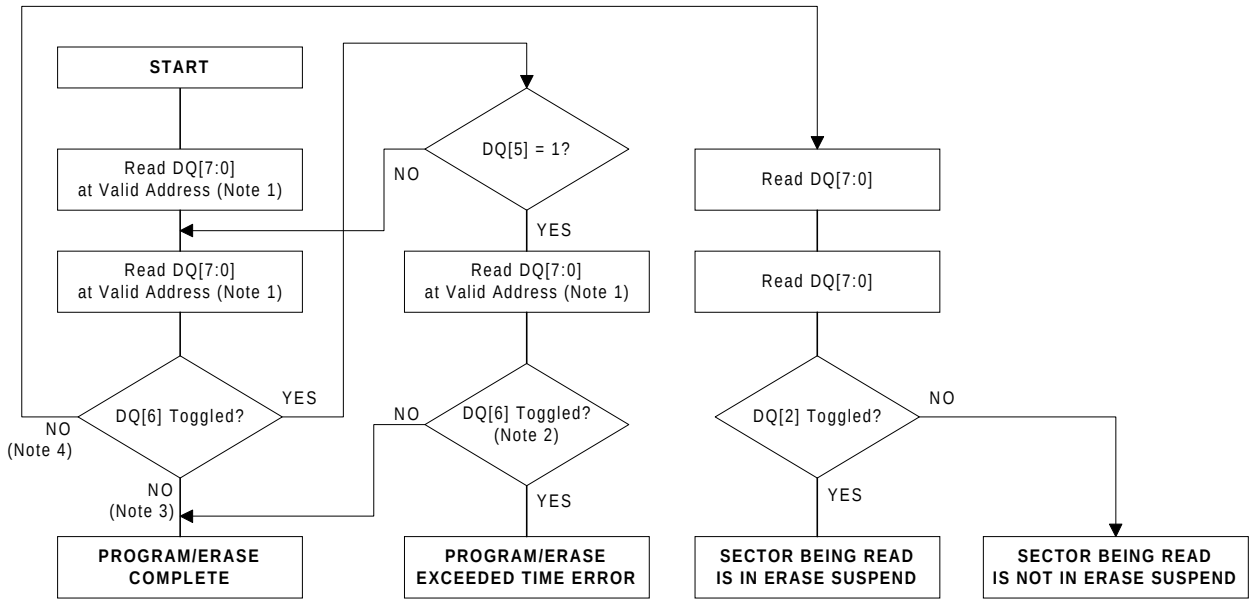
While the Automatic Erase algorithm is operating, successive read cycles at any address cause DQ[6] to toggle. DQ[6] stops toggling when the erase operation is complete or when the device is placed in the Erase Suspend mode. The host may use DQ[2] to determine which sectors are erasing or erase-suspended (see below). After an Erase command sequence is written, if all sectors selected for erasing are protected, DQ[6] toggles for approximately 100 µs, then returns to reading array data. If at least one selected sector is not protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

DQ[2] - Toggle Bit II

Toggle Bit II, DQ[2], when used with DQ[6], indicates whether a particular sector is actively erasing or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. The device toggles DQ[2] with each OE# or CE# read cycle.

DQ[2] toggles when the host reads at addresses within sectors that have been selected for erasure, but cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ[6], by comparison, indicates whether the device is actively erasing or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information.

Figure 7 illustrates the operation of Toggle Bits I and II.



Notes:
1. During programming, the program address.
   During sector erase, an address within any sector scheduled for erasure.
2. Recheck DQ[6] since toggling may stop at the same time as DQ[5] changes from 0 to 1.
3. Use this path if testing for Program/Erase status.
4. Use this path to test whether sector is in Erase Suspend mode.

Figure 7. Toggle Bit I and II Test Algorithm

DQ[5] - Exceeded Timing Limits

DQ[5] is set to a '1' when the program or erase time has exceeded a specified internal pulse count limit. This is a failure condition that indicates that the program or erase cycle was not successfully completed. DQ[5] status is valid only while DQ[7] or DQ[6] indicate that an Automatic Algorithm is in progress.

The DQ[5] failure condition will also be signaled if the host tries to program a '1' to a location that is previously programmed to '0', since only an erase operation can change a '0' to a '1'.

For both of these conditions, the host must issue a Read/Reset command to return the device to the Read mode.

DQ[3] - Sector Erase Timer

After writing a Sector Erase command sequence, the host may read DQ[3] to determine whether or not an erase operation has begun. When the sector erase time-out expires and the sector erase operation commences, DQ[3] switches from a '0' to a '1'. Refer to the "Sector Erase Command" section for additional information. Note that the sector erase timer does not apply to the Chip Erase command.

After the initial Sector Erase command sequence is issued, the system should read the status on DQ[7] (Data# Polling) or DQ[6] (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ[3]. If DQ[3] is a '1', the internally controlled erase cycle has begun and all further sector erase data cycles or commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ[3] is a '0', the device will accept a sector erase data cycle to mark an additional sector for erasure. To ensure that the data cycles have been accepted, the system software should check the status of DQ[3] prior to and following each subsequent sector erase data cycle. If DQ[3] is high on the second status check, the last data cycle might not have been accepted.

HARDWARE DATA PROTECTION

The HY29F040A provides several methods of protection to prevent accidental erasure or programming which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise. These methods are described in the sections that follow.

Command Sequences

Commands that may alter array data require a sequence of cycles as described in Table 5. This provides data protection against inadvertent writes.

Low V_{cc} Write Inhibit

To protect data during V_{CC} power-up and power-down, the device does not accept write cycles when V_{CC} is less than V_{LKO} (typically 3.7 volts). The command register and all internal program/erase circuits are disabled, and the device resets to the Read mode. Writes are ignored until V_{CC} is greater than V_{LKO} . The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by asserting any one of the following conditions: OE# = V_{IL} , CE# = V_{IH}, or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the Read mode on power-up.

Sector Protection

Additional data protection is provided by the HY29F040A’s sector protect feature, described previously, which can be used to protect sensitive areas of the Flash array from accidental or unauthorized attempts to alter the data.

ABSOLUTE MAXIMUM RATINGS [4]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	ºC
T_{BIAS}	Ambient Temperature with Power Applied	-55 to +125	ºC
V_{IN2}	Voltage on Pin with Respect to V_{SS} : VCC [1] A[9], OE# [2] All Other Pins [1]	 -2.0 to +7.0 -2.0 to +13.5 -2.0 to +7.0	 V V V
I_{OS}	Output Short Circuit Current [3]	200	mA

Notes:
1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to -2.0V for periods of up to 20 ns. See Figure 8. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 9.
2. Minimum DC input voltage on pins A[9] and OE# is -0.5 V. During voltage transitions, A[9] and OE# may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 8. Maximum DC input voltage on these pins is +12.5 V which may overshoot to 13.5 V for periods up to 20 ns.
3. No more than one output at a time may be shorted to V_{SS}. Duration of the short circuit should be less than one second.
4. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to +70	ºC
V_{CC}	Operating Supply Voltage	+4.50 to +5.50	V

Notes:
1. Recommended Operating Conditions define those limits between which the functionality of the device is guaranteed.

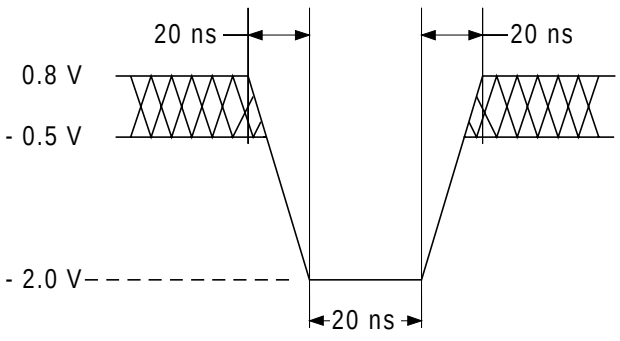


Figure 8. Maximum Undershoot Waveform

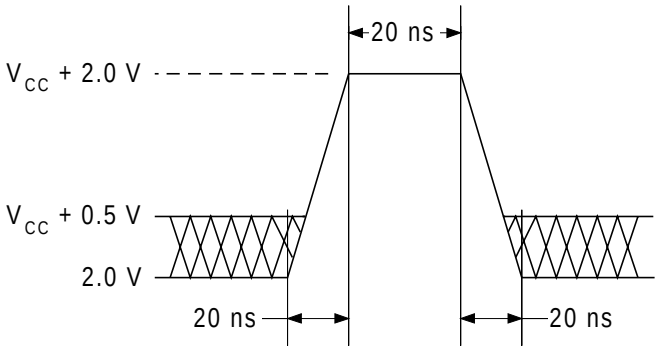


Figure 9. Maximum Overshoot Waveform

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter	Description	Test Setup	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A[9] Input Load Current	$V_{CC} = V_{CC}$ Max, A[9] = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Active Read Current [1]	CE# = V_{IL}, OE# = V_{IH}		20	30	mA
I_{CC2}	V_{CC} Active Write Current [2, 3]	CE# = V_{IL}, OE# = V_{IH}		30	40	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, CE# = V_{IH}		0.4	1.0	mA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{ID}	Voltage for Electronic ID and Temporary Sector Unprotect	V_{CC} = 5.25 V	10.5		12.5	V
V_{OL}	Output Low Voltage	$V_{CC} = V_{CC}$ Min, I_{OL} = 12.0ma			0.45	V
V_{OH}	Output High Voltage	$V_{CC} = V_{CC}$ Min, I_{OH} = -2.5 mA	2.4			V
V_{LKO}	Low V_{CC} Lockout Voltage		3.2		4.2	V

Notes:
1. Includes both the DC Operating Current and the frequency dependent component at 6 MHz. The read component of the I_{CC} current is typically less than 2 ma/MHz with OE# at V_{IH}.
2. I_{CC} active while Automatic Erase or Automatic Program algorithm is in progress.
3. Not 100% tested.

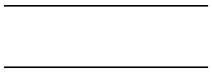
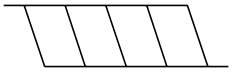
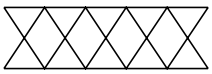
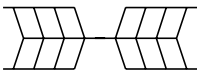
DC CHARACTERISTICS

CMOS Compatible

Parameter	Description	Test Setup	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A[9] Input Load Current	$V_{CC} = V_{CC}$ Max, A[9] = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Active Read Current [1]	CE# = V_{IL}, OE# = V_{IH}		20	30	mA
I_{CC2}	V_{CC} Active Write Current [2, 3]	CE# = V_{IL}, OE# = V_{IH}		30	40	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, CE# = V_{CC} ± 0.5V		1	5	µA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Electronic ID and Temporary Sector Unprotect	V_{CC} = 5.25V	10.5		12.5	V
V_{OL}	Output Low Voltage	$V_{CC} = V_{CC}$ Min, I_{OL} = 12.0ma			0.45	V
V_{OH}	Output High Voltage	$V_{CC} = V_{CC}$ Min, I_{OH} = -2.5 mA	0.85 x V_{CC}			V
		$V_{CC} = V_{CC}$ Min, I_{OH} = -100 µA	V_{CC} - 0.4			V
V_{LKO}	Low V_{CC} Lockout Voltage [3]		3.2		4.2	V

Notes:
1. Includes both the DC Operating Current and the frequency dependent component at 6 MHz. The read component of the I_{CC} current is typically less than 2 ma/MHz with OE# at V_{IH}.
2. I_{CC} active while Automatic Erase or Automatic Program algorithm is in progress.
3. Not 100% tested.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Centerline is High Impedance State (High Z)

TEST CONDITIONS

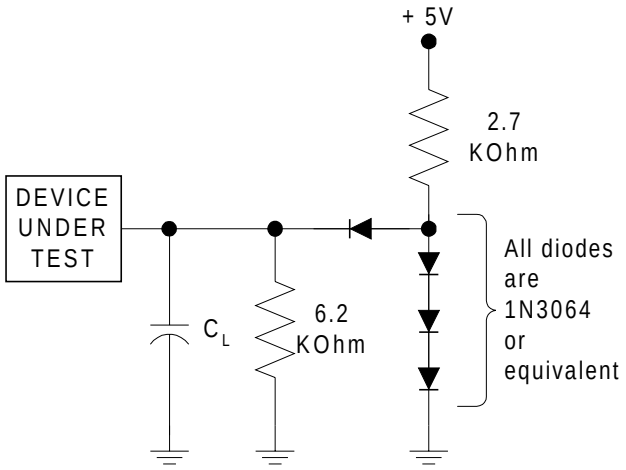
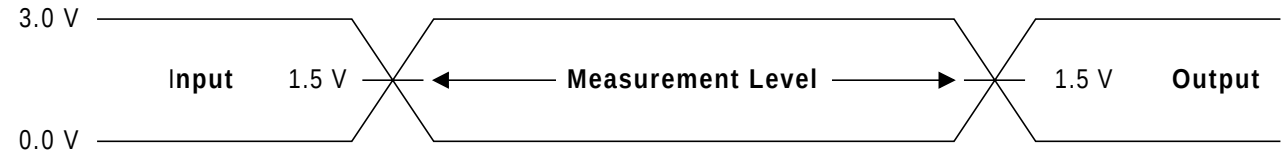


Figure 10. Test Setup

Table 7. Test Specifications

Test Condition	- 55	- 70 - 90 - 12	Unit
Output Load	1 TTL Gate		
Output Load Capacitance (C_L)	30	100	pF
Input Rise and Fall Times	5	20	ns
Input Signal Low Level	0.0	0.45	V
Input Signal High Level	3.0	2.4	V
Low Timing Measurement Signal Level	1.5	0.8	V
High Timing Measurement Signal Level	1.5	2.0	V



HY29F040A-55 Version

HY29F040A-70, -90, -12 Versions

Figure 11. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read Operations

Parameter		Description		Test Setup		Speed Option				Unit
JEDEC	Std					- 55	- 70	- 90	- 12	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	55	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	55	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	55	70	90	120	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	18	20	20	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		CE# = V_{IL}	Max	25	30	35	50	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	18	20	20	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0				ns

Notes:
1. Not 100% tested.
2. See Figure 10 and Table 7 for test conditions.

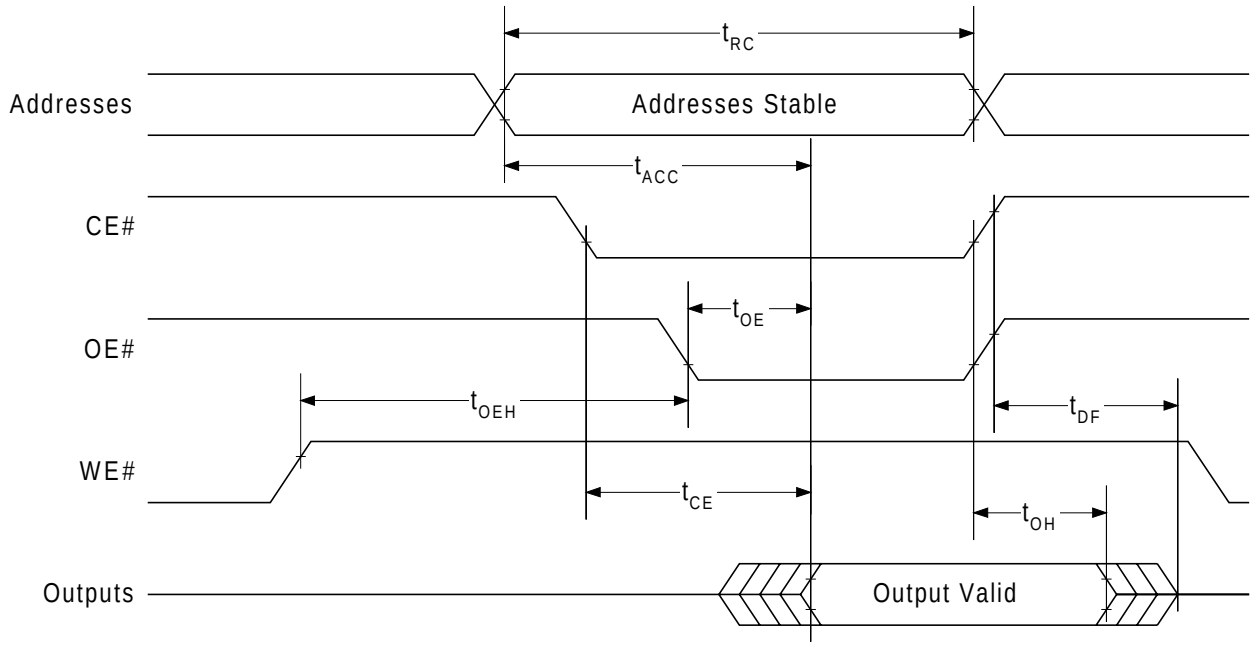


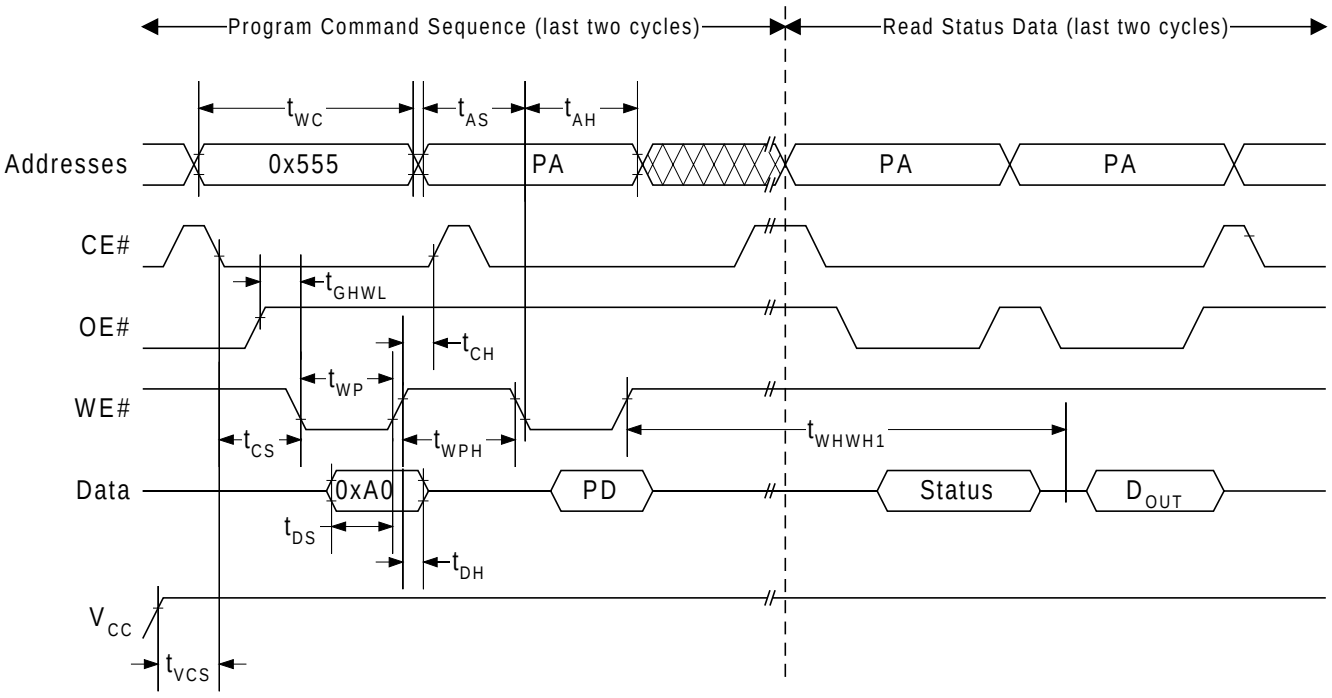
Figure 12. Read Operation Timings

AC CHARACTERISTICS

Program and Erase Operations

Parameter		Description		Speed Option				Unit
JEDEC	Std			- 55	- 70	- 90	- 12	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	25	30	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write	Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	30	35	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Notes 1, 2, 3)	Typ	7				µs
			Max	300				µs
		Chip Programming Operation (Notes 1, 2, 3, 5)	Typ	3.6				sec
			Max	10.8				sec
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 1, 2, 4)	Typ	1				sec
			Max	8				sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation (Notes 1, 2, 4)	Typ	8				sec
			Max	64				sec
		Erase and Program Cycle Endurance	Typ	1,000,000				cycles
			Min	100,000				cycles
	t_{VCS}	V_{CC} Setup Time	Min	50				µs

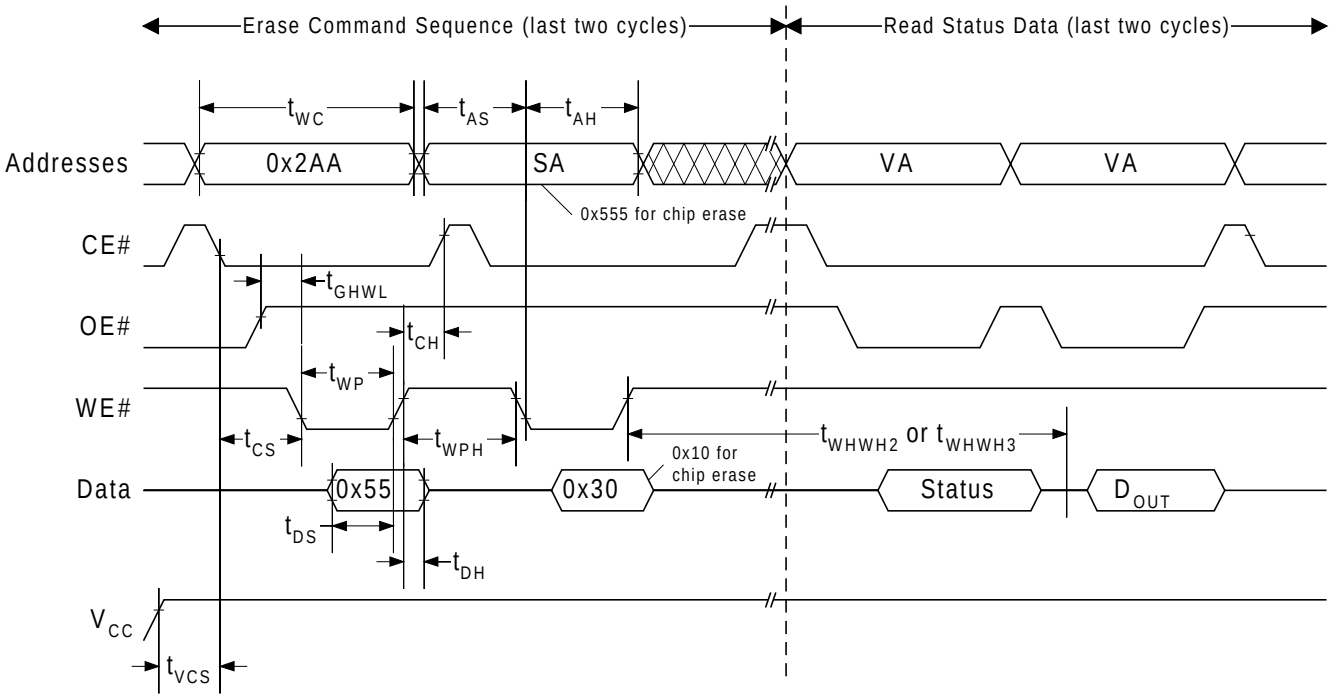
Notes:
1. Not 100% tested.
2. Typical program and erase times assume the following conditions: 25 °C, V_{CC} = 5.0 volts, 100,000 cycles. In addition, programming typicals assume a checkerboard pattern. Maximum program and erase times are under worst case conditions of 90 °C, V_{CC} = 4.5 volts, 100,000 cycles.
3. Excludes system-level overhead, which is the time required to execute the four-bus-cycle sequence for the program command. See Table 5 for further information on command sequences.
4. Excludes 0x00 programming prior to erasure. In the preprogramming step of the Automatic Erase algorithm, all bytes are programmed to 0x00 before erasure.
5. The typical chip programming time is considerably less than the maximum chip programming time listed since most bytes program faster than the maximum programming times specified. The device sets DQ[5] = 1 only If the maximum byte program time specified is exceeded. See Write Operation Status section for additional information.



Notes:
1. PA = Program Address, PD = Program Data, D_{OUT} is the true data at the program address.
2. V_{CC} shown only to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

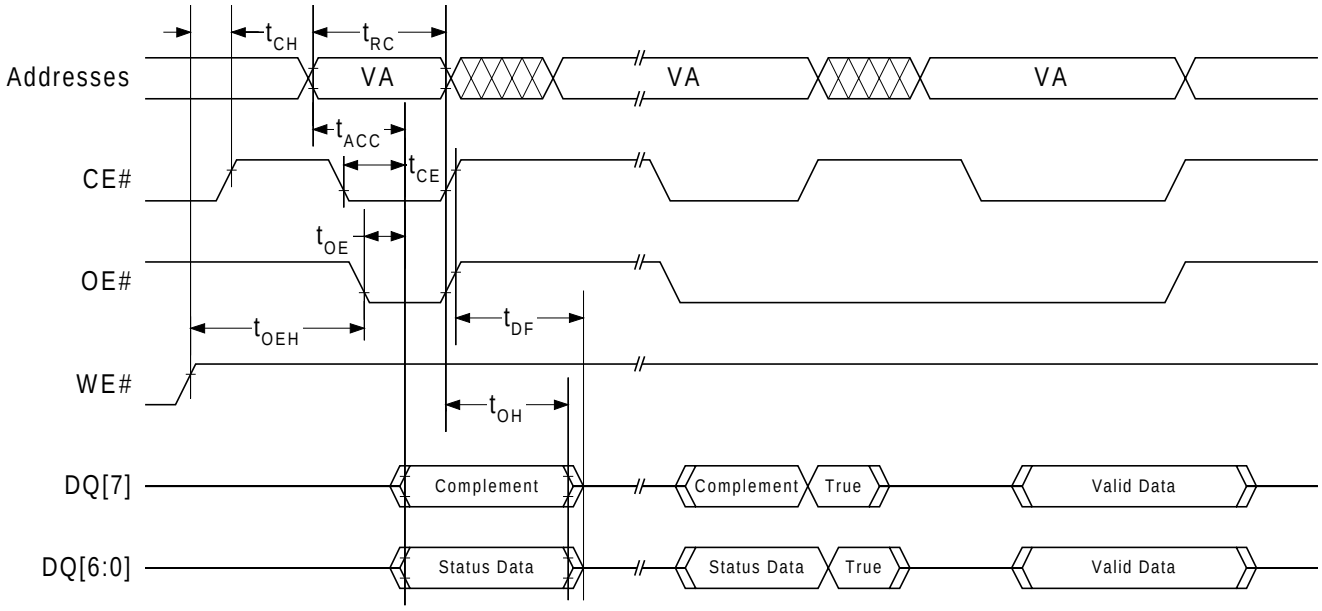
Figure 13. Program Operation Timings

AC CHARACTERISTICS



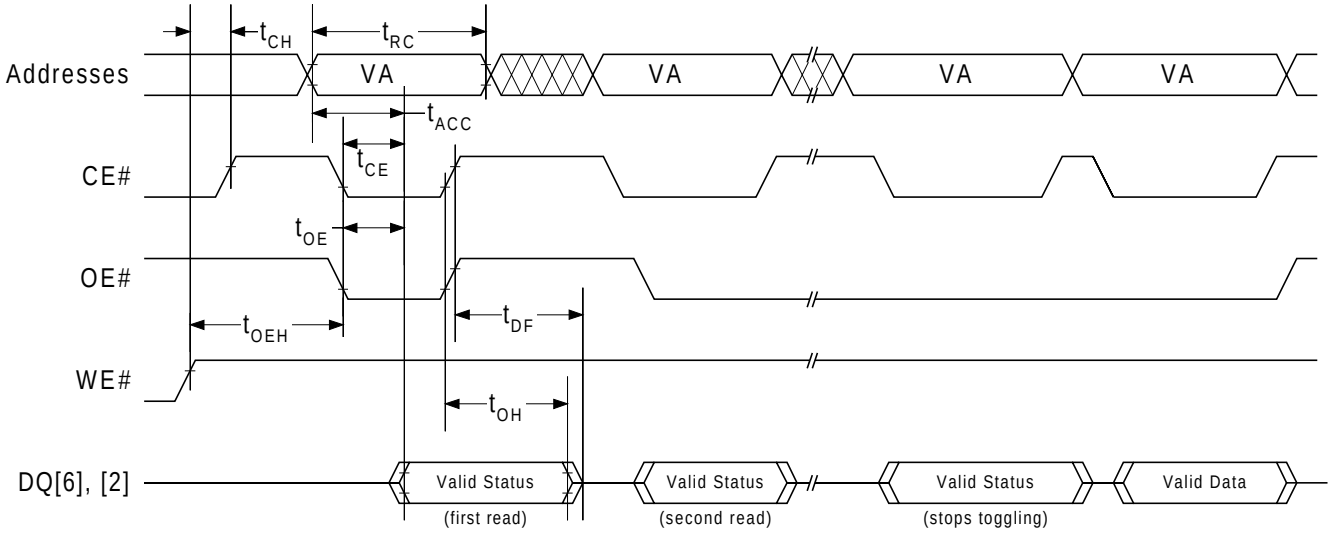
Notes:
1. SA =Sector Address (for sector erase), VA = Valid Address for reading status data (see Write Operation Status section), D_{OUT} is the true data at the read address.(0xFF after an erase operation).
2. V_{CC} shown only to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 14. Sector/Chip Erase Operation Timings



Notes:
1. VA = Valid Address for reading Data# Polling status data (see Write Operation Status section).
2. Illustration shows first status cycle after command sequence, last status read cycle and array data read cycle.

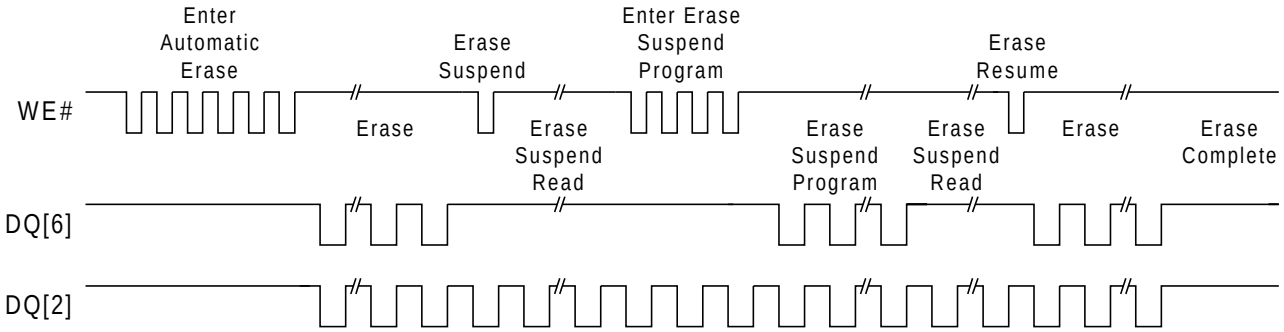
Figure 15. Data# Polling Timings (During Automatic Algorithms)



Notes:
1. VA = Valid Address for reading Toggle Bits (DQ2, DQ6) status data (see Write Operation Status section).
2. Illustration shows first two status read cycles after command sequence, last status read cycle and array data read cycle.

Figure 16. Toggle Polling Timings (During Automatic Algorithms)

AC CHARACTERISTICS



Notes:
1. The system may use CE# or OE# to toggle DQ[2] and DQ[6]. DQ[2] toggles only when read at an address within an erase-suspended sector.

Figure 17. DQ[2] and DQ[6] Operation

Sector Protect and Unprotect

Parameter		Description		Speed Option				Unit
JEDEC	Std			- 55	- 70	- 90	- 12	
	t_{ST}	Voltage Setup Time	Min	50				µs
	t_{CE}	Chip Enable to Output Delay	Max	55	70	90	120	ns
	t_{OE}	Output Enable to Output Delay	Max	25	30	35	50	ns
	t_{VLHT}	Voltage Transition Time for Sector Protect and Unprotect (Note 1)	Min	4				µs
	t_{WPP1}	Write Pulse Width for Sector Protect	Min	100				µs
	t_{WPP2}	Write Pulse Width for Sector Unprotect	Min	100				ms
	t_{OESP}	OE# Setup Time to WE# Active (Note 1)	Min	4				µs
	t_{CSP}	CE# Setup Time to WE# Active (Note 1)	Min	4				µs

Notes:
1. Not 100% tested.

AC CHARACTERISTICS

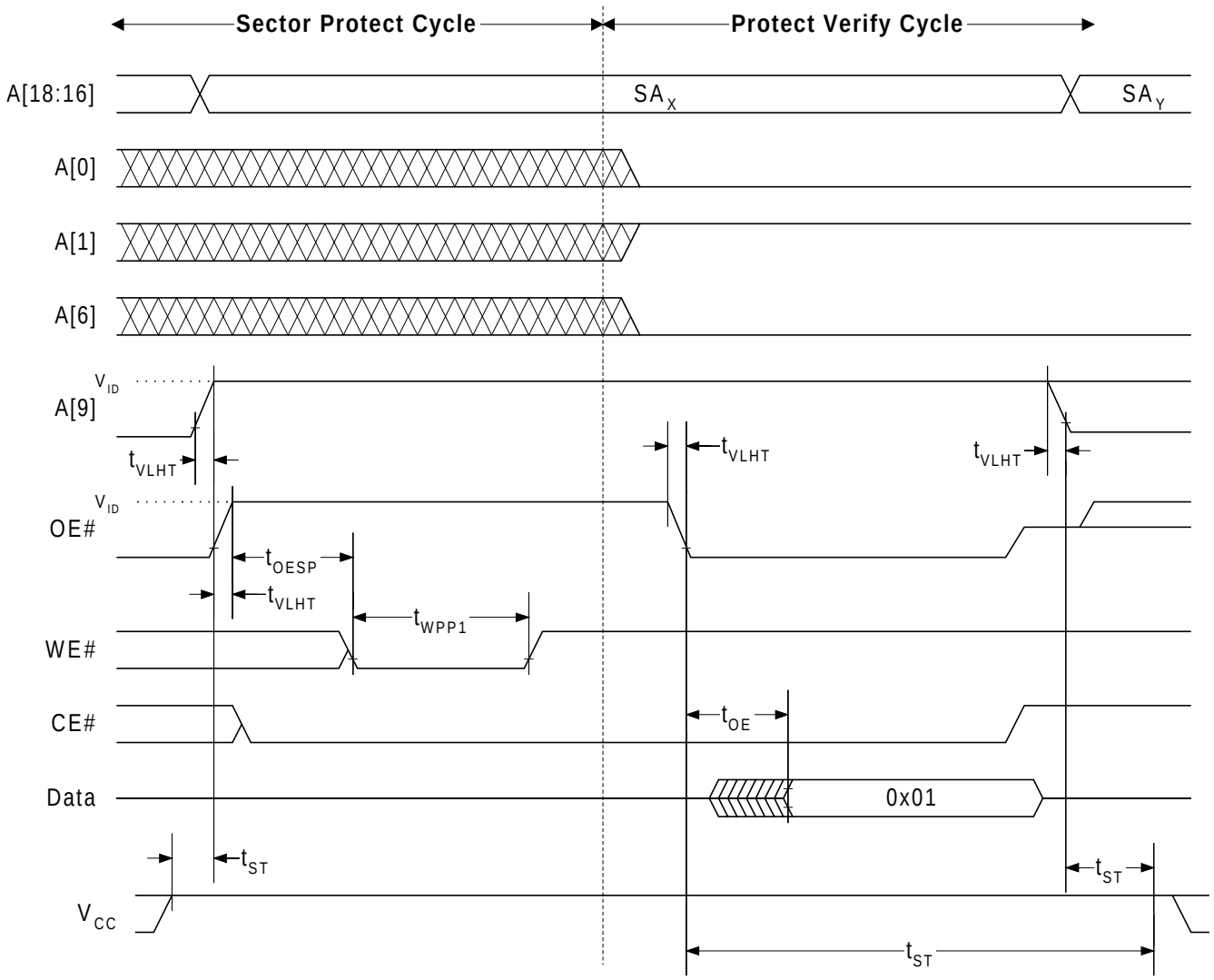


Figure 18. Sector Protect Timings

AC CHARACTERISTICS

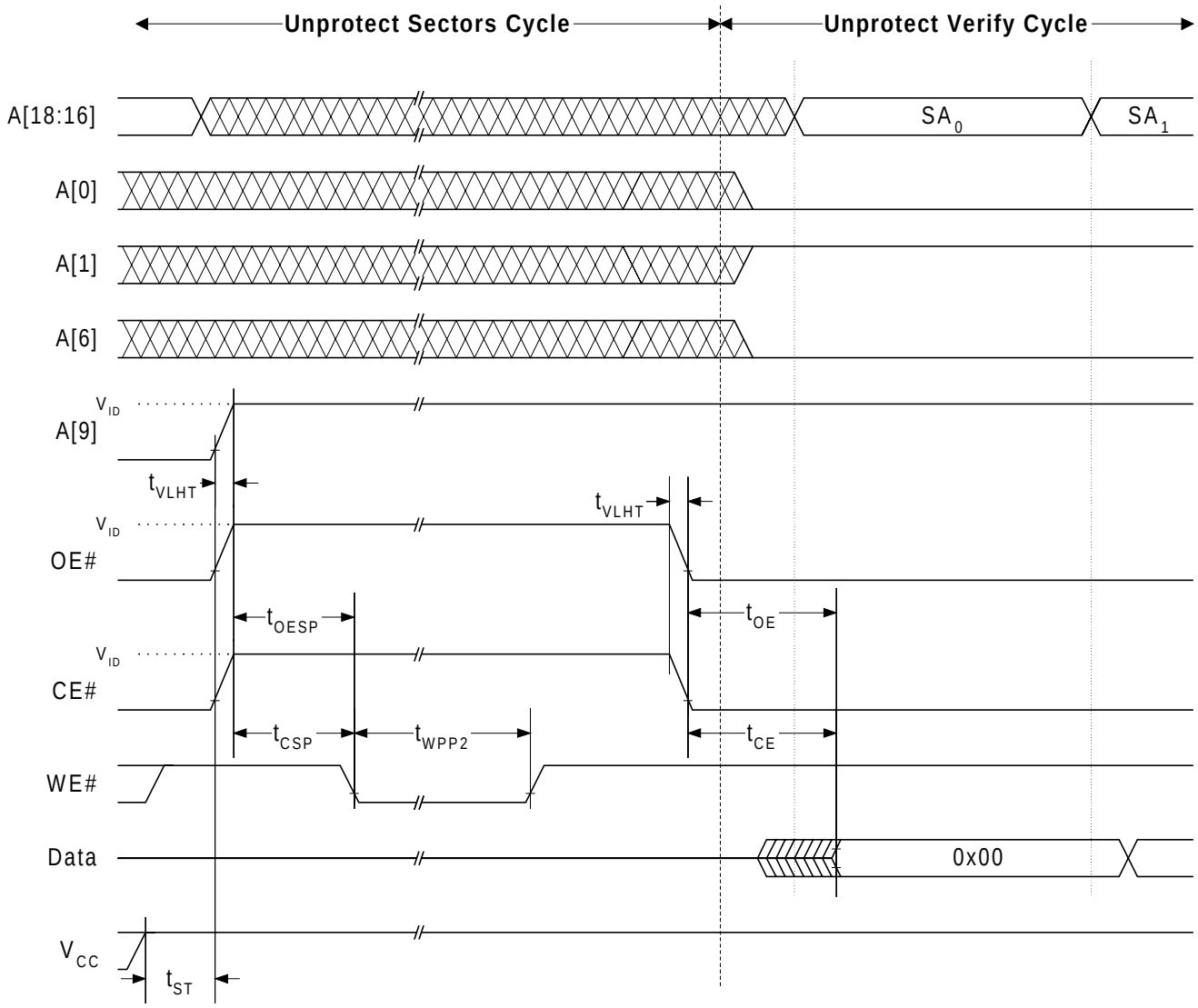


Figure 19. Sector Unprotect Timings

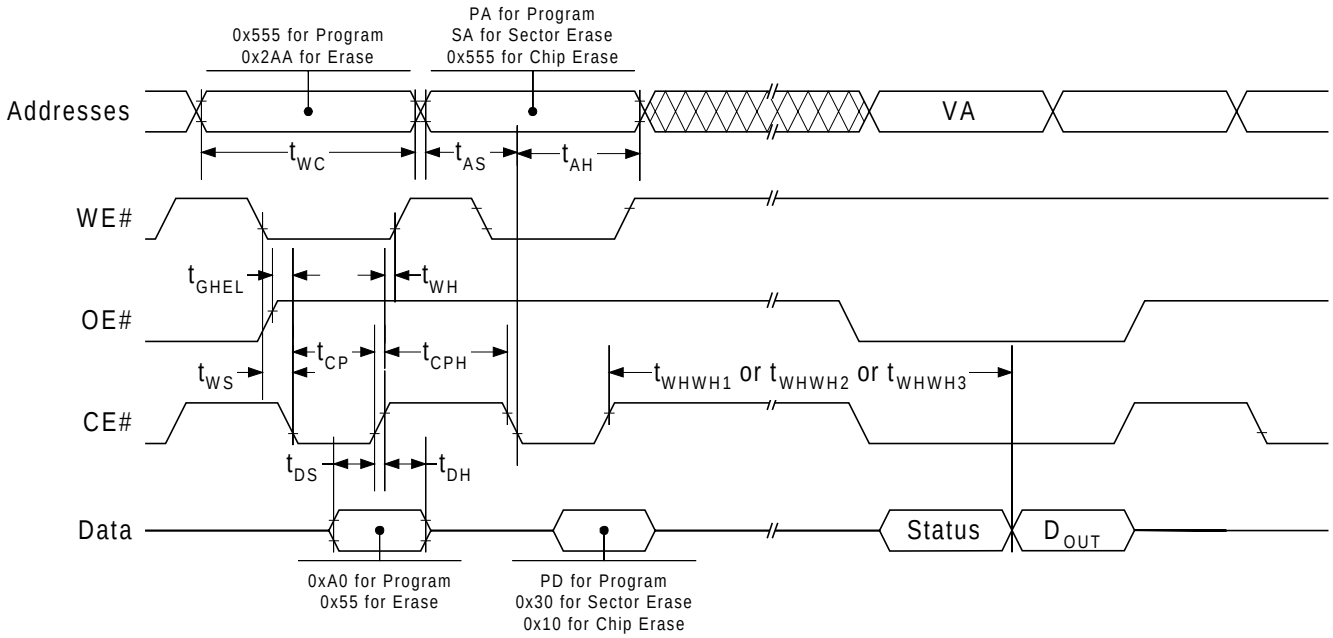
AC CHARACTERISTICS

Alternate CE# Controlled Erase/Program Operations

Parameter		Description		Speed Option				Unit
JEDEC	Std			- 55	- 70	- 90	- 12	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	25	30	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write	Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	30	35	45	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	20				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Notes 1, 2, 3)	Typ	7				µs
			Max	300				µs
		Chip Programming Operation (Notes 1, 2, 3, 5)	Typ	3.6				sec
			Max	10.8				sec
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 1, 2, 4)	Typ	1				sec
			Max	8				sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation (Notes 1, 2, 4)	Typ	8				sec
			Max	64				sec
		Erase and Program Cycle Endurance	Typ	1,000,000				cycles
			Min	100,000				cycles

Notes:
1. Not 100% tested.
2. Typical program and erase times assume the following conditions: 25 °C, V_{CC} = 5.0 volts, 100,000 cycles. In addition, programming typicals assume a checkerboard pattern. Maximum program and erase times are under worst case conditions of 90 °C, V_{CC} = 4.5 volts, 100,000 cycles.
3. Excludes system-level overhead, which is the time required to execute the four-bus-cycle sequence for the program command. See Table 5 for further information on command sequences.
4. Excludes 0x00 programming prior to erasure. In the preprogramming step of the Automatic Erase algorithm, all bytes are programmed to 0x00 before erasure.
5. The typical chip programming time is considerably less than the maximum chip programming time listed since most bytes program faster than the maximum programming times specified. The device sets DQ[5] = 1 only If the maximum byte program time specified is exceeded. See Write Operation Status section for additional information.

AC CHARACTERISTICS



Notes:

1. PA = program address, PD = program data, VA = Valid Address for reading program or erase status (see Write Operation Status section), D_{OUT} = array data read at VA.
2. Illustration shows the last two cycles of the program or erase command sequence and the last status read cycle.

Figure 20. Alternate CE# Controlled Write Operation Timings

Latchup Characteristics

Description	Minimum	Maximum	Unit
Input voltage with respect to V_{SS} on all I/O pins	- 1.0	V_{CC} + 1.0	V
V_{CC} Current	- 100	100	mA

Notes:
1. Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0V, one pin at a time.

TSOP Pin Capacitance

Symbol	Parameter	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions: T_A = 25 ºC, f = 1.0 MHz.

PLCC Pin Capacitance

Symbol	Parameter	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	12	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions: T_A = 25 ºC, f = 1.0 MHz.

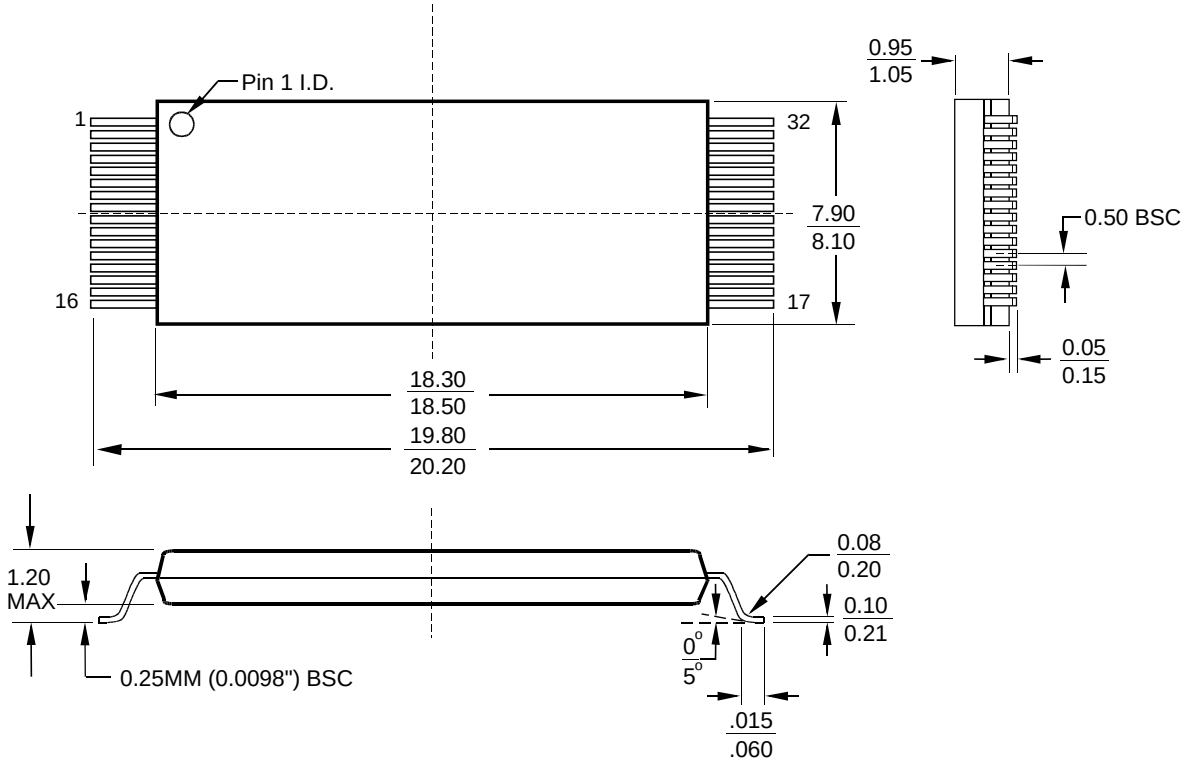
Data Retention

Parameter	Test Conditions	Minimum	Unit
Minimum Pattern Data Retention Time	150 ºC	10	Years
	125 ºC	20	Years

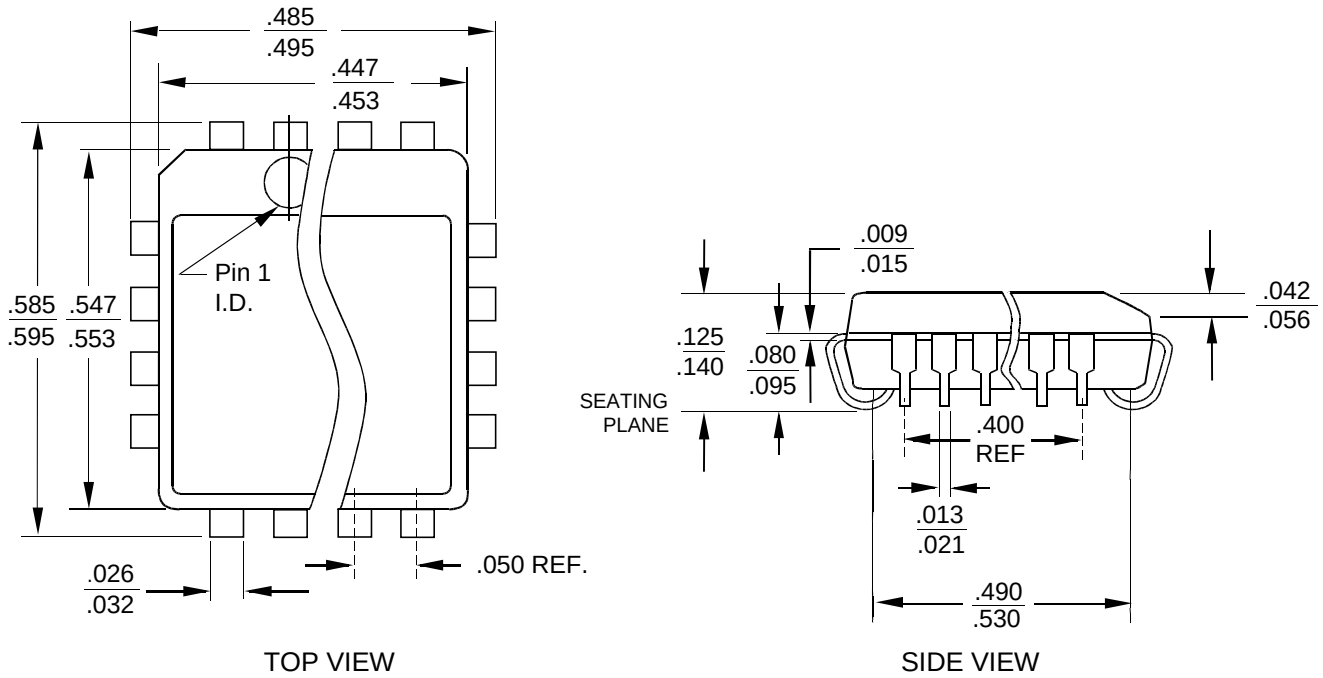
PACKAGE DRAWINGS

Physical Dimensions

TSOP32 - 32-pin Thin Small Outline Package (measurements in millimeters)

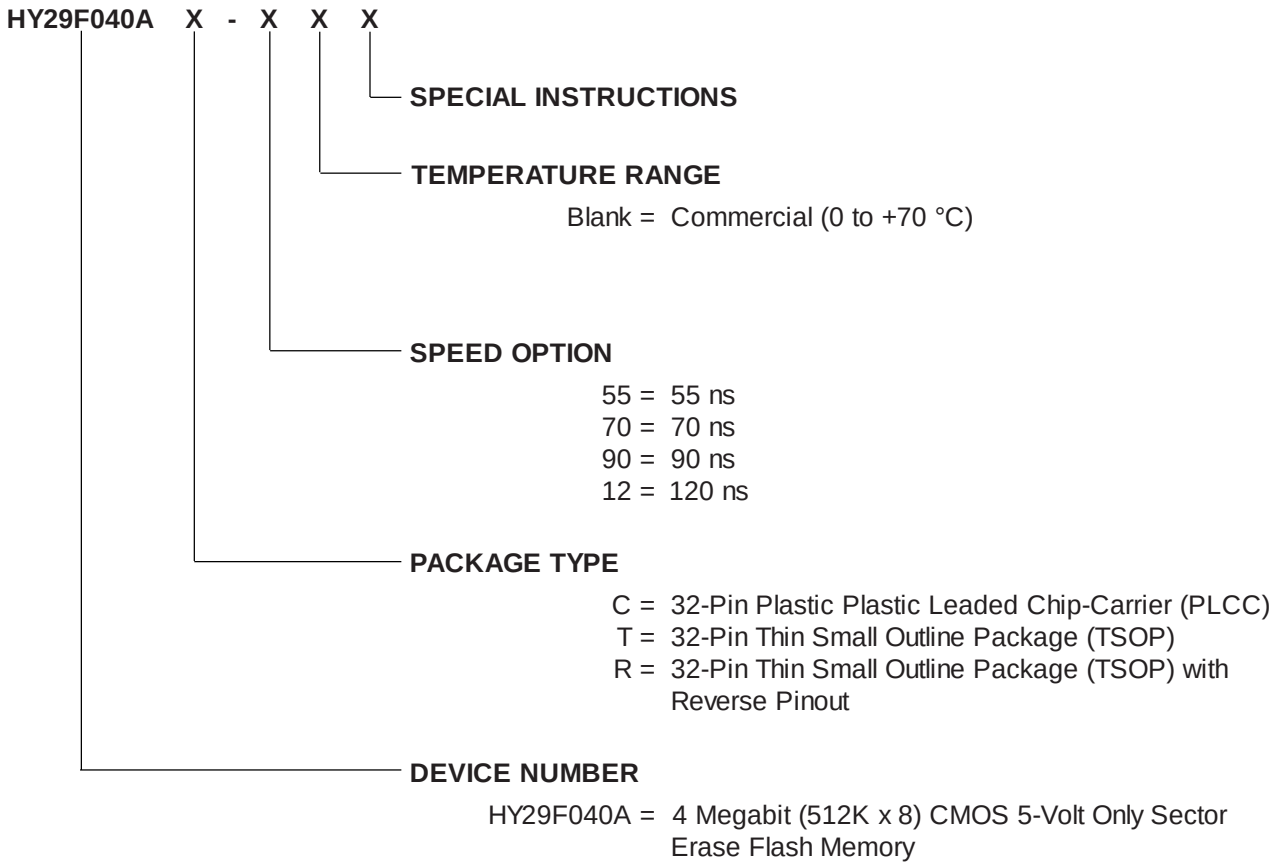


PLCC32 - 32-pin Plastic Leaded Chip Carrier (measurements in inches)



ORDERING INFORMATION

Hynix products are available in several speeds, packages and operating temperature ranges. The ordering part number is formed by combining a number of fields, as indicated below. Refer to the 'Valid Combinations' table, which lists the configurations that are planned to be supported in volume. Please contact your local Hynix representative or distributor to confirm current availability of specific configurations and to determine if additional configurations have been released.



VALID COMBINATIONS

	Package and Speed											
	PLCC				TSOP				Reverse TSOP			
Temperature	**55 ns**	**70 ns**	**90 ns**	**120 ns**	**55 ns**	**70 ns**	**90 ns**	**120 ns**	**55 ns**	**70 ns**	**90 ns**	**120 ns**
Commercial	C-55	C-70	C-90	C-12	T-55	T-70	T-90	T-12	R-55	R-70	R-90	R-12

Note:
1. The complete part number is formed by appending the suffix shown in the table to the Device Number. For example, the part number for a 90 ns, Commercial temperature range device in the TSOP package is *HY29F040AT-90*.

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Revision Record

Rev.	Date	Details
2.2	5/01	Change to Hynix format. Eliminated industrial and extended temperature versions.

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