Revision History

Revision No.	History	Draft Date	Remark
0.3	Changed TA, PKG Drawing, Output Load Circuit		
0.4	Changed Cin Value.		
0.6	1. Added Operation Code in Mode Register 2. Changed Burst Stop in Full Page	July 2003	1. Page 6 2. Page 8

DESCRIPTION

The Hynix Low Power SDRAM is suited for non-PC application which use the batteries such as PDAs, 2.5G and 3G cellular phones with internet access and multimedia capabilities, mini-notebook, handheld PCs

The Hynix HY5W2A2F series is a 134,217,728-bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY5W2A2F series is organized as 4banks of 1,048,576x32.

The Low Power SDRAM provides for programmable options including CAS latency of 1, 2, or 3, READ or WRITE burst length of 1, 2, 4, 8, or full page, and the burst count sequence(sequential or interleave). And the Low Power SDRAM also provides for special programmable options including Partial Array Self Refresh of 1bank, 2banks, or all banks, Temperature Compensated Self Refresh of 15, 45, 70, or 85 degrees C. A burst of Read or Write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst Read or Write command on any cycle(This pipelined design is not restricted by a 2N rule).

Deep Power Down Mode is a additional operating mode for Low Power SDRAM. This mode can achieve maximum power reduction by removing power to the memory array within each SDRAM. By using this feature, the system can cut off alomost all DRAM power without adding the cost of a power switch and giving up mother-board power-line layout flexibility.

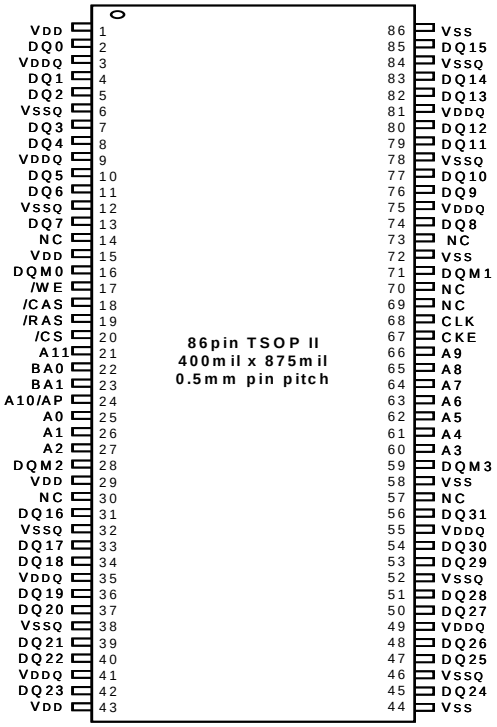
FEATURES

- Standard SDRAM Protocol
- Internal 4bank operation
- Voltage : VDD = 2.5V, VDDQ = 1.8V & 2.5V
- LVTTL compatible I/O Interface
- Low Voltage interface to reduce I/O power
- Low Power Features (HY5W22F / HY57W283220T series can't support these features)
  - PASR(Partial Array Self Refresh)
  - TCSR(Temperature Compensated Self Refresh)
  - Deep Power Down Mode
- Packages : 90ball, 0.8mm pitch FBGA / 86pin, TSOP
- -25 ~ 85C Operation

ORDERING INFORMATION

Part No.	Clock Frequency CAS Latench	Organization	Interface	Package
HY57W2A3220(L/S)T-H HY5W2A2(L/S)F-H	133MHz CL 3	4Banks x 1Mbits x32	LVTTL	90balls FBGA (HY5xxxxxxF) 86pin TSOP-II (HY5xxxxxxT)
HY57W2A3220(L/S)T-8 HY5W2A2(L/S)F-8	125MHz CL 3	4Banks x 1Mbits x32	LVTTL	
HY57W2A3220(L/S)T-P HY5W2A2(L/S)F-P	100MHz CL 2	4Banks x 1Mbits x32	LVTTL	
HY57W2A3220(L/S)T-S HY5W2A2(L/S)F-S	100MHz CL 3	4Banks x 1Mbits x32	LVTTL	
HY57W2A3220(L/S)T-B HY5W2A2(L/S)F-B	66MHz CL 2	4Banks x 1Mbits x32	LVTTL	

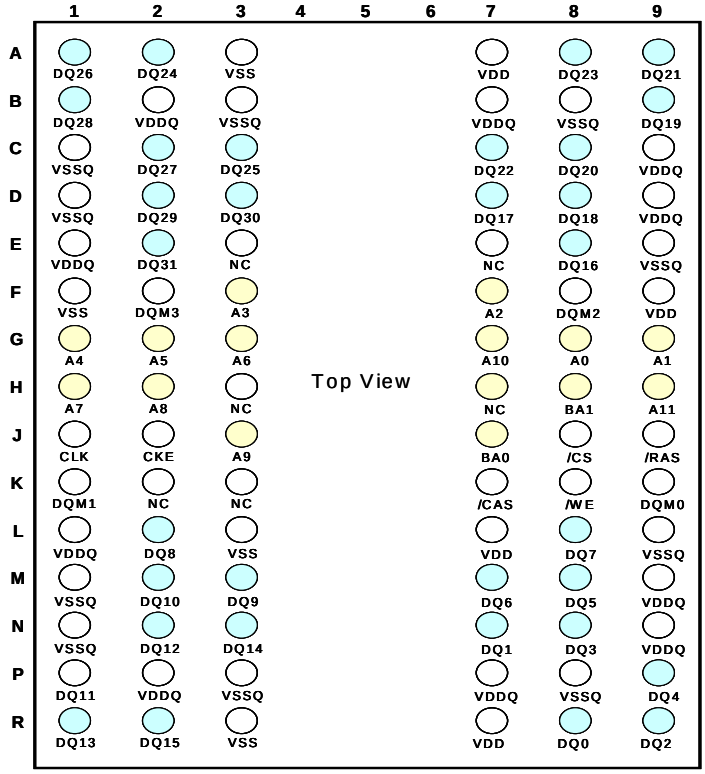
PIN CONFIGURATION (HY57W2A3220T Series)



PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0, BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
DQM0~3	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ31	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

Ball CONFIGURATION (HY5W2A2F Series)

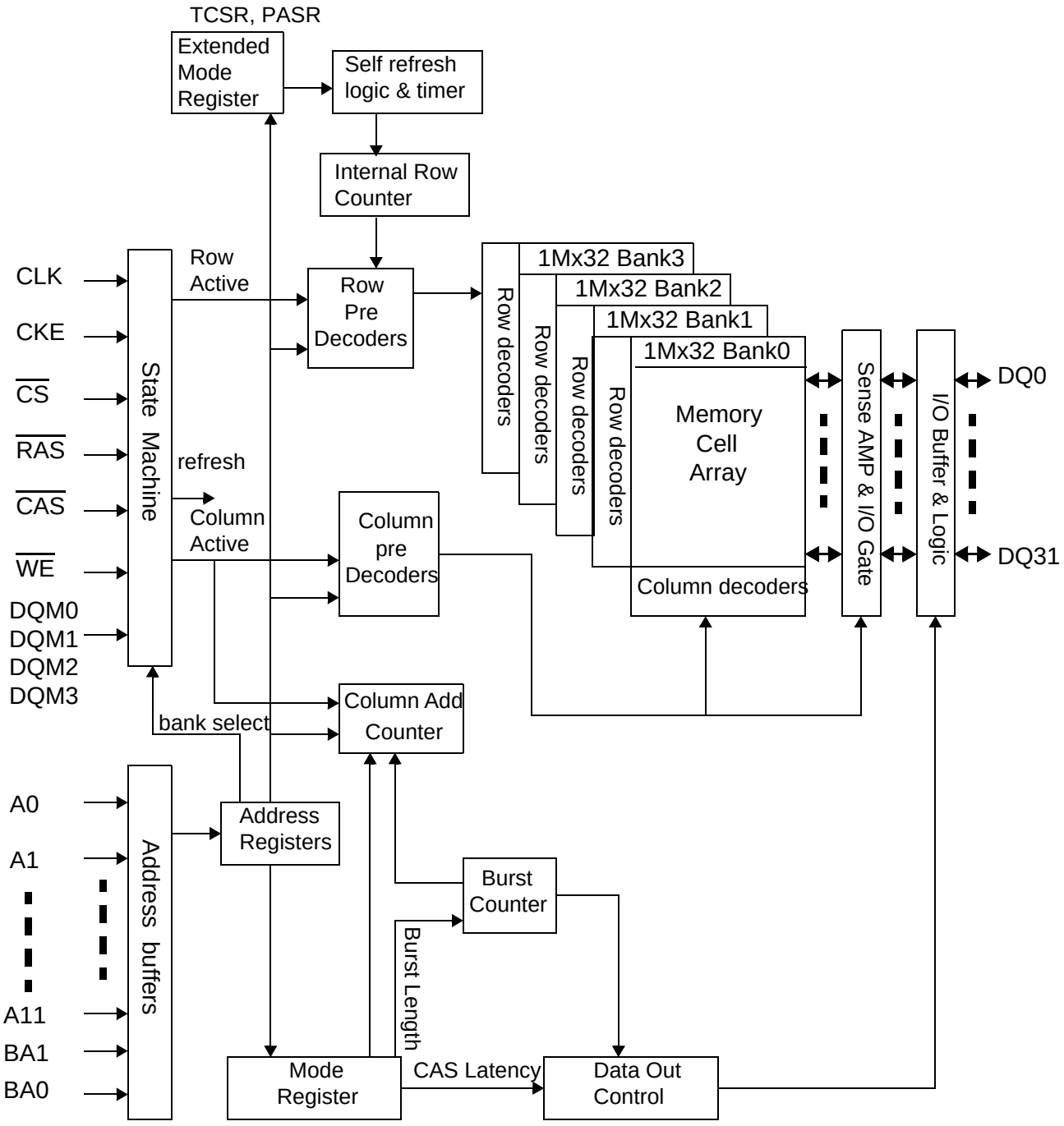


Ball DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0, BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
DQM0~3	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ31	Data Input/Output	Multiplexed data input / output pin
V_{DD}/V_{SS}	Power Supply/Ground	Power supply for internal circuits and input buffers
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

1Mbit x 4banks x 32 I/O Synchronous DRAM



BASIC FUNCTIONAL DESCRIPTION

Mode Register

BA1	BA0		A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0		OPERATION CODE				0	CAS Latency			BT	Burst Length		

OPERATION CODE

A11	A10	A9	A8	Write Mode
0	0	0	0	Burst read & Burst write
X	X	1	0	Burst read & Single write

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

BASIC FUNCTIONAL DESCRIPTION (Continued)

Extended Mode Register

BA1	BA0		A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0		0	0	0	0	0	0	0	TCSR		PASR		

TCSR (Temperature Compensated Self Refresh)

A4	A3	Temperature ^{o} C
0	0	70
0	1	45
1	0	15
1	1	85

PASR (Partial Array Self Refresh)

A2	A1	A0	Self Refresh Coverage
0	0	0	All Banks
0	0	1	Half of Total Bank (BA1=0)
0	1	0	Quarter of Total Bank (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Power Up and Initialization

Like a Synchronous DRAM, Low Power SDRAM must be powered up and initialized in a predefined manner. Power must be applied to VDD and VDDQ(simultaneously). The clock signal must be started at the same time. After power up, an initial pause of 200 μsec is required. And a precharge all command will be issued to the LP SDRAM. Then, 8 or more Auto refresh cycles will be provided. After the Auto refresh cycles are completed, a mode register set(MRS) command will be issued to program the specific mode of operation (Cas Latency, Burst length, etc.) And a extended mode register set command will be issued to program specific mode of self refresh operation(PASR & TCSR). The following these cycles, the LP SDRAM is ready for normal opeartion.

Programming the registers

Mode Register

The mode register contains the specific mode of operation of the LP SDRAM. This register includes the selection of a burst length(1, 2, 4, 8, Full Page), a cas latency(1, 2, or 3), a burst type, an opearting mode to differentiate between normal mode and a special burst read and single write mode. The mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of mode register set command.

Extended Mode Register

The extended mode register contains the specific features of self refresh opeartion of the LP SDRAM. This register includes the selection of partial arrays to be refreshed(half array, quarter array, etc.), tempearture range of the device(85, 70, 45, 15) for reducing current consumption during self refresh. The extended mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of extended mode register set command.

Bank(Row) Active

The Bank Active command is used to activate a row in a specified bank of the device. This command is initiated by activating $\overline{CS}$, $\overline{RAS}$ and deasserting $\overline{CAS}$, $\overline{WE}$ at the positive edge of the clock. The value on the BA1 and BA0 selects the bank, and the value on the A0-A11 selects the row. This row remains active for column access until a precharge command is issued to that bank. Read and write opeartions can only be initiated on this activated bank after the minimum tRCD time is passed from the activate command.

Read

The READ command is used to initiate the burst read of data. This command is initiated by activating $\overline{CS}$, $\overline{CAS}$, and deasserting $\overline{WE}$, $\overline{RAS}$ at the positive edge of the clock. BA1 and BA0 inputs select the bank, A8-A0 address inputs select the sarting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected the row being accessed will be precharged at the end of the READ burst; if Auto Precharge is not selected, the row will remain active for subsequent accesses.The length of burst and the CAS latency will be determined by the values programmed during the MRS command.

Write

The WRITE command is used to initiate the burst write of data. This command is initiated by activating $\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ and deasserting $\overline{RAS}$ at the positive edge of the clock. BA1 and BA0 inputs select the bank, A8-A0 address inputs select the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected the row being accessed will be precharged at the end of the WRITE burst; if Auto Precharge is not selected, the row will remain active for subsequent accesses.

Precharge

The Precharge command is used to close the open row in a particular bank or the open row in all banks. When the precharge command is issued with address A10, high, then all banks will be precharged, and If A10 is low, the open row in a particular bank will be precharged. The bank(s) will be available when the minimum tRP time is met after the precharge command is issued.

Auto Precharge

The Auto Precharge command is issued to close the open row in a particular bank after READ or WRITE operation. If A10 is high when a READ or WRITE command is issued, the READ or WRITE with Auto Precharge is initiated.

Burst Stop in full page

This command stops a full-page burst operation, and is illegal otherwise. Full page burst continues until this command is input.
When data input/output is completed for full-page of data, it automatically returns to the start address and input/output is performed repeatedly.

Data Mask

The Data Mask comamnd is used to mask READ or WRITE data. During a READ operation, When this command is issued, data ouputs are disabled and become high impedance after two clock delay. During a WRITE operation, When this command is issued, data inputs can't be written with no clock delay.

Clock Suspend

The Clock Suspend command is used to suspend the internal clock of DRAM. During normal access mode, CKE is keeping High. When CKE is low, it freezes the internal clock and extends data Read and Write operations.

Power Down

The Power Down command is used to reduce standby current. Before this command is issued, all banks must be precharged and tRP must be passed after a precharge command. Once the Power Down command is initiated by keeping CKE low, all of the input buffer except CKE are gated off.

Auto Refresh

The Auto Refresh command is used during normal operation and is similar to CBR refresh in Coventional DRAMs. This command must be issued each time a refresh is required. When an Auto Refresh command is issued , the address bits is "Don't care", because the specific address bits is generated by internal refresh address counter.

Self Refresh

The Self Refresh command is used to retain cell data in the Low Power SDRAM. In the Self Refresh mode, the Low Power SDRAM operates refresh cycle asynchronously. The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled(Low). The Low Power SDRAM can accomplish an special Self Refresh operation by the specific modes(TCSR, PASR) programmed in extended mode registers. The Low Power SDRAM can control the refresh rate by the temperature value of TCSR (Temperature Compensated Self Refresh) and select the memory array to be refreshed by the value of PASR(Partial Array Self Refresh). The Low Power SDRAM can reduce the self refresh current(IDD6) by using these two modes.

Deep Power Down

The Deep Power Down Mode is used to achieve maximum power reduction by cutting the power of the whole memory array of the devices. For more information, see the special operation for Low Power consumption of this data sheet.

COMMAND TRUTH TABLE

Function	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/AP	BA	Note
Mode Register Set	H	X	L	L	L	L	X	Op Code			2
Extended Mode Register Set	H	X	L	L	L	L	X	Op Code			2
No Operation	H	X	L	H	H	H	X	X			
Device Deselect	H	X	H	X	X	X	X	X			
Bank Active	H	X	L	L	H	H	X	Row Address		V	
Read	H	X	L	H	L	H		Column	L	V	
Read with Autoprecharge	H	X	L	H	L	H	X	Column	H	V	
Write	H	X	L	H	L	L	X	Column	L	V	
Write with Autoprecharge	H	X	L	H	L	L	X	Column	H	V	
Precharge All Banks	H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank	H	X	L	L	H	L	X	X	L	V	
Burst stop	H	X	L	H	H	L	X	X			
Data Write/Output Enable	H	X	X				X	X			
Data Mask/Output Disable	H	X	X				V	X			
Auto Refresh	H	H	L	L	L	H	X	X			
Self Refresh Entry	H	L	L	L	L	H	X	X			
Self Refresh Exit	L	H	H	X	X	X	X	X			1
			L	H	H	H					
Precharge Power Down Entry	H	L	H	X	X	X	X	X			
			L	H	H	H					
Precharge Power Down Exit	L	H	H	X	X	X	X	X			
			L	H	H	H					
Clock Suspend Entry	H	L	H	X	X	X	X	X			
			L	V	V	V					
Clock Suspend Exit	L	H	X				X	X			
Deep Power Down Entry	H	L	L	H	H	L	X	X			
Deep Power Down Exit	L	H	X				X	X			

Note : 1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.
2. BA1/BA0 must be issued 0/0 in the mode register set, and 1/0 in the extended mode register set.

CURRENT STATE TRUTH TABLE (Sheet 1 of 3)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,BA1	A11-A0	Description		
idle	L	L	L	L	OP Code		Mode Register Set	Set the Mode Register	14
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	5
	L	L	H	L	BA	X	Precharge	No Operation	
	L	L	H	H	BA	Row Add.	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4
	L	H	H	H	X	X	No Operation	No Operation	3
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	3
Row Active	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Precharge	7
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Start Write : optional AP(A10=H)	6
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Start Read : optional AP(A10=H)	6
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Termination Burst: Start the Precharge	
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Termination Burst: Start Write(optional AP)	8,9
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Termination Burst: Start Read(optional AP)	8
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Termination Burst: Start the Precharge	10
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Termination Burst: Start Write(optional AP)	8
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Termination Burst: Start Read(optional AP)	8,9
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

CURRENT STATE TRUTH TABLE (Sheet 2 of 3)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,BA1	A11-A0	Description		
Read with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	12
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	12
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Precharging	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	No Operation: Bank(s) idle after tRP	
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,12
	L	H	H	H	X	X	No Operation	No Operation: Bank(s) idle after tRP	
	H	X	X	X	X	X	Device Deselect	No Operation: Bank(s) idle after tRP	
Row Activating	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,11,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,12
	L	H	H	H	X	X	No Operation	No Operation: Row Active after tRCD	
	H	X	X	X	X	X	Device Deselect	No Operation: Row Active after tRCD	

CURRENT STATE TRUTH TABLE (Sheet 3 of 3)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,BA1	A11-A0	Description		
Write Recovering	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Start Write: Optional AP(A10=H)	
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Start Read: Optional AP(A10=H)	9
	L	H	H	H	X	X	No Operation	No Operation: Row Active after tDPL	
	H	X	X	X	X	X	Device Deselect	No Operation: Row Active after tDPL	
Write Recovering with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,9,12
	L	H	H	H	X	X	No Operation	No Operation: Precharge after tDPL	
	H	X	X	X	X	X	Device Deselect	No Operation: Precharge after tDPL	
Refreshing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	13
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	13
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	13
	L	H	H	H	X	X	No Operation	No Operation: idle after tRC	
	H	X	X	X	X	X	Device Deselect	No Operation: idle after tRC	
Mode Register Accessing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	13
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	13
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	13
	L	H	H	H	X	X	No Operation	No Operation: idle after 2 clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation: idle after 2 clock cycles	

Note :

1. H: Logic High, L: Logic Low, X: Don't care, BA: Bank Address, AP: Auto Precharge.
2. All entries assume that CKE was active during the preceding clock cycle.
3. If both banks are idle and CKE is inactive, then in power down cycle
4. Illegal to bank in specified states. Function may be legal in the bank indicated by Bank Address, depending on the state of that bank.
5. If both banks are idle and CKE is inactive, then Self Refresh mode.
6. Illegal if tRCD is not satisfied.
7. Illegal if tRAS is not satisfied.
8. Must satisfy burst interrupt condition.
9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
10. Must mask preceding data which don't satisfy tDPL.
11. Illegal if tRRD is not satisfied
12. Illegal for single bank, but legal for other banks in multi-bank devices.
13. Illegal for all banks.
14. Mode Register Set and Extended Mode Register Set is same command truth table except BA1.

CKE Enable(CKE) Truth TABLE

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0, BA1	A11-A0		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down mode exit, all banks idle	2
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
Deep Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	X	X	X	X	X	X	Deep Power Down mode exit	5
	L	L	X	X	X	X	X	X	Maintain Deep Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				3
	H	H	L	L	H	X				3
	H	H	L	L	L	H	X	X	Auto Refresh	
	H	H	L	L	L	L	Op Code		Mode Register Set	4
	H	L	H	X	X	X			Refer to the idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				3
	H	L	L	L	H	X				3
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L	Op Code		Mode Register Set	
	L	X	X	X	X	X	X	X	Power Down	4
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to operations of the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

Note : 1. For the given current state CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. When exiting power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high.
3. The address inputs depend on the command that is issued.
4. The Precharge Power Down mode, the Self Refresh mode, and the Mode Register Set can only be entered from the all banks idle state.
5. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. When exiting deep power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high and is maintained for a minimum 200μsec.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	-25 ~ 85	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 3.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITION (TA=-25 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	V_{DD}	2.3	2.5	2.7	V	1
Power Supply Voltage	V_{DDQ}	1.65	-	2.7	V	1, 2
Input High Voltage	V_{IH}	1.40	-	V_{DDQ}+0.3	V	1, 2, 3
Input Low Voltage	V_{IL}	-0.3	-	0.55	V	1, 2, 3

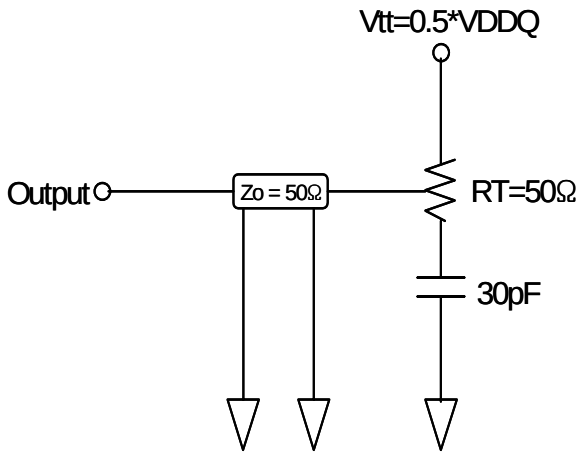
Note : 1. All Voltages are referenced to V_{SS} = 0V
2. V_{DDQ} must not exceed the level of V_{DD}
3. Internal V_{REF} = 0.9V

AC OPERATING CONDITION (TA=-25 to 85°C, 2.3V ≤V_{DD} ≤2.7V, V_{SS}=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	VIH / VIL	0.9*VDDQ/0.2	V	
Input Timing Measurement Reference Level Voltage	Vtrip	0.5*VDDQ	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	0.5*VDDQ	V	
Output Load Capacitance for Access Time Measurement	CL	Note 1	pF	1

Note : 1. Out Put Load Circuit : See the next page

OUTPUT LOAD CIRCUIT



CAPACITANCE (TA=25 C, f=1MHz, HY5xxxxxF Seires)

Parameter	Pin	Symbol	-H		-/8/P/S/B		Unit
			Min	Max	Min	Max	
Input capacitance	CLK	C_{I1}	TBD	TBD	2.5	4.0	pF
	A0~A11, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM0~3	C_{I2}	TBD	TBD	2.5	4.0	pF
Data input/output capacitance	DQ0 ~ DQ31	$C_{I/O}$	TBD	TBD	4.0	6.5	pF

DC CHARACTERISTICS I (TA= -25 to 85C)

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	I_{LI}	-1	1	μA	1
Output Leakage Current	I_{LO}	-1	1	μA	2
Output High Voltage	V_{OH}	VDDQ - 0.2	-	V	3
Output Low Voltage	V_{OL}	-	0.2	V	4

Note : 1. $V_{IN} \leq$ VDDQ. All other pins are not tested under V_{IN}=0V.
2. D_{OUT} is disabled. 0 $\leq V_{OUT} \leq$ VDDQ
3. IOUT = - 0.1mA
4. IOUT = + 0.1mA

DC CHARACTERISTICS II (TA= -25 to 85C)

Parameter	Symbol	Test Condition	Speed					Unit	Note
			-H	-8	-P	-S	-B		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA	TBD	90	75	75	75	mA	1
Precharge Standby Current in power down mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns	1.5					mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞	0.6						
Precharge Standby Current in non power down mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	11					mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	5						
Active Standby Current in power down mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns	5					mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞	5						
Active Standby Current in non power down mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	15					mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	15						
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	TBD	150	130	130	130	mA	1
Auto Refresh Current	IDD5	tRC ≥ tRC(min), All banks active	TBD	155	155	125	125	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V	See the next page table					mA	3
Standby Current in Deep Power Down Mode	TBD	TBD	TBD					μA	

Note : 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRRC (Refresh $\overline{RAS}$ cycle time) is shown at AC CHARACTERISTICS II.
3. See the tables of next page for more specific IDD6 current values.
- Normal Power : HY5W2A2F / HY57W2A3220T Series
- Low Power : HY5W2A2LF / HY57W2A3220LT Series
- Super Low Power : HY5W2A2SF / HY57W2A3220ST Series
- Standard Part : HY5W22F / HY57W283220T Series

DC CHARACTERISTICS III - Normal (IDD6) (VDD=2.5V, VDDQ=1.8V & 2.5V, VSS=0V)

Temp. (°C)	Memory Array			Unit
	4 Banks	2 Banks	1 Bank	
85	2000	520	440	μA
70	600	380	330	μA
-25~45	400	310	270	μA

DC CHARACTERISTICS III - Low Power (IDD6) (VDD=2.5V, VDDQ=1.8V & 2.5V, VSS=0V)

Temp. (°C)	Memory Array			Unit
	4 Banks	2 Banks	1 Bank	
85	550	450	320	μA
70	430	330	280	μA
-25~45	350	280	250	μA

DC CHARACTERISTICS III - Super Low Power (IDD6) (VDD=2.5V, VDDQ=1.8V & 2.5V, VSS=0V)

Temp. (°C)	Memory Array			Unit
	4 Banks	2 Banks	1 Bank	
85	370	TBD	TBD	μA
70	TBD	TBD	TBD	μA
-25~45	TBD	TBD	TBD	μA

DC CHARACTERISTICS III - Standard part (IDD6) (VDD=2.5V, VDDQ=1.8V & 2.5V, VSS=0V)

Temp. (°C)	Memory Array	Unit
	4 Banks	
-25~85	< 2000	μA

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	H		8		P		S		B		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CAS Latency=3	tCK3	7.5	1000	8	1000	10	1000	10	1000	15	1000	ns	
	CAS Latency=2	tCK2	10		10		10		12		15		ns	
Clock High Pulse Width		tCHW	2.5	-	3	-	3	-	3	-	3.5	-	ns	1
Clock Low Pulse Width		tCLW	2.5	-	3	-	3	-	3	-	3.5	-	ns	1
Access Time From Clock	CAS Latency=3	tAC3	-	5.4	-	6	-	7	-	7	-	9	ns	2
	CAS Latency=2	tAC2	-	7	-	7	-	7	-	8	-	9	ns	
Data-out Hold Time		tOH	1.5	-	2.0	-	3	-	3	-	3	-	ns	
Data-Input Setup Time		tDS	1.5	-	2.0	-	2	-	2	-	2	-	ns	1
Data-Input Hold Time		tDH	0.8	-	1.0	-	1	-	1	-	1	-	ns	1
Address Setup Time		tAS	1.5	-	2.0	-	2	-	2	-	2	-	ns	1
Address Hold Time		tAH	0.8	-	1.0	-	1	-	1	-	1	-	ns	1
CKE Setup Time		tCKS	1.5	-	2.0	-	2	-	2	-	2	-	ns	1
CKE Hold Time		tCKH	0.8	-	1.0	-	1	-	1	-	1	-	ns	1
Command Setup Time		tCS	1.5	-	2.0	-	2	-	2	-	2	-	ns	1
Command Hold Time		tCH	0.8	-	1.0	-	1	-	1	-	1	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1	-	1	-	1	-	1	-	1	-	ns	
CLK to Data Output in High-Z Time	CAS Latency=3	tOHZ3	2.7	5.4	2.5	6	3	6	3	6	3	9	ns	
	CAS Latency=2	tOHZ2	2.7	7	2.5	7	3	6	3	6	3	9	ns	

Note : 1. Assume tR / tF (input rise and fall time) is 1ns. If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter.
2. Access time to be measured with input signals of 1v/ns edge rate, from 0.8v to 0.2v. If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter.

AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Symbol	H		8		P		S		B		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time		tRC	65	-	68	-	70	-	70	-	90	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	20	-	20	-	20	-	30	-	30	-	ns	
$\overline{RAS}$ Active Time		tRAS	45	100K	48	100K	50	100K	50	100K	60	100K	ns	
$\overline{RAS}$ Precharge Time		tRP	20	-	20	-	20	-	30	-	30	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	15	-	20	-	20	-	20	-	20	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	1	-	1	-	1	-	tCK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	0	-	0	-	tCK	
Data-in to Precharge Command		tDPL	2	-	1	-	1	-	1	-	1	-	tCK	
Data-In to Active Command		tDAL	5	-	3	-	3	-	3	-	3	-	tCK	
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	2	-	tCK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	0	-	0	-	tCK	
MRS to New Command		tMRD	2	-	2	-	2	-	2	-	2	-	tCK	
Precharge to Data Output High-Z	$\overline{CAS}$ Latency=3	tPROZ3	3	-	3	-	3	-	3	-	3	-	tCK	
	$\overline{CAS}$ Latency=2	tPROZ2	2		2		2		2		2		tCK	
Power Down Exit Time		tDPE	1	-	1	-	1	-	1	-	1	-	tCK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	1	-	1	-	tCK	1
Refresh Time		tREF	-	64	-	64	-	64	-	64	-	64	ns	

Note : 1. A new command can be given tRRC after self refresh exit.

Special Operation for Low Power Consumption

Deep Power Down Mode

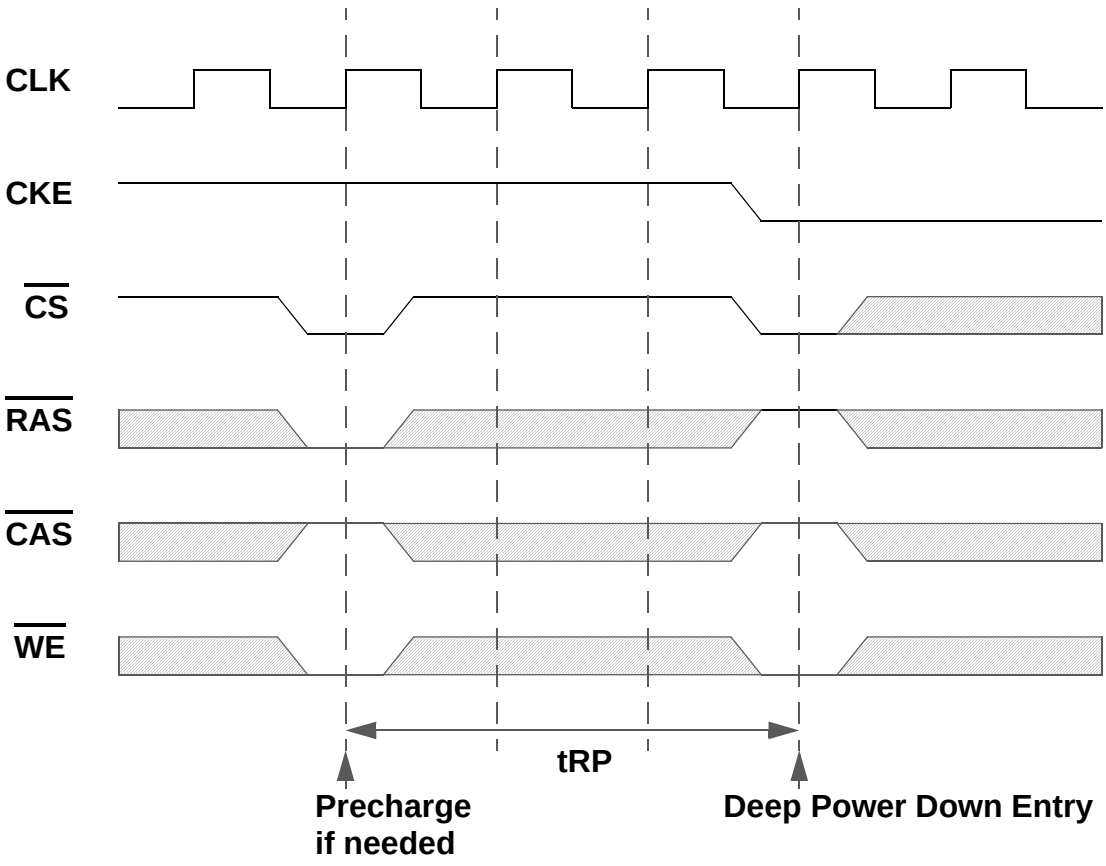
Deep Power Down Mode is an operating mode to achieve maximum power reduction by cutting the power of the whole memory array of the devices.
Data will not be retained once the device enters Deep Power Down Mode.
Full initialization is required when the device exits from Deep Power Down Mode.

Truth Table

Current State	Command	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Idle	Deep Power Down Entry	H	L	L	H	H	L
Deep Power Down	Deep Power Down Exit	L	H	X	X	X	X

Deep Power Down Mode Entry

The Deep Power Down Mode is entered by having /CS and /WE held low with /RAS and /CAS high at the rising edge of the clock, while CKE is low. The following diagram illustrates deep power down mode entry.



Deep Power Down Mode (Continued)

Deep Power Down Mode Exit Sequence

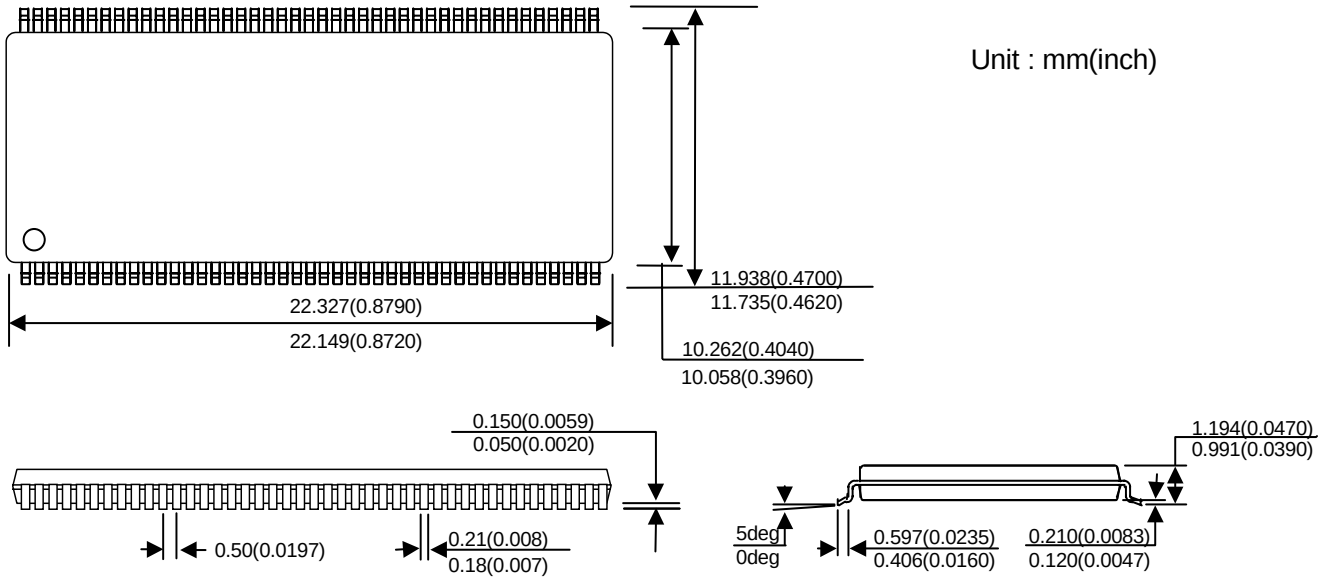
The Deep Power Down mode is exited by asserting CKE high.
After the exit, the following sequence is needed to enter a new command.

1. Maintain NOP input conditions for a minimum of 200μsec
2. Issue precharge commands for all banks of the device
3. Issue 8 or more auto refresh commands
4. Issue a mode register set command to initialize the mode register
5. Issue an extended mode register set command to initialize the extended mode register

The following timing diagram illustrates deep power down mode exit sequence.

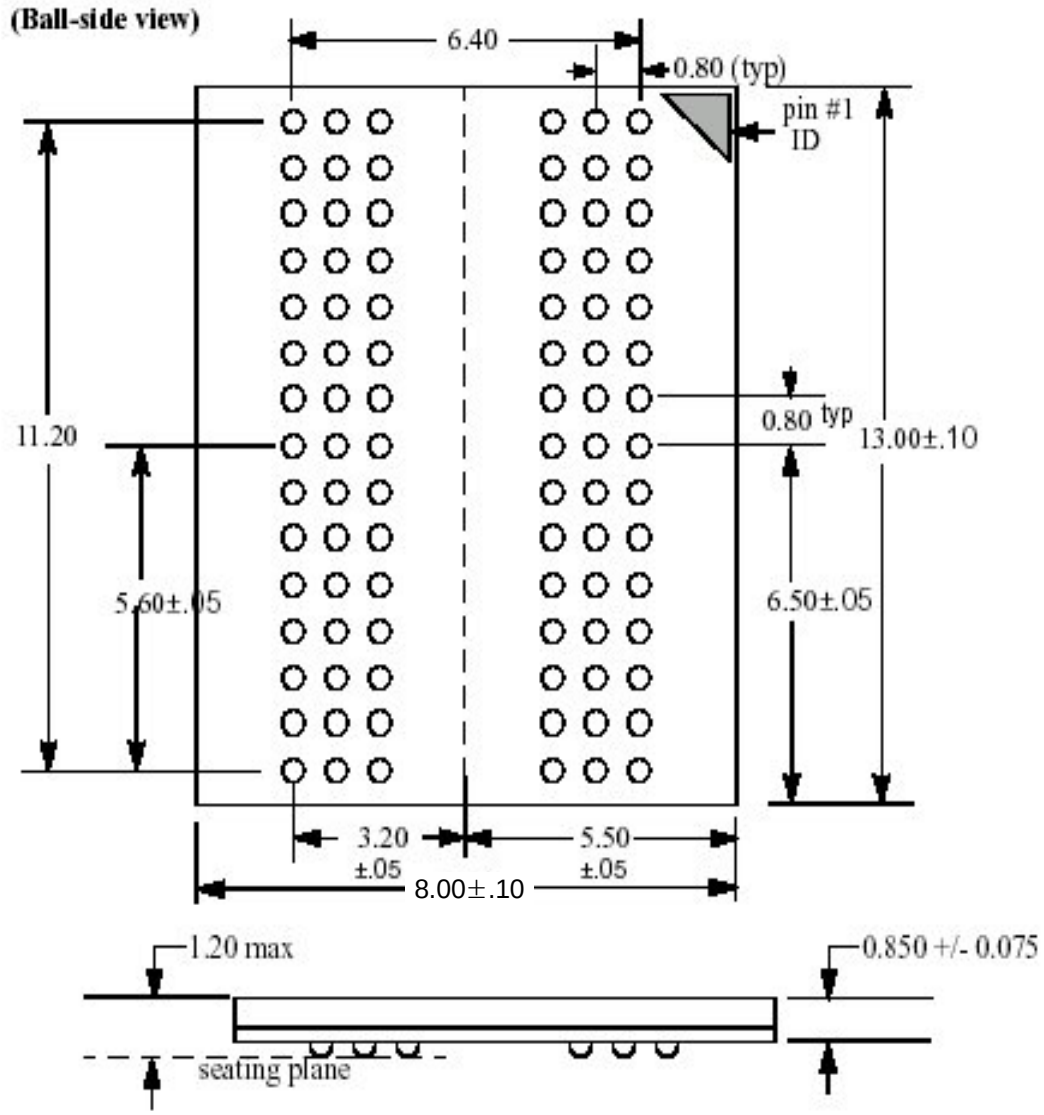
PACKAGE INFORMATION (HY57W2A3220T Series)

400mil 86pin Thin Small Outline Package



PACKAGE INFORMATION (HY5W2A2F Series)

90Ball FBGA with 0.8mm of pin pitch



All dimensions are in mm.