

8-Channel High Voltage Analog Switch

Ordering Information

$V_{PP} - V_{NN}$	Package Options		
	28-pin plastic DIP	28-lead plastic chip carrier	Die
160V	HV2216P	HV2216PJ	HV2216X

Features

- ☐ HVCMOS® technology for high performance
- ☐ Very low quiescent power dissipation – 10µA
- ☐ Output On-resistance typically 22 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ -50dB typical output off isolation at 5MHz
- ☐ CMOS logic circuitry for low power
- ☐ Excellent noise immunity
- ☐ On-chip shift register, latch and clear logic circuitry
- ☐ Flexible high voltage supplies
- ☐ Surface mount package available

General Description

Not recommended for new designs. Please use HV20220 for all new designs.

This device is an 8-channel high-voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feedthrough noise, Latch Enable (LE) should be left high until all bits are clocked in. Using HVCMOS technology, this switch combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

This IC is suitable for various combinations of high voltage supplies, e.g., for HV2216 +40V/-120V, or +80V/-80V or +150V/-10V.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +18V
$V_{PP} - V_{NN}$ Supply voltage	174V
V_{PP} Positive high voltage supply	-0.5V to +160V
V_{NN} Negative high voltage supply	+0.5V to -160V
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog Signal Range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	1.2W

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Electrical Characteristics

DC Characteristics (over recommended operating conditions unless otherwise noted)

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions	
		min	max	min	typ	max	min	max			
Small Signal Switch (ON) Resistance	R _{ONS}		30		26	32		35	ohms	I _{SIG} = 5mA	V _{PP} = 40V,
			25		22	27		32		I _{SIG} = 200mA	V _{NN} = −120V
			25		22	27		30		I _{SIG} = 5mA	V _{PP} = 80V,
			18		18	20		23		I _{SIG} = 200mA	V _{NN} = −80V
			23		20	25		30		I _{SIG} = 5mA	V _{PP} = 150V,
			22		16	25		27		I _{SIG} = 200mA	V _{NN} = −10V
Small Signal Switch (ON) Resistance Matching	ΔR _{ONS}		20		5.0	20		20	%	I _{SW} = 5mA, V _{PP} = 80V, V _{NN} = −80V	
Large Signal Switch (ON) Resistance	R _{ONL}				13	22			ohms	V _{SIG} = V _{PP} −10V, I _{SIG} = 1A	
Switch Off Leakage Per Switch	I _{SOL}		5.0		1.0	10		15	μA	V _{SIG} = V _{PP} −10V and V _{NN} +10V	
DC Offset Switch Off			300		100	300		300	mV	R _L = 100KΩ	
DC Offset Switch On			500		100	500		500	mV	R _L = 100KΩ	
Pos. HV Supply Current	I _{PPQ}				10	50			μA	ALL SWS OFF	
Neg. HV Supply Current	I _{NNQ}				-10	-50			μA	ALL SWS OFF	
Pos. HV Supply Current	I _{PPQ}				10	50			μA	ALL SWS ON I _{SW} = 5mA	
Neg. HV Supply Current	I _{NNQ}				-10	-50			μA	ALL SWS ON I _{SW} = 5mA	
Switch Output Peak Current			3.0		3.0	2.0		2.0	A	V _{SIG} ≤ 0.1% duty cycle	
Output Switch Frequency	f _{SW}					50			KHz	Duty Cycle = 50%	
I _{PP} Supply Current	I _{PP}		6.5			7.0		8.0	mA	V _{PP} = 40V, V _{NN} = −120V	50KHz Output Switching Frequency with no load
			4.0			5.0		5.5		V _{PP} = 80V, V _{NN} = −80V	
			4.0			5.0		5.5		V _{PP} = 150V, V _{NN} = −10V	
I _{NN} Supply Current	I _{NN}		6.5			7.0		8.0	mA	V _{PP} = 40V, V _{NN} = −120V	
			4.0			5.0		5.5		V _{PP} = 80V, V _{NN} = −80V	
			4.0			5.0		5.5		V _{PP} = 150V, V _{NN} = −10V	
Logic Supply Average Current	I _{DD}		6.0		4.0	6.0		6.0	mA	f _{CLK} = 3MHz,	
Logic Supply Quiescent Current	I _{DDQ}		10			10		10	μA		
Data Out Source Current	I _{SOR}	0.45		0.45	0.70		0.40		mA	V _{OUT} = V _{DD} - 0.7V	
Data Out Sink Current	I _{SINK}	0.45		0.45	0.70		0.40		mA	V _{OUT} = 0.7V	

Electrical Characteristics

AC Characteristics (over operating conditions $V_{DD} = 15V$, unless otherwise noted)

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Time to Turn Off V_{SIG}^*	$t_{SIG(OFF)}$			200					ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}	150		150			150		ns	
Time Width of $\overline{LE}$	t_{WLE}	150		150			150		ns	
Clock Delay Time to Data Out	t_{DO}		300		150	330		350	ns	
Time Width of CL	t_{WCL}	150		150			150		ns	
Set Up Time Data to Clock	t_{SU}	15		15	8.0		20		ns	
Hold Time Data from Clock	t_h	35		35			35		ns	
Clock Freq	f_{CLK}		3.0			3.0		3.0	MHz	50% duty cycle $f_{DATA} = f_{CLK}/2$
Turn On Time			2.0			2.0		2.0	μs	$V_{SIG} = V_{PP} -10V$, $R_L = 10K\Omega$
Turn Off Time			3.0			3.0		3.0	μs	$V_{SIG} = V_{PP} -10V$, $R_L = 10K\Omega$
Maximum V_{SIG} Slew Rate	dv/dt		10			10		10	V/ns	$V_{PP} = 150V$, $V_{NN} = -10V$
			10			10		10		$V_{PP} = 80V$, $V_{NN} = -80V$
			10			10		10		$V_{PP} = 40V$, $V_{NN} = -120V$
Off Isolation	KO	-30		-30	-33		-30		dB	$f = 5MHz$, 1K Ω //15pF load
		-45		-45	-50		-45		dB	$f = 5MHz$, 50 Ω load
Switch Crosstalk	K_{CR}	-60		-60	-70		-60		dB	$f = 5MHz$, 50 Ω load
Output Switch Isolation Diode Current	I_{ID}		300			300		300	mA	300ns pulse width, 2.0% duty cycle
Off Capacitance SW to GND	$C_{SG(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	0V, 1MHz
On Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, 1MHz

*Time required for analog signal to turn off before output switch turns off (critical timing).

Electrical Characteristics

AC Characteristics (over operating conditions $V_{DD} = 15V$, unless otherwise noted)

Characteristics	Sym	+25°C			Units	Test Conditions
		min	typ	max		
Output Voltage Spike	$+V_{SPK}$		1.0		V	$V_{PP} = 40V$, $V_{NN} = -120V$ $R_L = 50\Omega$
	$-V_{SPK}$		3.5			
	$+V_{SPK}$		12			$V_{PP} = 80V$, $V_{NN} = -80V$ $R_L = 50\Omega$
	$-V_{SPK}$		18			
	$+V_{SPK}$		6.0			$V_{PP} = 150V$, $V_{NN} = -10V$ $R_L = 50\Omega$
	$-V_{SPK}$		9.0			
Charge Injection	Q		1700		pC	$V_{PP} = 80V$, $V_{NN} = -80V$, $V_{SIG} = 0V$
			850			$V_{PP} = 80V$, $V_{NN} = -80V$, $V_{SIG} = 70V$
			600			$V_{PP} = 80V$, $V_{NN} = -80V$, $V_{SIG} = -70V$

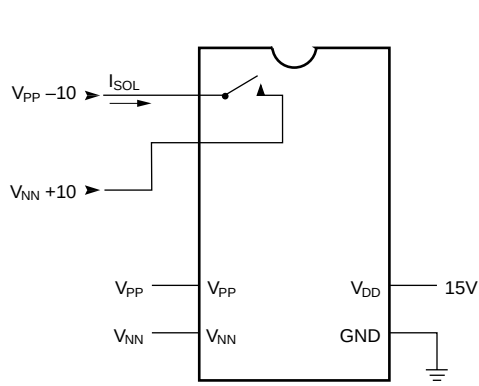
Operating Conditions

Symbol	Parameter	Value
V_{DD}	Logic power supply voltage ^{1, 3}	10.0 V to 15.5 V
V_{PP}	Positive high voltage supply ^{1, 3}	40V to $V_{NN} + 160V$
V_{NN}	Negative high voltage supply ^{1, 3}	-10.0V to -120V
V_{IH}	High-level input voltage	$V_{DD} - 2V$ to V_{DD}
V_{IL}	Low-level input voltage	0V to 2.0V
V_{SIG}	Analog signal voltage peak to peak ²	$V_{NN} + 10V$ to $V_{PP} - 10$
T_A	Operating free air-temperature	0°C to 70°C

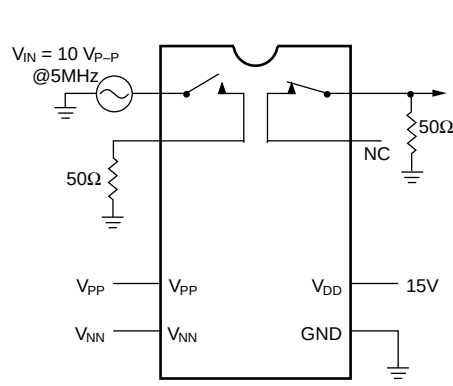
Notes:

- 1 Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
- 2 V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transision.
- 3 Rise and fall times of power supplies V_{DD} , V_{PP} , and V_{NN} should not be less than 1.0msec.

Test Circuits

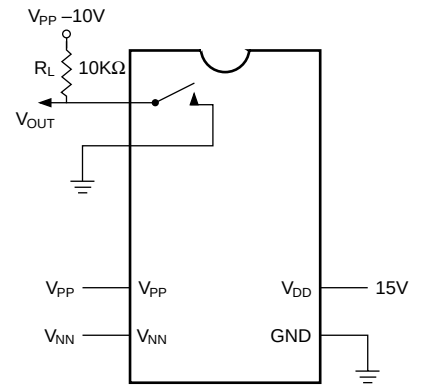
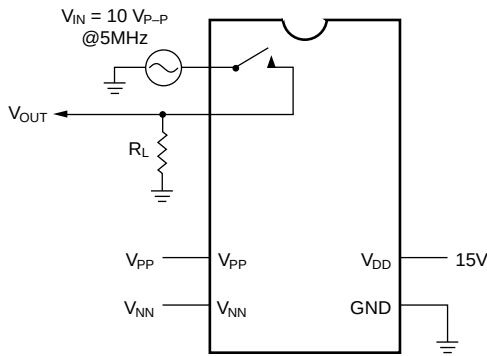


Switch OFF Leakage



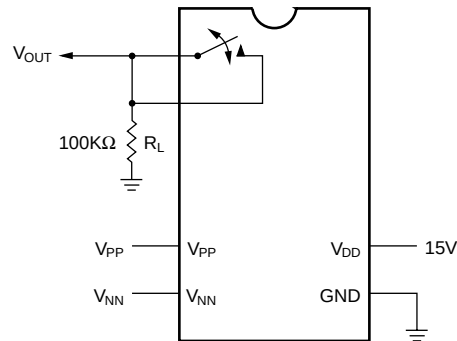
$$K_{CR} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Crosstalk

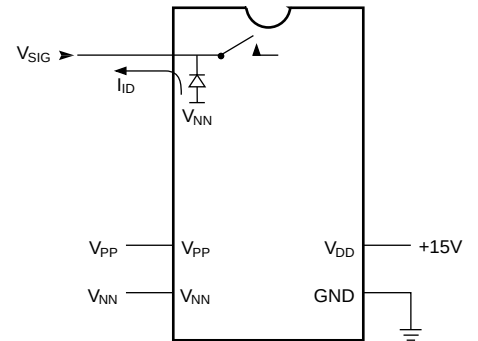
 T_{ON}/T_{OFF} Test Circuit

$$K_O = 20 \log \frac{V_{OUT}}{V_{IN}}$$

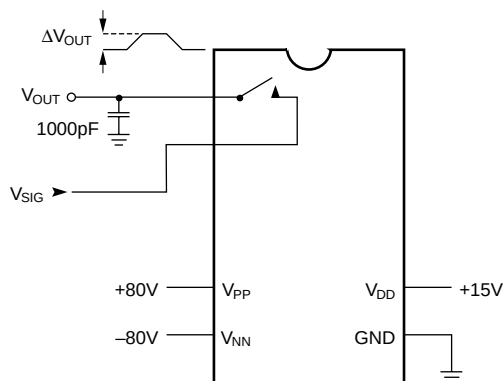
OFF Isolation



DC Offset ON/OFF

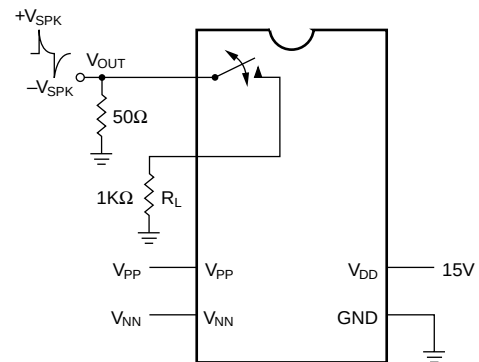


Isolation Diode Current



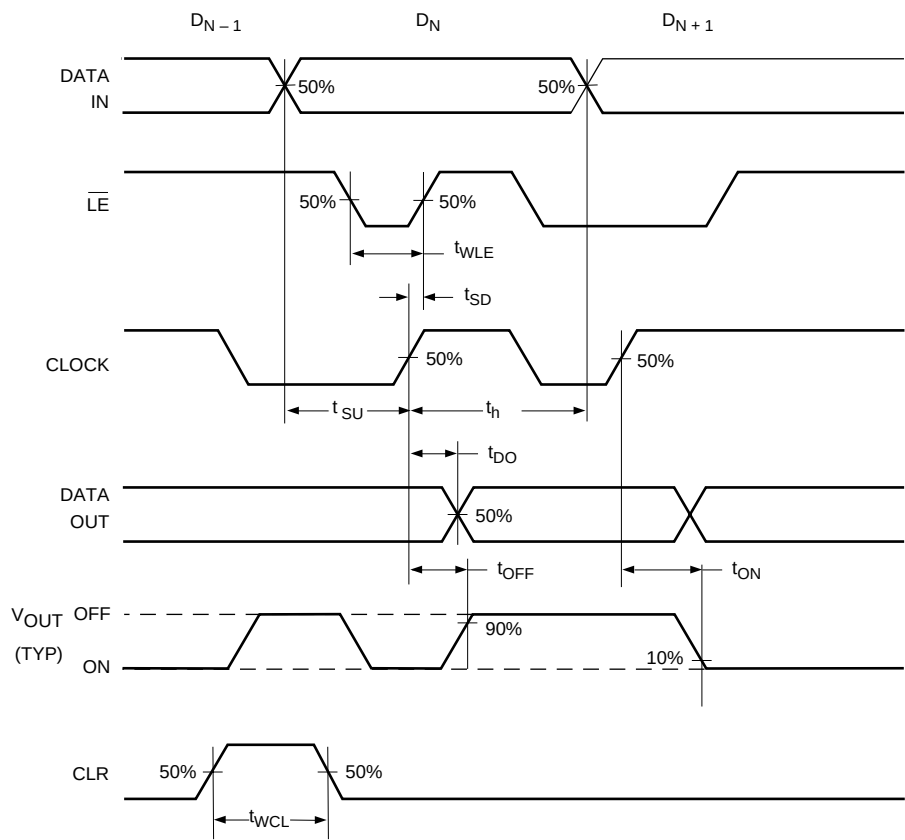
$$Q = 1000pF \times \Delta V_{OUT}$$

Charge Injection

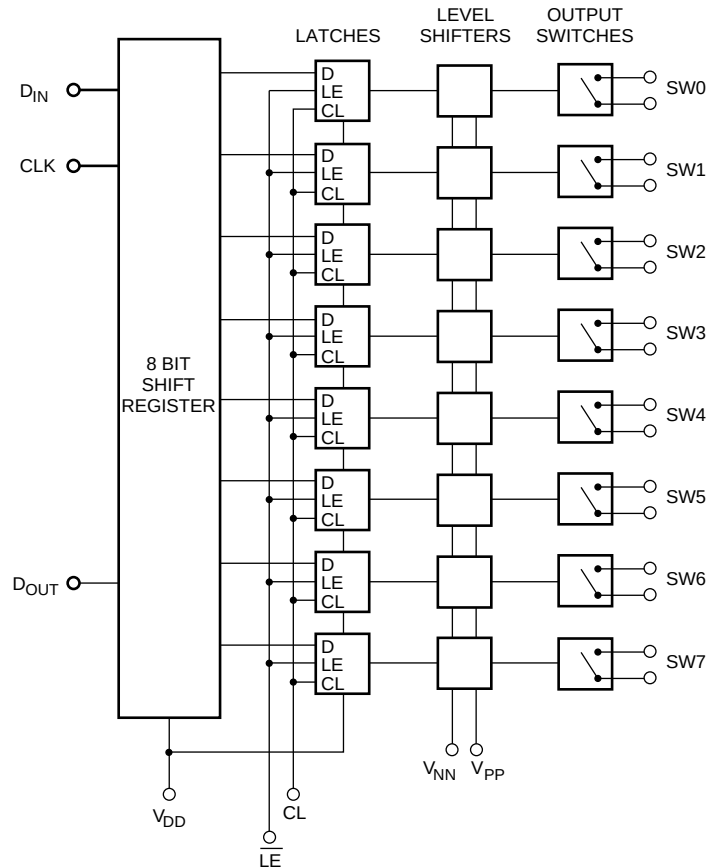


Output Voltage Spike

Logic Timing Waveforms



Logic Diagram



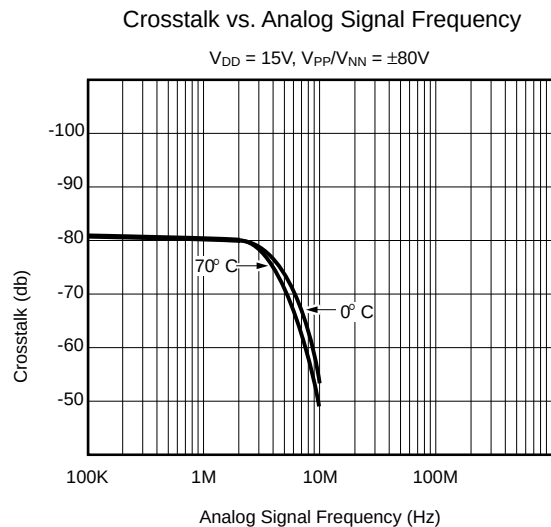
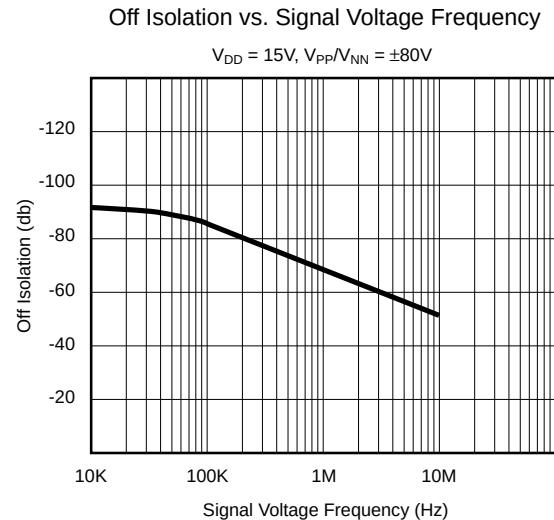
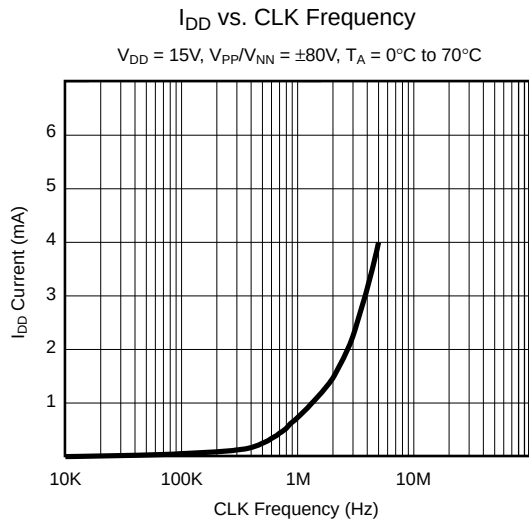
Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

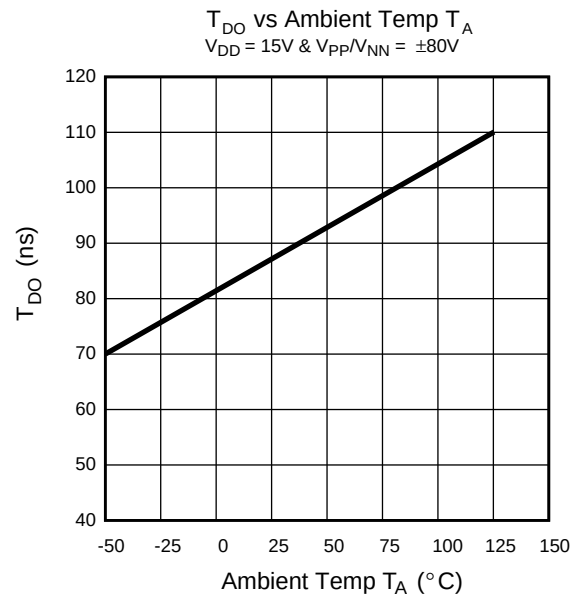
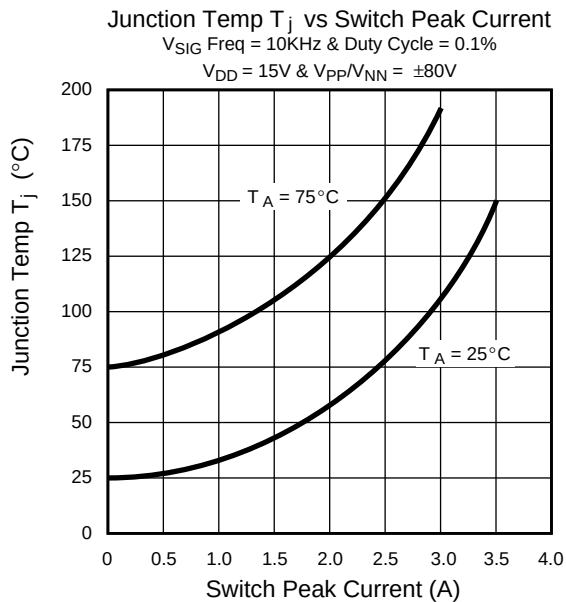
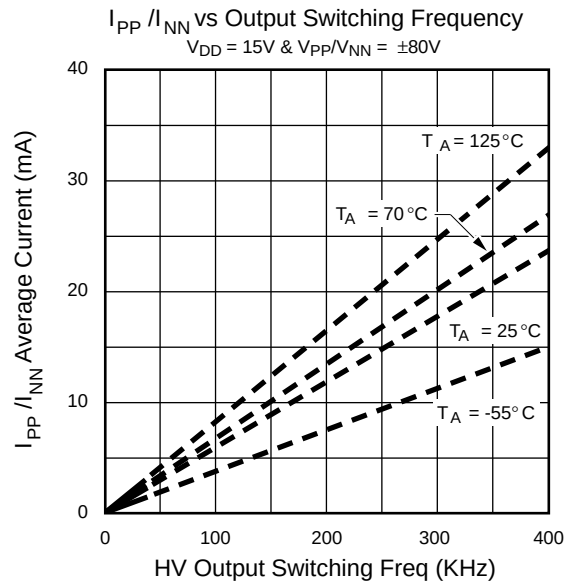
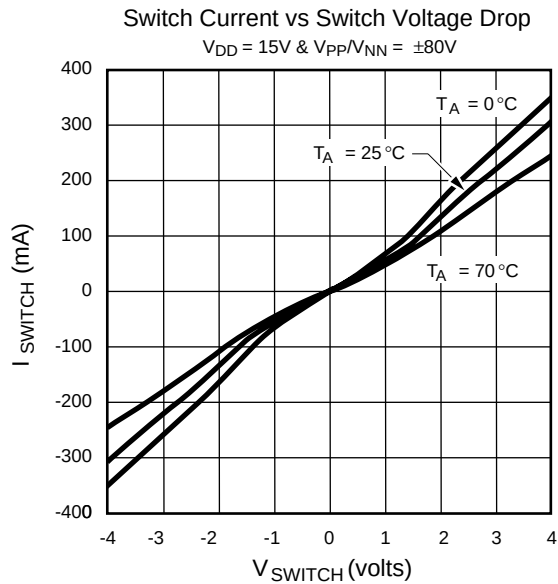
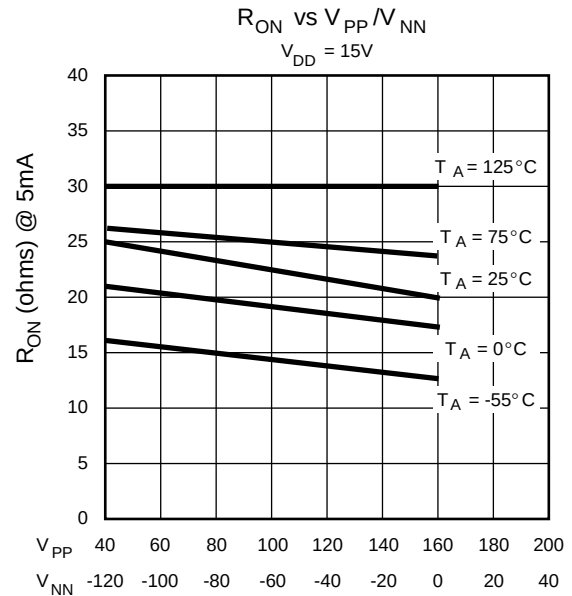
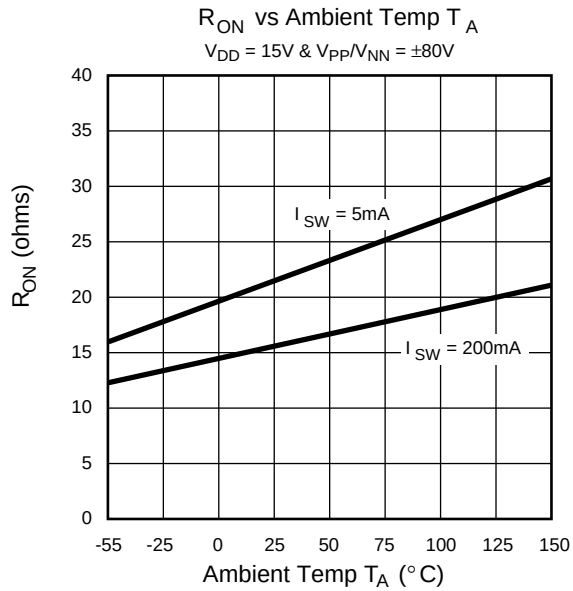
Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L→H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.
6. The clear input overrides all other inputs.

Typical Performance Curves



Typical Performance Curves

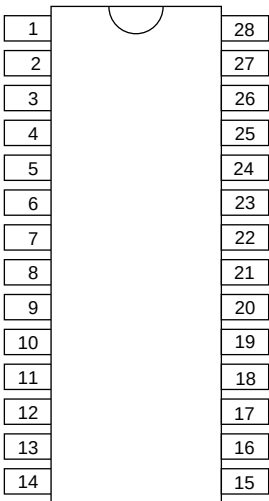


Pin Configurations

28-Pin DIP

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D _{IN}
3	SW2	17	CLK
4	SW2	18	LE
5	SW1	19	CL
6	SW1	20	D _{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V _{PP}	23	SW6
10	V _{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V _{DD}	27	SW4
14	N/C	28	SW4

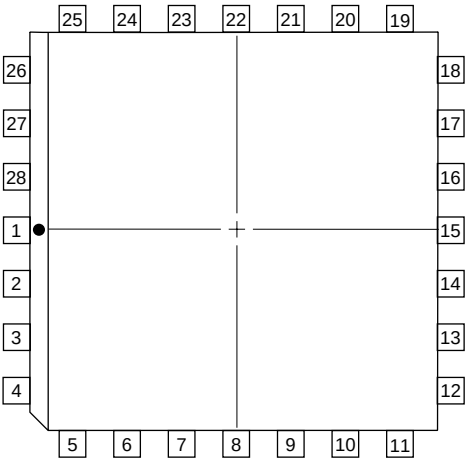
Package Outlines



top view
28-pin DIP

28-Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D _{IN}
3	SW2	17	CLK
4	SW2	18	LE
5	SW1	19	CL
6	SW1	20	D _{OUT}
7	SW0	21	SW7
8	SW0	22	SW7
9	V _{PP}	23	SW6
10	V _{NN}	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	V _{DD}	27	SW4
14	N/C	28	SW4



top view
28-pin J-Lead Package