Low Charge Injection
8-Channel High Voltage Analog Switch

Ordering Information

Operating V_{PP}	$V_{PP} - V_{NN}$	Package Options	
		28-lead plastic chip carrier	Die
40V to 80V	160V	HV21716PJ	HV21716X
80V to 150V	160V	HV21816PJ	HV21816X

Features

- ☐ HVCMOS® technology for high performance
- ☐ Low charge injection
- ☐ Very low quiescent power dissipation – 10µA
- ☐ Output On-resistance typically 22 ohms
- ☐ Low parasitic capacitances
- ☐ DC to 10MHz analog signal frequency
- ☐ -50dB typical output off isolation at 5MHz
- ☐ CMOS logic circuitry for low power
- ☐ Excellent noise immunity
- ☐ On-chip shift register and latch logic circuitry
- ☐ Flexible high voltage supplies
- ☐ Surface mount package available

General Description

Not recommended for new designs. Please use HV20220 for all new designs.

This device is a low charge injection 8-channel high-voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feedthrough noise, Latch Enable ($\overline{LE}$) should be left high until all bits are clocked in. Using HVCMOS technology, this switch combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Absolute Maximum Ratings*

V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V
V_{PP} positive high voltage supply	-0.5V to +160V
V_{NN} negative high voltage supply	+0.5V to -160V
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	1.2W

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V, and V_{DD}= 15V unless otherwise noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Small Signal Switch (ON) Resistance	R_{ONS}		24		22	25		28	ohms	I_{SIG} = 5mA
	R_{ONS}		18		18	20		23	ohms	I_{SIG} = 200mA
Small Signal Switch (ON) Resistance Matching	ΔR_{ONS}		20		5.0	20		20	%	I_{SW} = 5mA
Large Signal Switch (ON) Resistance	R_{ONL}				13	22			ohms	$V_{SIG} = V_{PP}$ -10V, I_{SIG} = 1.0A
Switch Off Leakage Per Switch	I_{SOL}		5.0		1.0	10		15	µA	$V_{SIG} = V_{PP}$ -10V and V_{NN} +10V
DC Offset Switch Off			300		100	300		300	mV	R_L = 100KΩ
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	
Pos. HV Supply Current	I_{PPQ}				10	50			µA	ALL SWS ON I_{SW} = 5mA
Neg. HV Supply Current	I_{NNQ}				-10	-50			µA	
Switch Output Peak Current			3.0		3.0	2.0		2.0	A	$V_{SIG} \leq 0.1\%$ Duty Cycle
Output Switch Frequency	f_{SW}					50			KHz	Duty Cycle = 50%
I_{PP} Supply Current	I_{PP}		4.0		3.5	5.0		5.5	mA	HV output switching frequency = 50KHz
I_{NN} Supply Current	I_{NN}		4.0		3.5	5.0		5.5	mA	
Logic Supply Average Current	I_{DD}		6.0		4.0	6.0		6.0	mA	f_{CLK} = 3MHz
Logic Supply Quiescent Current	I_{DDQ}		10			10		10	µA	
Data Out Source Current	I_{SOR}	0.45		0.45	0.70		0.40		mA	$V_{OUT} = V_{DD}$ - 0.7V
Data Out Sink Current	I_{SINK}	0.45		0.45	0.70		0.40		mA	V_{OUT} = 0.7V

AC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Time to Turn Off V_{SIG}*	$t_{SIG\ (OFF)}$			0					ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}	150		150			150		ns	
Time Width of $\overline{LE}$	t_{WLE}	150		150			150		ns	
Clock Delay Time to Data Out	t_{DO}		175			175		190	ns	
Turn On Time	t_{ON}		3.0			3.0		3.0	µs	R_L = 10KΩ
Turn Off Time	t_{OFF}		5.0			5.0		5.0	µs	R_L = 10KΩ
Off Isolation	KO	-30		-30	-33		-30		dB	f = 5MHz, 1KΩ// 15pF load
		-45		-45	-50		-45		dB	f = 5MHz, 50Ω load
Clock Freq	f_{CLK}		5.0			5.0		5.0	MHz	50% duty cycle $f_{DATA} = f_{CLK}/2$
Set Up Time Data to Clock	t_{SU}	15		15	8.0		20		ns	
Hold Time Data from Clock	t_H	35		35			35		ns	
Switch Crosstalk	K_{CR}	-60		-60	-70		-60		dB	f = 5MHz, 50Ω load
Off Capacitance SW to GND	$C_{SG(OFF)}$	5.0	17	5.0	12	17	5.0	17	pF	0V, 1MHz
On Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, 1MHz
Output Voltage Spike	$+V_{SPK}$				150				mV	V_{PP} = +80V, V_{NN} = -80V, R_L = 50Ω
	$-V_{SPK}$				150					

* Time required for analog signal to turn off before output switch turns off (critical timing).

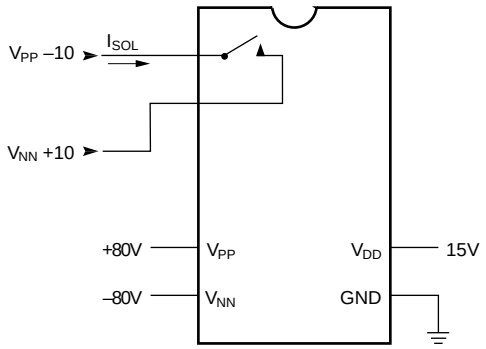
Operating Conditions*

Symbol	Device		Value
	HV21716	HV21816	
V_{PP}[1, 3]	X		40V to 80V
		X	80V to 150V
V_{NN}[1, 3]	X	X	-10V to V_{PP} -160V
V_{DD}[1, 3]	X	X	10V to 15.5V
V_{IH}	X	X	V_{DD} -2.0V to V_{DD}
V_{IL}	X	X	0V to 2.0V
V_{SIG}[2]	X	X	V_{NN} +10V to V_{PP} -10
T_A	X	X	0°C to 70°C

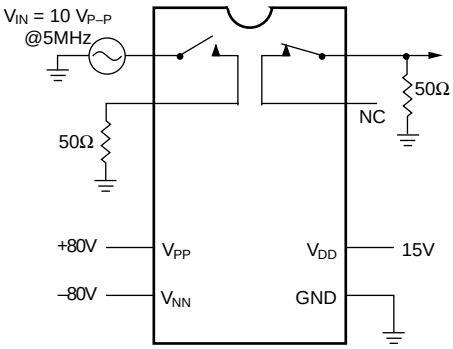
Notes:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transistion.
3. Rise and fall times of power supplies, $V_{DD,}$ $V_{PP,}$ and V_{NN} should not be less than 1.0msec.

Test Circuits

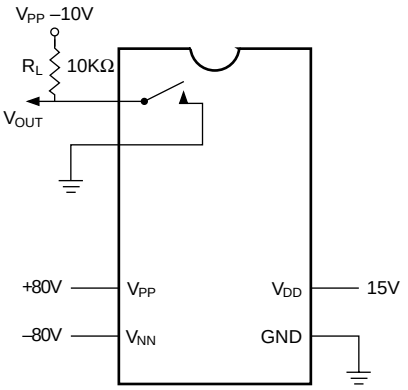


Switch OFF Leakage

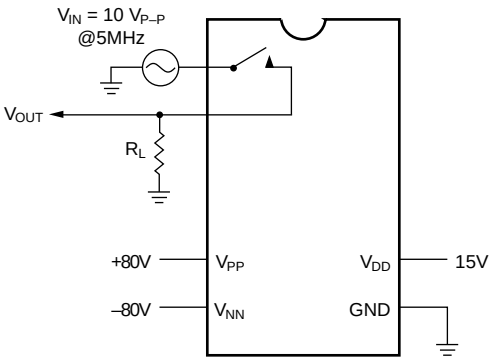


$K_{CR} = 20Log \frac{V_{OUT}}{V_{IN}}$

Crosstalk

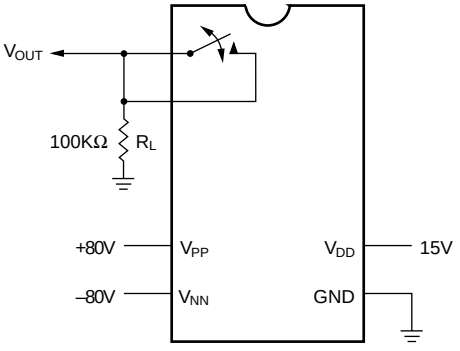


T_{ON}/T_{OFF}

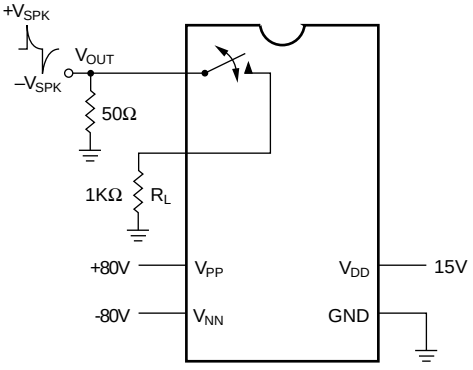


$K_O = 20Log \frac{V_{OUT}}{V_{IN}}$

OFF Isolation

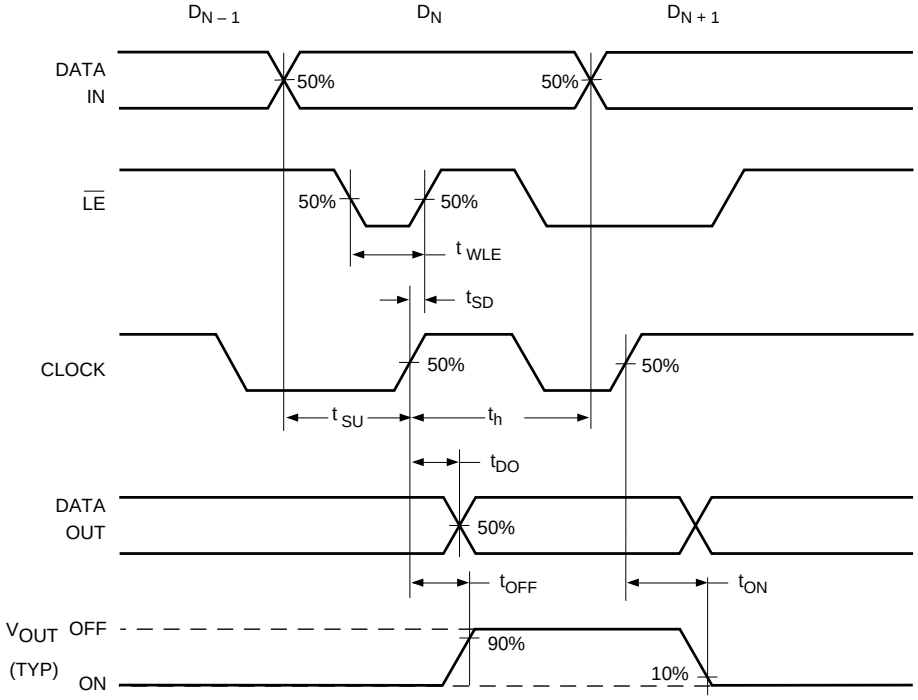


DC Offset ON/OFF

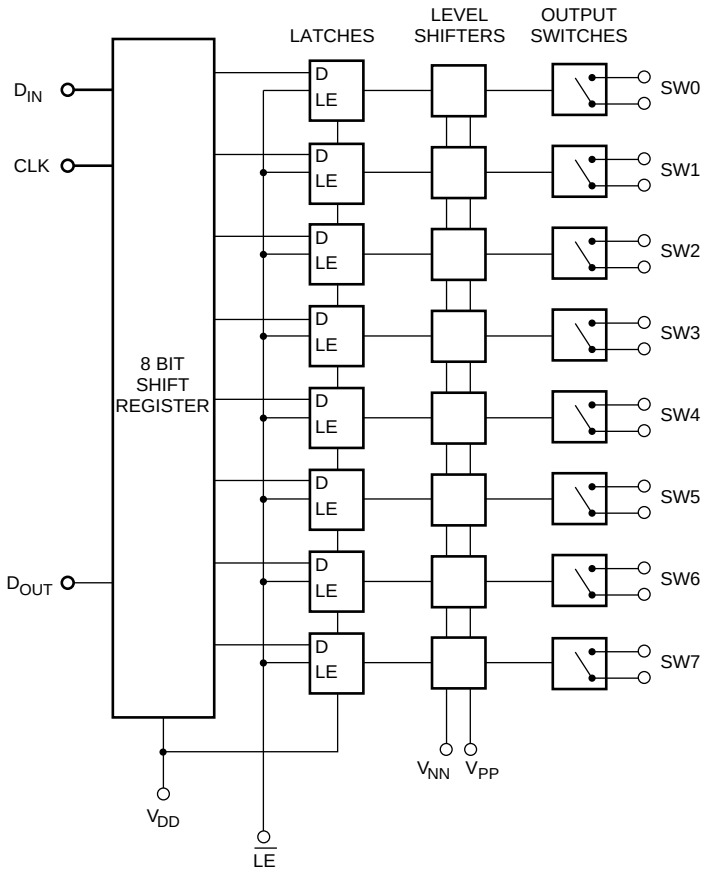


Output Voltage Spike

Logic Timing Waveforms



Logic Diagram



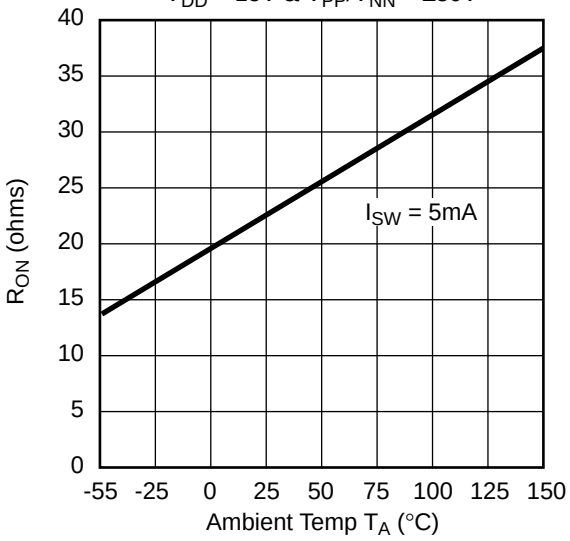
Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	OFF							
H								L	ON							
	L							L		OFF						
	H							L		ON						
		L						L			OFF					
		H						L			ON					
			L					L				OFF				
			H					L				ON				
				L				L					OFF			
				H				L					ON			
					L			L						OFF		
					H			L						ON		
						L		L							OFF	
						H		L							ON	
							L	L								OFF
							H	L								ON
X	X	X	X	X	X	X	X	H	HOLD PREVIOUS STATE							

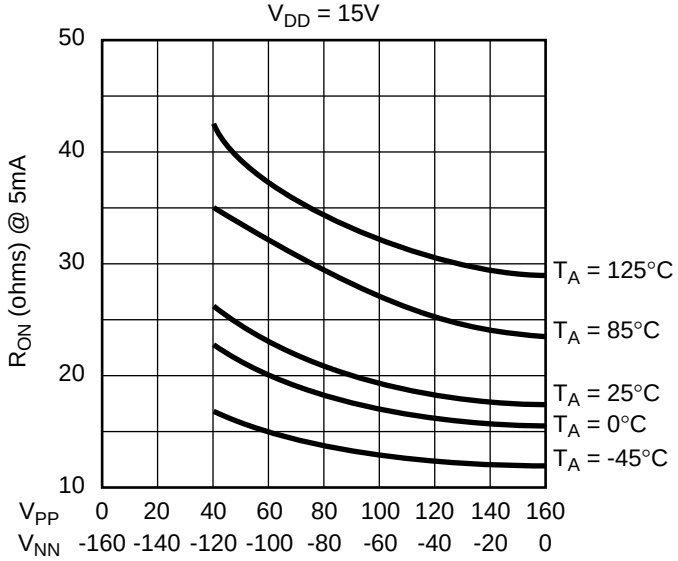
Notes:
1. The eight switches operate independently.
2. Serial data is clocked in on the L→ H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clockng has no effect on the switch states if $\overline{LE}$ is H.

Typical Performance Curves

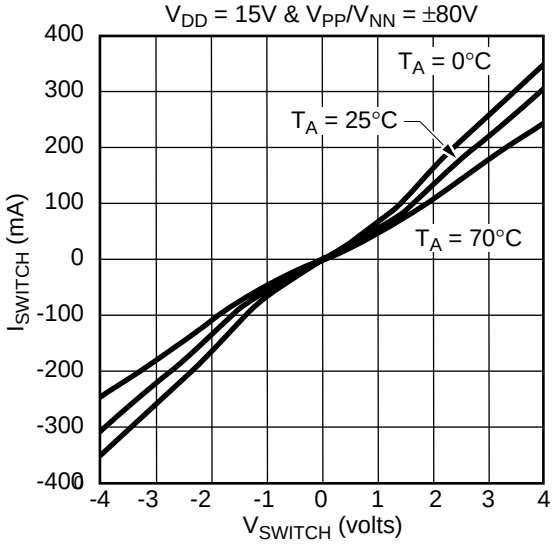
R_{ON} vs. Ambient Temp T_A
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



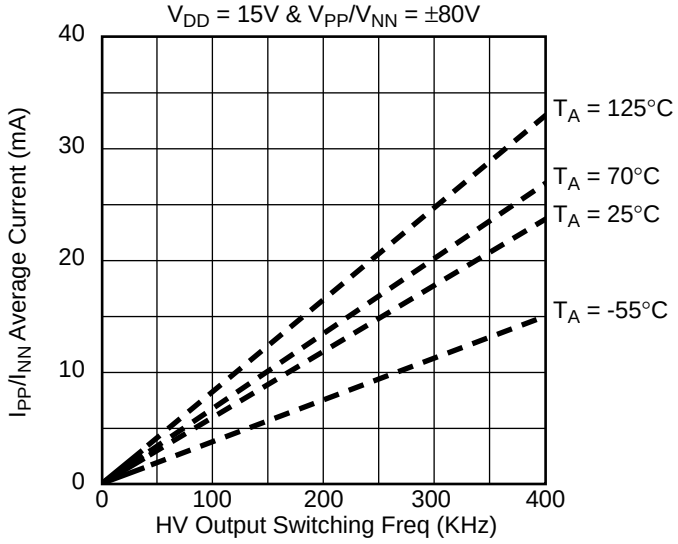
R_{ON} vs. V_{PP}/V_{NN}
V_{DD} = 15V



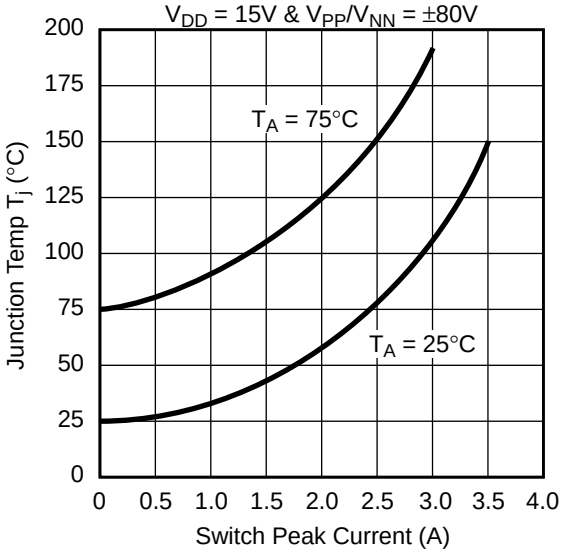
Switch Current vs. Switch Voltage Drop
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



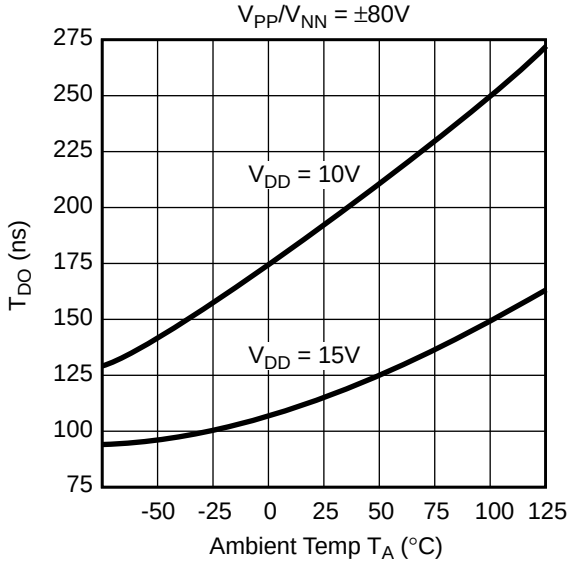
I_{PP}/I_{NN} vs. Output Switching Frequency
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V



Junction Temp T_j vs. Switch Peak Current
V_{SIG} Freq = 10KHz & Duty Cycle = 0.1%
V_{DD} = 15V & V_{PP}/V_{NN} = ±80V

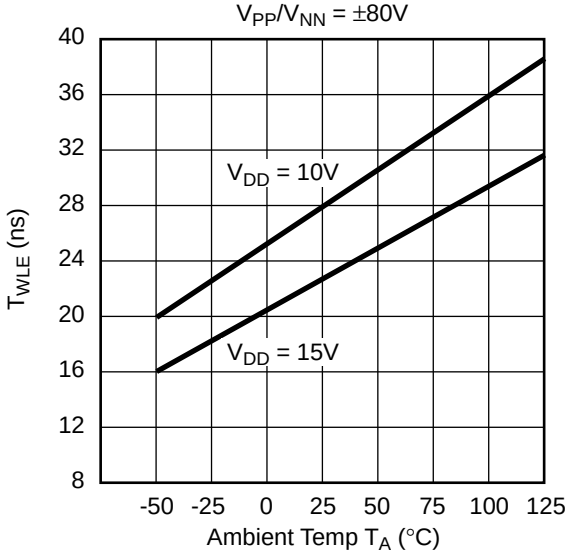


T_{DO} vs. Ambient Temp T_A
V_{PP}/V_{NN} = ±80V

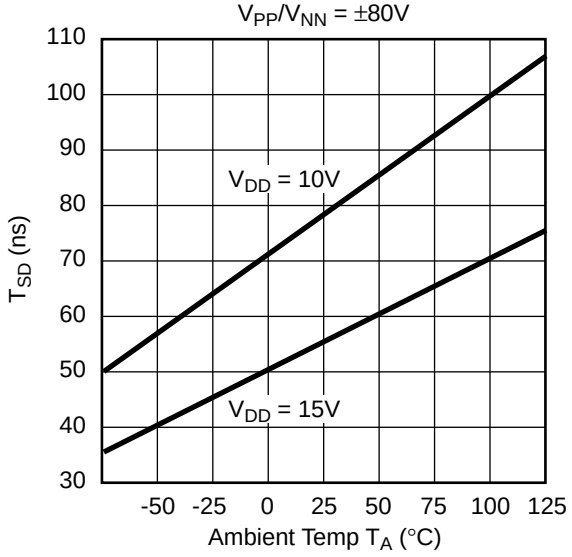


Typical Performance Curves

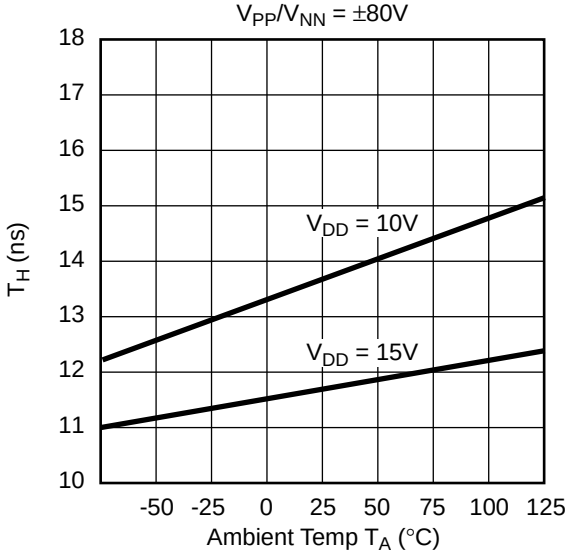
T_{WLE} vs. Ambient Temp
V_{PP}/V_{NN} = ±80V



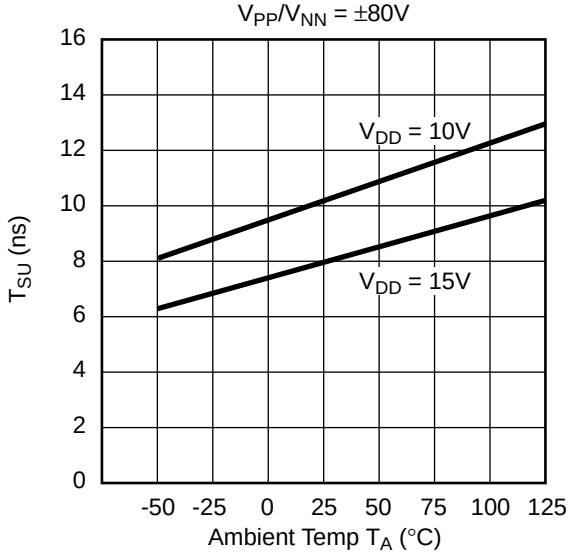
T_{SD} vs. Ambient Temp
V_{PP}/V_{NN} = ±80V



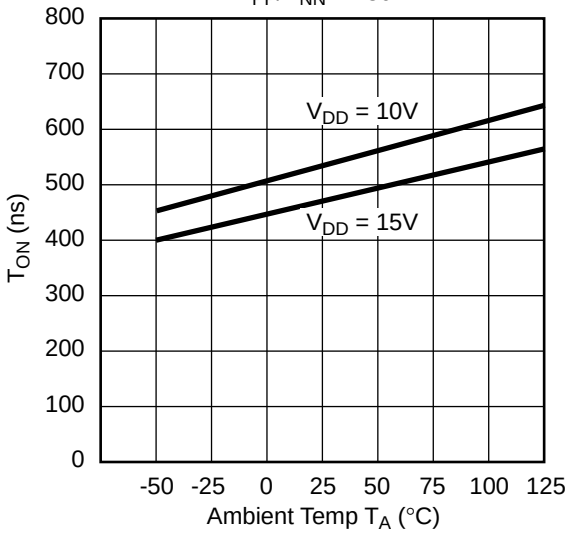
T_H vs. Ambient Temp
V_{PP}/V_{NN} = ±80V



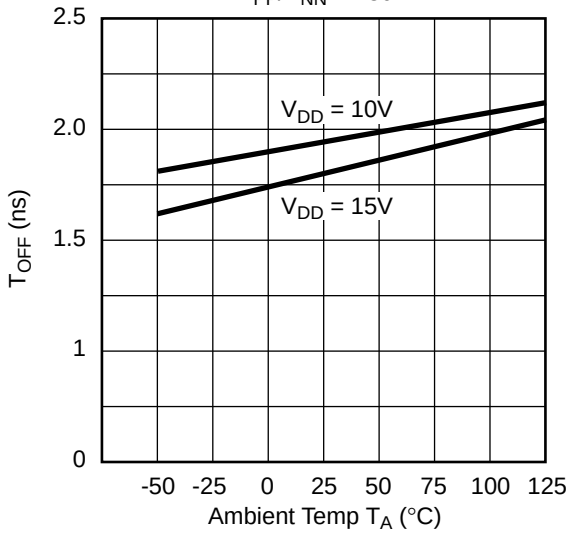
T_{SU} vs. Ambient Temp
V_{PP}/V_{NN} = ±80V



T_{ON} vs. Ambient Temp
V_{PP}/V_{NN} = ±80V



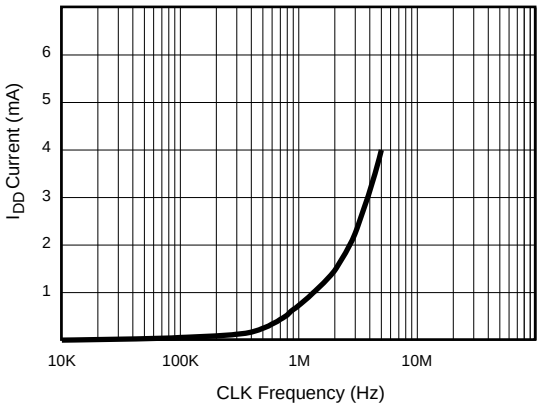
T_{OFF} vs. Ambient Temp
V_{PP}/V_{NN} = ±80V



Typical Performance Curves

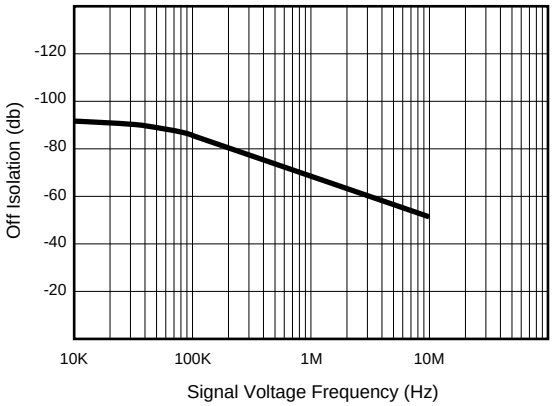
I_{DD} vs CLK Frequency

V_{DD} = 15V, V_{PP}/V_{NN} = ±80V, T_A = 0°C to 70°C



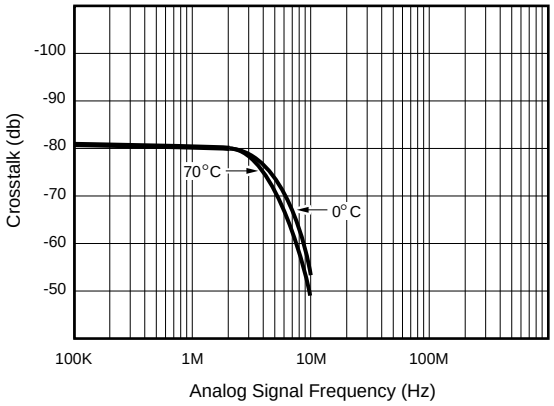
Off Isolation vs Signal Voltage Frequency

V_{DD} = 15V, V_{PP}/V_{NN} = ±80V



Crosstalk vs Analog Signal Frequency

V_{DD} = 15V, V_{PP}/V_{NN} = ±80V

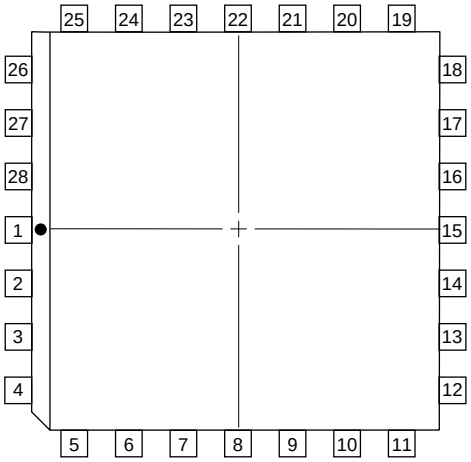


Pin Configurations

28-Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D_{IN}
3	SW2	17	CLK
4	SW2	18	$\overline{LE}$
5	N/C	19	D_{OUT}
6	N/C	20	SW7
7	SW1	21	SW7
8	SW1	22	SW6
9	SW0	23	SW6
10	SW0	24	N/C
11	V_{PP}	25	SW5
12	V_{NN}	26	SW5
13	GND	27	SW4
14	V_{DD}	28	SW4

Package Outlines



top view

28-pin J-Lead Package