HAT2022R

Silicon N-Channel Power MOS FET

HITACHI

Preliminary
November 1996

Application

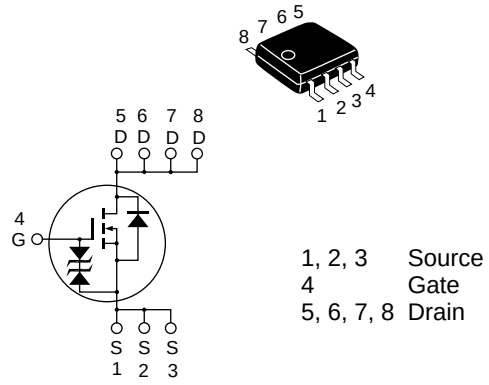
High speed power switching

Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

Outline

SOP–8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Ordering Information

Hitachi Code	FP-8DA
EIAJ Code	—
JEDEC Code	MS-012AA

Absolute Maximum Ratings (Ta = 25°C)

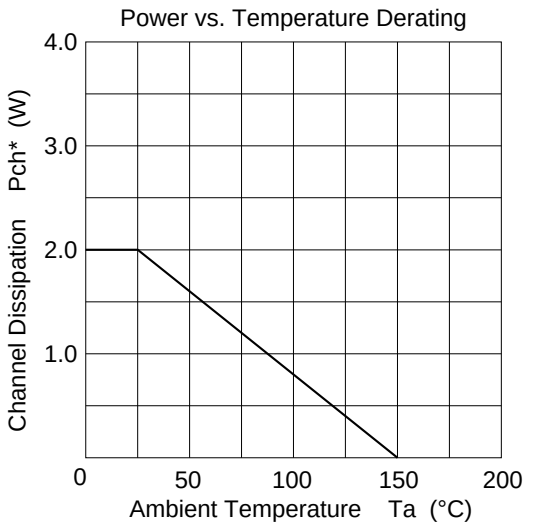
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$*[1]	40	A
Body to drain diode reverse drain current	I_{DR}	10	A
Channel dissipation	Pch*[2]	2.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. When using surface mounted on FR4 board

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.011)	0.0135	½	I_D = 5 A V_{GS} = 10 V*[1]
		—	(0.016)	0.02	½	I_D = 5 A V_{GS} = 4 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	(11)	(18)	—	S	I_D = 5 A V_{DS} = 10 V*[1]
Input capacitance	Ciss	—	(1250)	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	(820)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(300)	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	(35)	—	ns	V_{GS} = 4 V, I_D = 5 A
Rise time	t_r	—	(250)	—	ns	V_{DD} = 10 V
Turn-off delay time	$t_{d(off)}$	—	(140)	—	ns	
Fall time	t_f	—	(120)	—	ns	
Body to drain diode forward voltage	V_{DF}	—	(0.8)	—	V	I_F = 10 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	(90)	—	ns	I_F = 10 A, V_{GS} = 0 diF/dt = 20 A/µs

Note 1. Pulse Test



* When using surface mounted on FR4 board

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