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# HM628127HB Series

1 M High Speed SRAM (128-kword  $\times$  8-bit)

# HITACHI

ADE-203-350D (Z)

Rev. 4.0

Nov. 1997

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## Description

The HM628127HB is an asynchronous high speed static RAM organized as 128-k word  $\times$  8-bit. It realize high speed access time (15/20 ns) with employing 0.8  $\mu$ m shrink CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The HM628127HB is packaged in 400-mil 32-pin SOJ for high density surface mounting.

## Features

- Single 5 V supply
- Access time 15/20 ns (max)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - All inputs and outputs
- 400-mil 32-pin SOJ package
- Center  $V_{CC}$  and  $V_{SS}$  type pinout

## Ordering Information

Type No.	Access time	Package
HM628127HBJP-15	15 ns	400-mil 32-pin plastic SOJ (CP-32DB)
HM628127HBJP-20	20 ns	
HM628127HBLJP-15	15 ns	
HM628127HBLJP-20	20 ns	

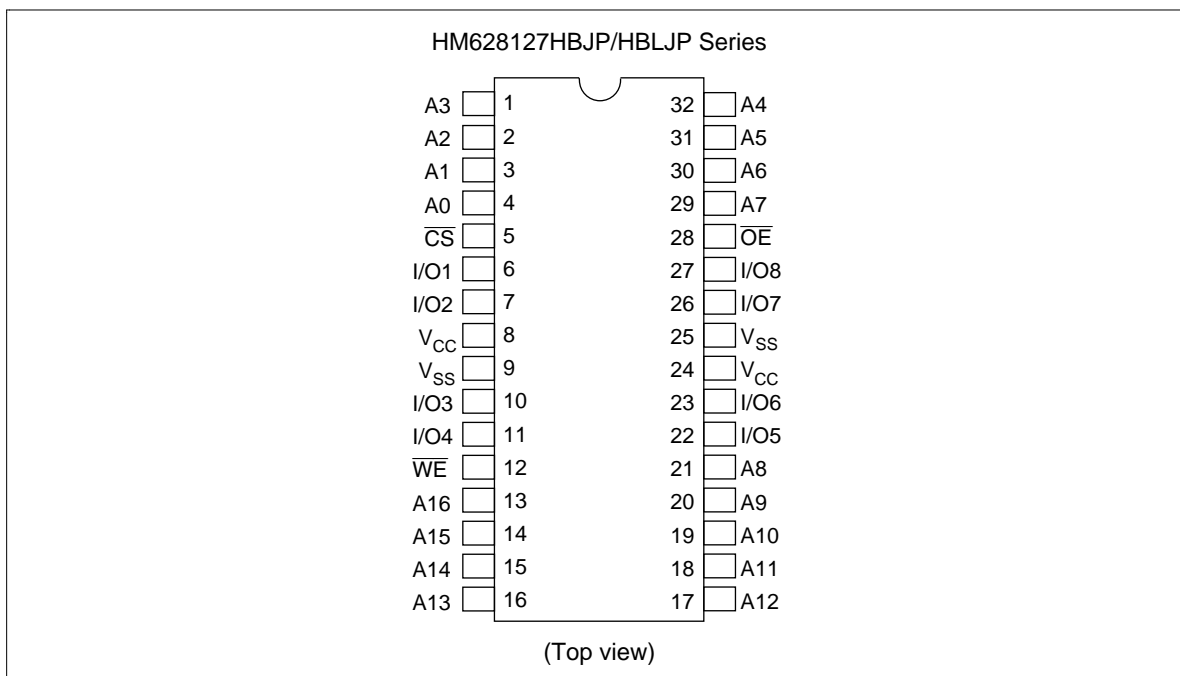
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## HM628127HB Series

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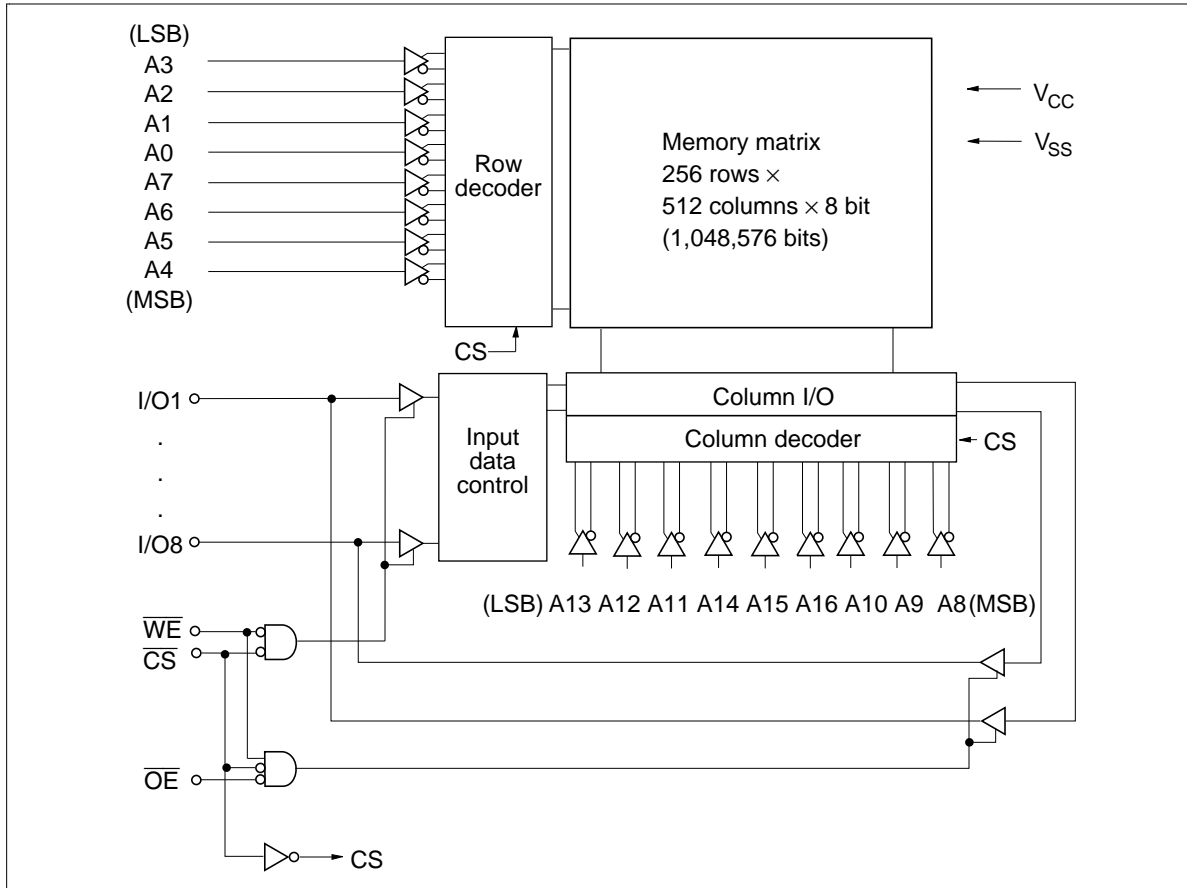
### Pin Arrangement



### Pin Description

Pin Name	Function
A0 to A16	Address input
I/O1 to I/O8	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$V_{CC}$	Power supply
$V_{SS}$	Ground

# Block Diagram



# Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	$V_{CC}$ current	I/O	Ref. cycle
H	×	×	Standby	$I_{SB}, I_{SB1}$	High-Z	—
L	H	H	Output disable	$I_{CC}$	High-Z	—
L	L	H	Read	$I_{CC}$	Dout	Read cycle (1) to (3)
L	H	L	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: ×: H or L

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### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +7.0	V
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5* <sup>1</sup> to $V_{CC}+0.5$	V
Power dissipation	$P_T$	1.0* <sup>2</sup> /1.5* <sup>3</sup>	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-10 to +85	°C

Notes: 1.  $V_T$  min = -2.5 V for pulse width (under shoot)  $\leq 10$  ns  
 2. At still air condition  
 3. At air flow  $\geq 1.0$  m/s

### Recommended DC Operating Conditions ( $T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}^{*2}$	4.5	5.0	5.5	V
	$V_{SS}^{*3}$	0	0	0	V
Input voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.5$	V
	$V_{IL}$	-0.5* <sup>1</sup>	—	0.8	V

Notes: 1.  $V_{IL}$  min = -2.0 V for pulse width (under shoot)  $\leq 10$  ns  
 2. The supply voltage with all  $V_{CC}$  pins must be on the same level.  
 3. The supply voltage with all  $V_{SS}$  pins must be on the same level.

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### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V)

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	I <sub>LI</sub>	—	—	2	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	—	2	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operation power supply current	15 ns cycle I <sub>CC</sub>	—	120	180	mA	$\overline{CS} = V_{IL}$ , I <sub>out</sub> = 0 mA Other inputs = V <sub>IH</sub> /V <sub>IL</sub>
	20 ns cycle I <sub>CC</sub>	—	100	150		
Standby power supply current	15 ns cycle I <sub>SB</sub>	—	55	100	mA	$\overline{CS} = V_{IH}$ , Other inputs = V <sub>IH</sub> /V <sub>IL</sub>
	20 ns cycle I <sub>SB</sub>	—	45	80		
	I <sub>SB1</sub>	—	—	2	mA	V <sub>CC</sub> ≥ $\overline{CS}$ ≥ V <sub>CC</sub> - 0.2 V, (1) 0 V ≤ V <sub>in</sub> ≤ 0.2 V or (2) V <sub>CC</sub> ≥ V <sub>in</sub> ≥ V <sub>CC</sub> - 0.2 V
		—* <sup>2</sup>	—* <sup>2</sup>	0.2* <sup>2</sup>		
Output voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 8 mA
	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -4 mA

Notes: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and not guaranteed.

2. This characteristics is guaranteed only for L-version.

### Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* <sup>1</sup>	C <sub>in</sub>	—	—	6	pF	V <sub>in</sub> = 0 V
Input/output capacitance* <sup>1</sup>	C <sub>I/O</sub>	—	—	8	pF	V <sub>I/O</sub> = 0 V

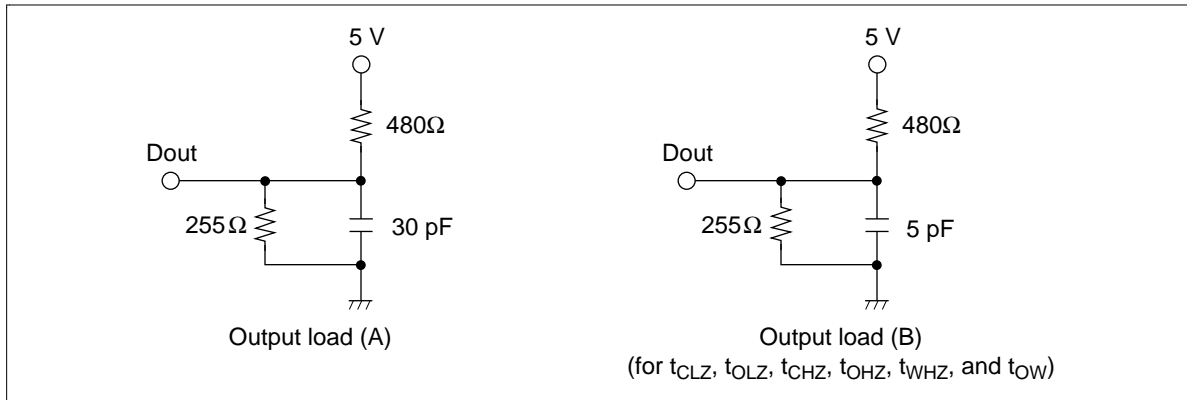
Note: 1. This parameter is sampled and not 100% tested.

## HM628127HB Series

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ , unless otherwise noted.)

### Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5V
- Output load: See figures (Including scope and jig)



### Read Cycle

Parameter	Symbol	HM628127HB-15		HM628127HB-20		Unit	Notes
		Min	Max	Min	Max		
Read cycle time	$t_{RC}$	15	—	20	—	ns	
Address access time	$t_{AA}$	—	15	—	20	ns	
Chip select access time	$t_{ACS}$	—	15	—	20	ns	
Output enable to output valid	$t_{OE}$	—	8	—	10	ns	
Output hold from address change	$t_{OH}$	5	—	5	—	ns	
Chip select to output in low-Z	$t_{CLZ}$	3	—	3	—	ns	1
Output enable to output in low-Z	$t_{OLZ}$	1	—	1	—	ns	1
Chip deselect to output in high-Z	$t_{CHZ}$	—	7	—	7	ns	1
Output disable to output in high-Z	$t_{OHZ}$	—	7	—	7	ns	1
Chip selection to power up time	$t_{PU}$	0	—	0	—	ns	
Chip selection to power down time	$t_{PD}$	—	15	—	20	ns	

**Write Cycle**

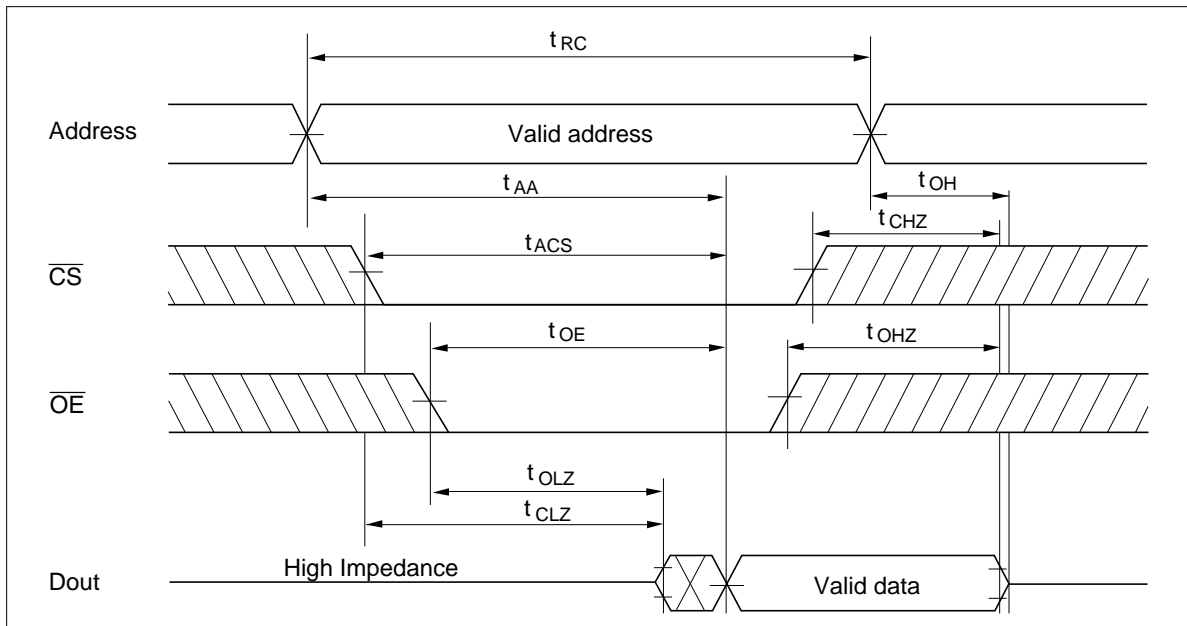
Parameter	Symbol	HM628127HB-15		HM628127HB-20		Unit	Notes
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	15	—	20	—	ns	
Address valid to end of write	$t_{AW}$	12	—	15	—	ns	
Chip select to end of write	$t_{CW}$	10	—	12	—	ns	9
Write pulse width	$t_{WP}$	10	—	12	—	ns	8
Address setup time	$t_{AS}$	0	—	0	—	ns	6
Write recovery time	$t_{WR}$	0	—	0	—	ns	7
Data to write time overlap	$t_{DW}$	8	—	10	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Write disable to output in low-Z	$t_{OW}$	3	—	3	—	ns	1
Output disable to output in high-Z	$t_{OHZ}$	—	7	—	7	ns	1
Write enable to output in high-Z	$t_{WHZ}$	—	7	—	7	ns	1

- Note:
1. Transition is measured  $\pm 200$  mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
  2. Address should be valid prior to or coincident with  $\overline{CS}$  transition low.
  3.  $\overline{WE}$  and/or  $\overline{CS}$  must be high during address transition time.
  4. If  $\overline{CS}$  and  $\overline{OE}$  are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
  5. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, output remains a high impedance state.
  6.  $t_{AS}$  is measured from the latest address transition to the later of  $\overline{CS}$  or  $\overline{WE}$  going low.
  7.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the first address transition.
  8. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  going low and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS}$  going high and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  9.  $t_{CW}$  is measured from the later of  $\overline{CS}$  going low to the end of write.

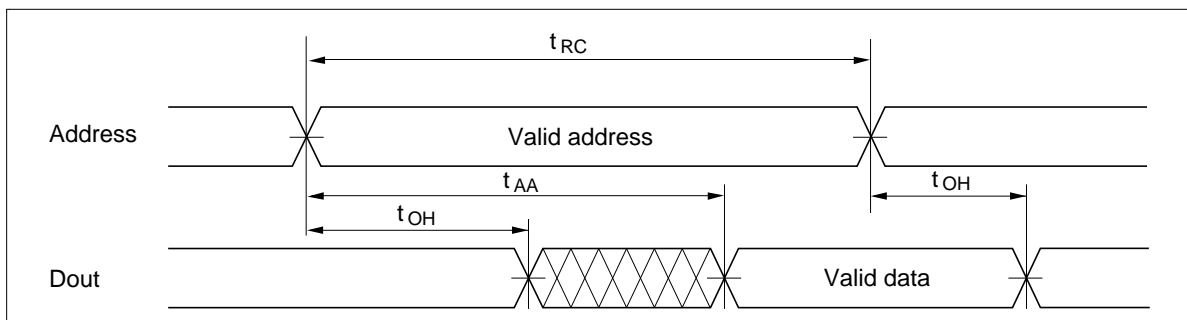
## HM628127HB Series

### Timing Waveforms

Read Timing Waveform (1) ( $\overline{WE} = V_{IH}$ )

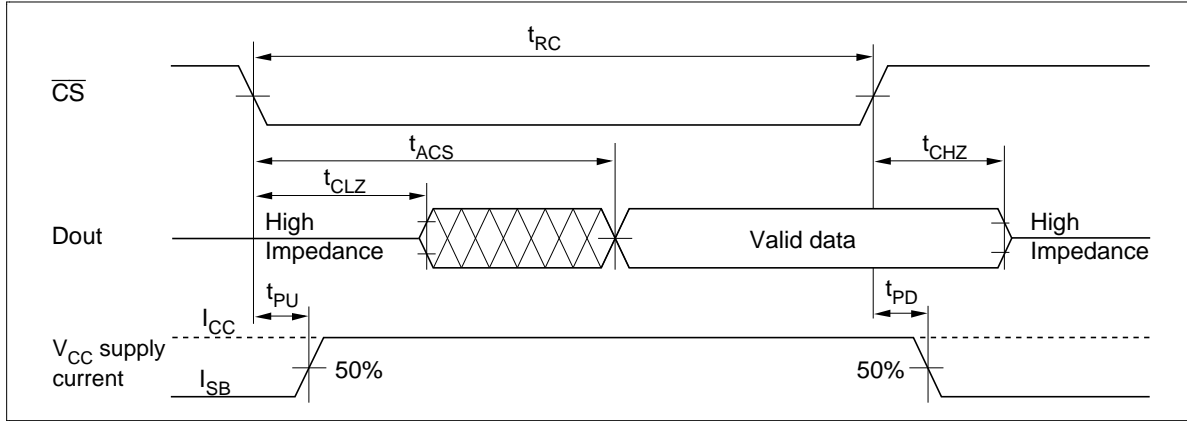


Read Timing Waveform (2) ( $\overline{WE} = V_{IH}$ ,  $\overline{CS} = V_{IL}$ ,  $\overline{OE} = V_{IL}$ )

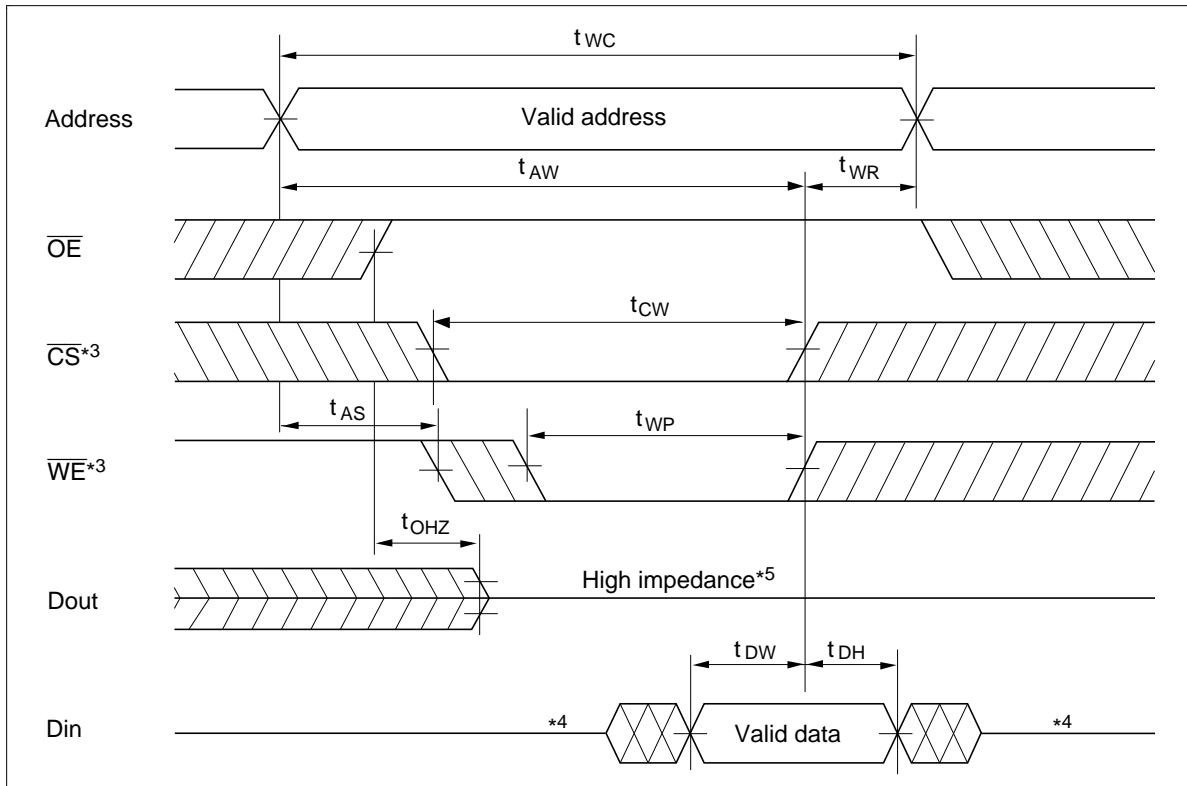




Read Timing Waveform (3) ( $\overline{WE} = V_{IH}$ ,  $\overline{CS} = V_{IL}$ ,  $\overline{OE} = V_{IL}$ )\*2

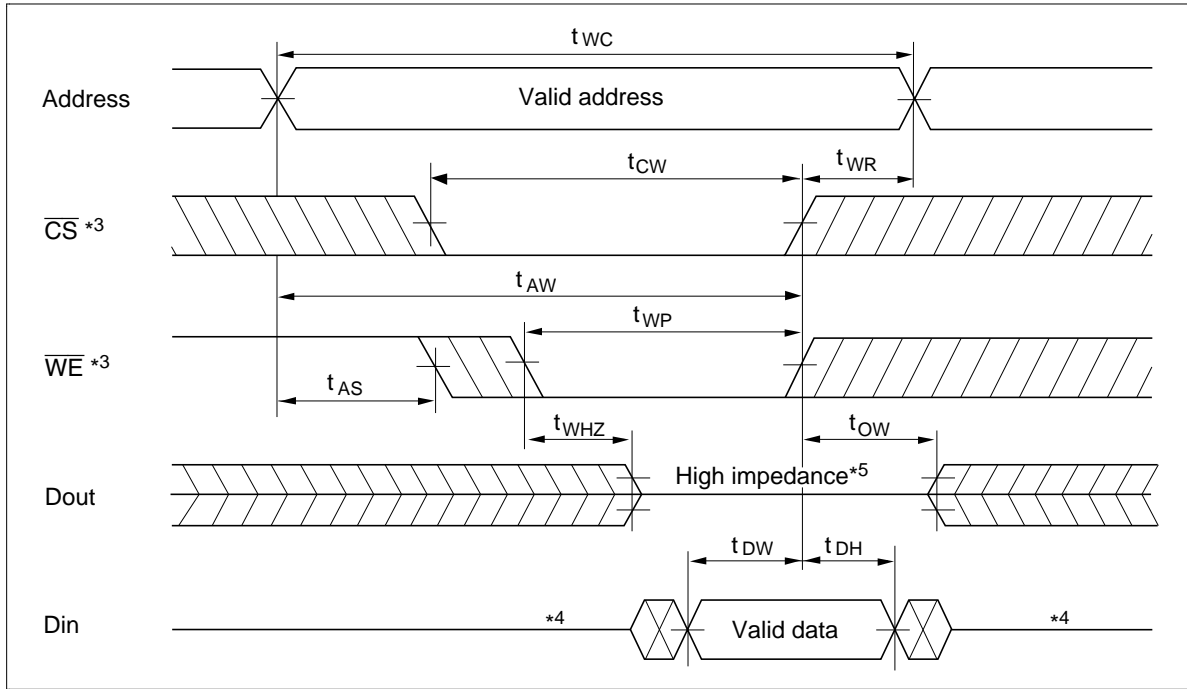


Write Timing Waveform (1) ( $\overline{WE}$  Controlled)



## HM628127HB Series

### Write Timing Waveform (2) ( $\overline{\text{CS}}$ Controlled)



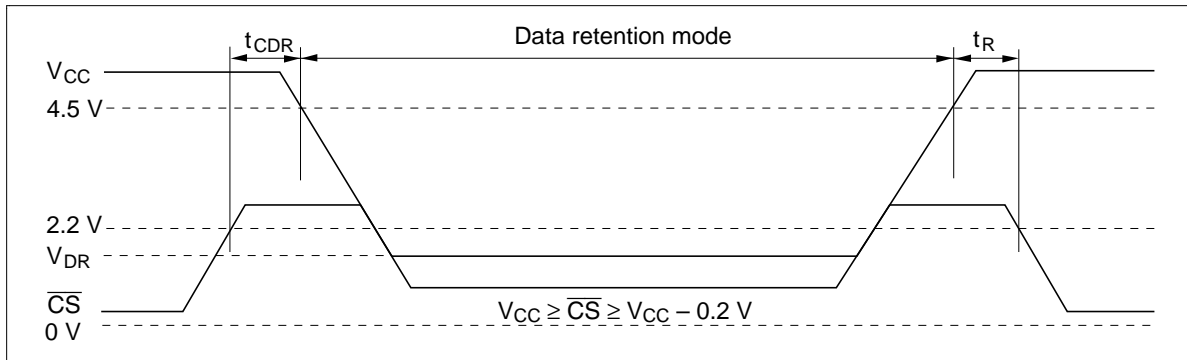
### Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $70^\circ\text{C}$ )

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2 \text{ V}$ (1) $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2 \text{ V}$
Data retention current	$I_{CCDR}$	—	2	80	$\mu\text{A}$	$V_{CC} = 3 \text{ V}$ , $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2 \text{ V}$ (1) $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2 \text{ V}$
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	—	ms	

Note: 1. Typical values are at  $V_{CC} = 3.0 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , and not guaranteed.

### Low $V_{CC}$ Data Retention Timing Waveform

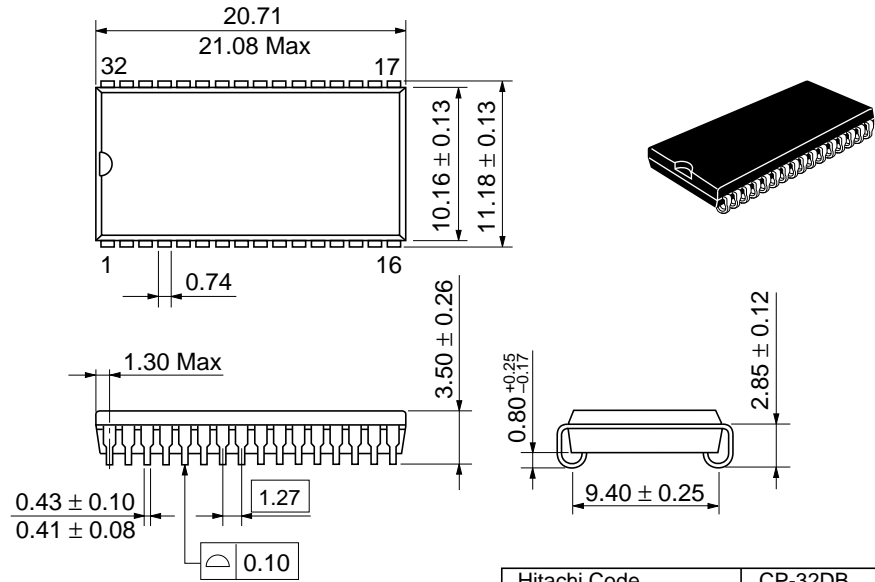


# HM628127HB Series

## Package Dimensions

HM628127HBJP/HBLJP Series (CP-32DB)

Unit: mm



Dimension including the plating thickness  
Base material dimension

Hitachi Code	CP-32DB
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.2 g

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## HM628127HB Series

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### Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Sep. 9, 1995	Initial issue	Y. Saitou	K. Yoshizaki
1.0	Nov. 15, 1995	Deletion of HM628127HB-25 series	Y. Saitou	K. Yoshizaki
2.0	Jun. 27 1996	Change of format Change of Block Diagram Function Table Addition of Mode parameter Recommended DC Operating Conditions Change of note 2. Addition of note 3. AC Characteristics Change order of notes Change of Timing Waveform Addition of Read timing waveform(2), (3) Low $V_{CC}$ Data Retention Characteristics Change of Test conditions for $I_{CCDR}$	Y. Saitou	A. Ide
3.0	Nov. 19, 1996	Change of Package Dimensions	Y. Saitou	A. Ide
4.0	Nov. 1997	Change of Subtitle		