# HB52RD168DB-D

128 MB Unbuffered SDRAM S.O.DIMM
16-Mword × 64-bit, 100 MHz Memory Bus, 1-Bank Module
(16 pcs of 16 M × 4 components)
PC100 SDRAM

HITACHI

ADE-203-990 (Z)
Preliminary, Rev. 0.0
Dec. 16, 1998

## Description

The HB52RD168DB is a 16M × 64 × 1 bank Synchronous Dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 16 pieces of 64-Mbit SDRAM (HM5264405DTB) sealed in TCP package and 1 piece of serial EEPROM (2-kbit EEPROM) for Presence Detect (PD). An outline of the HB52RD168DB is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB52RD168DB makes high density mounting possible without surface mount technology. The HB52RD168DB provides common data inputs and outputs. Decoupling capacitors are mounted beside TCP on the module board.

Note: Do not push the cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

## Features

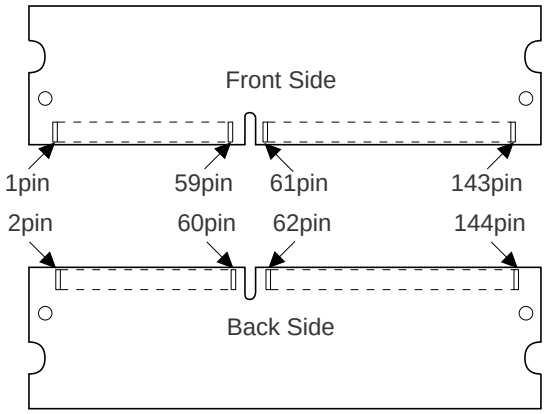
- Fully compatible with JEDEC standard outline unbuffered 8-byte S.O.DIMM
- 144-pin Zig Zag Dual tabs socket type
  - Outline: 67.60 mm (Length) × 25.40 mm (Height) × 3.80 mm (Thickness)
  - Lead pitch: 0.80 mm
- 3.3 V power supply
- Clock frequency: 100 MHz
- LVTTL interface
- Data bus width: × 64 Non parity
- Single pulsed $\overline{RAS}$
- 4 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length : 1/2/4/8/full page
- 2 variations of burst sequence
  - Sequential (BL = 1/2/4/8/full page)
  - Interleave (BL = 1/2/4/8)

- Programmable $\overline{CE}$ latency : 2/3 (HB52RD168DB-A6D/A6DL)
  : 3 (HB52RD168DB-B6D/B6DL)
- Byte control by DQMB
- Refresh cycles: 4096 refresh cycles/64 ms
- 2 variations of refresh
  — Auto refresh
  — Self refresh
- Low self refresh current: HB52RD168DB-A6DL/B6DL (L-version)
- Full page burst length capability
  — Sequential burst
  — Burst stop capability

## Ordering Information

| Type No. | Frequency | $\overline{CE}$ latency | Package | Contact pad |
|---|---|---|---|---|
| HB52RD168DB-A6D | 100 MHz | 2/3 | Small outline DIMM (144-pin) | Gold |
| HB52RD168DB-B6D | 100 MHz | 3 | | |
| HB52RD168DB-A6DL | 100 MHz | 2/3 | | |
| HB52RD168DB-B6DL | 100 MHz | 3 | | |

## Pin Arrangement



## Pin Arrangement (cont.)

| Front side | | | | Back side | | | |
|---|---|---|---|---|---|---|---|
| **Pin No.** | **Signal name** | **Pin No.** | **Signal name** | **Pin No.** | **Signal name** | **Pin No.** | **Signal name** |
| 1 | $V_{SS}$ | 73 | NC | 2 | $V_{SS}$ | 74 | CK1 |
| 3 | DQ0 | 75 | $V_{SS}$ | 4 | DQ32 | 76 | $V_{SS}$ |
| 5 | DQ1 | 77 | NC | 6 | DQ33 | 78 | NC |
| 7 | DQ2 | 79 | NC | 8 | DQ34 | 80 | NC |
| 9 | DQ3 | 81 | $V_{CC}$ | 10 | DQ35 | 82 | $V_{CC}$ |
| 11 | $V_{CC}$ | 83 | DQ16 | 12 | $V_{CC}$ | 84 | DQ48 |
| 13 | DQ4 | 85 | DQ17 | 14 | DQ36 | 86 | DQ49 |
| 15 | DQ5 | 87 | DQ18 | 16 | DQ37 | 88 | DQ50 |
| 17 | DQ6 | 89 | DQ19 | 18 | DQ38 | 90 | DQ51 |
| 19 | DQ7 | 91 | $V_{SS}$ | 20 | DQ39 | 92 | $V_{SS}$ |
| 21 | $V_{SS}$ | 93 | DQ20 | 22 | $V_{SS}$ | 94 | DQ52 |
| 23 | DQMB0 | 95 | DQ21 | 24 | DQMB4 | 96 | DQ53 |
| 25 | DQMB1 | 97 | DQ22 | 26 | DQMB5 | 98 | DQ54 |
| 27 | $V_{CC}$ | 99 | DQ23 | 28 | $V_{CC}$ | 100 | DQ55 |
| 29 | A0 | 101 | $V_{CC}$ | 30 | A3 | 102 | $V_{CC}$ |
| 31 | A1 | 103 | A6 | 32 | A4 | 104 | A7 |
| 33 | A2 | 105 | A8 | 34 | A5 | 106 | A13 (BA0) |
| 35 | $V_{SS}$ | 107 | $V_{SS}$ | 36 | $V_{SS}$ | 108 | $V_{SS}$ |
| 37 | DQ8 | 109 | A9 | 38 | DQ40 | 110 | A12 (BA1) |
| 39 | DQ9 | 111 | A10 (AP) | 40 | DQ41 | 112 | A11 |
| 41 | DQ10 | 113 | $V_{CC}$ | 42 | DQ42 | 114 | $V_{CC}$ |
| 43 | DQ11 | 115 | DQMB2 | 44 | DQ43 | 116 | DQMB6 |
| 45 | $V_{CC}$ | 117 | DQMB3 | 46 | $V_{CC}$ | 118 | DQMB7 |
| 47 | DQ12 | 119 | $V_{SS}$ | 48 | DQ44 | 120 | $V_{SS}$ |
| 49 | DQ13 | 121 | DQ24 | 50 | DQ45 | 122 | DQ56 |
| 51 | DQ14 | 123 | DQ25 | 52 | DQ46 | 124 | DQ57 |
| 53 | DQ15 | 125 | DQ26 | 54 | DQ47 | 126 | DQ58 |
| 55 | $V_{SS}$ | 127 | DQ27 | 56 | $V_{SS}$ | 128 | DQ59 |
| 57 | NC | 129 | $V_{CC}$ | 58 | NC | 130 | $V_{CC}$ |
| 59 | NC | 131 | DQ28 | 60 | NC | 132 | DQ60 |
| 61 | CK0 | 133 | DQ29 | 62 | CKE0 | 134 | DQ61 |
| 63 | $V_{CC}$ | 135 | DQ30 | 64 | $V_{CC}$ | 136 | DQ62 |
| 65 | $\overline{RE}$ | 137 | DQ31 | 66 | $\overline{CE}$ | 138 | DQ63 |

| Front side | | | | Back side | | | |
|---|---|---|---|---|---|---|---|
| **Pin No.** | **Signal name** | **Pin No.** | **Signal name** | **Pin No.** | **Signal name** | **Pin No.** | **Signal name** |
| 67 | $\overline{W}$ | 139 | $V_{SS}$ | 68 | NC | 140 | $V_{SS}$ |
| 69 | $\overline{S0}$ | 141 | SDA | 70 | NC | 142 | SCL |
| 71 | NC | 143 | $V_{CC}$ | 72 | NC | 144 | $V_{CC}$ |

## Pin Description

| Pin name | Function |
|---|---|
| A0 to A11 | Address input |
| | — Row address A0 to A11 |
| | — Column address A0 to A9 |
| A12/A13 | Bank select address BA1, BA0 |
| DQ0 to DQ63 | Data-input/output |
| $\overline{S0}$ | Chip select |
| $\overline{RE}$ | Row address asserted bank enable |
| $\overline{CE}$ | Column address asserted |
| $\overline{W}$ | Write enable |
| DQMB0 to DQMB7 | Byte input/output mask |
| CK0/CK1 | Clock input |
| CKE0 | Clock enable |
| SDA | Data-input/output for serial PD |
| SCL | Clock input for serial PD |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |
| NC | No connection |

## Serial PD Matrix*[1]

| Byte No. | Function described | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Hex value | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | Number of bytes used by module manufacturer | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | 128 |
| 1 | Total SPD memory size | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08 | 256 byte |
| 2 | Memory type | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 | SDRAM |
| 3 | Number of row addresses bits | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C | 12 |
| 4 | Number of column addresses bits | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A | 10 |
| 5 | Number of banks | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | 1 |
| 6 | Module data width | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | 64 |
| 7 | Module data width (continued) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | 0 (+) |
| 8 | Module interface signal levels | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | LVTTL |
| 9 | SDRAM cycle time (highest $\overline{CE}$ latency)<br>10 ns | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A0 | CL = 3 |
| 10 | SDRAM access from Clock (highest $\overline{CE}$ latency)<br>6 ns | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 60 | |
| 11 | Module configuration type | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | Non parity |
| 12 | Refresh rate/type | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | Normal (15.625 µs) Self refresh |
| 13 | SDRAM width | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 | 16M × 4 |
| 14 | Error checking SDRAM width | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | — |
| 15 | SDRAM device attributes: minimum clock delay for back-to-back random column addresses | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | 1 CLK |
| 16 | SDRAM device attributes: Burst lengths supported | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 8F | 1, 2, 4, 8, full page |
| 17 | SDRAM device attributes: number of banks on SDRAM device | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 | 4 |
| 18 | SDRAM device attributes: $\overline{CE}$ latency<br>(-A6D/A6DL) | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06 | 2, 3 |
| | (-B6D/B6DL) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 | 3 |

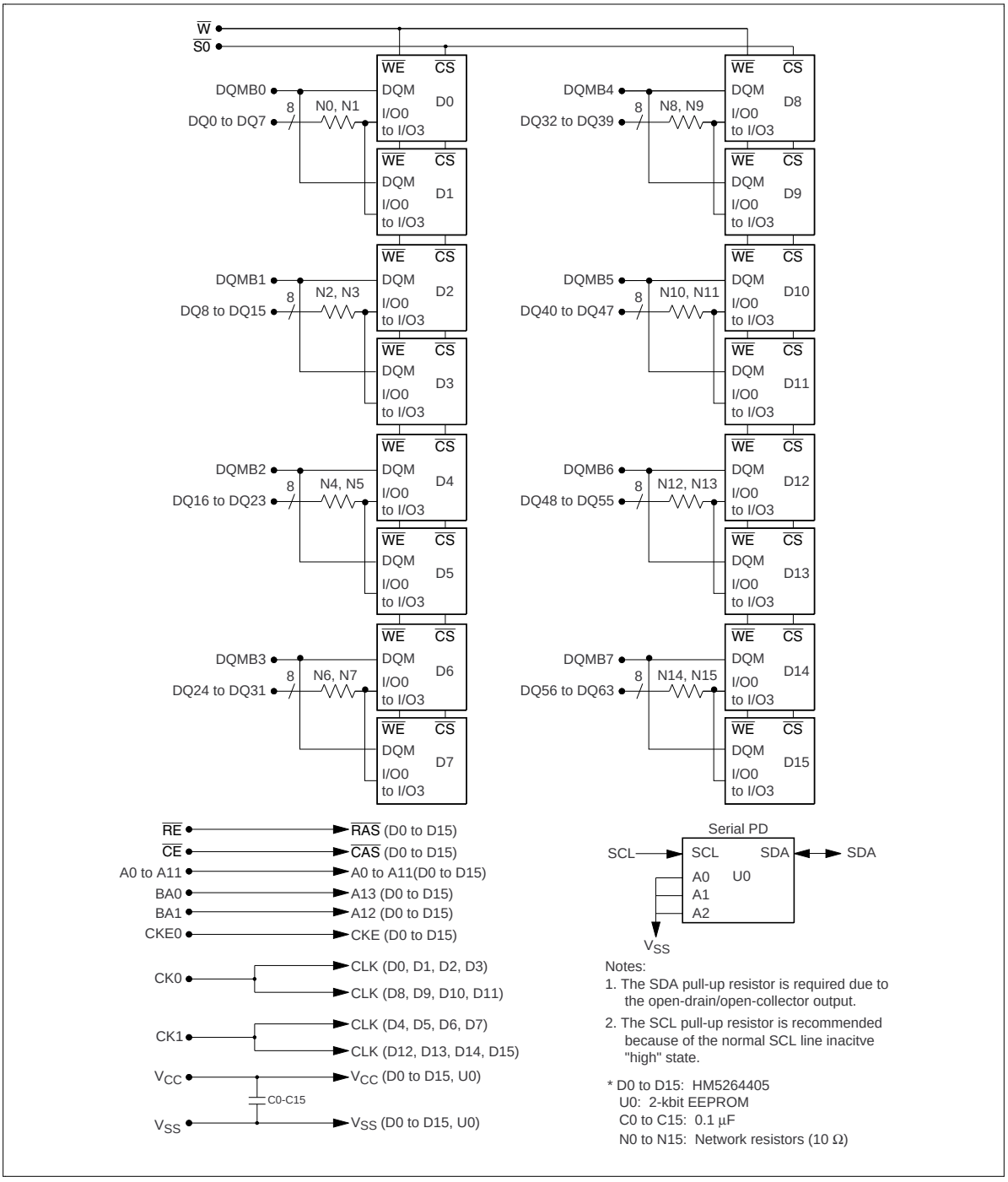
| Byte No. | Function described | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Hex value | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 19 | SDRAM device attributes: $\overline{S}$ latency | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | 0 |
| 20 | SDRAM device attributes: $\overline{W}$ latency | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | 0 |
| 21 | SDRAM module attributes | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | Non buffer |
| 22 | SDRAM device attributes: General | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0E | $V_{CC} \pm 10\%$ |
| 23 | SDRAM cycle time (2nd highest $\overline{CE}$ latency) (-A6D/A6DL) 10 ns | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A0 | CL = 2 |
| | SDRAM cycle time (2nd highest $\overline{CE}$ latency) (-B6D/B6DL) Undefined | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | |
| 24 | SDRAM access from Clock (2nd highest $\overline{CE}$ latency) (-A6D/A6DL) 6 ns | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 60 | |
| | SDRAM access from Clock (2nd highest $\overline{CE}$ latency) (-B6D/B6DL) Undefined | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | |
| 25 | SDRAM cycle time (3rd highest $\overline{CE}$ latency) Undefined | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | |
| 26 | SDRAM access from Clock (3rd highest $\overline{CE}$ latency) Undefined | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | |
| 27 | Minimum row precharge time | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14 | 20 ns |
| 28 | Row active to row active min | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14 | 20 ns |
| 29 | $\overline{RE}$ to $\overline{CE}$ delay min | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14 | 20 ns |
| 30 | Minimum $\overline{RE}$ pulse width | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32 | 50 ns |
| 31 | Density of each bank on module | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | 128M byte |
| 32 | Address and command signal input setup time | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | 2.0 ns*[2] |
| 33 | Address and command signal input hold time | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | 1.0 ns*[2] |
| 34 | Data signal input setup time | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | 3 ns*[2] |
| 35 | Data signal input hold time | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | 1.5 ns*[2] |
| 36 to 61 | Superset information | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | Future use |
| 62 | SPD data revision code | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12 | Rev. 1.2A |

| Byte No. | Function described | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Hex value | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 63 | Checksum for bytes 0 to 62 (-A6D/A6DL) | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 92 | 146 |
| | (-B6D/B6DL) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | 16 |
| 64 | Manufacturer's JEDEC ID code | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 | HITACHI |
| 65 to 71 | Manufacturer's JEDEC ID code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | |
| 72 | Manufacturing location | × | × | × | × | × | × | × | × | ×× | *3 (ASCII-8bit code) |
| 73 | Manufacturer's part number | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 48 | H |
| 74 | Manufacturer's part number | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | B |
| 75 | Manufacturer's part number | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 | 5 |
| 76 | Manufacturer's part number | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32 | 2 |
| 77 | Manufacturer's part number | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52 | R |
| 78 | Manufacturer's part number | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 | D |
| 79 | Manufacturer's part number | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 31 | 1 |
| 80 | Manufacturer's part number | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36 | 6 |
| 81 | Manufacturer's part number | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38 | 8 |
| 82 | Manufacturer's part number | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 | D |
| 83 | Manufacturer's part number | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | B |
| 84 | Manufacturer's part number | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2D | — |
| 85 | Manufacturer's part number (-A6D/A6DL) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41 | A |
| | (-B6D/B6DL) | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | B |
| 86 | Manufacturer's part number | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36 | 6 |
| 87 | Manufacture's part number | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 | D |
| 88 | Manufacturer's part number (L-version) | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 4C | L |
| | Manufacturer's part number | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | (Space) |
| 89 | Manufacturer's part number | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | (Space) |
| 90 | Manufacturer's part number | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | (Space) |
| 91 | Revision code | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 | Initial |
| 92 | Revision code | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | (Space) |
| 93 | Manufacturing date | × | × | × | × | × | × | × | × | ×× | Year code (BCD)*4 |
| 94 | Manufacturing date | × | × | × | × | × | × | × | × | ×× | Week code (BCD)*4 |

| Byte No. | Function described | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Hex value | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 95 to 98 | Assembly serial number | *6 | | | | | | | | | |
| 99 to 125 | Manufacturer specific data | — | — | — | — | — | — | — | — | — | *5 |
| 126 | Intel specification frequency | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 64 | 100 MHz |
| 127 | Intel specification $\overline{CE}$# latency support (-A6D/A6DL) | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | C7 | CL = 2, 3 |
| | (-B6D/B6DL) | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | C5 | CL = 3 |

Notes:
1. All serial PD data are not protected. 0: Serial data, “driven Low”, 1: Serial data, “driven High” These SPD are based on Intel specification (Rev.1.2A).
2. Regarding byte32 to 35, based on JEDEC Committee Ballot JC42.5-97-119.
3. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows “J” on ASCII code.)
4. Regarding byte93 and 94, based on JEDEC Committee Ballot JC42.5-97-135. BCD is “Binary Coded Decimal”.
5. All bits of 99 through 125 are not defined (“1” or “0”).
6. Bytes 95 through 98 are assembly serial number.

## Block Diagram




Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

* D0 to D15: HM5264405
U0: 2-kbit EEPROM
C0 to C15: 0.1 µF
N0 to N15: Network resistors (10 Ω)

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | –0.5 to $V_{CC}$ + 0.5 (≤ 4.6 (max)) | V | 1 |
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +4.6 | V | 1 |
| Short circuit output current | Iout | 50 | mA | |
| Power dissipation | $P_T$ | 16 | W | |
| Operating temperature | Topr | 0 to +65 | °C | |
| Storage temperature | Tstg | –55 to +125 | °C | |

Note: 1. Respect to $V_{SS}$.

## DC Operating Conditions (Ta = 0 to +65°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | 1, 2 |
| | $V_{SS}$ | 0 | 0 | 0 | V | 3 |
| Input high voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ + 0.3 | V | 1, 4, 5 |
| Input low voltage | $V_{IL}$ | –0.3 | — | 0.8 | V | 1, 6 |
| Ambient illuminance | — | — | — | 100 | lx | |

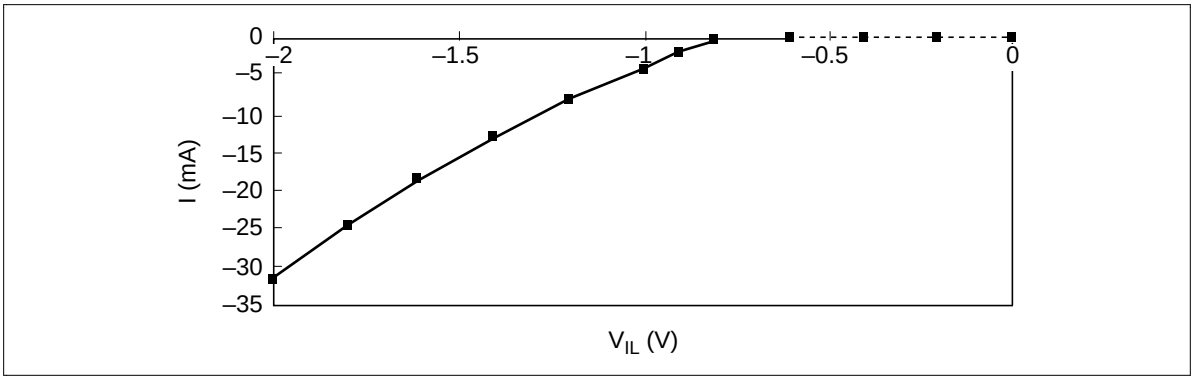
Notes: 1. All voltage referred to $V_{SS}$
2. The supply voltage with all $V_{CC}$ pins must be on the same level.
3. The supply voltage with all $V_{SS}$ pins must be on the same level.
4. CK, CKE, $\overline{S}$, DQMB, DQ pins: $V_{IH}$ (max) = $V_{CC}$ + 0.5 V for pulse width ≤ 5 ns at $V_{CC}$.
5. Others: $V_{IH}$ (max) = 4.6 V for pulse width ≤ 5 ns at $V_{CC}$.
6. $V_{IL}$ (min) = –1.0 V for pulse width ≤ 5 ns at $V_{SS}$.

## $V_{IL}/V_{IH}$ Clamp (Component characteristic)

This SDRAM component has $V_{IL}$ and $V_{IH}$ clamp for CK, CKE, $\overline{S}$, DQMB and DQ pins.

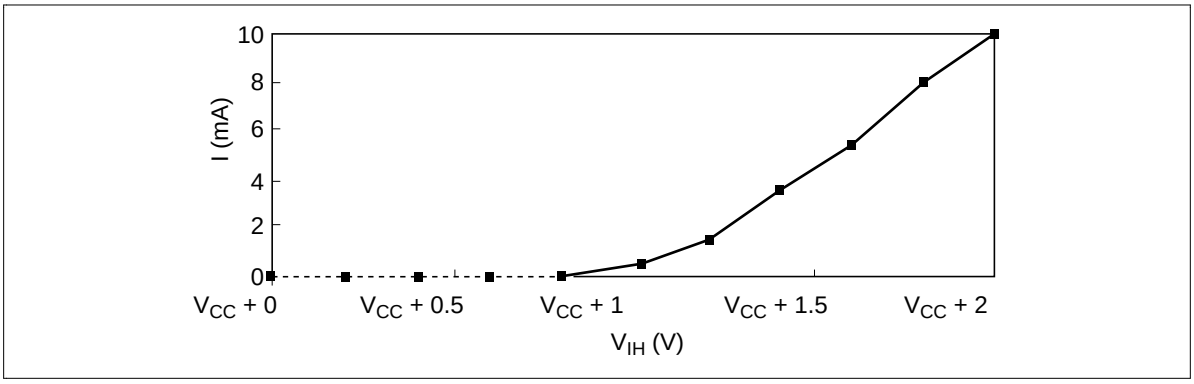
**Minimum $V_{IL}$ Clamp Current**

| $V_{IL}$ (V) | I (mA) |
|---|---|
| –2 | –32 |
| –1.8 | –25 |
| –1.6 | –19 |
| –1.4 | –13 |
| –1.2 | –8 |
| –1 | –4 |
| –0.9 | –2 |
| –0.8 | –0.6 |
| –0.6 | 0 |
| –0.4 | 0 |
| –0.2 | 0 |
| 0 | 0 |



**Minimum $V_{IH}$ Clamp Current**

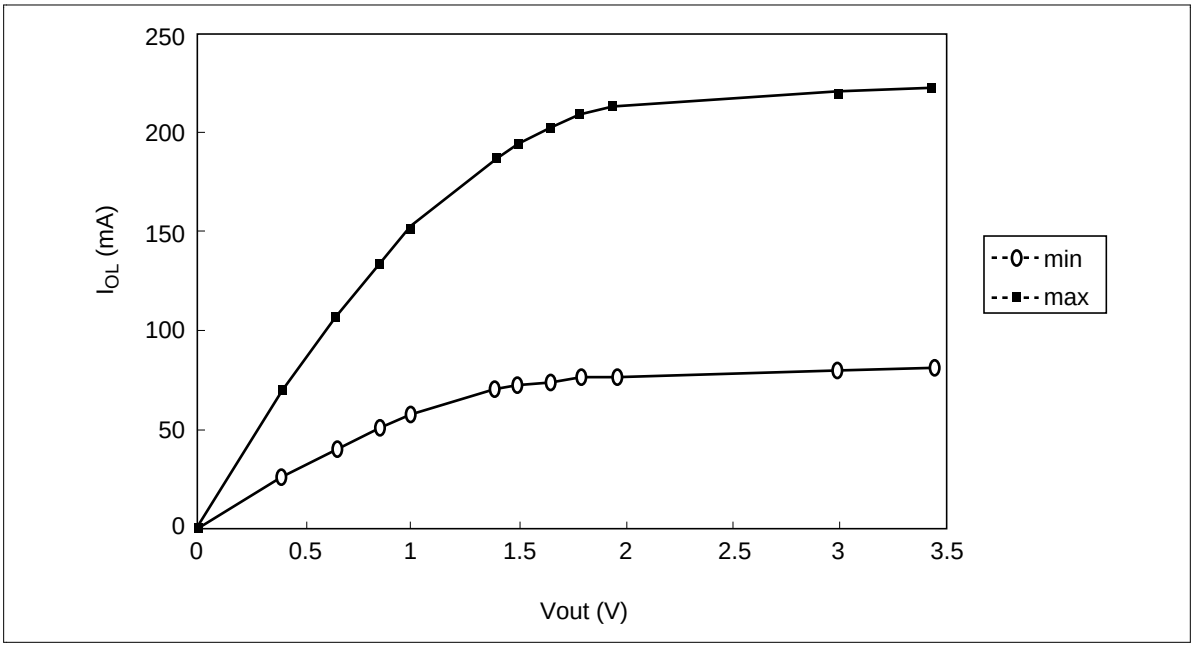
| $V_{IH}$ (V) | I (mA) |
|---|---|
| $V_{CC}$ + 2 | 10 |
| $V_{CC}$ + 1.8 | 8 |
| $V_{CC}$ + 1.6 | 5.5 |
| $V_{CC}$ + 1.4 | 3.5 |
| $V_{CC}$ + 1.2 | 1.5 |
| $V_{CC}$ + 1 | 0.3 |
| $V_{CC}$ + 0.8 | 0 |
| $V_{CC}$ + 0.6 | 0 |
| $V_{CC}$ + 0.4 | 0 |
| $V_{CC}$ + 0.2 | 0 |
| $V_{CC}$ + 0 | 0 |



## $I_{OL}/I_{OH}$ Characteristics (Component characteristic)

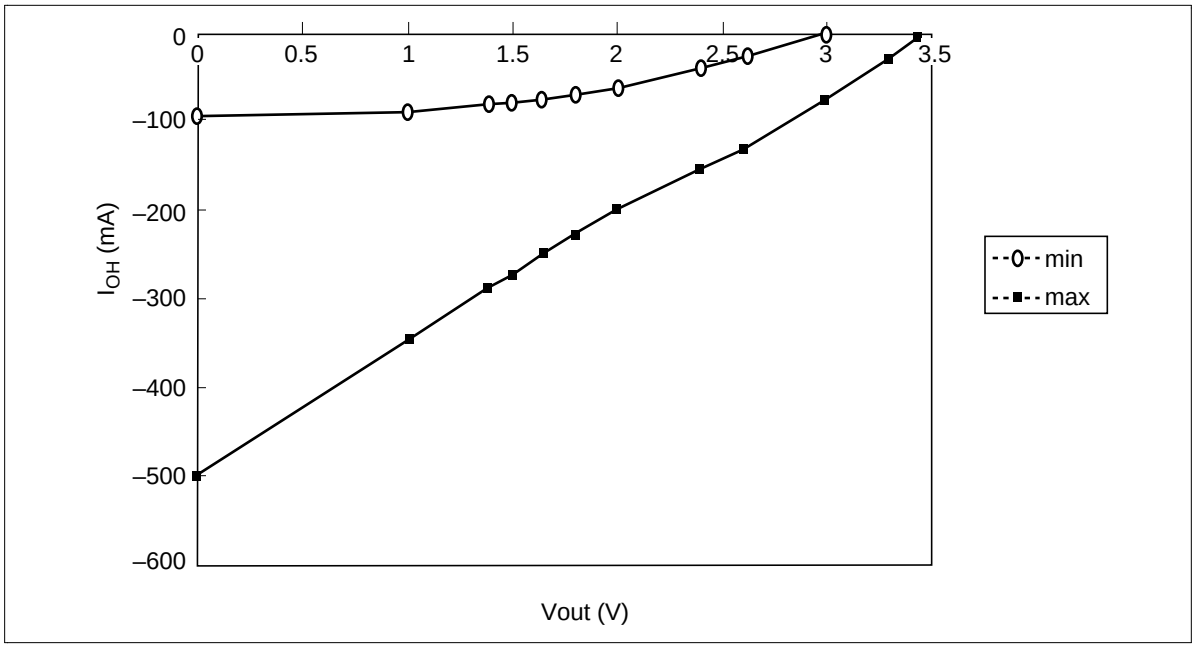
**Output Low Current** ($I_{OL}$)

| | $I_{OL}$ | $I_{OL}$ |
|---|---|---|
| **Vout (V)** | **Min (mA)** | **Max (mA)** |
| 0 | 0 | 0 |
| 0.4 | 27 | 71 |
| 0.65 | 41 | 108 |
| 0.85 | 51 | 134 |
| 1 | 58 | 151 |
| 1.4 | 70 | 188 |
| 1.5 | 72 | 194 |
| 1.65 | 75 | 203 |
| 1.8 | 77 | 209 |
| 1.95 | 77 | 212 |
| 3 | 80 | 220 |
| 3.45 | 81 | 223 |



**Output High Current** ($I_{OH}$) (Ta = 0 to 65°C, $V_{CC}$ = 3.0 V to 3.45 V, $V_{SS}$ = 0 V)

| | $I_{OH}$ | $I_{OH}$ |
|---|---|---|
| **Vout (V)** | **Min (mA)** | **Max (mA)** |
| 3.45 | — | –3 |
| 3.3 | — | –28 |
| 3 | 0 | –75 |
| 2.6 | –21 | –130 |
| 2.4 | –34 | –154 |
| 2 | –59 | –197 |
| 1.8 | –67 | –227 |
| 1.65 | –73 | –248 |
| 1.5 | –78 | –270 |
| 1.4 | –81 | –285 |
| 1 | –89 | –345 |
| 0 | –93 | –503 |



## DC Characteristics (Ta = 0 to 65°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V)

| | | HB52RD168DB -A6D/A6DL/B6D/B6DL | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** | **Test conditions** | **Notes** |
| Operating current ($\overline{CE}$ latency = 2) | $I_{CC1}$ | — | 1040 | mA | Burst length = 1<br>$t_{RC}$ = min | 1, 2, 3 |
| ($\overline{CE}$ latency = 3) | $I_{CC1}$ | — | 1120 | mA | | |
| Standby current in power down | $I_{CC2P}$ | — | 48 | mA | CKE0 = $V_{IL}$, $t_{CK}$ = 15 ns | 6 |
| Standby current in power down (input signal stable) | $I_{CC2PS}$ | — | 32 | mA | CKE0 = $V_{IL}$, CK0/CK1 = $V_{IL}$ or $V_{IH}$ Fixed | 7 |
| Standby current in non power down | $I_{CC2N}$ | — | 256 | mA | CKE0, $\overline{S}$ = $V_{IH}$,<br>$t_{CK}$ = min | 4 |
| Active standby current in power down | $I_{CC3P}$ | — | 64 | mA | CKE0, $\overline{S}$ = $V_{IH}$,<br>$t_{CK}$ = min | 1, 2, 6 |
| Active standby current in non power down | $I_{CC3N}$ | — | 320 | mA | CKE0, $\overline{S}$ = $V_{IH}$,<br>$t_{CK}$ = min | 1, 2, 4 |
| Burst operating current ($\overline{CE}$ latency = 2) | $I_{CC4}$ | — | 960 | mA | $t_{CK}$ = min, BL = 4 | 1, 2, 5 |
| ($\overline{CE}$ latency = 3) | $I_{CC4}$ | — | 1120 | mA | | |
| Refresh current | $I_{CC5}$ | — | 1840 | mA | $t_{RC}$ = min | 3 |
| Self refresh current | $I_{CC6}$ | — | 16 | mA | $V_{IH} \geq V_{CC} - 0.2$ V<br>$V_{IL} \leq 0.2$ V | 8 |
| Self refresh current (L-version) | $I_{CC6}$ | — | 6.4 | mA | $V_{IH} \geq V_{CC} - 0.2$ V<br>$V_{IL} \leq 0.2$ V | |
| Input leakage current | $I_{LI}$ | –10 | 10 | µA | $0 \leq Vin \leq V_{CC}$ | |
| Output leakage current | $I_{LO}$ | –10 | 10 | µA | $0 \leq Vout \leq V_{CC}$<br>DQ = disable | |
| Output high voltage | $V_{OH}$ | 2.4 | — | V | $I_{OH}$ = –2 mA | |
| Output low voltage | $V_{OL}$ | — | 0.4 | V | $I_{OL}$ = 2 mA | |

Notes: 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ (max) is specified at the output open condition.
2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, CK0/CK1 operating current.
7. After power down mode, no CK0/CK1 operating current.
8. After self refresh mode set, self refresh current.

**Capacitance** (Ta = 25°C, $V_{CC}$ = 3.3 V ± 0.3 V)

| Parameter | Symbol | Max | Unit | Notes |
|---|---|---|---|---|
| Input capacitance (Address) | $C_{IN}$ | 90 | pF | 1, 2, 4 |
| Input capacitance ($\overline{RE}$, $\overline{CE}$, $\overline{W}$, $\overline{S}$, CKE) | $C_{IN}$ | 90 | pF | 1, 2, 4 |
| Input capacitance ( CK ) | $C_{IN}$ | 60 | pF | 1, 2, 4 |
| Input capacitance (DQMB0 to DQMB7) | $C_{IN}$ | 20 | pF | 1, 2, 4 |
| Input/Output capacitance (DQ0 to DQ63) | $C_{I/O}$ | 20 | pF | 1, 2, 3, 4 |

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. Measurement condition: f = 1 MHz, 1.4 V bias, 200 mV swing.
3. DQMB = $V_{IH}$ to disable Data-out.
4. This parameter is sampled and not 100% tested.

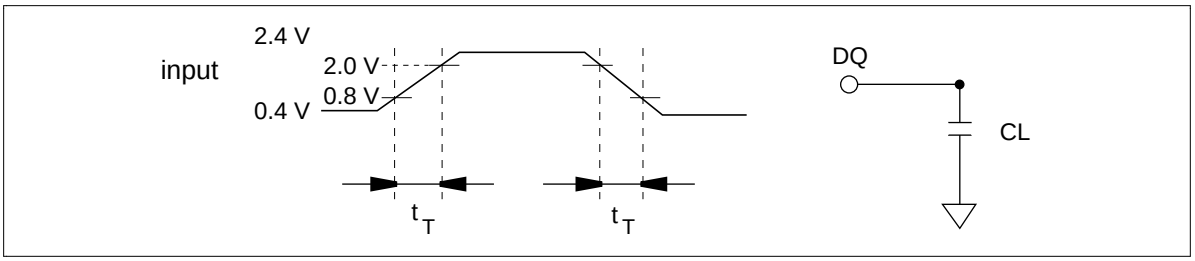
## AC Characteristics (Ta = 0 to 65°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V)

| | | | HB52RDR168DB -A6D/A6DL/B6D/B6DL | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **HITACHI Symbol** | **PC100 Symbol** | **Min** | **Max** | **Unit** | **Notes** |
| System clock cycle time ($\overline{CE}$ latency = 2) | $t_{CK}$ | Tclk | 10 | — | ns | 1 |
| ($\overline{CE}$ latency = 3) | $t_{CK}$ | Tclk | 10 | — | ns | |
| CK high pulse width | $t_{CKH}$ | Tch | 3 | — | ns | 1 |
| CK low pulse width | $t_{CKL}$ | Tcl | 3 | — | ns | 1 |
| Access time from CK ($\overline{CE}$ latency = 2) | $t_{AC}$ | Tac | — | 6 | ns | 1, 2 |
| ($\overline{CE}$ latency = 3) | $t_{AC}$ | Tac | — | 6 | ns | |
| Data-out hold time | $t_{OH}$ | Toh | 3 | — | ns | 1, 2 |
| CK to Data-out low impedance | $t_{LZ}$ | | 2 | — | ns | 1, 2, 3 |
| CK to Data-out high impedance | $t_{HZ}$ | | — | 6 | ns | 1, 4 |
| Data-in setup time | $t_{DS}$ | Tsi | 2 | — | ns | 1 |
| Data in hold time | $t_{DH}$ | Thi | 1 | — | ns | 1 |
| Address setup time | $t_{AS}$ | Tsi | 2 | — | ns | 1 |
| Address hold time | $t_{AH}$ | Thi | 1 | — | ns | 1 |
| CKE setup time | $t_{CES}$ | Tsi | 2 | — | ns | 1, 5 |
| CKE setup time for power down exit | $t_{CESP}$ | Tpde | 2 | — | ns | 1 |
| CKE hold time | $t_{CEH}$ | Thi | 1 | — | ns | 1 |
| Command setup time | $t_{CS}$ | Tsi | 2 | — | ns | 1 |
| Command hold time | $t_{CH}$ | Thi | 1 | — | ns | 1 |
| Ref/Active to Ref/Active command period | $t_{RC}$ | Trc | 70 | — | ns | 1 |
| Active to precharge command period | $t_{RAS}$ | Tras | 50 | 120000 | ns | 1 |
| Active command to column command (same bank) | $t_{RCD}$ | Trcd | 20 | — | ns | 1 |
| Precharge to active command period | $t_{RP}$ | Trp | 20 | — | ns | 1 |
| Write recovery or data-in to precharge lead time | $t_{DPL}$ | Tdpl | 15 | — | ns | 1 |
| Active (a) to Active (b) command period | $t_{RRD}$ | Trrd | 20 | — | ns | 1 |
| Transition time (rise to fall) | $t_{T}$ | | 1 | 5 | ns | |
| Refresh period | $t_{REF}$ | | — | 64 | ms | |

Notes: 1. AC measurement assumes $t_T$ = 1 ns. Reference level for timing of input signals is 1.5 V.
2. Access time is measured at 1.5 V. Load condition is $C_L$ = 50 pF.
3. $t_{LZ}$ (max) defines the time at which the outputs achieves the low impedance state.
4. $t_{HZ}$ (max) defines the time at which the outputs achieves the high impedance state.
5. $t_{CES}$ defines CKE setup time to CK rising edge except power down exit command.

**Test Conditions**

- Input and output timing reference levels: 1.5 V
- Input waveform and output load: See following figures



**Relationship Between Frequency and Minimum Latency**

| Parameter | | | HB52RDR168DB -A6D/A6DL/B6D/B6DL | |
|---|---|---|---|---|
| **Frequency (MHz)** | | | **100** | |
| **$t_{CK}$ (ns)** | **HITACHI Symbol** | **PC100 Symbol** | **10** | **Notes** |
| Active command to column command (same bank) | $I_{RCD}$ | | 2 | 1 |
| Active command to active command (same bank) | $I_{RC}$ | | 7 | = [$I_{RAS}$ + $I_{RP}$] 1 |
| Active command to precharge command (same bank) | $I_{RAS}$ | | 5 | 1 |
| Precharge command to active command (same bank) | $I_{RP}$ | | 2 | 1 |
| Write recovery or data-in to precharge command (same bank) | $I_{DPL}$ | Tdpl | 2 | 1 |
| Active command to active command (different bank) | $I_{RRD}$ | | 2 | 1 |
| Self refresh exit time | $I_{SREX}$ | Tsrx | 1 | 2 |
| Last data in to active command (Auto precharge, same bank) | $I_{APW}$ | Tdal | 4 | = [$I_{DPL}$ + $I_{RP}$] |
| Self refresh exit to command input | $I_{SEC}$ | | 7 | = [$I_{RC}$] 3 |
| Precharge command to high impedance ($\overline{CE}$ latency = 2) | $I_{HZP}$ | Troh | 2 | |
| ($\overline{CE}$ latency = 3) | $I_{HZP}$ | Troh | 3 | |
| Last data out to active command (auto precharge) (same bank) | $I_{APR}$ | | 1 | |
| Last data out to precharge (early precharge) ($\overline{CE}$ latency = 2) | $I_{EP}$ | | –1 | |
| ($\overline{CE}$ latency = 3) | $I_{EP}$ | | –2 | |
| Column command to column command | $I_{CCD}$ | Tccd | 1 | |
| Write command to data in latency | $I_{WCD}$ | Tdwd | 0 | |
| DQMB to data in | $I_{DID}$ | Tdqm | 0 | |
| DQMB to data out | $I_{DOD}$ | Tdqz | 2 | |
| CKE to CK disable | $I_{CLE}$ | Tcke | 1 | |
| Register set to active command | $I_{RSA}$ | Tmrd | 1 | |
| $\overline{S}$ to command disable | $I_{CDD}$ | | 0 | |
| Power down exit to command input | $I_{PEC}$ | | 1 | |

| Parameter | | | HB52RDR168DB -A6D/A6DL/B6D/B6DL | |
|---|---|---|---|---|
| **Frequency (MHz)** | | | **100** | |
| **$t_{CK}$ (ns)** | **HITACHI Symbol** | **PC100 Symbol** | **10** | **Notes** |
| Burst stop to output valid data hold ($\overline{CE}$ latency = 2) | $I_{BSR}$ | | 1 | |
| ($\overline{CE}$ latency = 3) | $I_{BSR}$ | | 2 | |
| Burst stop to output high impedance ($\overline{CE}$ latency = 2) | $I_{BSH}$ | | 2 | |
| ($\overline{CE}$ latency = 3) | $I_{BSH}$ | | 3 | |
| Burst stop to write data ignore | $I_{BSW}$ | | 0 | |

Notes: 1. $I_{RCD}$ to $I_{RRD}$ are recommended value.
2. Be valid [DSEL] or [NOP] at next command of self refresh exit.
3. Except [DSEL] and [NOP]

## Pin Functions

**CK0/CK1 (input pin):** CK is the master clock input to this pin. The other input signals are referred at CK rising edge.

**$\overline{S0}$ (input pin):** When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

**$\overline{RE}$, $\overline{CE}$ and $\overline{W}$ (input pins):** Although these pin names are the same as those of conventional DRAM modules, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

**A0 to A11 (input pins):** Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address (AY0 to AY9) is determined by A0 to A9 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A12/A13 (BA) is precharged.

**A12/A13 (input pin):** A12/A13 is a bank select signal (BA). The memory array is divided into bank0, bank1, bank2 and bank3, If A12 is Low and A13 is Low, bank0 is selected. If A12 is High and A13 is Low, bank1 is selected. If A12 is Low and A13 is High, bank2 is selected. If A12 is High and A13 is HIgh, bank3 is selected.

**CKE0 (input pin):** This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.

**DQMB0 to DQMB7 (input pins):** Read operation: If DQMB is High, the output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z.

Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.

**DQ0 to DQ63 (DQ pins):** Data is input to and output from these pins.

**$V_{CC}$ (power supply pins):** 3.3 V is applied.

**$V_{SS}$ (power supply pins):** Ground is connected.

## Command Operation

### Command Truth Table

The SDRAM module recognizes the following commands specified by the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, $\overline{W}$ and address pins.

| | | CKE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Command** | **Symbol** | **n - 1** | **n** | $\overline{S}$ | $\overline{RE}$ | $\overline{CE}$ | $\overline{W}$ | **A12/A13** | **A10** | **A0 to A11** |
| Ignore command | DESL | H | × | H | × | × | × | × | × | × |
| No operation | NOP | H | × | L | H | H | H | × | × | × |
| Burst stop in full page | BST | H | × | L | H | H | L | × | × | × |
| Column address and read command | READ | H | × | L | H | L | H | V | L | V |
| Read with auto-precharge | READ A | H | × | L | H | L | H | V | H | V |
| Column address and write command | WRIT | H | × | L | H | L | L | V | L | V |
| Write with auto-precharge | WRIT A | H | × | L | H | L | L | V | H | V |
| Row address strobe and bank active | ACTV | H | × | L | L | H | H | V | V | V |
| Precharge select bank | PRE | H | × | L | L | H | L | V | L | × |
| Precharge all bank | PALL | H | × | L | L | H | L | × | H | × |
| Refresh | REF/SELF | H | V | L | L | L | H | × | × | × |
| Mode register set | MRS | H | × | L | L | L | L | V | V | V |

Note: H: $V_{IH}$. L: $V_{IL}$. ×: $V_{IH}$ or $V_{IL}$. V: Valid address input

**Ignore command [DESL]:** When this command is set ($\overline{S}$ is High), the SDRAM module ignore command input at the clock. However, the internal status is held.

**No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

**Burst stop in full-page [BST]:** This command stops a full-page burst operation (burst length = full-page) and is illegal otherwise. When data input/output is completed for a full page of data, it automatically returns to the start address, and input/output is performed repeatedly.

**Column address strobe and read command [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address and the bank select address (BA). After the read operation, the output buffer becomes High-Z.

**Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

**Column address strobe and write command [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address and the bank select address (BA) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address and the bank select address (BA).

**Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

**Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by bank select address (BA) and determines the row address (AX0 to AX11). When A12 and A13 are Low, bank 0 is activated. When A12 is High and A13 is Low, bank 1 is activated. When A12 is Low and A13 is High, bank 2 is activated. When A12 and A13 are High, bank 3 is activated.

**Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A12/A13. If A12 and A13 are Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 and A13 are High, bank 3 is selected.

**Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

**Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

**Mode register set [MRS]:** The SDRAM module has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A13) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

**DQMB Truth Table**

| Command | Symbol | CKE n - 1 | CKE n | DQMB |
|---|---|---|---|---|
| Write enable/output enable | ENB | H | × | L |
| Write inhibit/output disable | MASK | H | × | H |

Note: H: $V_{IH}$. L: $V_{IL}$. ×: $V_{IH}$ or $V_{IL}$.
Write: $I_{DID}$ is needed.
Read: $I_{DOD}$ is needed.

The SDRAM module can mask input/output data by means of DQMB.

During reading, the output buffer is set to Low-Z by setting DQMB to Low, enabling data output. On the other hand, when DQMB is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQMB to Low. When DQMB is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQMB. For details, refer to the DQMB control section of the SDRAM module operating instructions.

**CKE Truth Table**

| Current state | Command | CKE n - 1 | CKE n | $\overline{S}$ | $\overline{RE}$ | $\overline{CE}$ | $\overline{W}$ | Address |
|---|---|---|---|---|---|---|---|---|
| Active | Clock suspend mode entry | H | L | H | × | × | × | × |
| Any | Clock suspend | L | L | × | × | × | × | × |
| Clock suspend | Clock suspend mode exit | L | H | × | × | × | × | × |
| Idle | Auto-refresh command (REF) | H | H | L | L | L | H | × |
| Idle | Self-refresh entry (SELF) | H | L | L | L | L | H | × |
| Idle | Power down entry | H | L | L | H | H | H | × |
| | | H | L | H | × | × | × | × |
| Self refresh | Self refresh exit (SELFX) | L | H | L | H | H | H | × |
| | | L | H | H | × | × | × | × |
| Power down | Power down exit | L | H | L | H | H | H | × |
| | | L | H | H | × | × | × | × |

Note: H: $V_{IH}$. L: $V_{IL}$. ×: $V_{IH}$ or $V_{IL}$.

**Clock suspend mode entry:** The SDRAM module enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

**ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

**READ suspend and READ with Auto-precharge suspend:** The data being output is held (and continues to be output).

**WRITE suspend and WRIT with Auto-precharge suspend:** In this mode, external signals are not accepted. However, the internal state is held.

**Clock suspend:** During clock suspend mode, keep the CKE to Low.

**Clock suspend mode exit:** The SDRAM module exits from clock suspend mode by setting CKE to High during the clock suspend state.

**IDLE:** In this state, all banks are not selected, and completed precharge operation.

**Auto-refresh command [REF]:** When this command is input from the IDLE state, the SDRAM module starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the SDRAM module. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

**Self-refresh entry [SELF]:** When this command is input during the IDLE state, the SDRAM module starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

**Power down mode entry:** When this command is executed during the IDLE state, the SDRAM module enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

**Self-refresh exit:** When this command is executed during self-refresh mode, the SDRAM module can exit from self-refresh mode. After exiting from self-refresh mode, the SDRAM module enters the IDLE state.

**Power down exit:** When this command is executed at the power down mode, the SDRAM module can exit from power down mode. After exiting from power down mode, the SDRAM module enters the IDLE state.

### Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the SDRAM module. The following table assumes that CKE is high.

| Current state | $\overline{S}$ | $\overline{RE}$ | $\overline{CE}$ | $\overline{W}$ | Address | Command | Operation |
|---|---|---|---|---|---|---|---|
| Precharge | H | × | × | × | × | DESL | Enter IDLE after $t_{RP}$ |
| | L | H | H | H | × | NOP | Enter IDLE after $t_{RP}$ |
| | L | H | H | L | × | BST | NOP |
| | L | H | L | H | BA, CA, A10 | READ/READ A | ILLEGAL*[4] |
| | L | H | L | L | BA, CA, A10 | WRIT/WRIT A | ILLEGAL*[4] |
| | L | L | H | H | BA, RA | ACTV | ILLEGAL*[4] |
| | L | L | H | L | BA, A10 | PRE, PALL | NOP*[6] |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |
| Idle | H | × | × | × | × | DESL | NOP |
| | L | H | H | H | × | NOP | NOP |
| | L | H | H | L | × | BST | NOP |
| | L | H | L | H | BA, CA, A10 | READ/READ A | ILLEGAL*[5] |
| | L | H | L | L | BA, CA, A10 | WRIT/WRIT A | ILLEGAL*[5] |
| | L | L | H | H | BA, RA | ACTV | Bank and row active |
| | L | L | H | L | BA, A10 | PRE, PALL | NOP |
| | L | L | L | H | × | REF, SELF | Refresh |
| | L | L | L | L | MODE | MRS | Mode register set |
| Row active | H | × | × | × | × | DESL | NOP |
| | L | H | H | H | × | NOP | NOP |
| | L | H | H | L | × | BST | NOP |
| | L | H | L | H | BA, CA, A10 | READ/READ A | Begin read |
| | L | H | L | L | BA, CA, A10 | WRIT/WRIT A | Begin write |
| | L | L | H | H | BA, RA | ACTV | Other bank active<br>ILLEGAL on same bank*[3] |
| | L | L | H | L | BA, A10 | PRE, PALL | Precharge |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |

| Current state | $\overline{S}$ | $\overline{RE}$ | $\overline{CE}$ | $\overline{W}$ | Address | Command | Operation |
|---|---|---|---|---|---|---|---|
| Read | H | × | × | × | × | DESL | Continue burst to end |
| | L | H | H | H | × | NOP | Continue burst to end |
| | L | H | H | L | × | BST | Burst stop to full page |
| | L | H | L | H | BA, CA, A10 | READ/READ A | Continue burst read to $\overline{CE}$ latency and New read |
| | L | H | L | L | BA, CA, A10 | WRIT/WRIT A | Term burst read/start write |
| | L | L | H | H | BA, RA | ACTV | Other bank active ILLEGAL on same bank*[3] |
| | L | L | H | L | BA, A10 | PRE, PALL | Term burst read and Precharge |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |
| Read with auto-precharge | H | × | × | × | × | DESL | Continue burst to end and precharge |
| | L | H | H | H | × | NOP | Continue burst to end and precharge |
| | L | H | H | L | × | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READ A | ILLEGAL*[4] |
| | L | H | L | L | BA, CA, A10 | WRIT/WRIT A | ILLEGAL*[4] |
| | L | L | H | H | BA, RA | ACTV | Other bank active ILLEGAL on same bank*[3] |
| | L | L | H | L | BA, A10 | PRE, PALL | ILLEGAL*[4] |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |
| Write | H | × | × | × | × | DESL | Continue burst to end |
| | L | H | H | H | × | NOP | Continue burst to end |
| | L | H | H | L | × | BST | Burst stop on full page |
| | L | H | L | H | BA, CA, A10 | READ/READ A | Term burst and New read |
| | L | H | L | L | BA, CA, A10 | WRIT/WRIT A | Term burst and New write |
| | L | L | H | H | BA, RA | ACTV | Other bank active ILLEGAL on same bank*[3] |
| | L | L | H | L | BA, A10 | PRE, PALL | Term burst write and Precharge*[2] |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |

| Current state | $\overline{S}$ | $\overline{RE}$ | $\overline{CE}$ | $\overline{W}$ | Address | Command | Operation |
|---|---|---|---|---|---|---|---|
| Write with auto-precharge | H | × | × | × | × | DESL | Continue burst to end and precharge |
| | L | H | H | H | × | NOP | Continue burst to end and precharge |
| | L | H | H | L | × | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READ A | ILLEGAL*[4] |
| | L | H | L | L | BA, CA, A10 | WRIT/WRIT A | ILLEGAL*[4] |
| | L | L | H | H | BA, RA | ACTV | Other bank active<br>ILLEGAL on same bank*[3] |
| | L | L | H | L | BA, A10 | PRE, PALL | ILLEGAL*[4] |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |
| Refresh (auto-refresh) | H | × | × | × | × | DESL | Enter IDLE after $t_{RC}$ |
| | L | H | H | H | × | NOP | Enter IDLE after $t_{RC}$ |
| | L | H | H | L | × | BST | Enter IDLE after $t_{RC}$ |
| | L | H | L | H | BA, CA, A10 | READ/READ A | ILLEGAL*[5] |
| | L | H | L | L | BA, CA, A10 | WRIT/WRIT A | ILLEGAL*[5] |
| | L | L | H | H | BA, RA | ACTV | ILLEGAL*[5] |
| | L | L | H | L | BA, A10 | PRE, PALL | ILLEGAL*[5] |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |

Notes: 1. H: $V_{IH}$. L: $V_{IL}$. ×: $V_{IH}$ or $V_{IL}$.
The other combinations are inhibit.
2. An interval of $t_{DPL}$ is required between the final valid data input and the precharge command.
3. If $t_{RRD}$ is not satisfied, this operation is illegal.
4. Illegal for same bank, except for another bank.
5. Illegal for all banks.
6. NOP for same bank, except for another bank.

**From PRECHARGE state, command operation**

**To [DESL], [NOP] or [BST]:** When these commands are executed, the SDRAM module enters the IDLE state after $t_{RP}$ has elapsed from the completion of precharge.

**From IDLE state, command operation**

**To [DESL], [NOP], [BST], [PRE] or [PALL]:** These commands result in no operation.

**To [ACTV]:** The bank specified by the address pins and the ROW address is activated.

**To [REF], [SELF]:** The SDRAM module enters refresh mode (auto-refresh or self-refresh).

**To [MRS]:** The SDRAM module enters the mode register set cycle.

**From ROW ACTIVE state, command operation**

**To [DESL], [NOP] or [BST]:** These commands result in no operation.

**To [READ], [READ A]:** A read operation starts. (However, an interval of $t_{RCD}$ is required.)

**To [WRIT], [WRIT A]:** A write operation starts. (However, an interval of $t_{RCD}$ is required.)

**To [ACTV]:** This command makes the other bank active. (However, an interval of $t_{RRD}$ is required.) Attempting to make the currently active bank active results in an illegal command.

**To [PRE], [PALL]:** These commands set the SDRAM module to precharge mode. (However, an interval of $t_{RAS}$ is required.)

**From READ state, command operation**

**To [DESL], [NOP]:** These commands continue read operations until the burst operation is completed.

**To [BST]:** This command stops a full-page burst.

**To [READ], [READ A]:** Data output by the previous read command continues to be output. After $\overline{CE}$ latency, the data output resulting from the next command will start.

**To [WRIT], [WRIT A]:** These commands stop a burst read, and start a write cycle.

**To [ACTV]:** This command makes other banks bank active. (However, an interval of $t_{RRD}$ is required.) Attempting to make the currently active bank active results in an illegal command.

**To [PRE], [PALL]:** These commands stop a burst read, and the SDRAM module enters precharge mode.

**From READ with AUTO-PRECHARGE state, command operation**

**To [DESL], [NOP]:** These commands continue read operations until the burst operation is completed, and the SDRAM module then enters precharge mode.

**To [ACTV]:** This command makes other banks bank active. (However, an interval of $t_{RRD}$ is required.) Attempting to make the currently active bank active results in an illegal command.

**From WRITE state, command operation**

**To [DESL], [NOP]:** These commands continue write operations until the burst operation is completed.

**To [BST]:** This command stops a full-page burst.

**To [READ], [READ A]:** These commands stop a burst and start a read cycle.

**To [WRIT], [WRIT A]:** These commands stop a burst and start the next write cycle.

**To [ACTV]:** This command makes the other bank active. (However, an interval of $t_{RRD}$ is required.) Attempting to make the currently active bank active results in an illegal command.

**To [PRE], [PALL]:** These commands stop burst write and the SDRAM module then enters precharge mode.

**From WRITE with AUTO-PRECHARGE state, command operation**

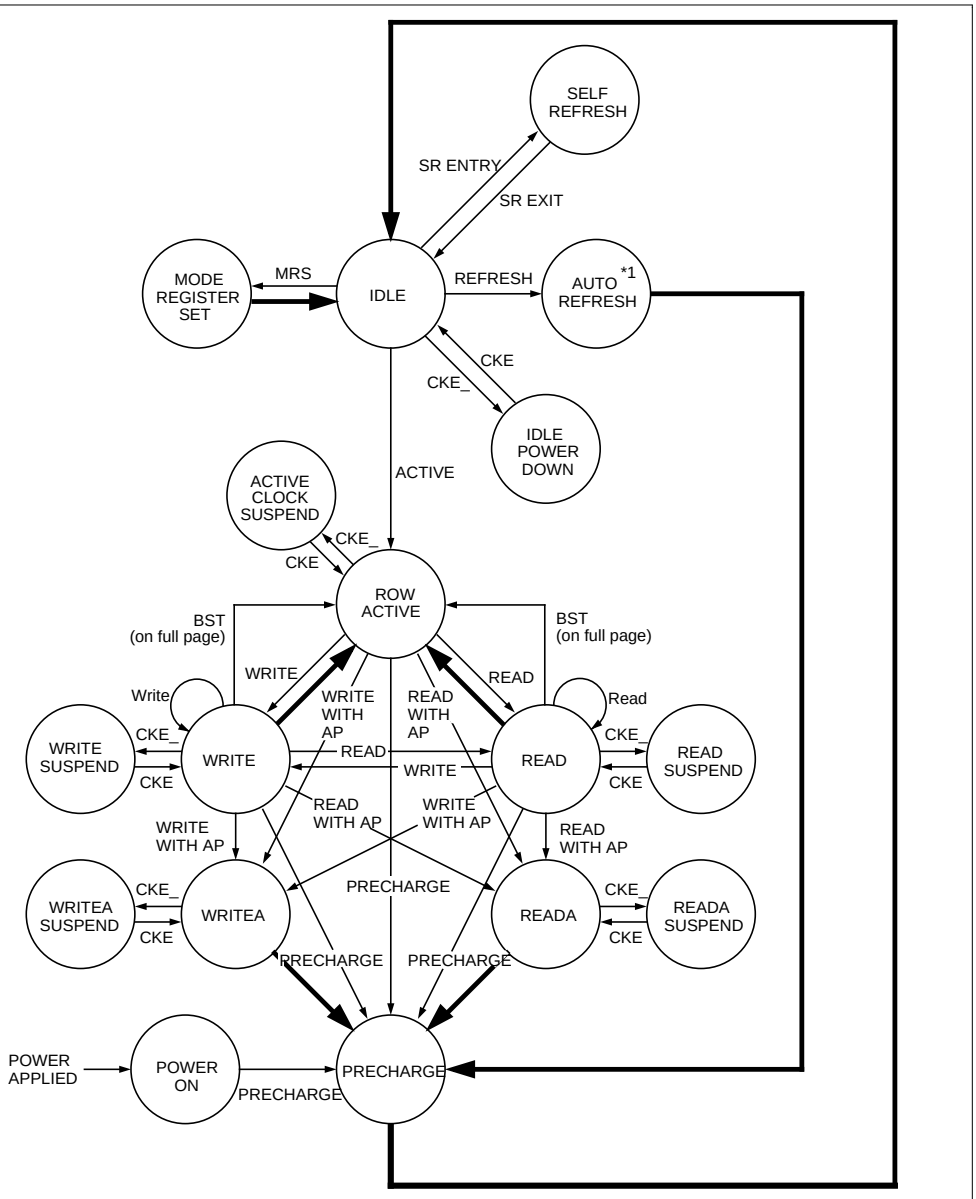
**To [DESL], [NOP]:** These commands continue write operations until the burst is completed, and the SDRAM module enters precharge mode.

**To [ACTV]:** This command makes the other bank active. (However, an interval of $t_{RRD}$ is required.) Attempting to make the currently active bank active results in an illegal command.

**From REFRESH state, command operation**

**To [DESL], [NOP], [BST]:** After an auto-refresh cycle (after $t_{RC}$), the SDRAM module automatically enters the IDLE state.

## Simplified State Diagram




Automatic transition after completion of command.

Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

## Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A13) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

**A13, A12, A11, A10, A9 A8: (OPCODE):** The SDRAM module has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

**Burst read and burst write:** Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

**Burst read and single write:** Data is only written to the column address specified during the write cycle, regardless of the burst length.

**A7:** Keep this bit Low at the mode register set cycle. If this pin is high, the vender test mode is set.

**A6, A5, A4: (LMODE):** These pins specify the $\overline{CE}$ latency.

**A3: (BT):** A burst type is specified. When full-page burst is performed, only "sequential" can be selected.

**A2, A1, A0: (BL):** These pins specify the burst length.

| A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPCODE | | | | | | 0 | LMODE | | | BT | BL | | |

| A6 | A5 | A4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | R |
| 0 | 0 | 1 | R |
| 0 | 1 | 0 | 2* |
| 0 | 1 | 1 | 3 |
| 1 | X | X | R |

| A3 | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

| A2 | A1 | A0 | Burst Length | |
|---|---|---|---|---|
| | | | BT=0 | BT=1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | R | R |
| 1 | 0 | 1 | R | R |
| 1 | 1 | 0 | R | R |
| 1 | 1 | 1 | F.P. | R |

| A13 | A12 | A11 | A10 | A9 | A8 | Write mode |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Burst read and burst write |
| X | X | X | X | 0 | 1 | R |
| X | X | X | X | 1 | 0 | Burst read and single write |
| X | X | X | X | 1 | 1 | R |

F.P. = Full Page
R is Reserved (inhibit)
X: 0 or 1

Note: only -A6.

**Burst Sequence**

Burst length = 2

| Starting Ad. | Addressing(decimal) | |
|---|---|---|
| A0 | Sequential | Interleave |
| 0 | 0, 1, | 0, 1, |
| 1 | 1, 0, | 1, 0, |

Burst length = 4

| Starting Ad. | | Addressing(decimal) | |
|---|---|---|---|
| A1 | A0 | Sequential | Interleave |
| 0 | 0 | 0, 1, 2, 3, | 0, 1, 2, 3, |
| 0 | 1 | 1, 2, 3, 0, | 1, 0, 3, 2, |
| 1 | 0 | 2, 3, 0, 1, | 2, 3, 0, 1, |
| 1 | 1 | 3, 0, 1, 2, | 3, 2, 1, 0, |

Burst length = 8

| Starting Ad. | | | Addressing(decimal) | |
|---|---|---|---|---|
| A2 | A1 | A0 | Sequential | Interleave |
| 0 | 0 | 0 | 0, 1, 2, 3, 4, 5, 6, 7, | 0, 1, 2, 3, 4, 5, 6, 7, |
| 0 | 0 | 1 | 1, 2, 3, 4, 5, 6, 7, 0, | 1, 0, 3, 2, 5, 4, 7, 6, |
| 0 | 1 | 0 | 2, 3, 4, 5, 6, 7, 0, 1, | 2, 3, 0, 1, 6, 7, 4, 5, |
| 0 | 1 | 1 | 3, 4, 5, 6, 7, 0, 1, 2, | 3, 2, 1, 0, 7, 6, 5, 4, |
| 1 | 0 | 0 | 4, 5, 6, 7, 0, 1, 2, 3, | 4, 5, 6, 7, 0, 1, 2, 3, |
| 1 | 0 | 1 | 5, 6, 7, 0, 1, 2, 3, 4, | 5, 4, 7, 6, 1, 0, 3, 2, |
| 1 | 1 | 0 | 6, 7, 0, 1, 2, 3, 4, 5, | 6, 7, 4, 5, 2, 3, 0, 1, |
| 1 | 1 | 1 | 7, 0, 1, 2, 3, 4, 5, 6, | 7, 6, 5, 4, 3, 2, 1, 0, |

## Operation of the SDRAM module

### Read/Write Operations

**Bank active:** Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Bank 0, bank 1, bank 2 or bank 3 is activated according to the status of the bank select address (BA) pin, and the row address (AX0 to AX11) is activated by the A0 to A11 pins at the bank active command cycle. An interval of $t_{RCD}$ is required between the bank active command input and the following read/write command input.

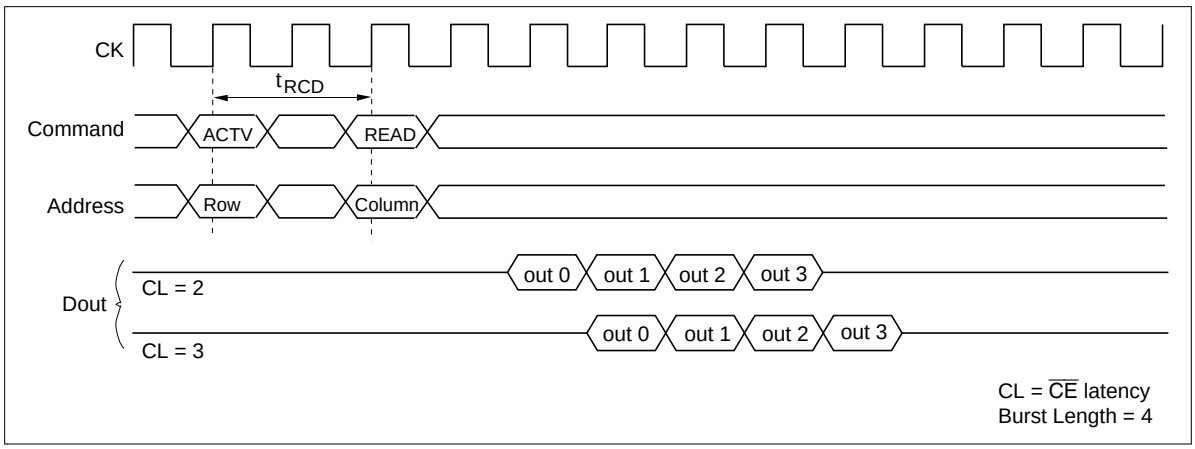
**Read operation:** A read operation starts when a read command is input. Output buffer becomes Low-Z in the ($\overline{CE}$ Latency - 1) cycle after read command set. The SDRAM module can perform a burst read operation.

The burst length can be set to 1, 2, 4, 8 or full-page. The start address for a burst read is specified by the column address and the bank select address (BA) at the read command set cycle. In a read operation, data output starts after the number of clocks specified by the $\overline{CE}$ Latency. The $\overline{CE}$ Latency can be set to 2 or 3.

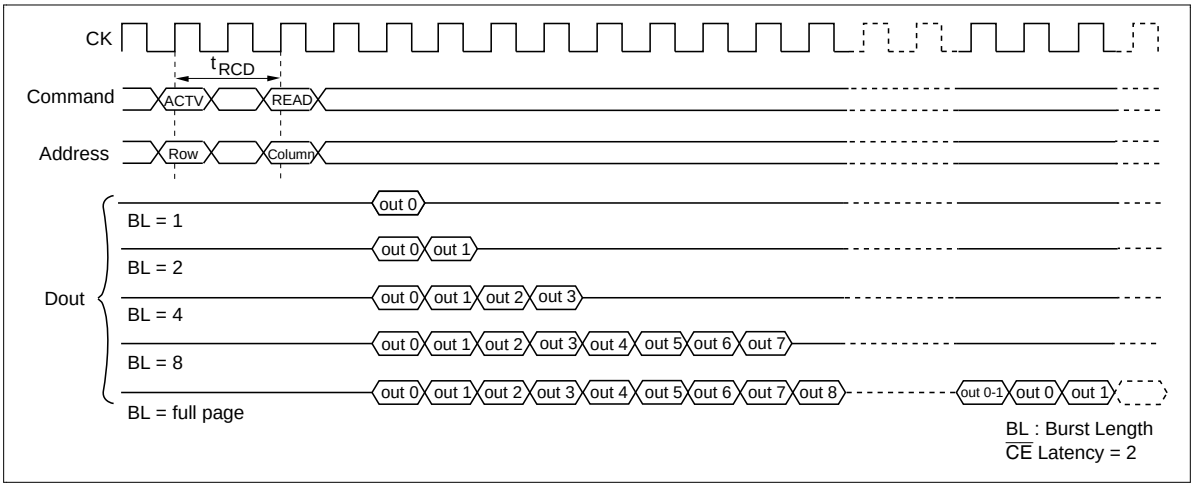
When the burst length is 1, 2, 4 or 8, the Dout buffer automatically becomes High-Z at the next clock after the successive burst-length data has been output.

The $\overline{CE}$ latency and burst length must be specified at the mode register.

### $\overline{CE}$ Latency

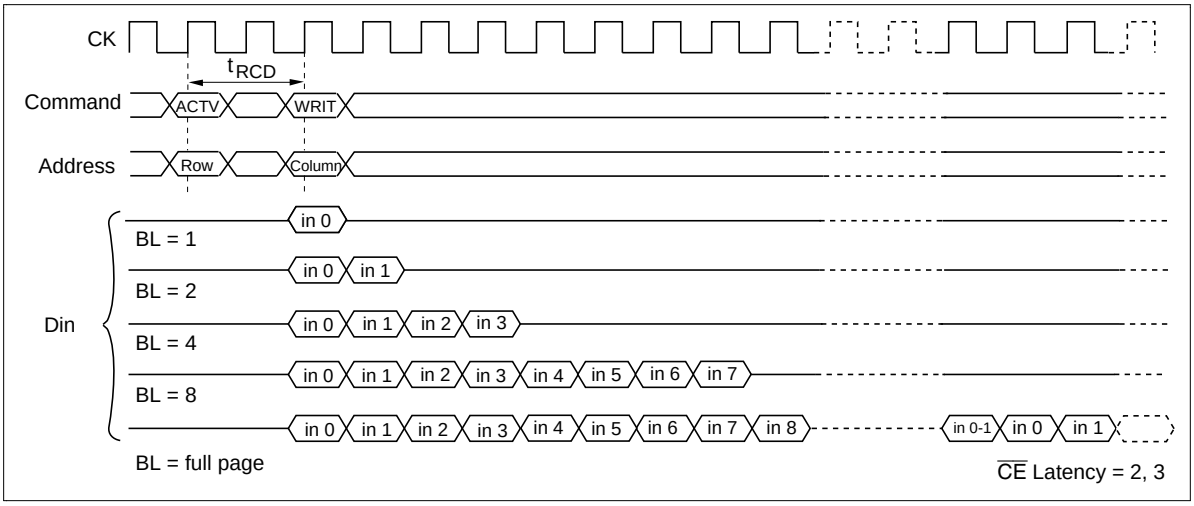


**Burst Length**

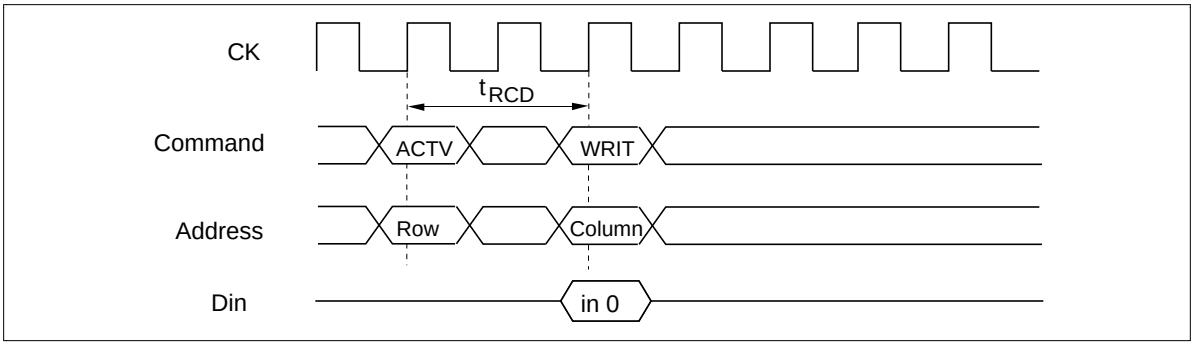



**Write operation:** Burst write or single write mode is selected by the OPCODE (A13, A12, A11, A10, A9, A8) of the mode register.

**1. Burst write:** A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same clock as a write command set. (The latency of data input is 0 clock.) The burst length can be set to 1, 2, 4, 8, and full-page, like burst read operations. The write start address is specified by the column address and the bank select address (BA) at the write command set cycle.



**2. Single write:** A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address and the bank select address (BA) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0 clock).

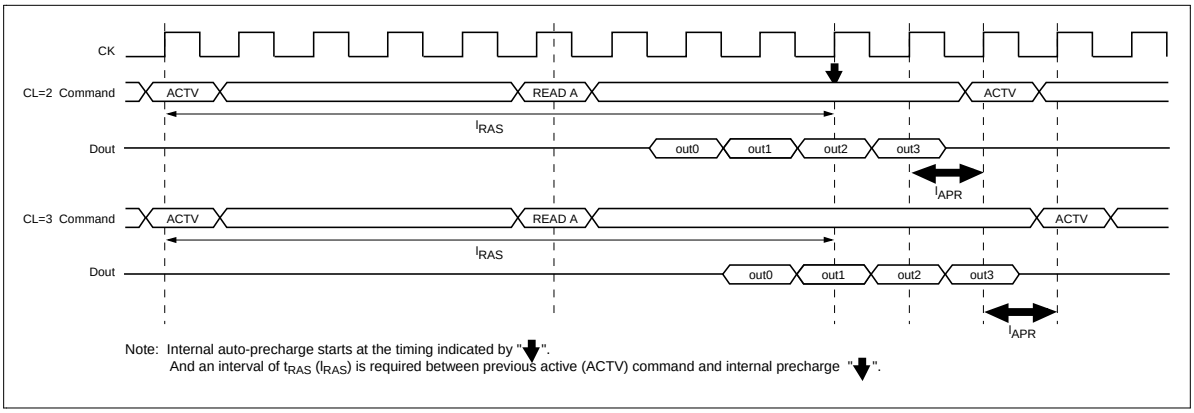



**Auto Precharge**

**Read with auto-precharge:** In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by $l_{APR}$ is required before execution of the next command.

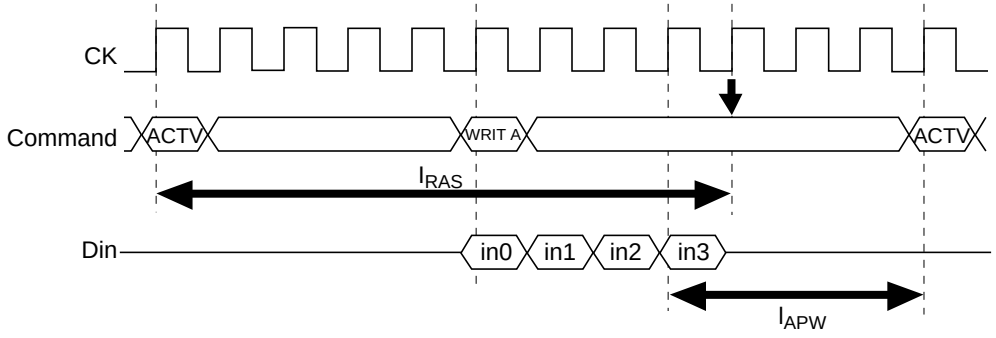
| $\overline{CE}$ latency | Precharge start cycle |
|---|---|
| 3 | 2 cycle before the final data is output |
| 2 | 1 cycle before the final data is output |

**Burst Read (Burst Length = 4)**



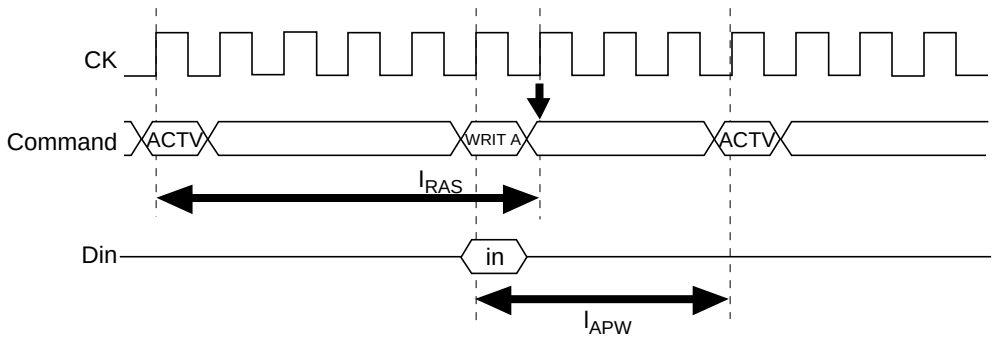
**Write with auto-precharge:** In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of $l_{APW}$ is required between the final valid data input and input of next command.

**Burst Write (Burst Length = 4)**




Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of $t_{RAS}$ ($l_{RAS}$) is required between previous active (ACTV) command and internal precharge "↓".

**Single Write**



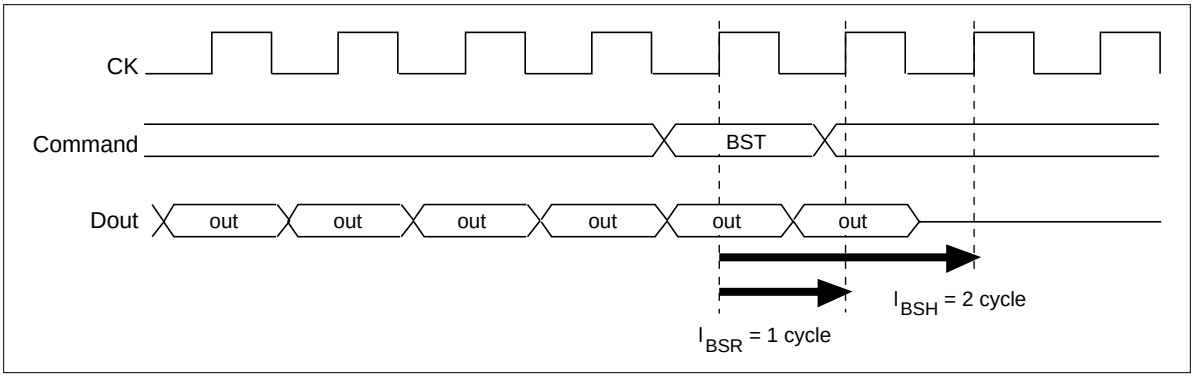

Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of $t_{RAS}$ ($l_{RAS}$) is required between previous active (ACTV) command and internal precharge "↓".

### Full-page Burst Stop

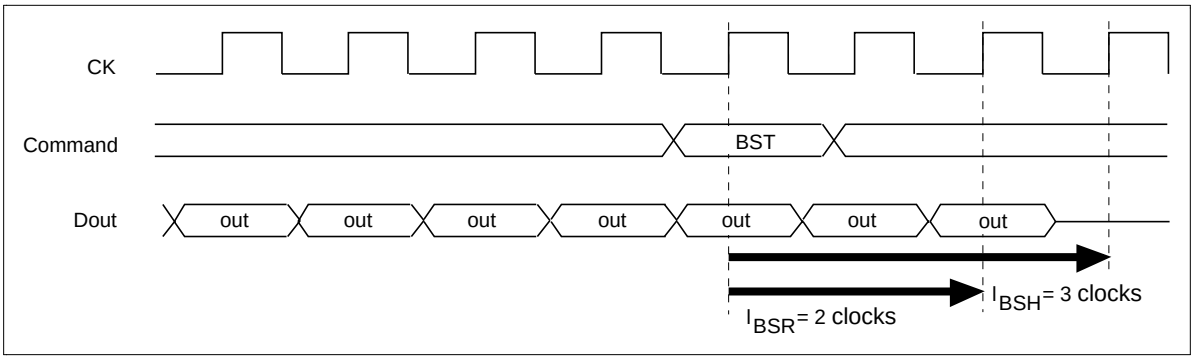
**Burst stop command during burst read:** The burst stop (BST) command is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read. The timing from command input to the last data changes depending on the $\overline{CE}$ latency setting. In addition, the BST command is valid only during full-page burst mode, and is illegal with burst lengths 1, 2, 4 and 8.

| $\overline{CE}$ latency | BST to valid data | BST to high impedance |
|---|---|---|
| 2 | 1 | 2 |
| 3 | 2 | 3 |

**$\overline{CE}$ Latency = 2, Burst Length = full page**

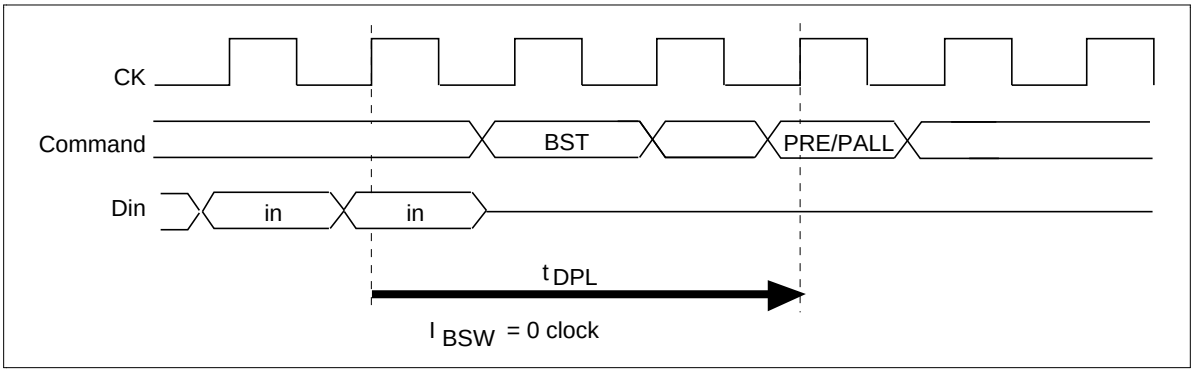



**$\overline{CE}$ Latency = 3, Burst Length = full page**



**Burst stop command at burst write:** The burst stop command (BST command) is used to stop data input during a full-page burst write. No data is written in the same clock as the BST command, and in subsequent clocks. In addition, the BST command is only valid during full-page burst mode, and is illegal with burst lengths of 1, 2, 4 and 8. And an interval of $t_{DPL}$ is required between last data-in and the next precharge command.

**Burst Length = full page**

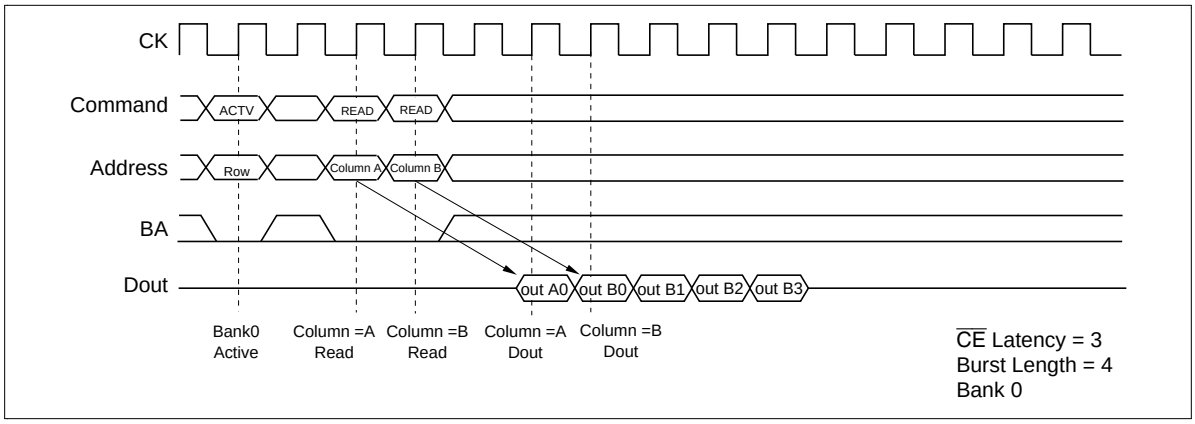


**Command Intervals**

**Read command to Read command interval:**

**1. Same bank, same ROW address:** When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 clock. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

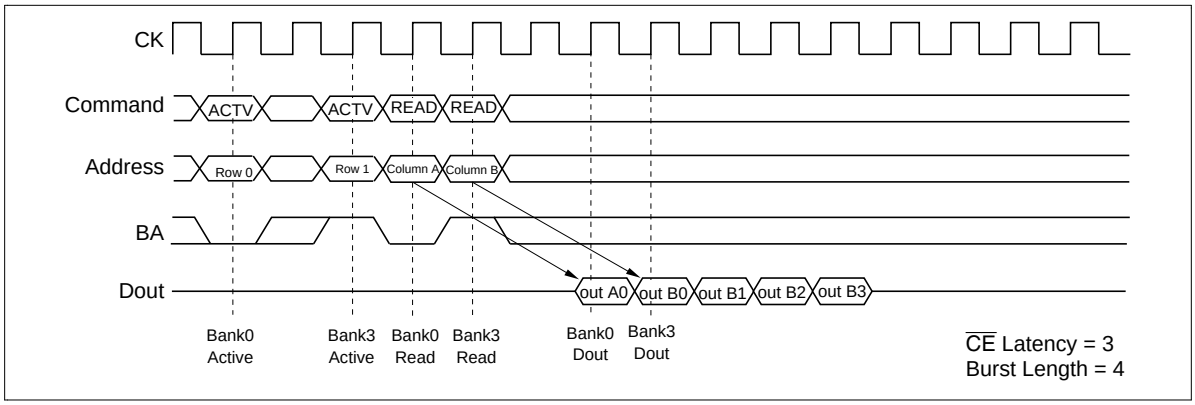
**READ to READ Command Interval** (same ROW address in same bank)




**2. Same bank, different ROW address:** When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank-active command.

**3. Different bank:** When the bank changes, the second read can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

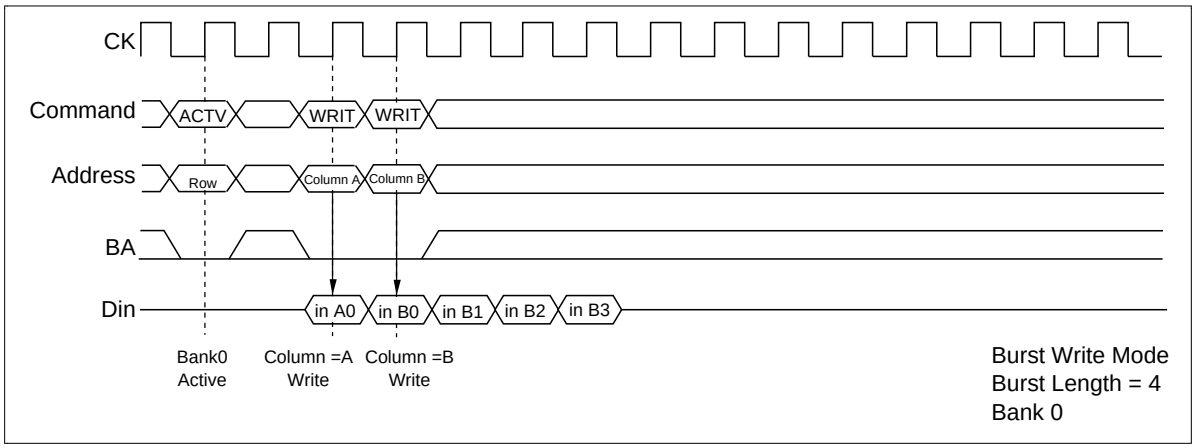
**READ to READ Command Interval** (different bank)



**Write command to Write command interval:**

**1. Same bank, same ROW address:** When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 clock. In the case of burst writes, the second write command has priority.

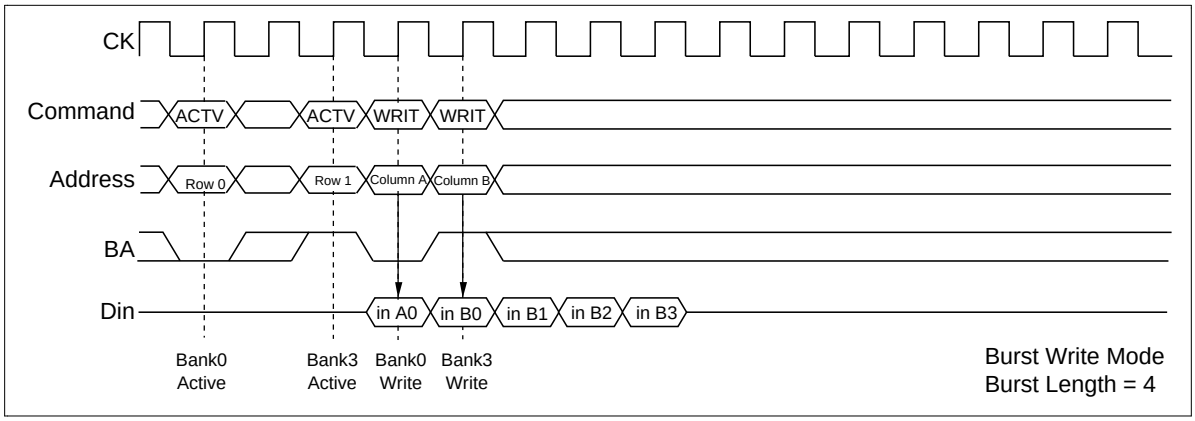
**WRITE to WRITE Command Interval** (same ROW address in same bank)




**2. Same bank, different ROW address:** When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

**3. Different bank:** When the bank changes, the second write can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

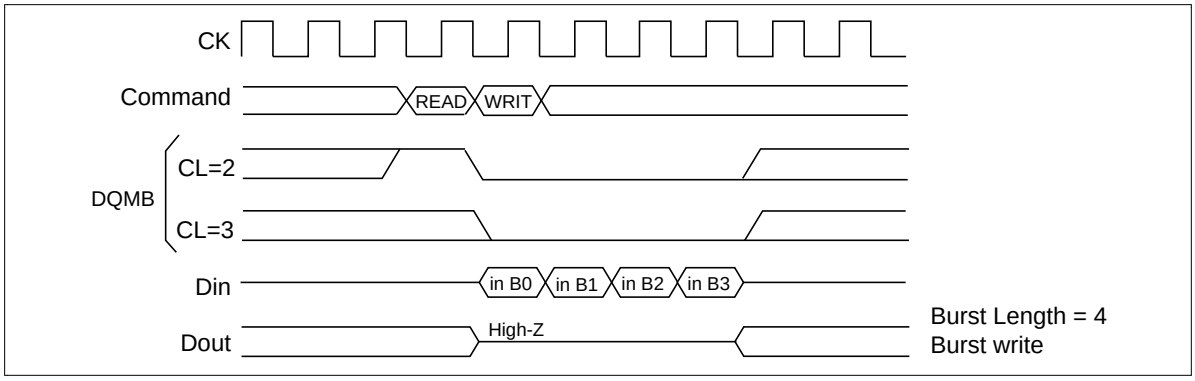
**WRITE to WRITE Command Interval** (different bank)



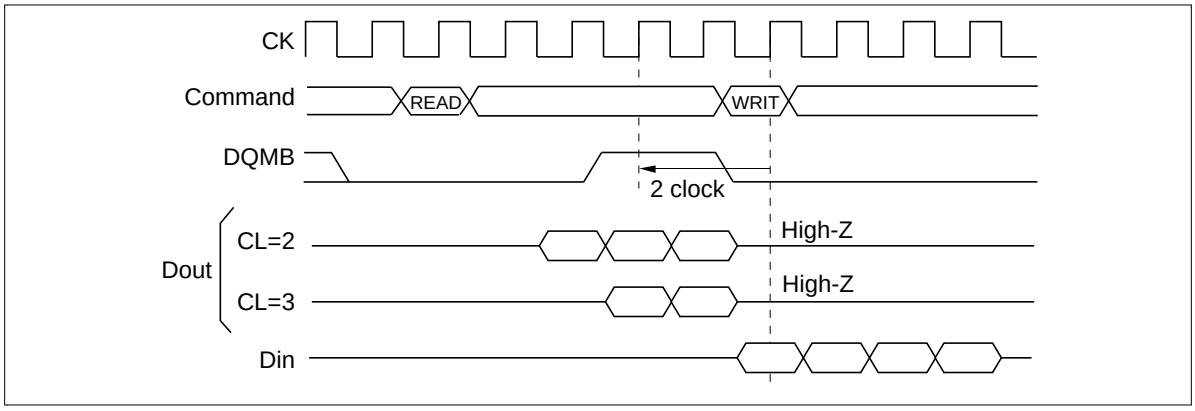
**Read command to Write command interval:**

**1. Same bank, same ROW address:** When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 clock. However, DQMB must be set High so that the output buffer becomes High-Z before data input.

**READ to WRITE Command Interval (1)**




**READ to WRITE Command Interval (2)**



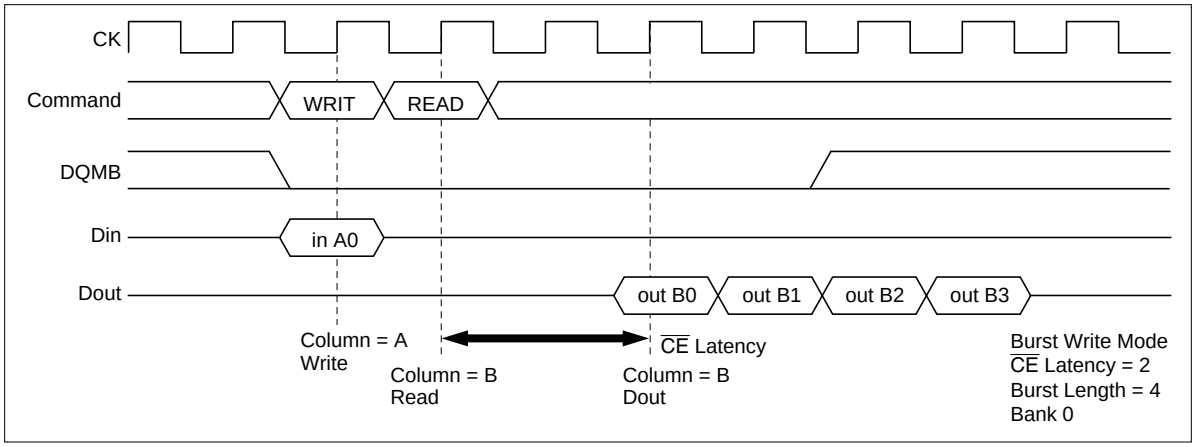

**2. Same bank, different ROW address:** When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

**3. Different bank:** When the bank changes, the write command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. However, DQMB must be set High so that the output buffer becomes High-Z before data input.

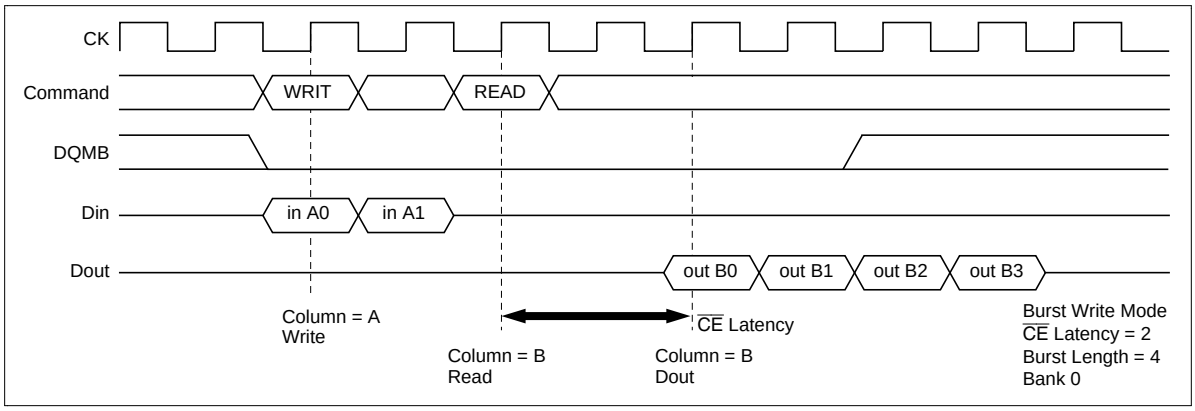
**Write command to Read command interval:**

**1. Same bank, same ROW address:** When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 clock. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

**WRITE to READ Command Interval (1)**




**WRITE to READ Command Interval (2)**



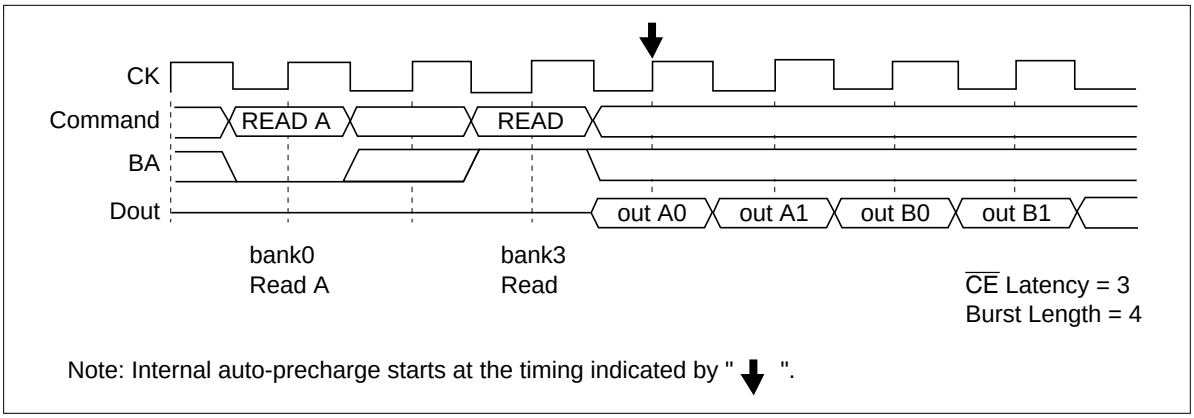

**2. Same bank, different ROW address:** When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

**3. Different bank:** When the bank changes, the read command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed (as in the case of the same bank and the same address).

**Read with auto precharge to Read command interval**

**1. Different bank:** When some banks are in the active state, the second read command (another bank) is executed. Even when the first read with auto-precharge is a burst read that is not yet finished, the data read by the second command is valid. The internal auto-precharge of one bank starts at the next clock of the second command.

**Read with Auto Precharge to Read Command Interval** (Different bank)

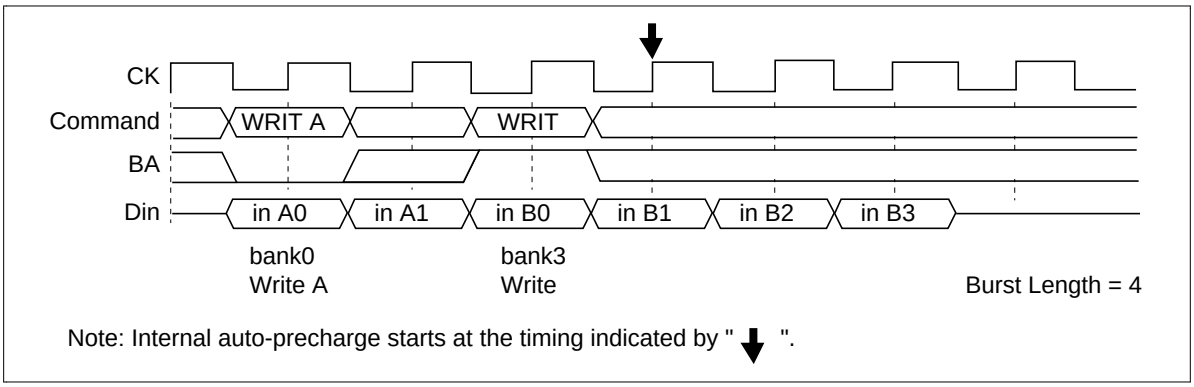



**2. Same bank:** The consecutive read command (the same bank) is illegal.

**Write with auto precharge to Write command interval**

**1. Different bank:** When some banks are in the active state, the second write command (another bank) is executed. In the case of burst writes, the second write command has priority. The internal auto-precharge of one bank starts at the next clock of the second command .

**Write with Auto Precharge to Write Command Interval** (Different bank)

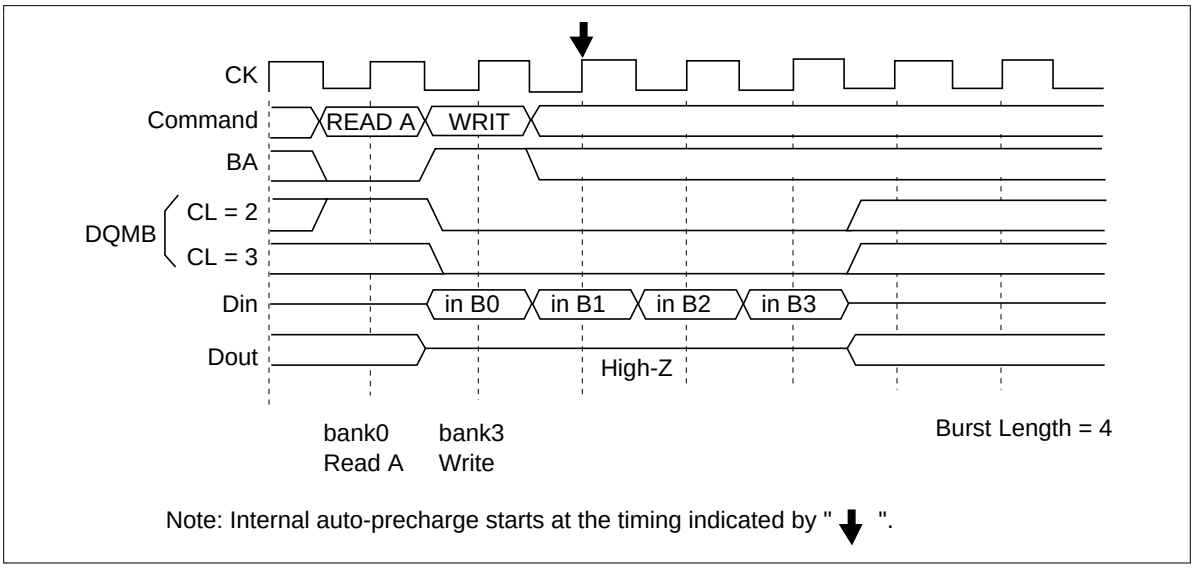



**2. Same bank:** The consecutive write command (the same bank) is illegal.

**Read with auto precharge to Write command interval**

**Different bank:** When some banks are in the active state, the second write command (another bank) is executed. However, DQMB must be set High so that the output buffer becomes High-Z before data input. The internal auto-precharge of one bank starts at the next clock of the second command.

**Read with Auto Precharge to Write Command Interval** (Different bank)

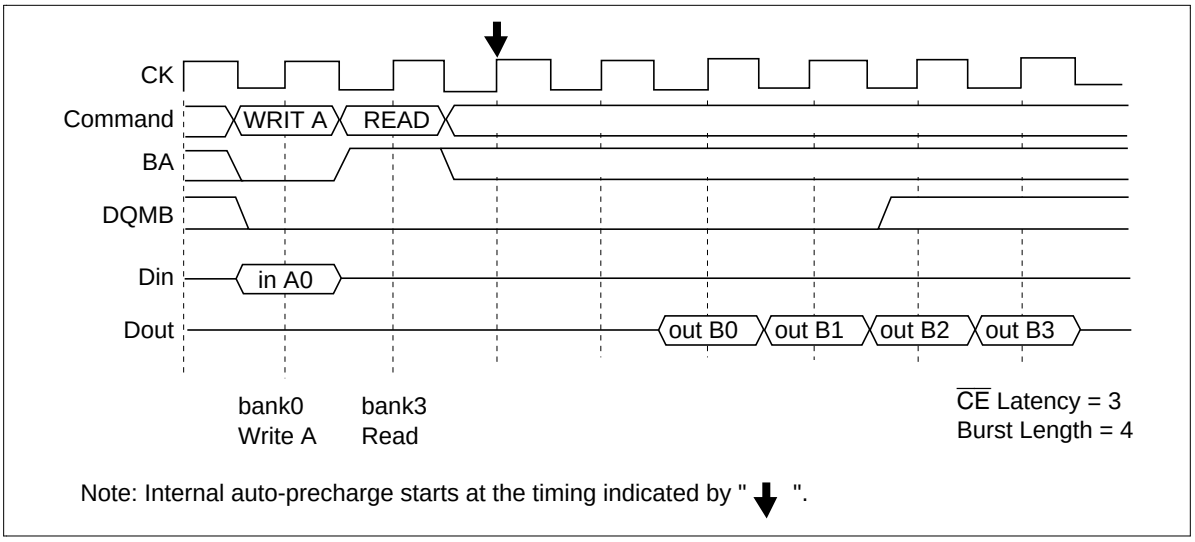



**2. Same bank:** The consecutive write command from read with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

**Write with auto precharge to Read command interval**

**1. Different bank:** When some banks are in the active state, the second read command (another bank) is executed. However, in case of a burst write, data will continue to be written until one clock before the read command is executed. The internal auto-precharge of one bank starts at the next clock of the second command.

**Write with Auto Precharge to Read Command Interval** (Different bank)



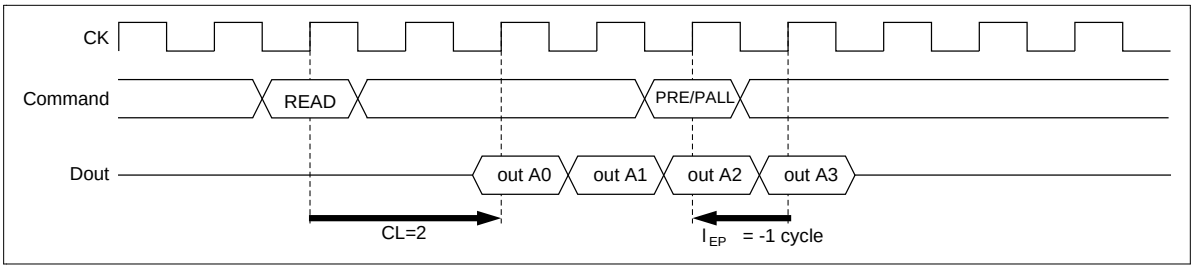

**2. Same bank:** The consecutive read command from write with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

**Read command to Precharge command interval (same bank):**

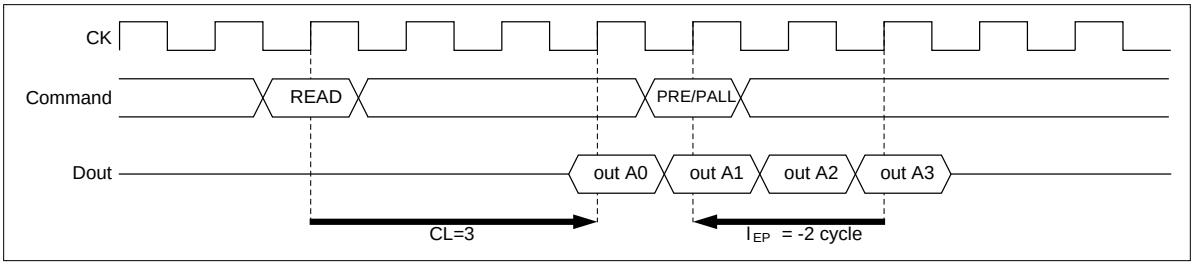
When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one clock. However, since the output buffer then becomes High-Z after the clocks defined by $l_{HZP}$, there is a case of interruption to burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the clocks defined by $l_{EP}$ must be assured as an interval from the final data output to precharge command execution.

**READ to PRECHARGE Command Interval (same bank): To output all data**

**$\overline{CE}$ Latency = 2, Burst Length = 4**

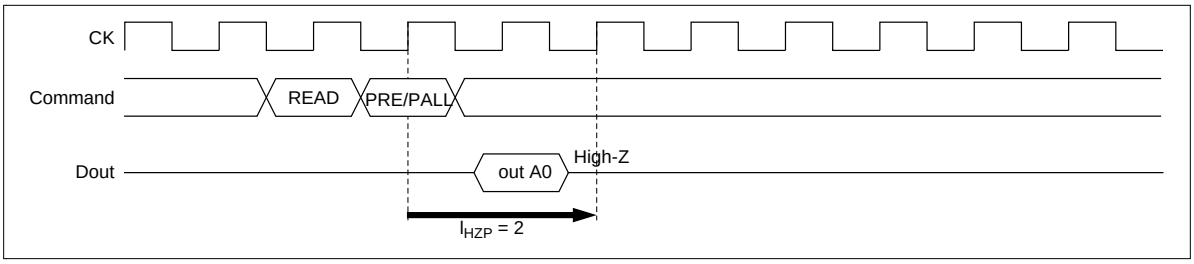



**$\overline{CE}$ Latency = 3, Burst Length = 4**

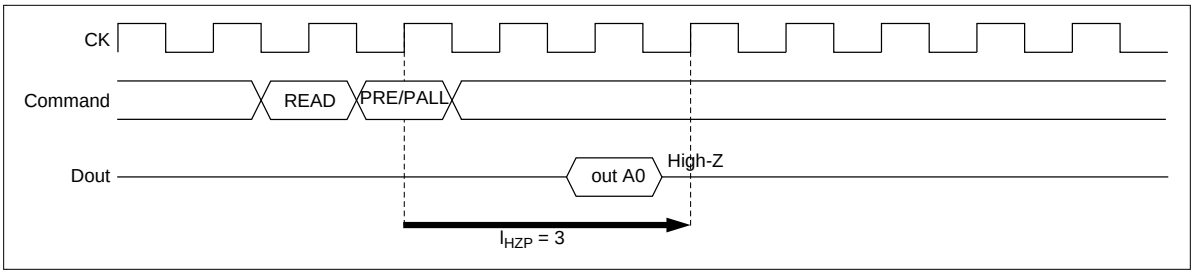


**READ to PRECHARGE Command Interval (same bank): To stop output data**

**$\overline{CE}$ Latency = 2, Burst Length = 1, 2, 4, 8, full page burst**



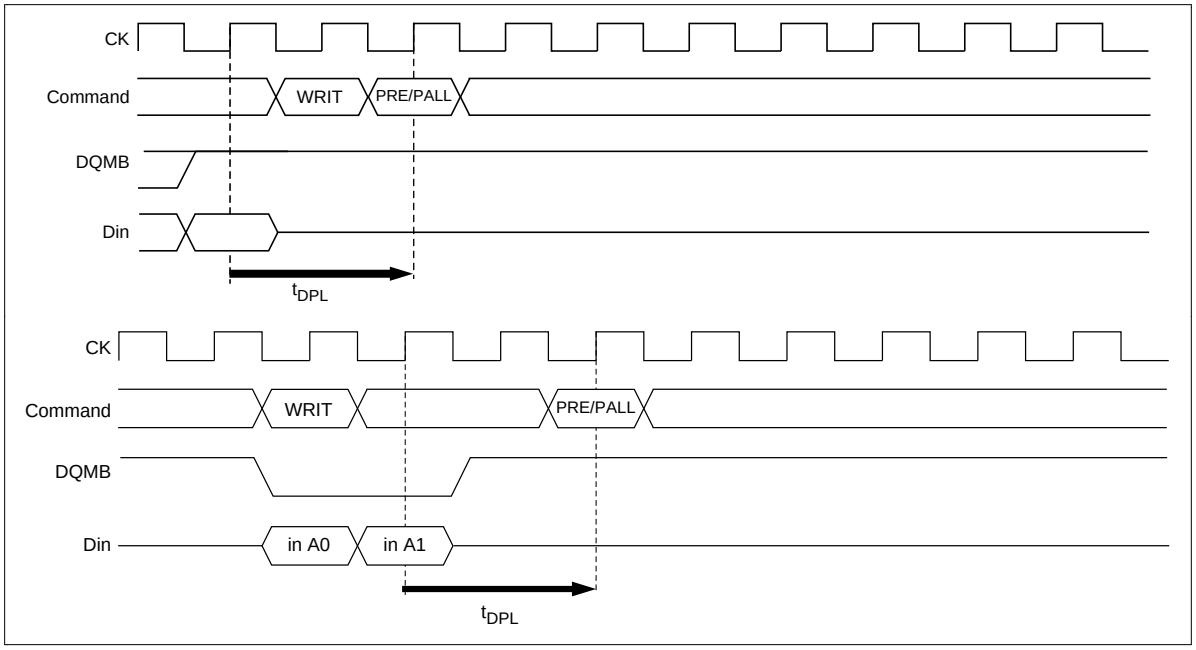

**$\overline{CE}$ Latency = 3, Burst Length = 1, 2, 4, 8, full page burst**



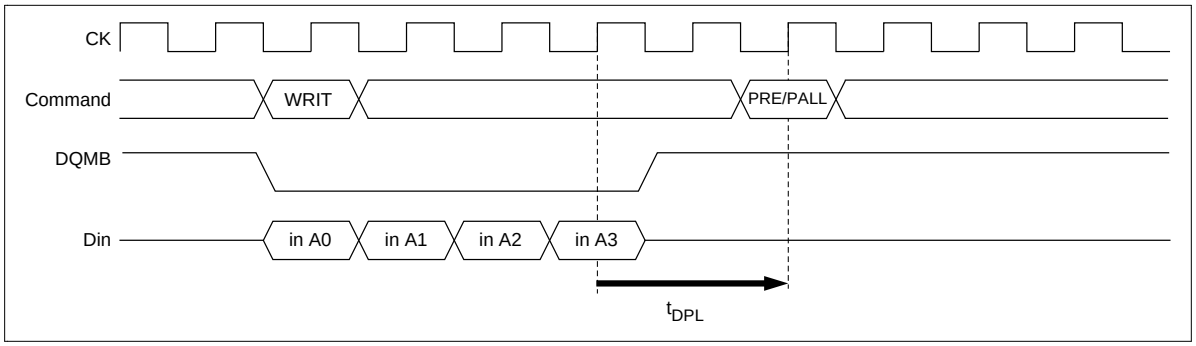
**Write command to Precharge command interval (same bank):** When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 clock. However, if the burst write operation is unfinished, the input data must be masked by means of DQMB for assurance of the clock defined by $t_{DPL}$.

**WRITE to PRECHARGE Command Interval (same bank):**

**Burst Length = 4** (To stop write operation)



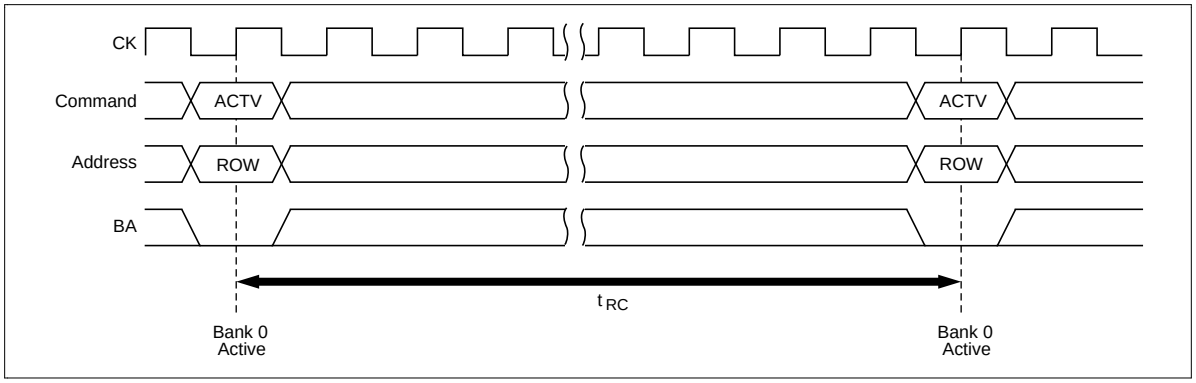

**Burst Length = 4** (To write all data)



**Bank active command interval:**

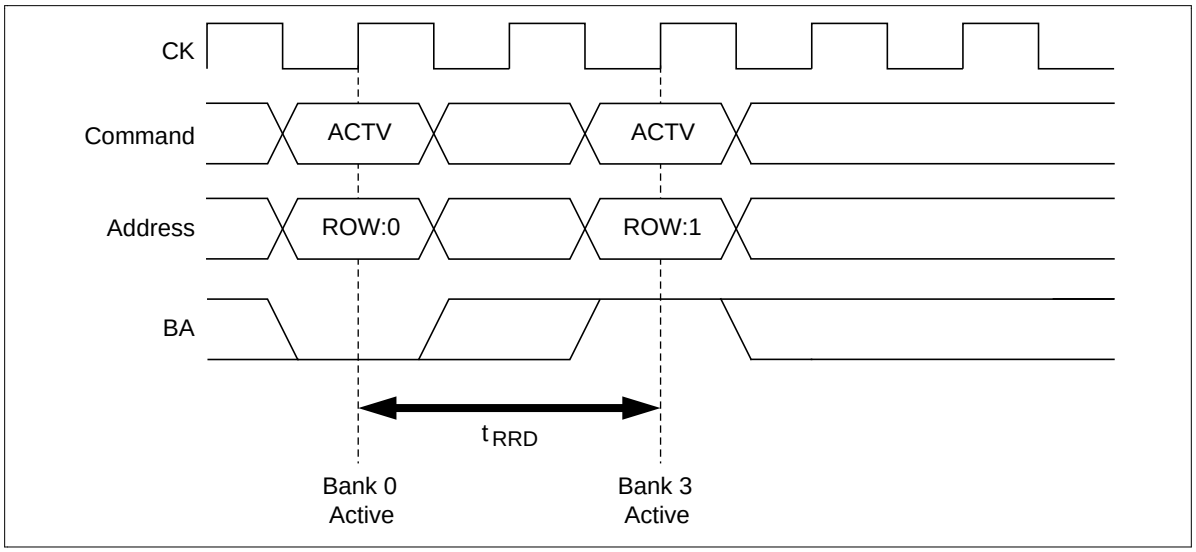
**1. Same bank:** The interval between the two bank-active commands must be no less than $t_{RC}$.

**Bank Active to Bank Active for Same Bank**

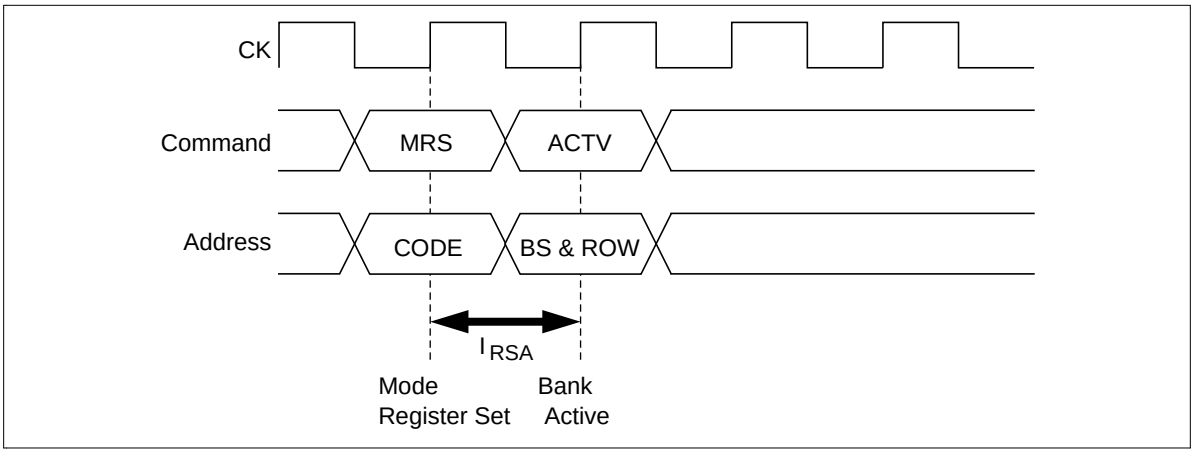



**2. In the case of different bank-active commands:** The interval between the two bank-active commands must be no less than $t_{RRD}$.

**Bank Active to Bank Active for Different Bank**



**Mode register set to Bank-active command interval:** The interval between setting the mode register and executing a bank-active command must be no less than $l_{RSA}$.



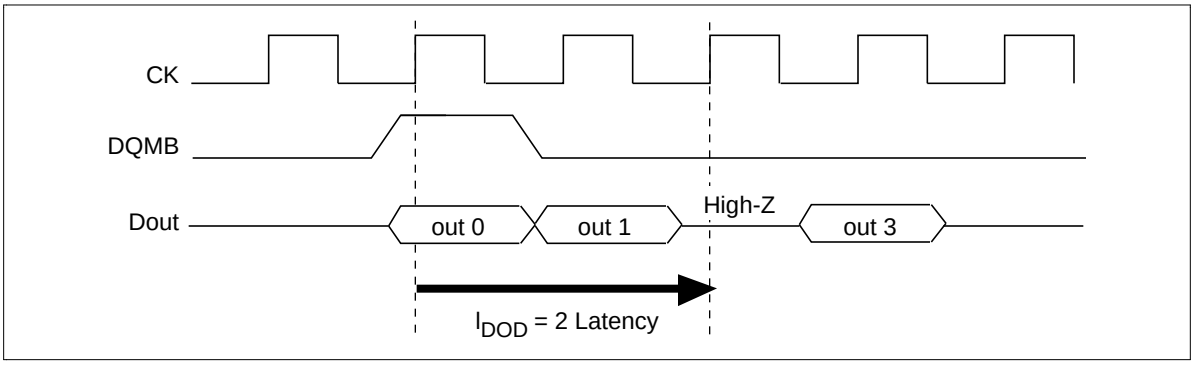

**DQMB Control**

The DQMB mask the DQ data. The timing of DQMB is different during reading and writing.

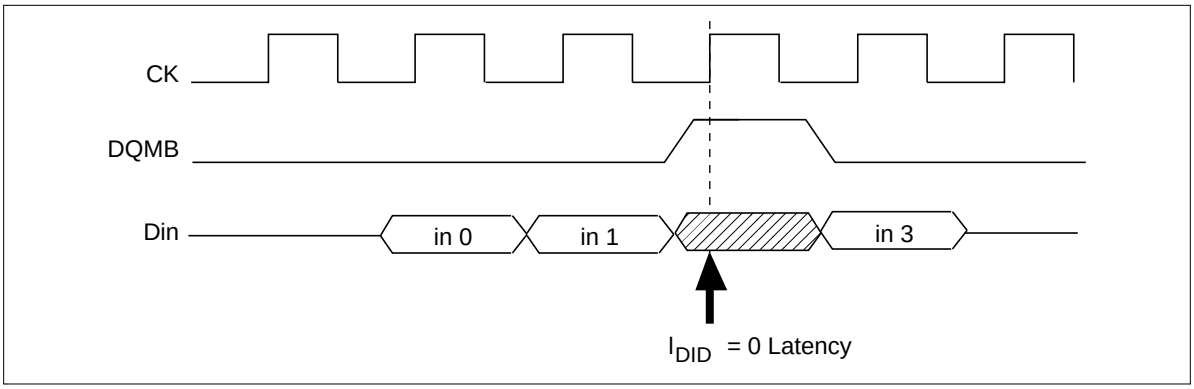
**Reading:** When data is read, the output buffer can be controlled by DQMB. By setting DQMB to Low, the output buffer becomes Low-Z, enabling data output. By setting DQMB to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQMB during reading is 2 clocks.

**Writing:** Input data can be masked by DQMB. By setting DQMB to Low, data can be written. In addition, when DQMB is set to High, the corresponding data is not written, and the previous data is held. The latency of DQMB during writing is 0 clock.

**Reading**




**Writing**



**Refresh**

**Auto-refresh:** All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 4096 cycles/64 ms. (4096 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

**Self-refresh:** After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. Before and after self-refresh mode, execute auto-refresh to all refresh addresses in or within 64 ms period on the condition (1) and (2) below.

(1) Enter self-refresh mode within 15.6 μs after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
(2) Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6 μs after exiting from self-refresh mode.

**Others**

**Power-down mode:** The SDRAM module enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the SDRAM module exits from the power down mode, and command input is enabled from the next clock. In this mode, internal refresh is not performed.

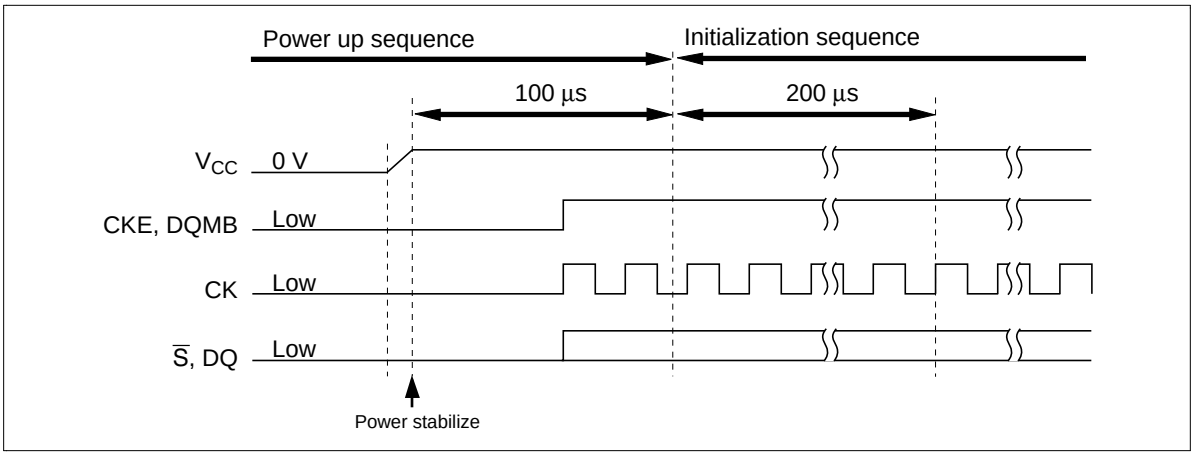
**Clock suspend mode:** By driving CKE to Low during a bank-active or read/write operation, the SDRAM module enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the SDRAM module terminates clock suspend mode, and command input is enabled from the next clock. For details, refer to the "CKE Truth Table".

**Power-up sequence:** The SDRAM module should be gone on the following sequence with power up.

The CK, CKE, $\overline{S}$, DQMB and DQ pins keep low till power stabilizes.
The CK pin is stabilized within 100 μs after power stabilizes before the following initialization sequence.
The CKE and DQMB is driven to high between power stabilizes and the initialization sequence.

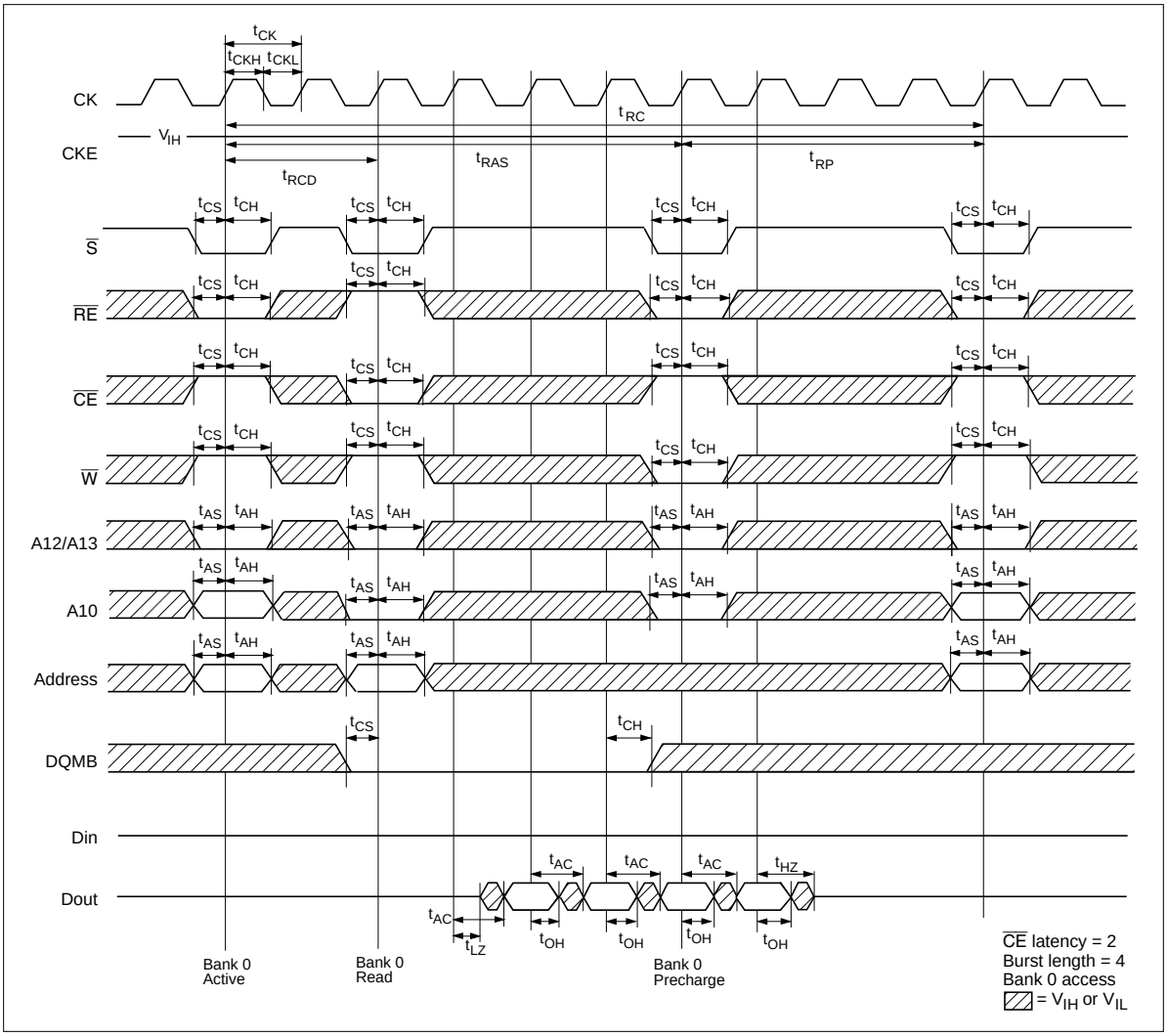
This SDRAM module has $V_{CC}$ clamp diodes for CK, CKE, $\overline{S}$, DQMB and DQ pins. If these pins go high before power up, the large current flows from these pins to $V_{CC}$ through the diodes.

**Initialization sequence:** When 200 μs or more has past after the above power-up sequence, all banks must be precharged using the precharge command (PALL). After $t_{RP}$ delay, set 8 or more auto refresh commands (REF). Set the mode register set command (MRS) to initialize the mode register. We recommend that by keeping DQMB to High, the output buffer becomes High-Z during Initialization sequence, to avoid DQ bus contention on memory system formed with a number of device.

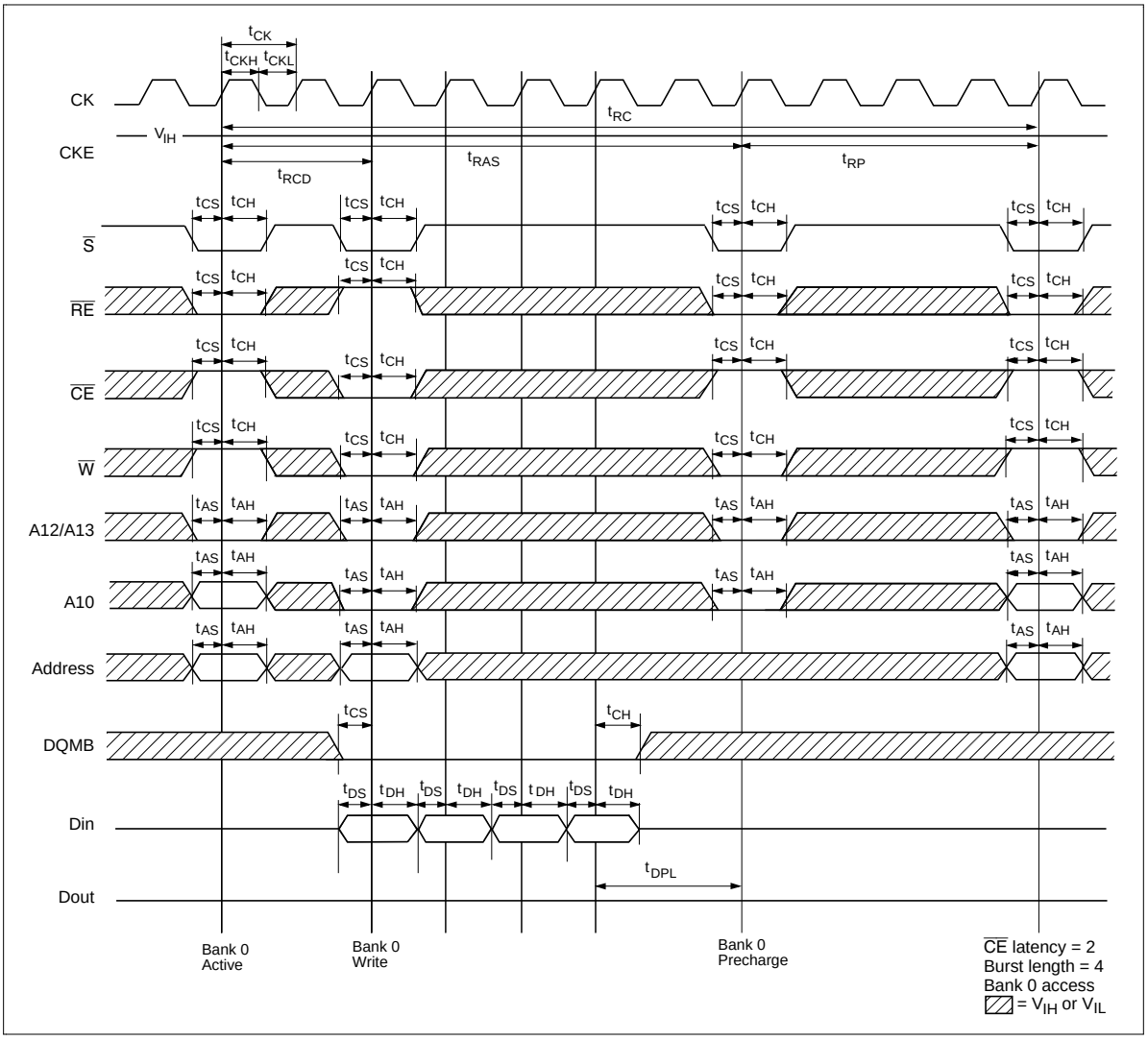

Power up sequence
Initialization sequence
100 µs
200 µs
$V_{CC}$
0 V
CKE, DQMB
Low
CK
Low
$\overline{S}$, DQ
Low
Power stabilize

## Timing Waveforms

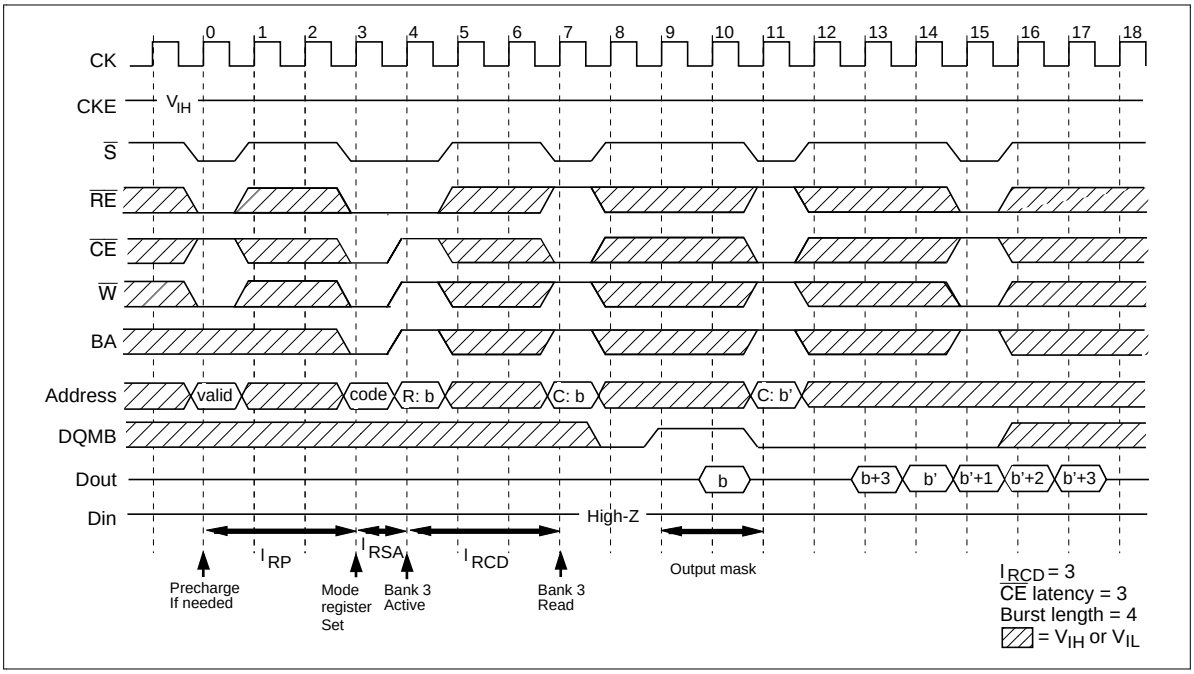
### Read Cycle



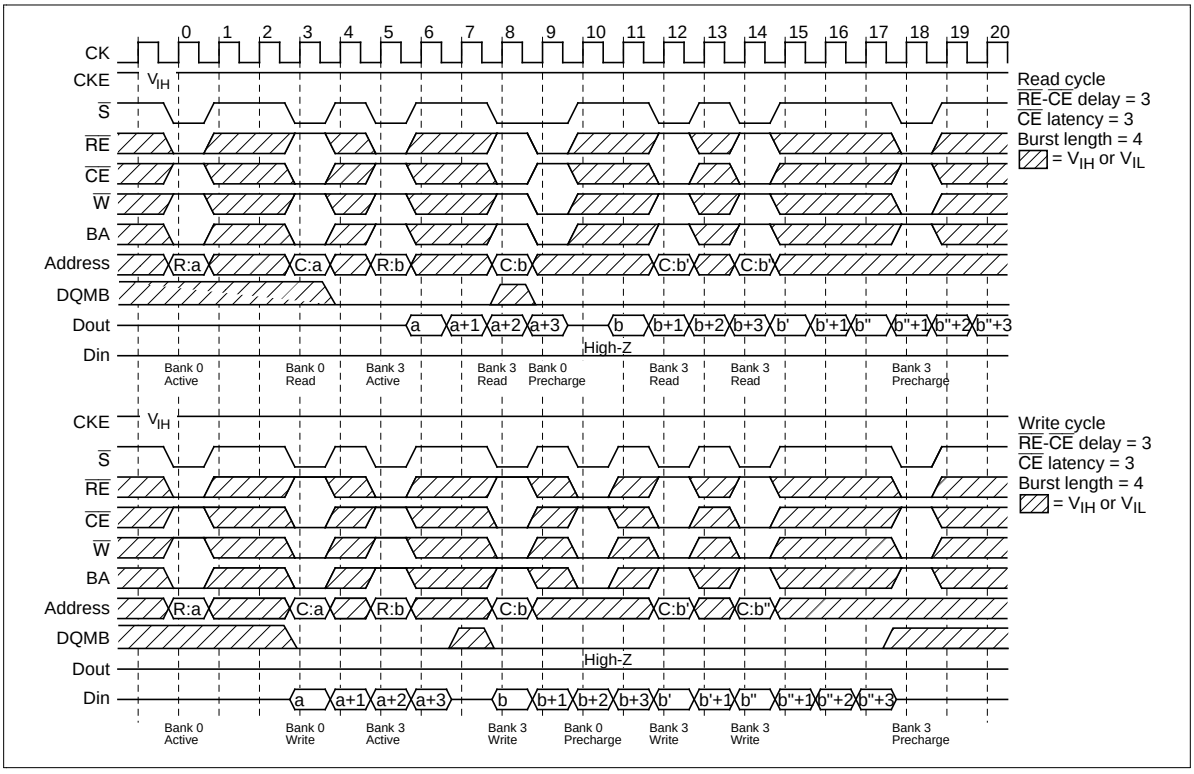
### Write Cycle


tCK
tCKH tCKL
CK
tRC
VIH
CKE
tRAS
tRP
tRCD
tCS tCH
S
RE
CE
W
tAS tAH
A12/A13
A10
Address
DQMB
tDS tDH
Din
tDPL
Dout
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
CE latency = 2
Burst length = 4
Bank 0 access
= VIH or VIL

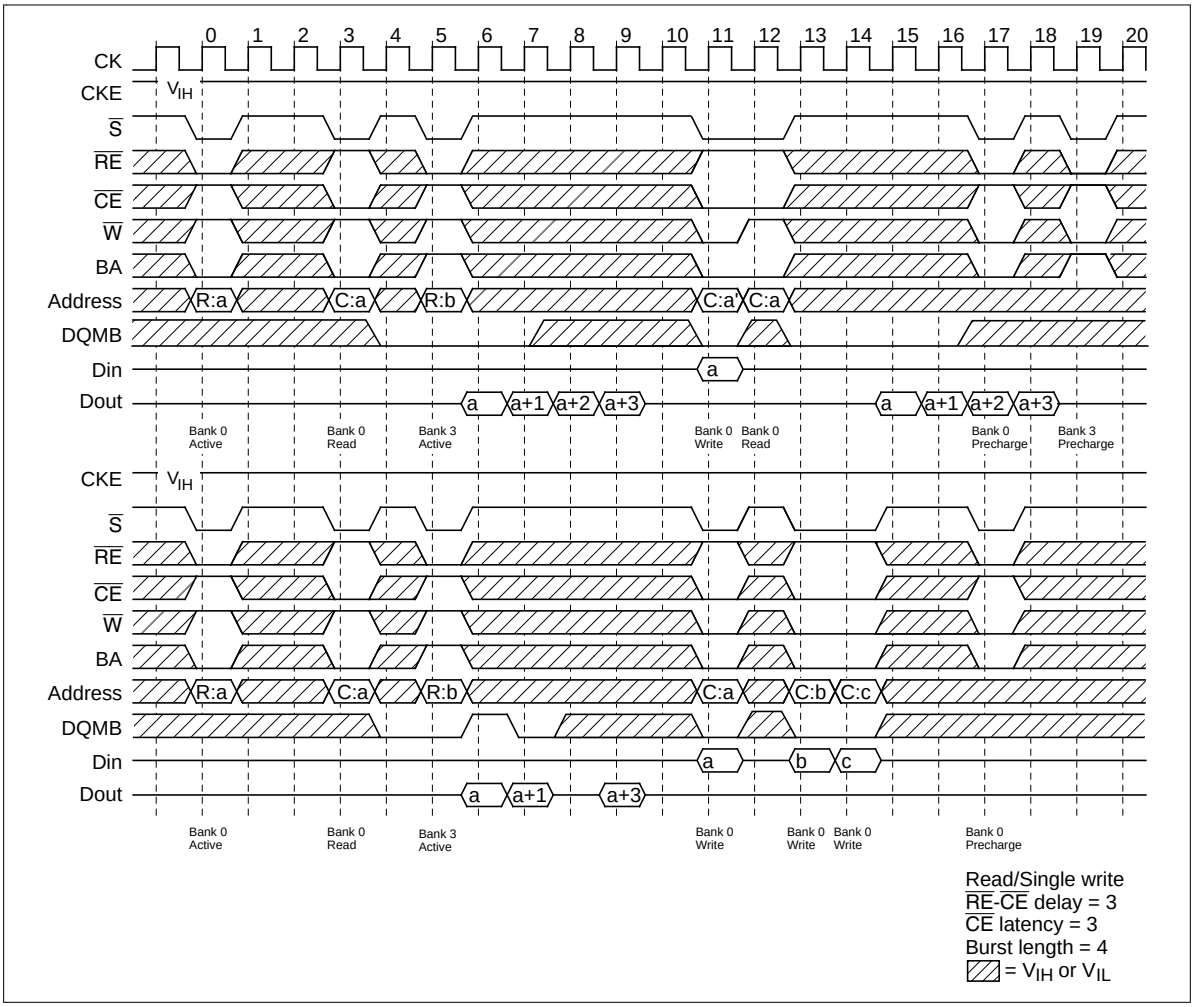
**Mode Register Set Cycle**



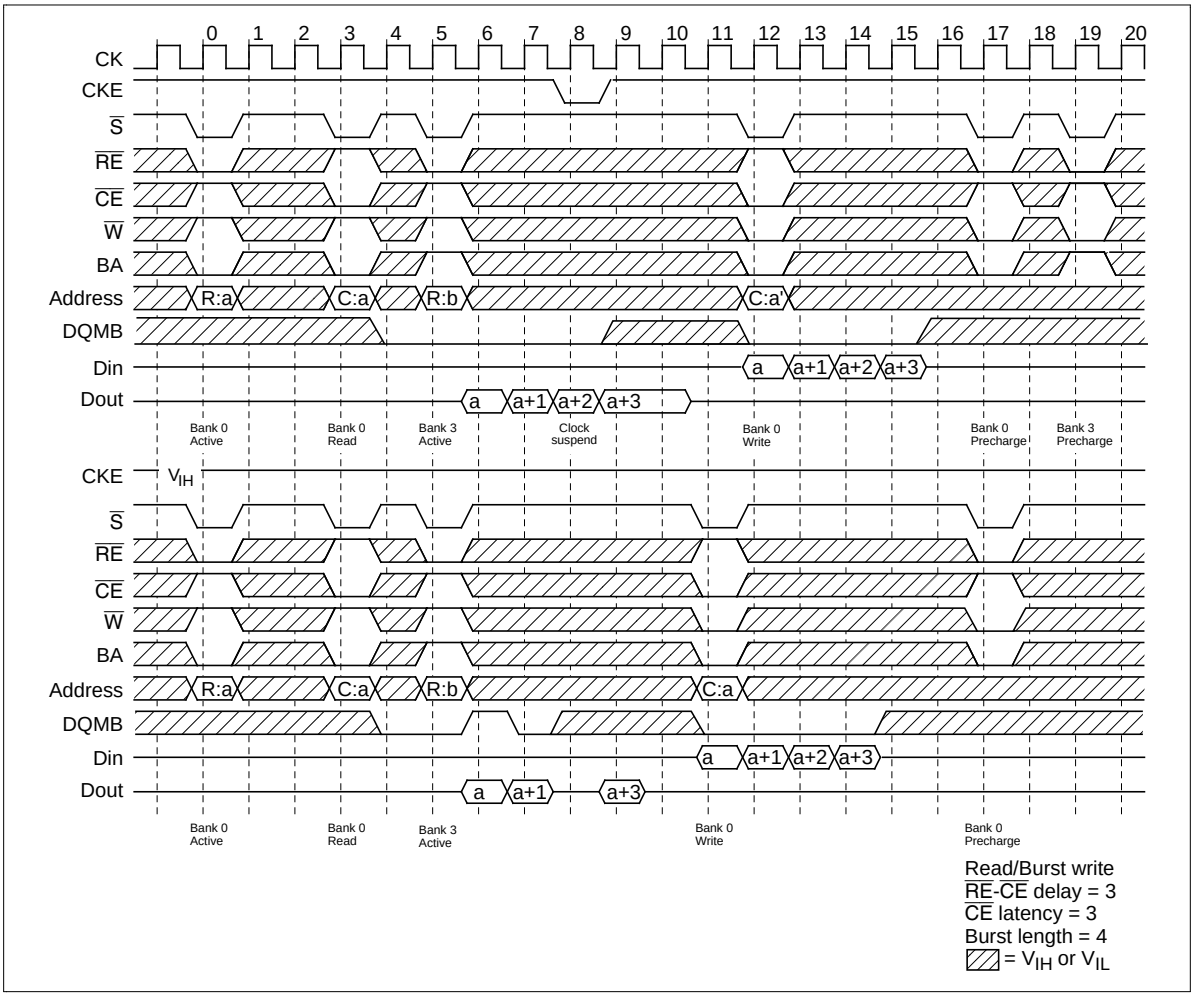
### Read Cycle/Write Cycle



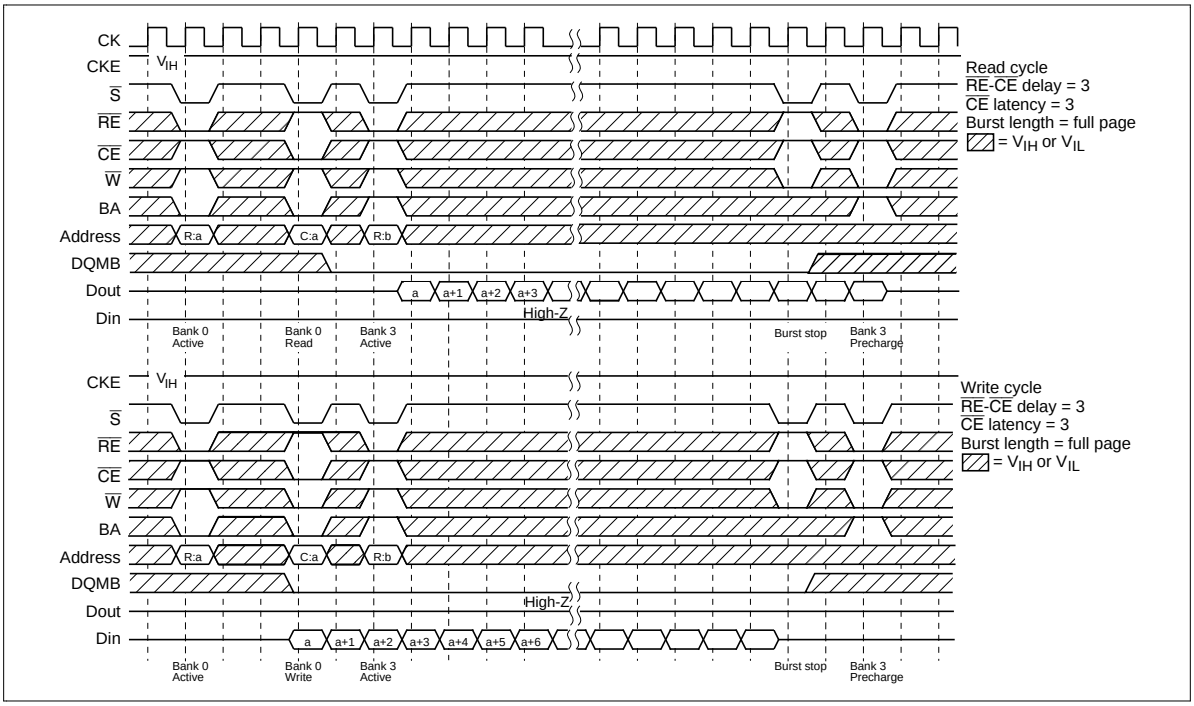
**Read/Single Write Cycle**



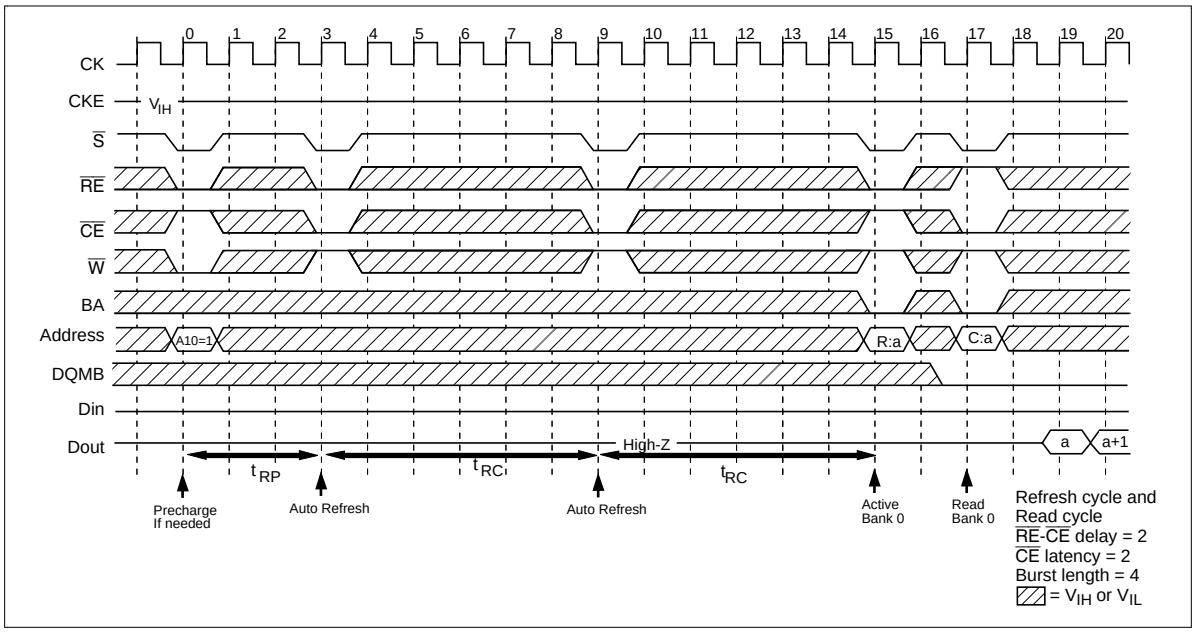
**Read/Burst Write Cycle**



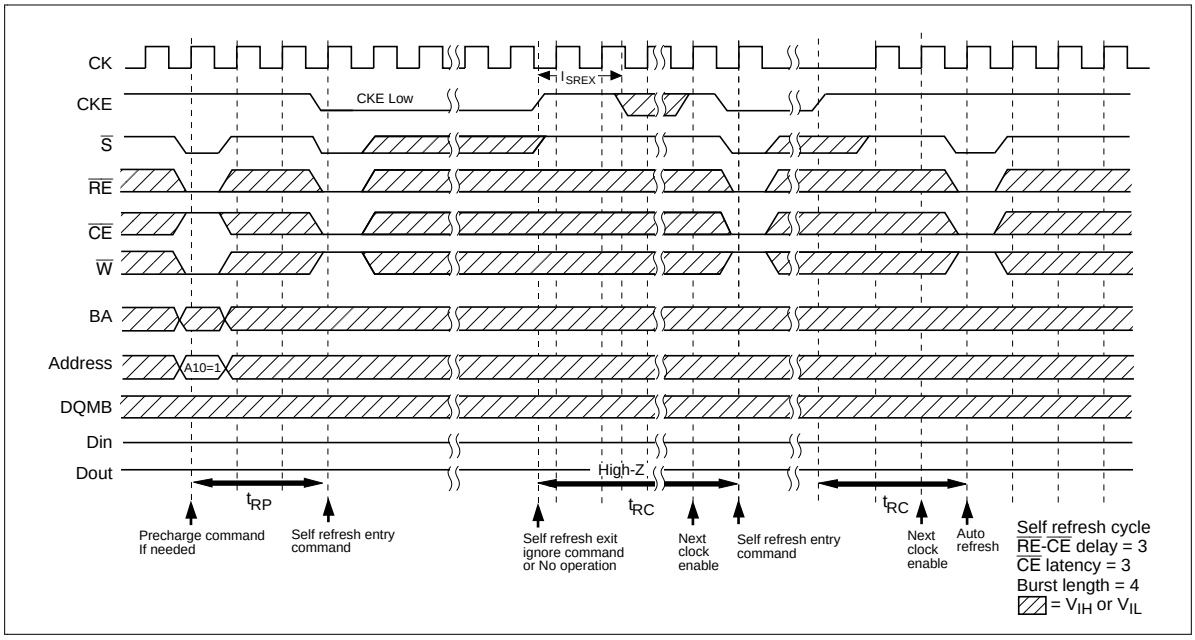
## Full Page Read/Write Cycle



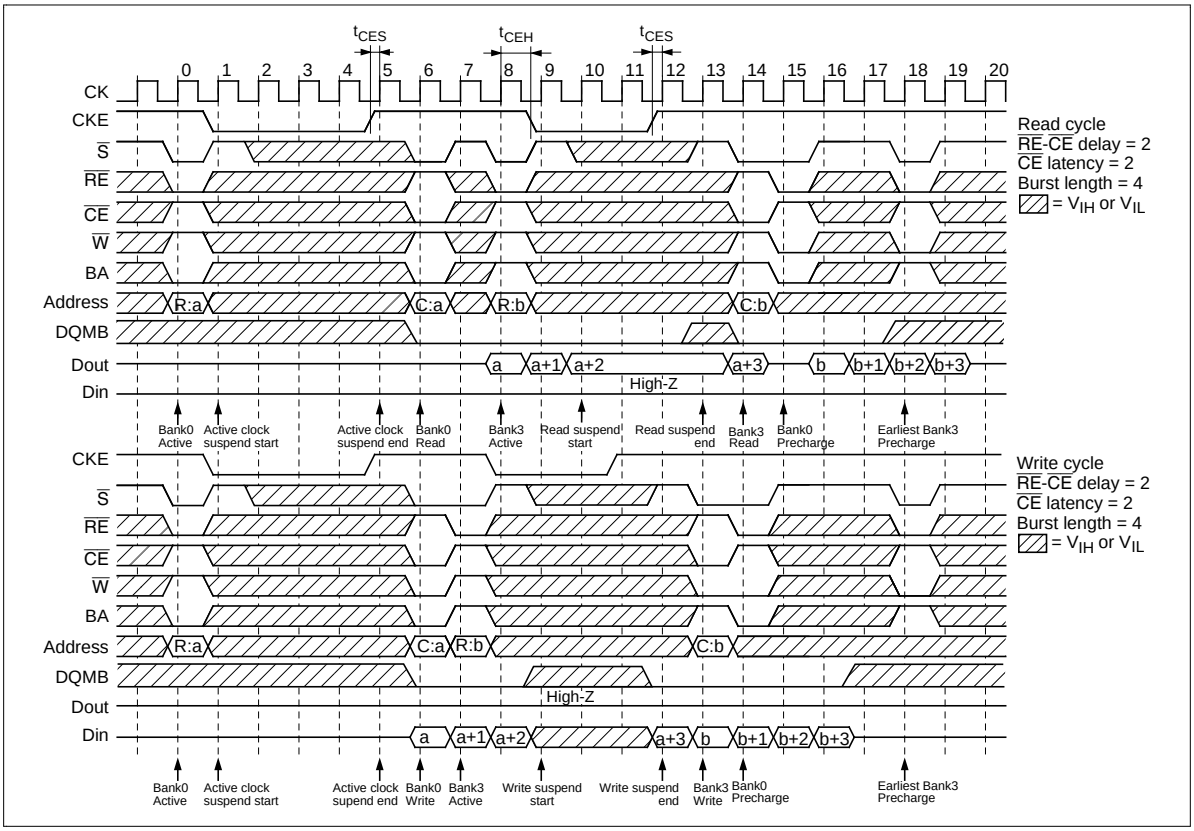
### Auto Refresh Cycle



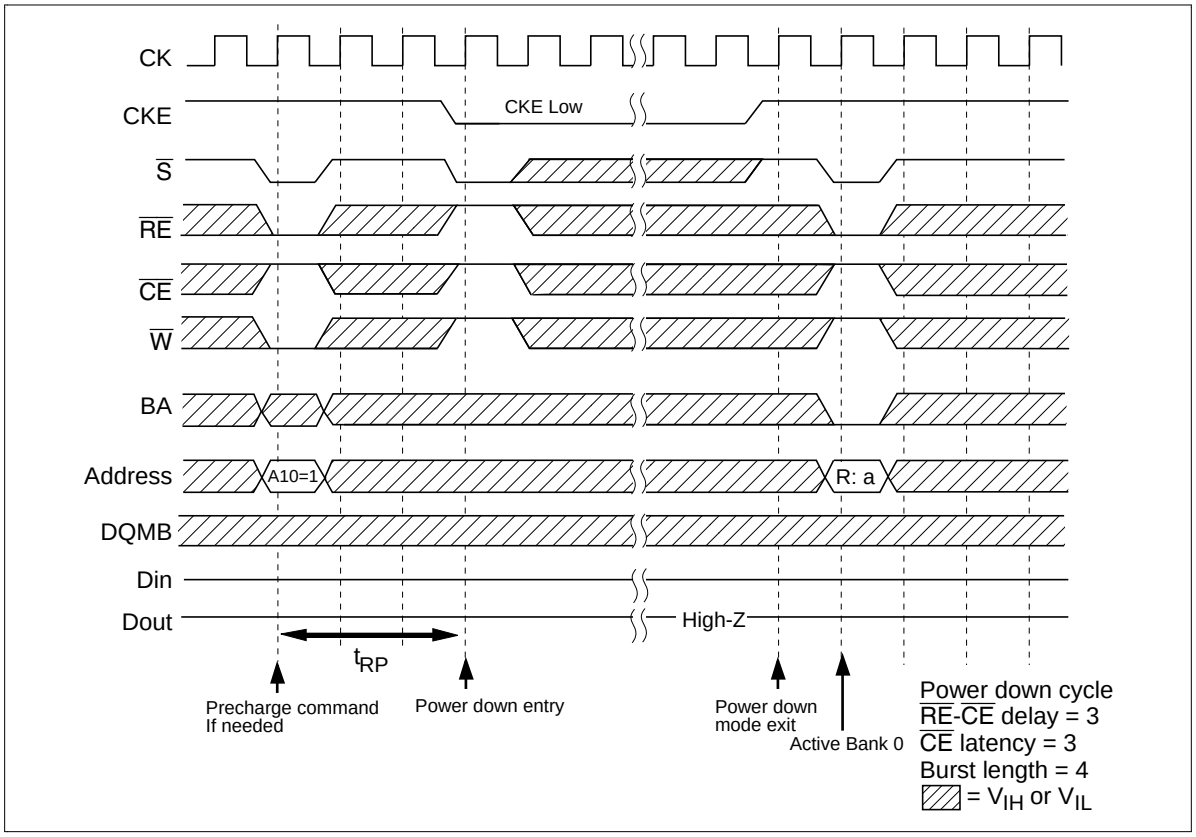

### Self Refresh Cycle



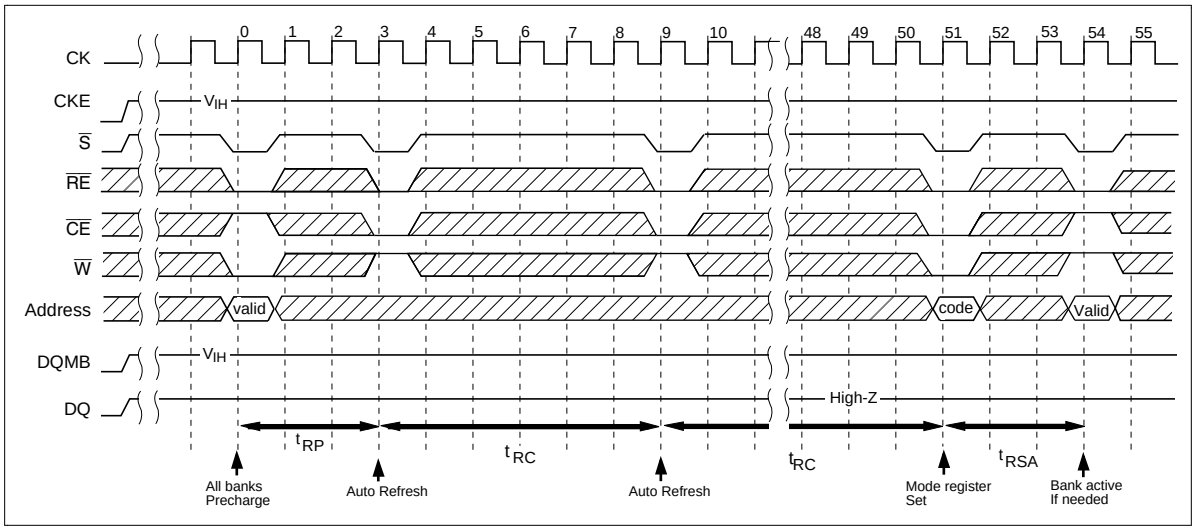
## Clock Suspend Mode



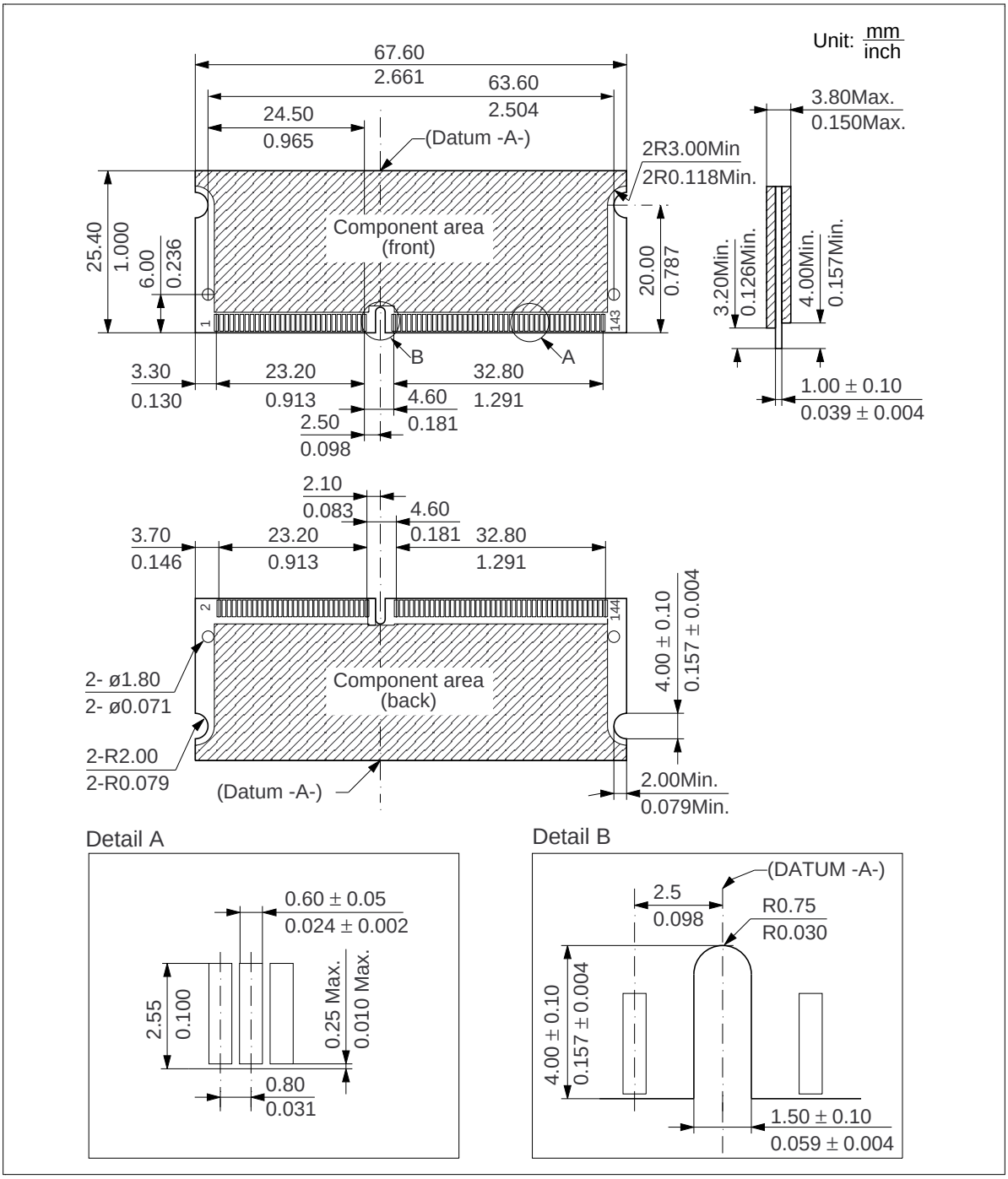
### Power Down Mode




### Initialization Sequence



## Physical Outline



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## Revision Record

| Rev. | Date | Contents of Modification | Drawn by | Approved by |
|---|---|---|---|---|
| 0.0 | Dec. 16, 1998 | Initial issue<br>(referred to HM5264165D/HM5264805D/HM5264405D-A60 and HM5264165D/HM5264805D/HM5264405D-B60 rev 1.0) | | |