HB54A89FM Series
HB54A169FN Series

HB54A89FM
64 MB Unbuffered DDR SDRAM DIMM
8-Mword × 72-bit, 1-Bank Module
(9 pcs of 8 M × 8 Components)
HB54A169FN
128 MB Unbuffered DDR SDRAM DIMM
16-Mword × 72-bit, 2-Bank Module
(18 pcs of 8 M × 8 Components)

HITACHI

ADE-203-948 (Z)
Preliminary, Rev. 0.0
Aug. 7, 1998

Description

The HB54A89FM, HB54A169FN belong to 8-byte DIMM (Dual In-line Memory Module) family, and have been developed as an optimized main memory solution for 8-byte processor applications. The HB54A89FM is a 8M × 72 × 1-bank Double Data Rate (DDR) SDRAM Module, mounted 9 pieces of 64-Mbit DDR SDRAM (HM5464801DTT) sealed in TSOP package, and 1 piece of serial EEPROM (2-kbit EEPROM) for Presence Detect (PD). The HB54A169FN is a 8M × 72 × 2-bank Double Data Rate (DDR) SDRAM Module, mounted 18 pieces of 64-Mbit DDR SDRAM (HM5464801DTT) sealed in TSOP package, and 1 piece of serial EEPROM (2-kbit EEPROM) for Presence Detect (PD). Read and write operations are performed at the cross points of the CK and the $\overline{CK}$. This high speed data transfer is realized by the 2-bit prefetch piplined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. An outline of the products is 184-pin socket type package (dual lead out). Therefore, they make high density mounting possible without surface mount technology. They provide common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

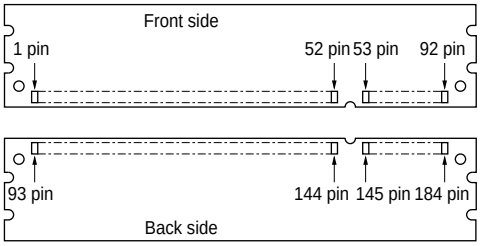
Features

- 184-pin socket type package (dual lead out)
  - Lead pitch: 1.27 mm
- Power supply
  - V_{DD} pin: 2.5 V ± 0.2 V
  - V_{DDQ} pin: 2.5 V ± 0.2 V
  - V_{33} pin: 3.3 V ± 0.3 V
- SSTL-2 interface for all inputs and outputs
- Clock frequency: 125 MHz/100 MHz
- DLL "ON" and "OFF" mode
- Data inputs, outputs, and DM are synchronized with DQS
- 4 banks can operate simultaneously and independently
- Burst read/write operation
- Programmable burst length: 2/4/8
  - Burst read stop capability
- Programmable burst sequence
  - Sequential/interleave
- Start addressing capability
  - Even and Odd
- Programmable $\overline{CAS}$ latency: 2/2.5
- 4096 refresh cycles: 64ms
- 2variations of refresh
  - Auto refresh
  - Self refresh

Ordering Information

Type No.	Frequency	Package	Contact pad
HB54A89FM-8D	125 MHz	184-pin dual lead out socket type	Gold
HB54A89FM-10D	100 MHz		
HB54A169FN-8D	125 MHz		
HB54A169FN-10D	100 MHz		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{REF}	47	DQS8	93	V_{SS}	139	V_{SS}
2	DQ0	48	A0	94	DQ4	140	DM8
3	V_{SS}	49	CB2	95	DQ5	141	A10
4	DQ1	50	V_{SS}	96	V_{CCQ}	142	CB6
5	DQS0	51	CB3	97	DM0	143	V_{CCQ}
6	DQ2	52	BA1	98	DQ6	144	CB7
7	V_{CC}	53	DQ32	99	DQ7	145	V_{SS}
8	DQ3	54	V_{CCQ}	100	V_{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	V_{CC}
11	V_{SS}	57	DQ34	103	NC	149	DM4
12	DQ8	58	V_{SS}	104	V_{CCQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V_{SS}
15	V_{CCQ}	61	DQ40	107	DM1	153	DQ44
16	CK0	62	V_{CCQ}	108	V_{CC}	154	$\overline{RAS}$
17	$\overline{CK0}$	63	$\overline{WE}$	109	DQ14	155	DQ45
18	V_{SS}	64	DQ41	110	DQ15	156	V_{CCQ}
19	DQ10	65	$\overline{CAS}$	111	NC (CKE1)*[1]	157	$\overline{S0}$
20	DQ11	66	V_{SS}	112	V_{CCQ}	158	NC ($\overline{S1}$)*[2]
21	CKE0	67	DQS5	113	NC	159	DM5
22	V_{CCQ}	68	DQ42	114	DQ20	160	V_{SS}
23	DQ16	69	DQ43	115	NC	161	DQ46
24	DQ17	70	V_{CC}	116	V_{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
26	V_{SS}	72	DQ48	118	A11	164	V_{CCQ}
27	A9	73	DQ49	119	DM2	165	DQ52
28	DQ18	74	V_{SS}	120	V_{CC}	166	DQ53
29	A7	75	$\overline{CK2}$	121	DQ22	167	NC
30	V_{CCQ}	76	CK2	122	A8	168	V_{CC}
31	DQ19	77	V_{CCQ}	123	DQ23	169	DM6
32	A5	78	DQS6	124	V_{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V_{SS}	80	DQ51	126	DQ28	172	V_{CCQ}
35	DQ25	81	V_{SS}	127	DQ29	173	NC
36	DQS3	82	V_{CCID}	128	V_{CCQ}	174	DQ60
37	A4	83	DQ56	129	DM3	175	DQ61
38	V_{CC}	84	DQ57	130	A3	176	V_{SS}
39	DQ26	85	V_{CC}	131	DQ30	177	DM7
40	DQ27	86	DQS7	132	V_{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V_{SS}	88	DQ59	134	CB4	180	V_{CCQ}
43	A1	89	V_{SS}	135	CB5	181	SA0
44	CB0	90	WP	136	V_{CCQ}	182	SA1
45	CB1	91	SDA	137	CK1	183	SA3
46	V_{CC}	92	SCL	138	$\overline{CK1}$	184	V_{33}

Notes: 1. NC: HB54A89FM, CKE1: HB54A169FN
2. NC: HB54A89FM, $\overline{S1}$: HB54A169FN

Pin Description (HB54A89FM)

Pin name	Function
A0 to A11	Address input — Row address A0 to A11 — Column address A0 to A8
A13/A12	Bank select address BA0/BA1
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable
$\overline{S0}$	Chip select
CKE0	Clock enable
CK0 to CK2	Clock input
$\overline{CK0}$ to $\overline{CK2}$	Differential clock input
DQS0 to DQS8	Input and output data strobe
DM0 to DM8	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
WP	Write protect for serial PD
SA0 to SA2	Serial address input
V_{CC}	Power for internal circuit
V_{CCQ}	Power for DQ circuit
V_{33}	Power for serial EEPROM
V_{REF}	Input reference voltage
V_{SS}	Ground
V_{CCID}	V_{CC} indentication flag
NC	No connection

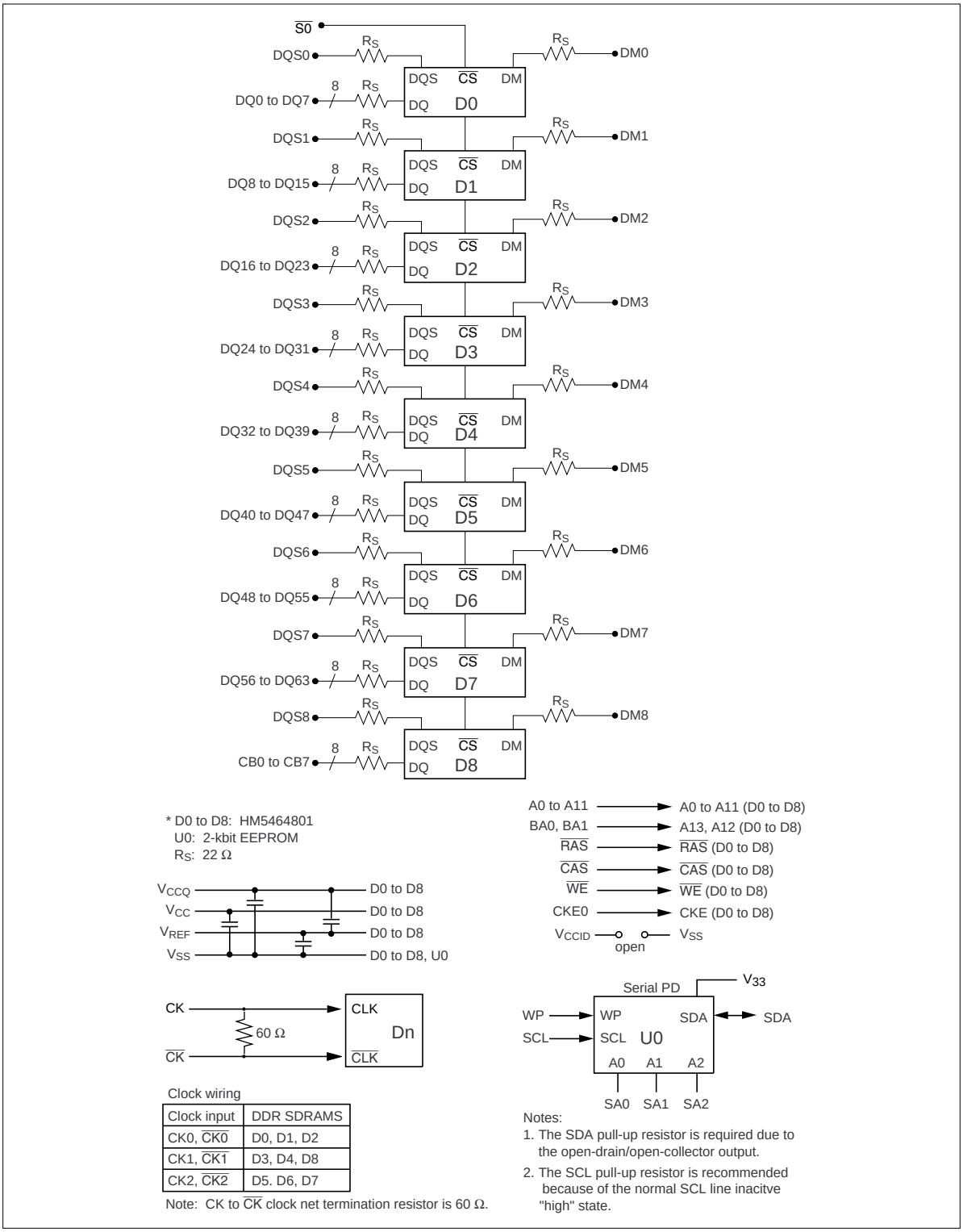
Pin Description (HB54A169FN)

Pin name	Function
A0 to A11	Address input — Row address A0 to A11 — Column address A0 to A8
A13/A12	Bank select address BA0/BA1
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable
$\overline{S0}$, $\overline{S1}$	Chip select
CKE0, CKE1	Clock enable
CK0 to CK2	Clock input
$\overline{CK0}$ to $\overline{CK2}$	Differential clock input
DQS0 to DQS8	Input and output data strobe
DM0 to DM8	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
WP	Write protect for serial PD
SA0 to SA2	Serial address input
V_{CC}	Power for internal circuit
V_{CCQ}	Power for DQ circuit
V_{33}	Power for serial EEPROM
V_{REF}	Input reference voltage
V_{SS}	Ground
V_{CCID}	V_{CC} identification flag
NC	No connection

Serial PD Matrix

TBD

Block Diagram (HB54A89FM)



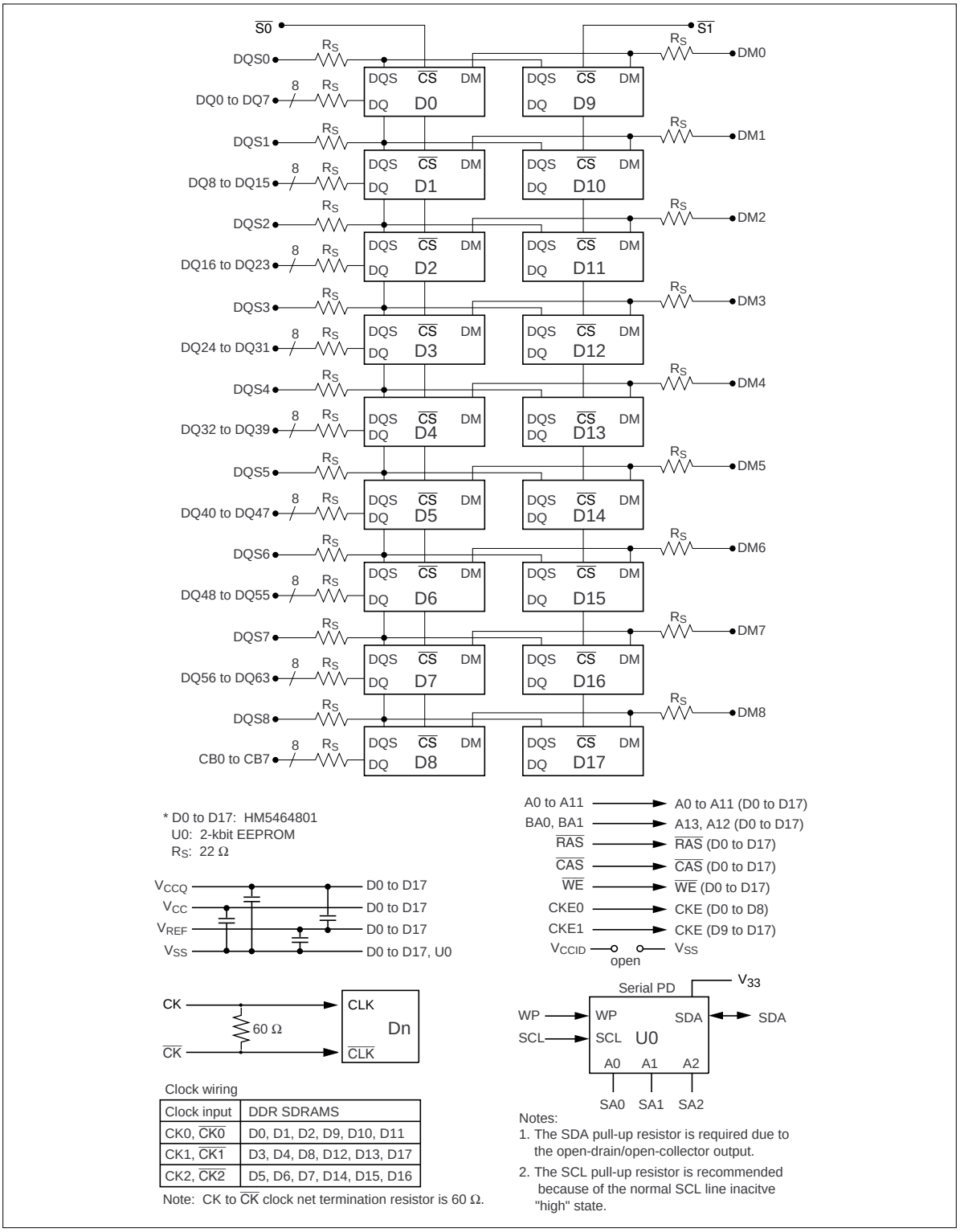
Clock wiring

Clock input	DDR SDRAMS
CK0, $\overline{CK0}$	D0, D1, D2
CK1, $\overline{CK1}$	D3, D4, D8
CK2, $\overline{CK2}$	D5. D6, D7

Note: CK to $\overline{CK}$ clock net termination resistor is 60 Ω.

Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

Block Diagram (HB54A169FN)



Clock wiring

Clock input	DDR SDRAMS
CK0, $\overline{CK0}$	D0, D1, D2, D9, D10, D11
CK1, $\overline{CK1}$	D3, D4, D8, D12, D13, D17
CK2, $\overline{CK2}$	D5, D6, D7, D14, D15, D16

Note: CK to $\overline{CK}$ clock net termination resistor is 60 Ω.

Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

Pin Functions (1)

CK (CLK), $\overline{CK}$ ($\overline{CLK}$) (input pin): The CK and the $\overline{CK}$ are the master clock inputs to the device. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the V_{REF} level. When a read operation, DQSs and DQs are referred to the cross point of the CK and the $\overline{CK}$. When a write operation, DMs and DQs are referred to the cross point of the DQS and the V_{REF} level. DQSs for write operation are referred to the cross point of the CK and the $\overline{CK}$.

$\overline{S}$ ($\overline{CS}$) (input pin): When $\overline{S}$ is Low, commands and data can be input. When $\overline{S}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins): These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A11 (input pins): Row address (AX0 to AX11) is determined by the A0 to the A11 level at the cross point of the CK rising edge and the V_{REF} level in a bank active command cycle. Column address is loaded via the A0 to the A8 at the cross point of the CK rising edge and the V_{REF} level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP): A10 defines the precharge mode when a precharge operation, a read operation or a write operation. When A10 = High in a precharge command cycle, both banks are precharged. When A10 = Low in a precharge command cycle, only the bank that is selected by A12 (BA1)/A13 (BA0) is precharged. When A10 = High in a read or a write operation, auto-precharge function is enabled. While A10 = Low, auto-precharge function is disabled.

A12 (BA1)/A13 (BA0) (input pin): A12 (BA1)/A13 (BA0) are bank select signals. The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If A12 = Low and A13 = Low, bank 0 is selected. If A12= High and A13 = Low, bank 1 is selected. If A12 = Low and A13 = High, bank 2 is selected. If A12 = High and A13 = High, bank 3 is selected.

CKE (input pin): CKE of the DDR SDRAM module has the similar function with CKE of regular SDRAMs. CKE controls power down and self-refresh while all banks are in idle. The power down and the self-refresh commands are entered when the CKE is driven Low and exited when it resumes to High.

The CKE level must be kept for 1 CK cycle (= L_{CKEPW}) at least, that is, if CKE changes at the cross point of the CK rising edge and the V_{REF} level with proper setup time t_{IS}, at the next CK rising edge CKE must be kept with proper hold time t_{IH}.

Pin Functions (2)

DM (input pins): DM is the reference signals of the data input mask function. DMs are sampled at the cross point of DQS and V_{REF}.

DQ, CB (input and output pins): Data are input to and output from these pins.

DQS (input and output pin): DQS provide the read data strobes (as output) and the write data strobes (as input).

V_{CC} and V_{CCQ} (power supply pins): 2.5 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)

V_{33} (power supply pin): 3.3 V is applied (For serial EEPROM).

V_{SS} (power supply pin): Ground is connected.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{ss}	V_T	–1.0 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}, V_{CCQ}	–1.0 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	9	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. Respect to V_{SS}

DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}, V_{CCQ}	2.3	2.5	2.7	V	1, 2
	V_{SS}	0	0	0	V	
Input reference voltage	V_{REF}	1.15	1.25	1.35	V	1
Termination voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.05	V	1
DC input high voltage	V_{IH}	V_{REF} + 0.18	—	V_{CCQ} + 0.3	V	1, 3
DC input low voltage	V_{IL}	–0.3	—	V_{REF} – 0.18	V	1, 4

Notes: 1. All parameters are referred V_{SS}, when measured.
2. V_{CCQ} must be lower than or equal to V_{CC}.
3. V_{IH} is allowed to exceed V_{CC} up to 4.6 V for the period shorter than or equal to 5 ns.
4. V_{IL} is allowed to outreach below V_{SS} down to –1.0 V for the period shorter than or equal to 5 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V, V_{SS} = 0 V) (HB54A89FM)

		HB54A89FM						
		-8D		-10D				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	TBD	—	TBD	mA	Burst length = 2 t_{RC} = min	1, 2, 4
Standby current (IDLE)	I_{CC2}	—	TBD	—	TBD	mA	CKE = V_{IL}, t_{CK} = min	
		—	TBD	—	TBD	mA	CK = V_{IL} or V_{IH} Fixed	
		—	TBD	—	TBD	mA	CKE = V_{IH}, t_{CK} = min NOP command	3
Active standby current (One Bank active)	I_{CC3}	—	TBD	—	TBD	mA	CKE = V_{IL}, t_{CK} = min DQ = High-Z	1, 2
Burst operating current ($\overline{CAS}$ latency = 2)	I_{CC4}	—	TBD	—	TBD	mA	t_{CK} = min, BL = 8	1, 2, 5
($\overline{CAS}$ latency = 2.5)	I_{CC4}	—	TBD	—	TBD	mA		
Auto refresh current	I_{CC5}	—	TBD	—	TBD	mA	t_{RC} = min, Address = V_{IL} or V_{IH} Fixed	
Self refresh current	I_{CC6}	—	18	—	18	mA	$V_{IH} \geq V_{CC} - 0.2$ $V_{IL} \leq 0.2$ V	
Input leakage current	I_{LI}	–10	10	–10	10	µA	$0 \leq Vin \leq V_{CC}$	
Output leakage current	I_{LO}	–10	10	–10	10	µA	$0 \leq Vout \leq V_{CC}$ DQ = High-Z	
Output high voltage	V_{OH}	V_{TT} + 0.38	—	V_{TT} + 0.38	—	V	I_{OH} = –15.2 mA	
Output low voltage	V_{OL}	—	V_{TT} – 0.38	—	V_{TT} – 0.38	V	I_{OL} = 15.2 mA	

Notes: 1. This I_{CC} data is measured under condition that DQ pins are not connected.
2. One bank operation.
3. Input signal transition is once per two clock cycles.
4. Input signal transition is once per one clock cycle.
5. Input signal transition is once per eight clock cycles.

DC Characteristics (Ta = 0 to +70°C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V, V_{SS} = 0 V) (HB54A169FN)

		HB54A169FN						
		-8D		-10D				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	TBD	—	TBD	mA	Burst length = 2 t_{RC} = min	1, 2, 4
Standby current (IDLE)	I_{CC2}	—	TBD	—	TBD	mA	CKE = V_{IL}, t_{CK} = min	
		—	TBD	—	TBD	mA	CK = V_{IL} or V_{IH} Fixed	
		—	TBD	—	TBD	mA	CKE = V_{IH}, t_{CK} = min NOP command	3
Active standby current (One Bank active)	I_{CC3}	—	TBD	—	TBD	mA	CKE = V_{IL}, t_{CK} = min DQ = High-Z	1, 2
Burst operating current ($\overline{CAS}$ latency = 2)	I_{CC4}	—	TBD	—	TBD	mA	t_{CK} = min, BL = 8	1, 2, 5
($\overline{CAS}$ latency = 2.5)	I_{CC4}	—	TBD	—	TBD	mA		
Auto refresh current	I_{CC5}	—	TBD	—	TBD	mA	t_{RC} = min, Address = V_{IL} or V_{IH} Fixed	
Self refresh current	I_{CC6}	—	36	—	36	mA	$V_{IH} \geq V_{CC} - 0.2$ $V_{IL} \leq 0.2$ V	
Input leakage current	I_{LI}	–10	10	–10	10	µA	$0 \leq Vin \leq V_{CC}$	
Output leakage current	I_{LO}	–10	10	–10	10	µA	$0 \leq Vout \leq V_{CC}$ DQ = High-Z	
Output high voltage	V_{OH}	V_{TT} + 0.38	—	V_{TT} + 0.38	—	V	I_{OH} = –15.2 mA	
Output low voltage	V_{OL}	—	V_{TT} – 0.38	—	V_{TT} – 0.38	V	I_{OL} = 15.2 mA	

Notes: 1. This I_{CC} data is measured under condition that DQ pins are not connected.
2. One bank operation.
3. Input signal transition is once per two clock cycles.
4. Input signal transition is once per one clock cycle.
5. Input signal transition is once per eight clock cycles.

Capacitance (Ta = 25°C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V)

Parameter	Symbol	Max	Unit	Notes
Input capacitance (Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I1}	TBD	pF	1
Input capacitance ($\overline{S}$, CKE)	C_{I2}	TBD	pF	1
Input capacitance (CK, $\overline{CK}$)	C_{I3}	TBD	pF	1
Input capacitance (DM)	C_{I4}	TBD	pF	1
Input/output capacitance (DQ, CB, DQS)	C_O	TBD	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. Dout circuits are disabled.

AC Characteristics (Ta = 0 to +70°C, V_{CC}, V_{CCQ} = 2.5 V ± 0.2 V, V_{SS} = 0 V)

		HB54A89FM/HB54A169FN					
		-8D		-10D			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Clock cycle time (CAS latency = 2)	t_{CK}	8	15	10	15	ns	1, 8
(CAS latency = 2.5)	t_{CK}	7	15	8	15	ns	
Input clock high level time (CAS latency = 2)	t_{CH}	3.6	—	4.5	—	ns	1, 5
(CAS latency = 2.5)	t_{CH}	3.2	—	3.6	—	ns	
Input clock low level time (CAS latency = 2)	t_{CL}	3.6	—	4.5	—	ns	1, 5
(CAS latency = 2.5)	t_{CL}	3.2	—	3.6	—	ns	
CK to DQS skew (CAS latency = 2)	t_{DQSCK}	–0.4	1.2	–0.6	1.4	ns	3, 4, 5
(CAS latency = 2.5)	t_{DQSCK} DLL = ON	–0.3	1.1	–0.4	1.2	ns	
	t_{DQSCK} DLL = OFF	2.4	6.9	2.4	7.4	ns	
DATA to CK skew (CAS latency = 2)	t_{AC}	–0.4	1.2	–0.6	1.4	ns	3, 4, 5
(CAS latency = 2.5)	t_{AC} DLL = ON	–0.3	1.1	–0.4	1.2	ns	
	t_{AC} DLL = OFF	2.4	6.9	2.4	7.4	ns	
DOUT to DQS skew (CAS latency = 2)	t_{DQSQ}	-0.6	0.6	-0.8	0.8	ns	3, 4, 6
(CAS latency = 2.5)	t_{DQSQ}	-0.5	0.5	-0.6	0.6	ns	
DOUT valid window (CAS latency = 2)	t_{DV}	2.4	—	3	—	ns	4
(CAS latency = 2.5)	t_{DV}	2.1	—	2.4	—	ns	
DQS valid window (CAS latency = 2)	t_{DQSV}	2.4	—	3	—	ns	4
(CAS latency = 2.5)	t_{DQSV}	2.1	—	2.4	—	ns	
DQS read preamble (CAS latency = 2)	t_{RPRE}	7.2	8.8	9	11	ns	3, 4, 5, 6
(CAS latency = 2.5)	t_{RPRE}	6.3	7.7	7.2	8.8	ns	

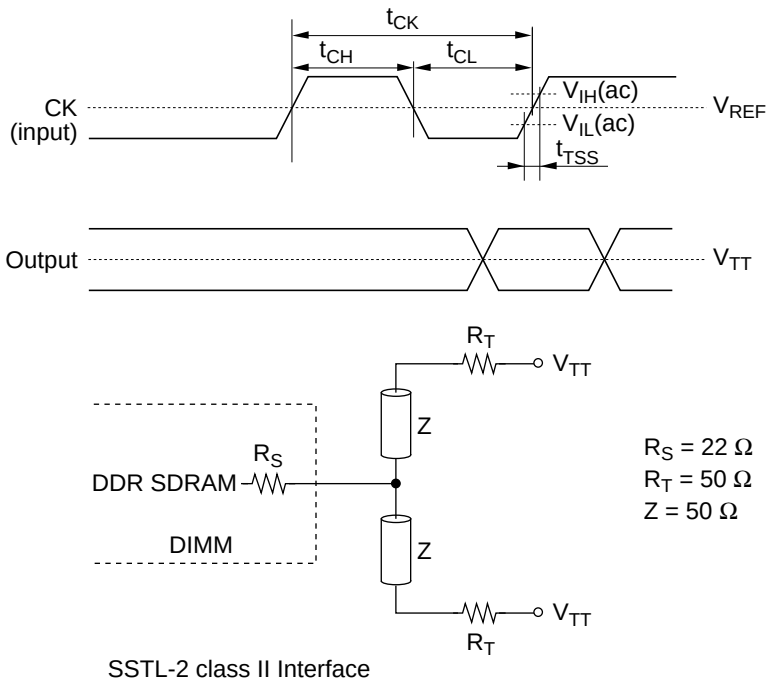
		HB54A89FM/HB54A169FN					
		-8D		-10D			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
DQS read postamble							3, 4, 5, 6
($\overline{CAS}$ latency = 2)	t_{RPST}	3.2	4.8	4	6	ns	
($\overline{CAS}$ latency = 2.5)	t_{RPST}	2.8	4.2	3.2	4.8	ns	
Data to data strobe setup time							1, 6
($\overline{CAS}$ latency = 2)	t_{QDQSS}	0.6	—	0.7	—	ns	
($\overline{CAS}$ latency = 2.5)	t_{QDQSS}	0.5	—	0.6	—	ns	
Data to data strobe hold time							1, 6
($\overline{CAS}$ latency = 2)	t_{QDQSH}	0.6	—	0.7	—	ns	
($\overline{CAS}$ latency = 2.5)	t_{QDQSH}	0.5	—	0.6	—	ns	
Data mask to data strobe setup time							1, 6
($\overline{CAS}$ latency = 2)	t_{DMDQSS}	0.6	—	0.7	—	ns	
($\overline{CAS}$ latency = 2.5)	t_{DMDQSS}	0.5	—	0.6	—	ns	
Data mask to data strobe hold time							1, 6
($\overline{CAS}$ latency = 2)	t_{DMDQSH}	0.6	—	0.7	—	ns	
($\overline{CAS}$ latency = 2.5)	t_{DMDQSH}	0.5	—	0.6	—	ns	
Clock to DQS write preamble setup time	t_{WPRES}	0	—	0	—	ns	1, 5
Clock to DQS write preamble hold time							1, 5
($\overline{CAS}$ latency = 2)	t_{WPREH}	2	—	2.5	—	ns	
($\overline{CAS}$ latency = 2.5)	t_{WPREH}	1.7	—	2	—	ns	
DQS last edge to High-Z time (DQS write postamble)							3, 6, 7
($\overline{CAS}$ latency = 2)	t_{WPST}	3.2	4.8	4	6	ns	
($\overline{CAS}$ latency = 2.5)	t_{WPST}	2.8	4.2	3.2	4.8	ns	
Clock to DQS first edge for write delay							1, 5
($\overline{CAS}$ latency = 2)	t_{DQSS}	6	10	7.5	12.5	ns	
($\overline{CAS}$ latency = 2.5)	t_{DQSS}	5.3	8.8	6	10	ns	
DQS high pulse width (DQS write)							
($\overline{CAS}$ latency = 2)	t_{DQSH}	3.2	4.8	4	6	ns	
($\overline{CAS}$ latency = 2.5)	t_{DQSH}	2.8	4.2	3.2	4.8	ns	

		HB54A89FM/HB54A169FN					
		-8D		-10D			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
DQS low pulse width (DQS write)							
($\overline{CAS}$ latency = 2)	t_{DQSL}	3.2	4.8	4	6	ns	
($\overline{CAS}$ latency = 2.5)	t_{DQSL}	2.8	4.2	3.2	4.8	ns	
Input command and address setup time							1, 5
($\overline{CAS}$ latency = 2)	t_{IS}	2.7	—	3.0	—	ns	
($\overline{CAS}$ latency = 2.5)	t_{IS}	2.5	—	2.7	—	ns	
Input command and address hold time							1
($\overline{CAS}$ latency = 2)	t_{IH}	0.7	—	1.0	—	ns	
($\overline{CAS}$ latency = 2.5)	t_{IH}	0.5	—	0.7	—	ns	
Ref/Active command period	t_{RC}	64	—	80	—	ns	1, 5
Active to Precharge command period	t_{RAS}	40	120000	50	120000	ns	1, 5
Active to column command period	t_{RCD}	16	—	20	—	ns	1, 5
Precharge to active command period	t_{RP}	16	—	20	—	ns	1, 5
Write recovery	t_{WR}	7	—	8	—	ns	1, 5
Active to active command period	t_{RRD}	16	—	20	—	ns	1, 5
Refresh period	t_{REF}	—	64	—	64	ms	
CKE pulse width for reset	t_{RESET}	0.2	—	0.2	—	ms	
SSTK input transition time	t_{TSS}	—	0.7	—	0.7	ns	

Notes:
1. AC measurement regarding input signal assumes $t_{T(SS)} = [V_{IH}(ac)-V_{IL}(ac)]/SLEW$. Timing reference voltage level for this AC parameter is V_{REF}.
2. Min. specifications are given, assuming min. t_{CK} with the $\overline{CAS}$ latency in general.
3. Both the min. and the max. of this spec. is proportional to t_{CK}, values are appeared on the table assume t_{CK} min.
4. AC measurement regarding output signal assumes load capacitor CL = 30 pF with current source. See "Test conditions". Timing reference voltage level for this AC parameter is V_{TT}.
5. As for this AC parameter, timing is measured from the cross point of the CK and $\overline{CK}$.
6. As for this AC parameter, timing is measured from the point where DQS rising or falling edge crosses V_{TT}.
7. Transition from 'High impedance' to 'Low' of DQS pin is defined to occur when the level of DQ pin changes from V_{TT} to beyond $V_{TT} \pm 0.1$ V or vice versa.
8. t_{CK} max. is determined by the lock range of the DLL. Beyond the max. limitation of t_{CK}, the DLL does not work.

Test Conditions

Parameter	Symbol	Value	Unit
Input reference voltage	V_{REF}	$V_{CCQ} \times 0.5$	V
Termination voltage	V_{TT}	V_{REF}	V
AC input high voltage	V_{IH} (ac)	$V_{REF} + 0.35$	V
AC input low voltage	V_{IL} (ac)	$V_{REF} - 0.35$	V
Input signal slew rate	SLEW	1.0	V/ns



SSTL-2 class II Interface

Timing parameter measured in clock cycle (L-SPEC.)

Parameter	Symbol	Number of clock cycle Min	Max	Note
Write to pre-charge command delay (same bank)	L_{WPD}	2 + BL/2		
Read to pre-charge command delay (same bank)	L_{RPD}	BL/2		
Write to read command delay (to input all data)	L_{WRD}	2 + BL/2		
Burst stop command to write command delay ($\overline{CAS}$ latency = 2)	L_{BSTW}	2		
($\overline{CAS}$ latency = 2.5)		3		
Burst stop command to DQ high-Z ($\overline{CAS}$ latency = 2)	L_{BSTZ}	2		
($\overline{CAS}$ latency = 2.5)		2.5		
Read command to write command delay (to output all data) ($\overline{CAS}$ latency = 2)	L_{RWD}	2 + BL/2		
($\overline{CAS}$ latency = 2.5)		3 + BL/2		
Pre-charge command to High-Z ($\overline{CAS}$ latency = 2)	L_{HZP}	2		
($\overline{CAS}$ latency = 2.5)		2.5		
Write command to data in latency	L_{WCD}	1		
DM to data in latency	L_{DID}	0		
Register set command to active or register set command	L_{RSA}	2		
Self refresh exit time	L_{SREX} DLL = OFF	$[t_{RC}] + 1$		1
	L_{SREX} DLL = ON	200		
Power down entry	L_{PDEN}		1	
Power down exit to command input	L_{PDEX}		1	
CKE minimum pulse width	L_{CKEW}	1		

Note: 1. $[t_{RC}]$ means the lager one of the two closest integer to t_{RC}/ t_{CK}.

Command Operation

Command Truth Table

The DDR SDRAM module recognizes the following commands specified by the $\overline{S}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins. All other combinations than those in the table below are illegal.

		CKE									
Function	**Symbol**	**n – 1**	**n**	**$\overline{S}$**	**$\overline{RAS}$**	**$\overline{CAS}$**	**$\overline{WE}$**	**A12**	**A13**	**A10**	**A0 to A11**
Ignore command	DESL	H	×	H	×	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×	×
Burst stop in read command	BST	H	×	L	H	H	L	×	×	×	×
Column address and read command	READ	H	×	L	H	L	H	V	V	L	V
Read with auto-precharge	READA	H	×	L	H	L	H	V	V	H	V
Column address and write command	WRIT	H	×	L	H	L	L	V	V	L	V
Write with auto-precharge	WRITA	H	×	L	H	L	L	V	V	H	V
Row address strobe and bank active	ACTV	H	×	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	V	L	×
Precharge all bank	PALL	H	×	L	L	H	L	×	×	H	×
Refresh	REF	H	H	L	L	L	H	×	×	×	×
	SELF	H	L	L	L	L	H	×	×	×	×
Mode register set	MRS	H	×	L	L	L	L	L	L	L	V
	EMRS	H	×	L	L	L	L	L	H	L	V

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}. V: Valid address input

Ignore command [DESL]: When $\overline{S}$ is High at the cross point of the CK rising edge and the V_{REF} level, every input are neglected and internal status is held.

No operation [NOP]: As long as this command is input at the cross point of the CK rising edge and the V_{REF} level, address and data input are neglected and internal status is held.

Burst stop in read operation [BST]: This command stops a burst read operation, which is not applicable for a burst write operation.

Column address strobe and read command [READ]: This command starts a read operation. The start address of the burst read is determined by the column address and the bank select address (BA). After the completion of the read operation, the output buffer becomes High-Z.

Read with auto-precharge [READA]: This command starts a read operation. After completion of the read operation, the precharge is automatically executed.

Column address strobe and write command [WRIT]: This command starts a write operation. The start address of the burst write is determined by the column address and the bank select address (BA).

Write with auto-precharge [WRITA]: This command starts a write operation. After completion of the write operation, the precharge is automatically executed.

Row address strobe and bank activate [ACTV]: This command activates a bank selected by A12/A13 (BA) and determines a row address (AX0 to AX11). When A12 = A13 = Low, bank 0 is activated. When A12 = High and A13 = Low, bank 1 is activated. When A12 = Low and A13=s High, bank 2 is activated. When A12 = A13 = High, bank 3 is activated.

Precharge selected bank [PRE]: This command starts the pre-charge operation for the bank selected by A12/A13.

Precharge all banks [PALL]: This command starts the precharge operation for all banks.

Refresh [REF/SELF]: This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

Mode register set/Extended mode register set [MRS/EMRS]: The DDR SDRAM module has the two mode registers, the mode register and the extended mode register, to defines how it works. The both mode registers are set through the address pins (the A0 to the A13) in the mode register set cycle. For details, refer to "Mode register and extended mode register set".

CKE Truth Table

		CKE							
Current state	**Function**	**n – 1**	**n**	**$\overline{S}$**	**$\overline{RAS}$**	**$\overline{CAS}$**	**$\overline{WE}$**	**Address**	**Notes**
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	×	2
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	×	2
Idle	Power down entry (PDEN)	H	L	L	H	H	H	×	2
		H	L	H	×	×	×	×	
Self refresh	Self refresh exit (SELFX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	
Power down	Power down exit (PDEX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	

Notes: 1. H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
2. All the banks must be in IDLE before executing this command.

Auto-refresh command [REF]: This command executes an auto-refresh command. The banks and the ROW addresses to be refreshed are internally determined by the internal refresh controller. The refresh cycle is 4096 cycles/64ms. The output buffer becomes High-Z after auto-refresh start. Precharge has been completed automatically after the auto-refresh. The ACTV or MRS command can be issued t_{RC} after the last auto-refresh command.

Self-refresh entry [SELF]: This command starts the self-refresh operation. The self-refresh operation continues as long as CKE is held Low. During the self-refresh operation, all ROW addresses are repeated refreshing by the internal refresh controller. A self-refresh is terminated by a self-refresh exit command.

Power down mode entry [PDEN]: LPDEN (= 1 cycle) after issuing [PDEN] or changing CKE from High to Low in all-banks-IDLE mode, the SDRAM enters into power-down mode. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. No internal refresh operation occurs during the power down mode.

Self-refresh exit [SELFX]: This command is executed to exit from self-refresh mode. After the exit, in case DLL = ON, keeping NOP condition for 200 cycles (= L_{SREX}) to lock the DLL, then start activating a bank or rewrite the mode register. While in case DLL = OFF, keeping NOP condition for $[t_{RC}]+1$ (= L_{SREX}) cycles after the exit, then start activating a bank. After the exit, 4096 cycles of auto-refresh should be executed within 64 ms at least. $[t_{RC}]$ is the larger one of the two closest integers to t_{RC}/t_{CK}.

Power down exit [PDEX]: When this command is executed at the power down mode, the SDRAM can exit from power down mode. The DDR SDRAM module resumes IDLE state and LDEX (= 1 cycle min.) after the exit, the MRS command or a ACTV command can be accepted.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the DDR SDRAM module.

Function Truth Table (1)

Current state	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation	Next state
Precharging*[2]	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL*[10]	Idle
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[10]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[10]	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[10]	—
	L	L	H	L	BA, A10	PRE, PALL	NOP	Idle
	L	L	L	×	×		ILLEGAL	—
Idle*[3]	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL*[10]	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[10]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[10]	—
	L	L	H	H	BA, RA	ACTV	Active*[12]	Activating
	L	L	H	L	BA, A10	PRE, PALL	NOP	Idle
	L	L	L	H	×	REF, SELF	Refresh/ Selfrefresh*[12]	Idle/ Selfrefresh
	L	L	L	L	MODE	MRS	Mode register set	Idle
Refresh (auto-refresh)	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	H	H	H	L	×	BST	ILLEGAL	—
	L	H	L	×	×		ILLEGAL	—
	L	L	×	×	×		ILLEGAL	—

Function Truth Table (2)

Current state	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation	Next state
Activating*[4]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL*[10]	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[10]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[10]	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[10]	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[10]	—
	L	L	L	×	×		ILLEGAL	—
Active[5]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL	Active
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation	Read/READA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting write operation	Write recovering/precharging
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[11.]	—
	L	L	H	L	BA, A10	PRE, PALL	Pre-charge	Idle
	L	L	L	×	×		ILLEGAL	—
Read*[6]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	BST	Active
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst read operation to start new read	Active
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[13]	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[10]	—
	L	L	H	L	BA, A10	PRE, PALL	Interrupting burst read operation to start pre-charge	Precharging
	L	L	L	×	×		ILLEGAL	—

Function Truth Table (3)

Current state	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation	Next state
Read with auto-pre- charge*[7]	H	×	×	×	×	DESL	NOP	Precharging
	L	H	H	H	×	NOP	NOP	Precharging
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[10.]	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[10.]	—
	L	L	L	×	×		ILLEGAL	—
Write*[8.]	H	×	×	×	×	DESL	NOP	Write recovering
	L	H	H	H	×	NOP	NOP	Write recovering
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst write operation to start read operation.	Read/ReadA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Interrupting burst write operation to start new write operation.	Write/WriteA
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[10.]	—
	L	L	H	L	BA, A10	PRE, PALL	Interrupting write operation to start pre-charge.	Idle
	L	L	L	×	×		ILLEGAL	—
Write recovering*[8.]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation.	Read/ReadA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting new write operation.	Write/WriteA
	L	L	H	H	BA, RA	ACTV	ILLEGAL*[10.]	—
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL*[10.]	—
	L	L	L	×	×		ILLEGAL	—

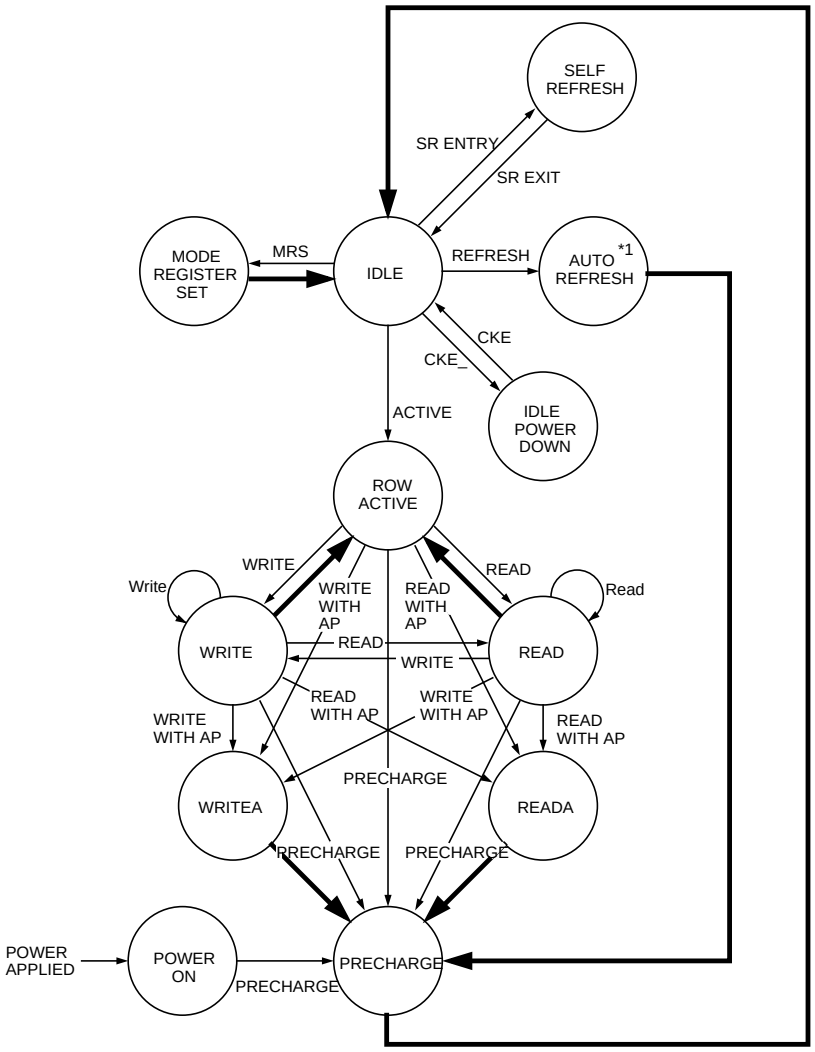
Function Truth Table (4)

Current state	$\overline{S}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation	Next state
Write with auto-pre-charge*9.	H	×	×	×	×	DESL	NOP	Precharging
	L	H	H	H	×	NOP	NOP	Precharging
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	—
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL	—
	L	L	H	H	BA, RA	ACTV	ILLEGAL*10.	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*10.	—
	L	L	L	×	×		ILLEGAL	—

Notes: 1. H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.

2. The DDR SDRAM module is in the "Precharging" state for t_{RP} after the precharge command are issued.
3. The DDR SDRAM module reaches IDLE state t_{RP} after the precharge command are issued.
4. The DDR SDRAM module is in the "Activating" for t_{RCD} after the ACTV command are issued.
5. The DDR SDRAM module is in the "READ" state until burst data have been output and DQ output circuits are turned off.
6. The DDR SDRAM module is in the "READ with auto-precharge" from the READA command until burst data has been output and DQ output circuits are turned off.
7. The DDR SDRAM module is in the "WRITE" state from the WRIT command to the last burst data are input.
8. The DDR SDRAM module is in the "Write recovering" for t_{WR} after the last data are input.
9. The DDR SDRAM module is in the "Write with auto-precharge" until t_{WR} after the last data has been input.
10. This command may be issued for other banks, depending on the state of the banks.
11. For the bank for which the current state is defined, this command cannot be issued, or ILLEGAL. For the other banks, depending on the state of the banks, this command can be issued t_{RRD} after the preceded active command.
12. All banks must be in the IDLE.
13. Before executing a write command to stop the preceding burst read operation, BST command must be issued

Simplified State Diagram



Automatic transition after completion of command.
Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

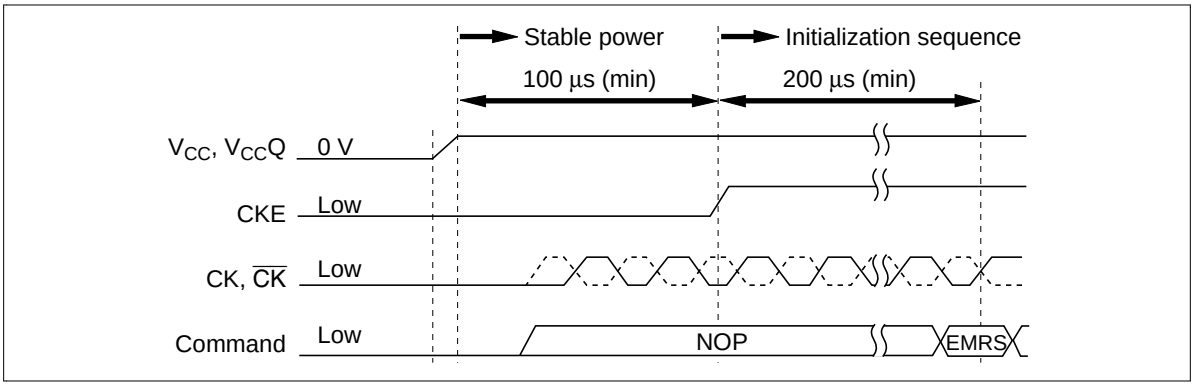
Operation of the DDR SDRAM module

Power-up sequence:

The following sequence is recommended for Power-up.

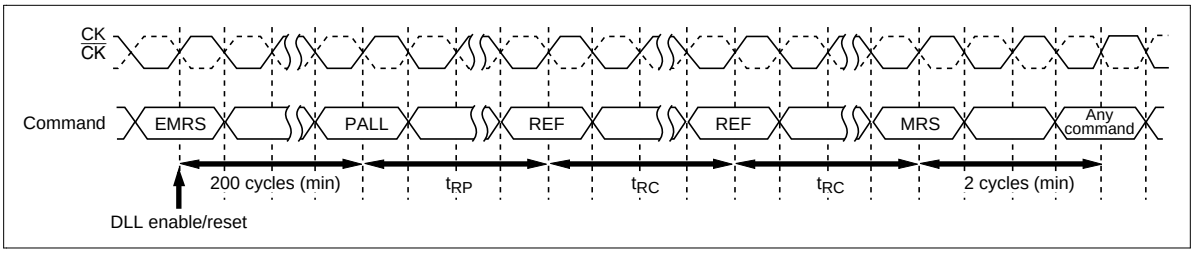
(1) The CK, CKE, $\overline{S}$, DM and I/O pins keep low till stable power is achieved.
(2) The CK and the $\overline{CK}$ inputs need to be stabilized within 100 µs after power is stabilized.
(3) 100 µs or later after power is stabilized, the CKE is driven high to set the NOP condition.
(4) Maintain stable power, stable clock and the NOP condition for more than 200 µs.

Power-up sequence ((1)-(4))



(5) Issue the extended mode register set command for "DLL Enable/Reset". An additional 200 cycles of clock input are required to lock the DLL. In case DLL "off" mode is used, by executing EMRS, DLL must be disabled.
(6) All banks must be precharged using the precharge command.
(7) After t_{RP} delay, set 2 or more auto refresh commands.
(8) Issue the mode register set command to set parameter onto the mode register.

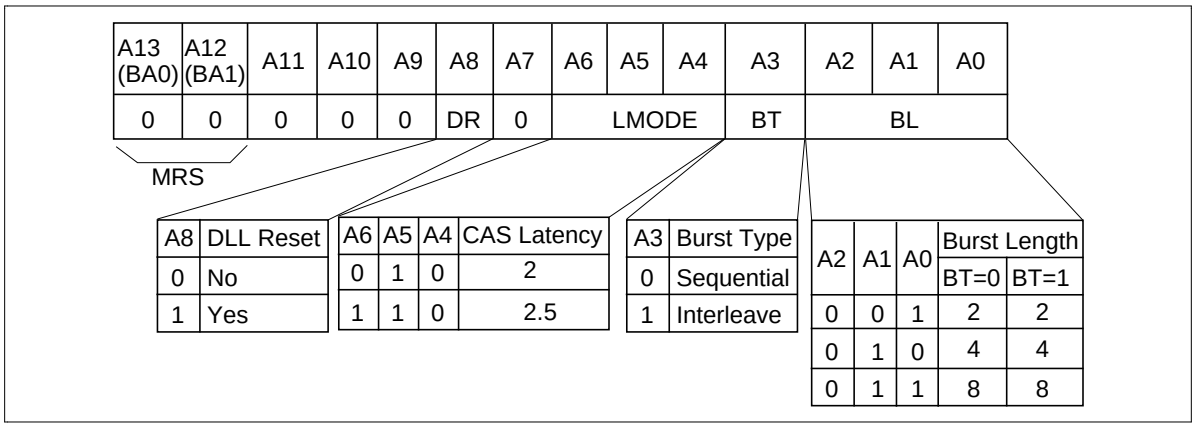
Initialization ((5)-(8))



Mode Register and Extended Mode Register set

There are two mode registers, the mode register and the extended mode register so as to define the operating mode. Parameter are set to both through the A10 to the A13 pins by the mode register set command [MRS] or the extended mode register set command [EMRS]. The mode register and the extended mode register are set by inputting signal via the A0 to the A13 during mode register set cycles. AY13 (BA0) and AY12 (BA1) determine which one of the mode register or the extended mode register are set. Prior to a read or a write operation, the mode register must be set.
When all banks are idle, by executing EMRS, DLL can be disabled. In order to set DLL on again, execute EMRS to enable DLL. 200 cycles after EMRS command is issued, ACTIVE or MRS command can be executed
Remind that no other parameters are shown in the table bellow are allowed to input to the registers.

Mode Register Set [MRS] (A13 = 0, A12 = 0)



A13 (BA0)	A12 (BA1)	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	DR	0	LMODE			BT	BL		

MRS

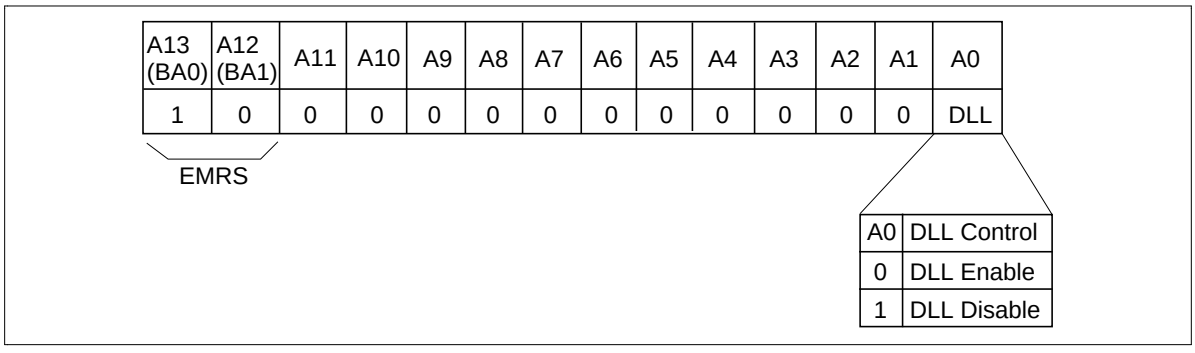
A8	DLL Reset
0	No
1	Yes

A6	A5	A4	CAS Latency
0	1	0	2
1	1	0	2.5

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8

Extended Mode Register Set [EMRS] (A13 = 1, A12 = 0)



A13 (BA0)	A12 (BA1)	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	0	0	0	0	0	DLL

EMRS

A0	DLL Control
0	DLL Enable
1	DLL Disable

Burst operation

The burst type (BL) and the first three bits of the column address determines the order of a data out.

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

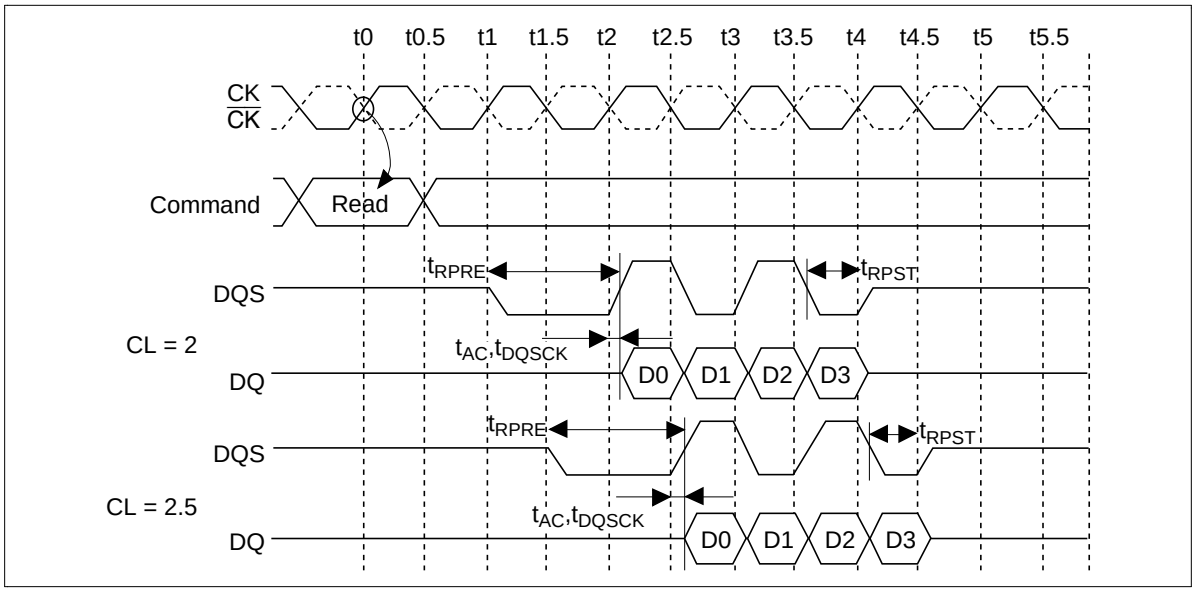
Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

Read/Write Operations

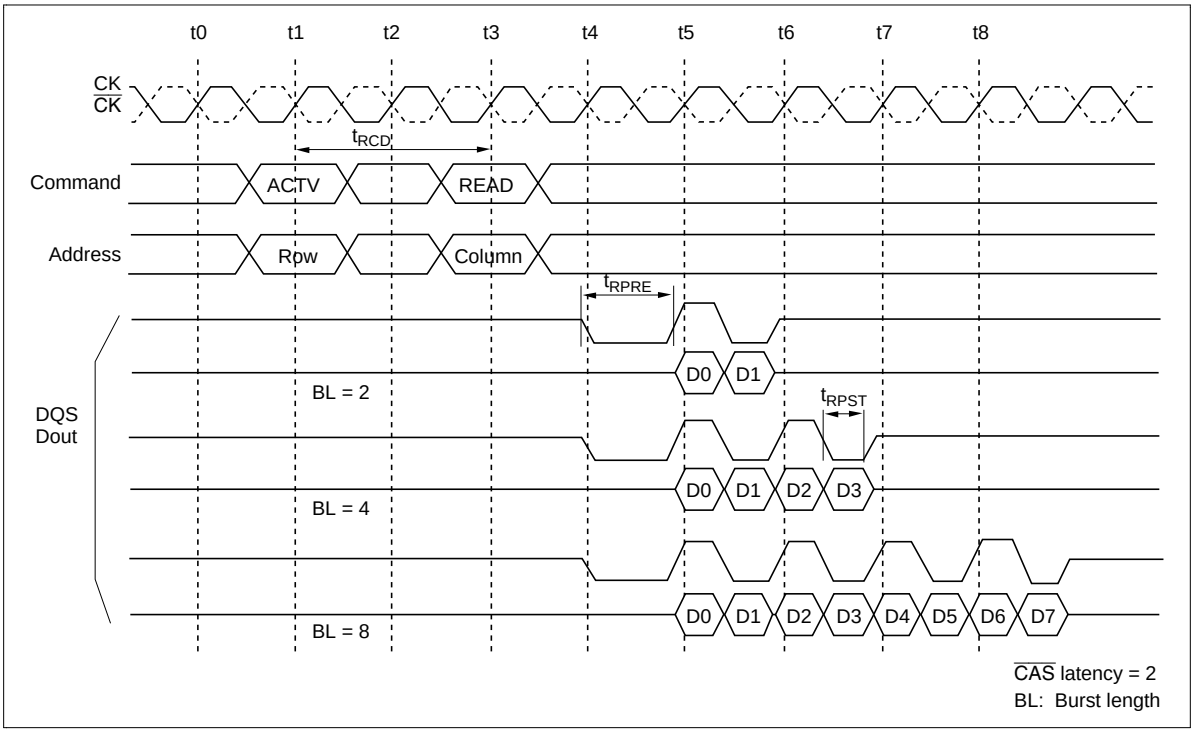
Bank active: A read or a write operation begins with the bank active command [ACTV]. The bank active command determines a bank address (AX13, AX12) and a row address (AX0 to AX11). For the bank and the row, a read or a write command can be issued t_{RCD} after the ACTV is issued.

Read operation: The burst length (BL), the $\overline{CAS}$ latency (CL) and the burst type (BT) of the mode register are referred when a read command is issued. The burst length (BL) determines the length of a sequential output data by the read command which can be set to 2, 4, or 8. The starting address of the burst read is defined by the column address, the bank select address (AX13, AX12) which are loaded via the A0 to A13 pins in the cycle when the read command is issued. $\overline{CAS}$ latency (CL) determines the latency of the data output from the read command, which can be set to 2 or 2.5. The DDR SDRAM module output the data strobe simultaneously. t_{RPRE} prior to the first rising edge of the data strobe, the DQS is driven LOW from V_{TT} level. The burst data are output coincidentally at both the rising edge and the falling edge of the data strobe. The DQ pins become High-Z in the next cycle after the successive burst data has been completed. t_{RPST} from the last falling edge of the data strobe, the DQS pins become High-Z.

Read Operation ($\overline{CAS}$ Latency)

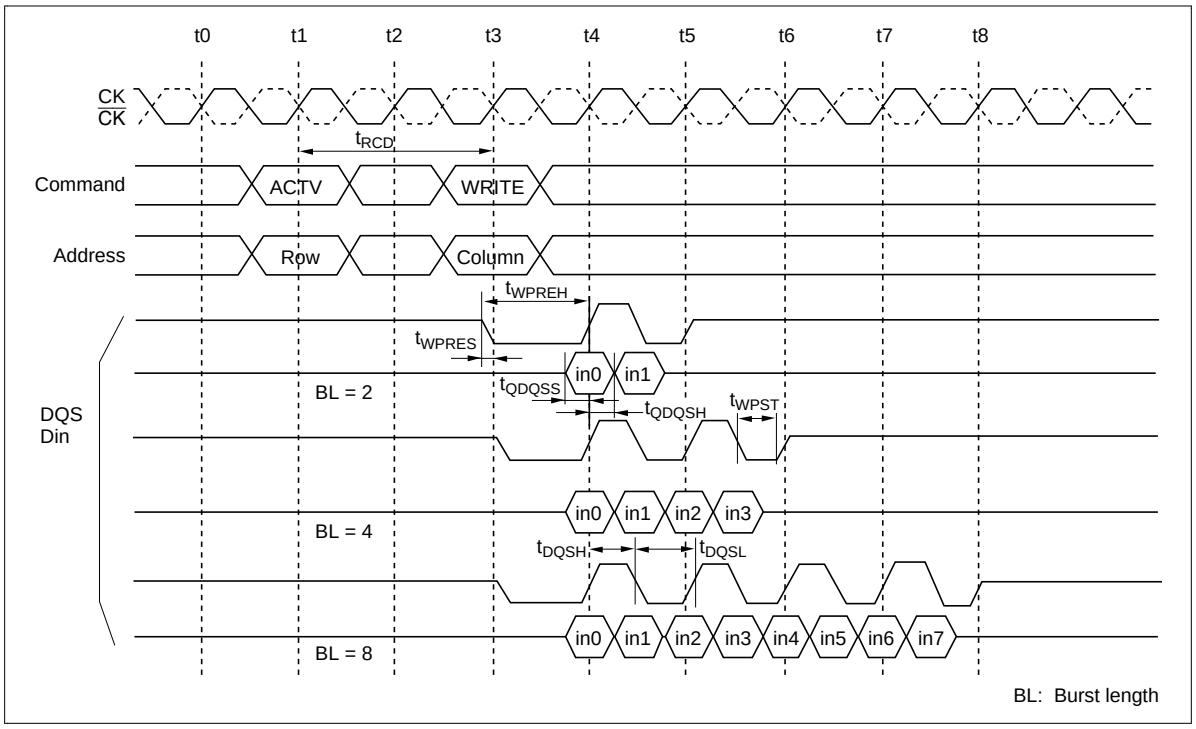


Read Operation (Burst Length)



Write operation: The burst length (BL) and the burst type (BT) of the mode register are referred when a write command is issued. The burst length (BL) determines the length of a sequential data input by the write command which can be set to 2, 4, or 8. The latency from write command to data input is 1. The starting address of the burst read is defined by the column address, the bank select address (AX13, AX12) which are loaded via the A0 to A13 pins in the cycle when the write command is issued. DQS should be input as the strobe for the input-data and DM as well during burst operation. t_{WPREH} prior to the first rising edge of the DQS should be set to LOW and t_{WPST} after the last falling edge of the data strobe should be set to high-Z.

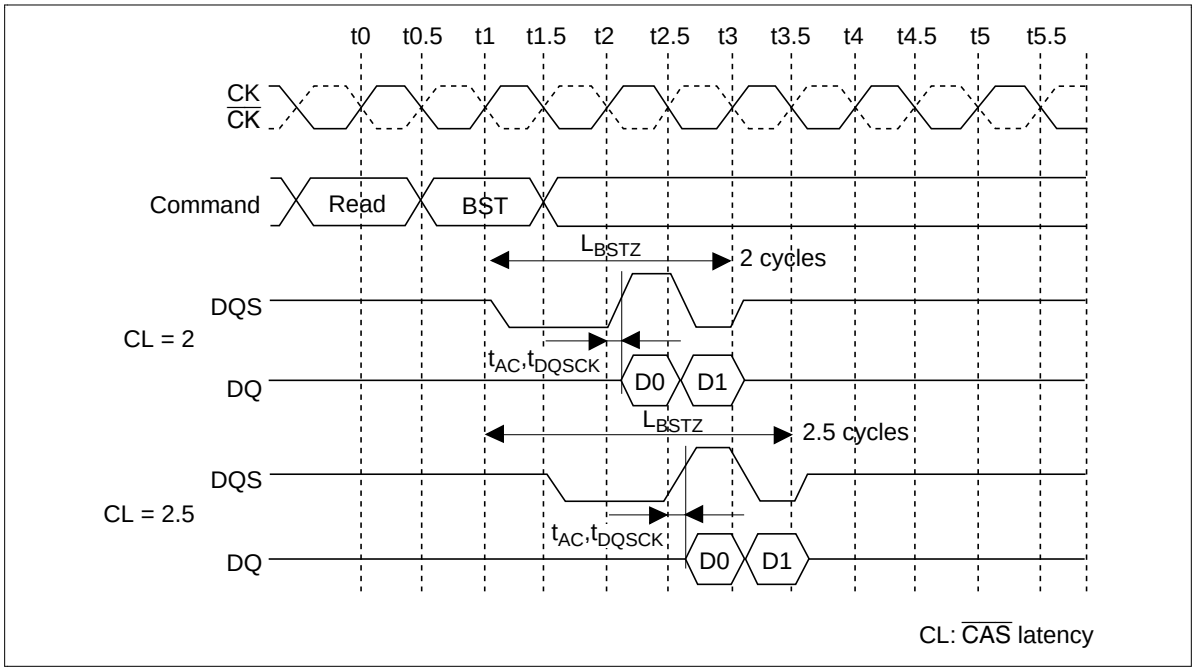
Write operation



Burst stop

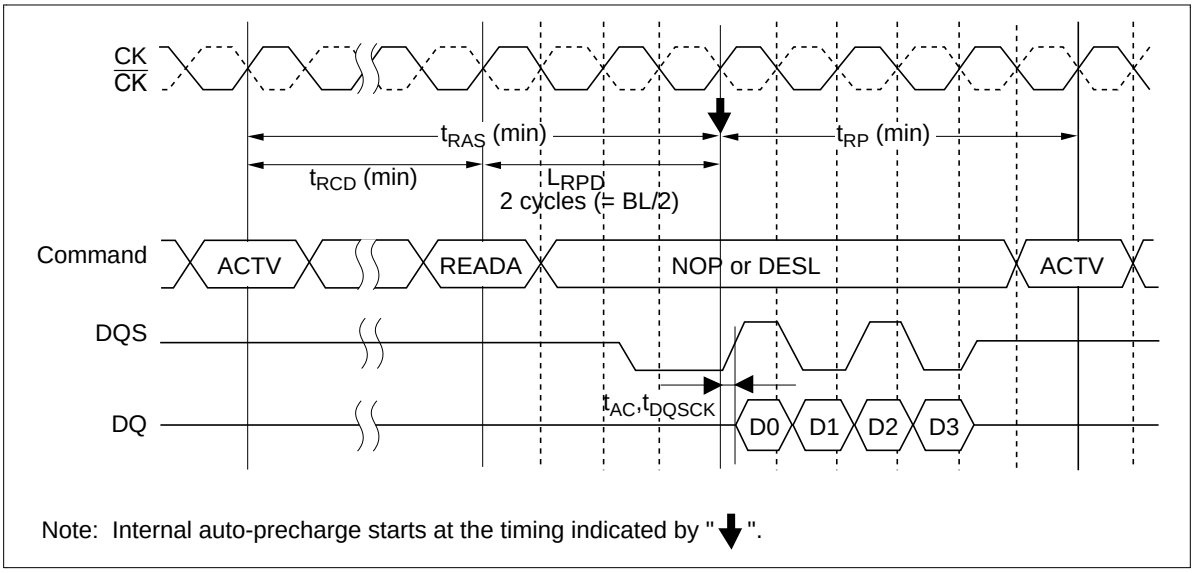
Burst stop command during burst read: The burst stop (BST) command is used to stop data output during a burst read. The BST command stops the burst read and sets the output buffer to High-Z. L_{BSTZ} (= CL) cycles after a BST command issued, the DQ pins become high-Z. The BST command is not supported for the burst write operation.

Burst stop during a read operation



Auto Precharge

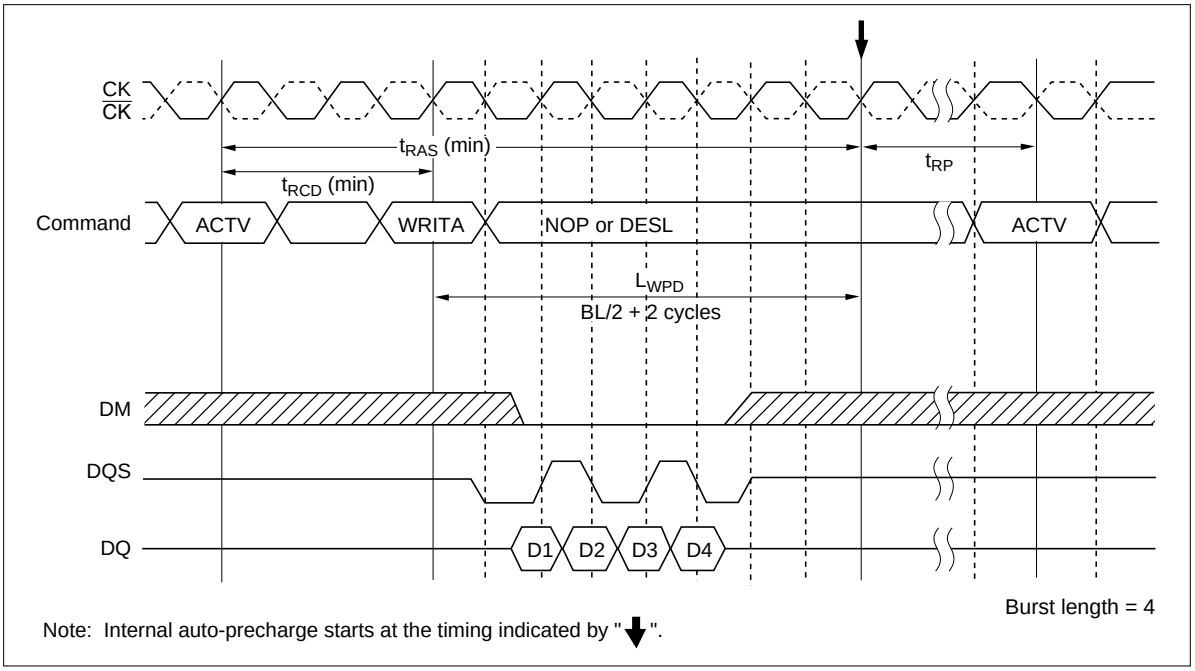
Read with auto-precharge: The precharge is automatically performed after completing a read operation. The precharge starts L_{RPD} (BL/2) cycle after READA command input. t_{RCD} for READA should be determined so that t_{RC} (ACTV to ACTV) spec. is obeyed when READA is issued successively after a bank active command, that is t_{RCD} (READA) ≥ t_{RC} (min.)-t_{RP} (min.)-L_{RPD}. A column command to the other active bank can be issued the next cycle after the last data output.



Note: Internal auto-precharge starts at the timing indicated by "↓".

Write with auto-precharge: The precharge is automatically performed after completing a burst write operation. The precharge operation is started L_{WPD} (= BL/ 2 + 2) cycles after WRITA command issued. t_{RCD} for WRITA should be determined so that t_{RC} (ACTV to ACTV) spec. is obeyed when WRITA is issued successively after a bank active command, that is t_{RCD} (WRITA) ≥ t_{RC}(min.)-t_{RP}(min.)-L_{WPD}. A column command to the other active command can be issued the next cycle after the internal precharge command issued.

Burst Write (Burst Length = 4)



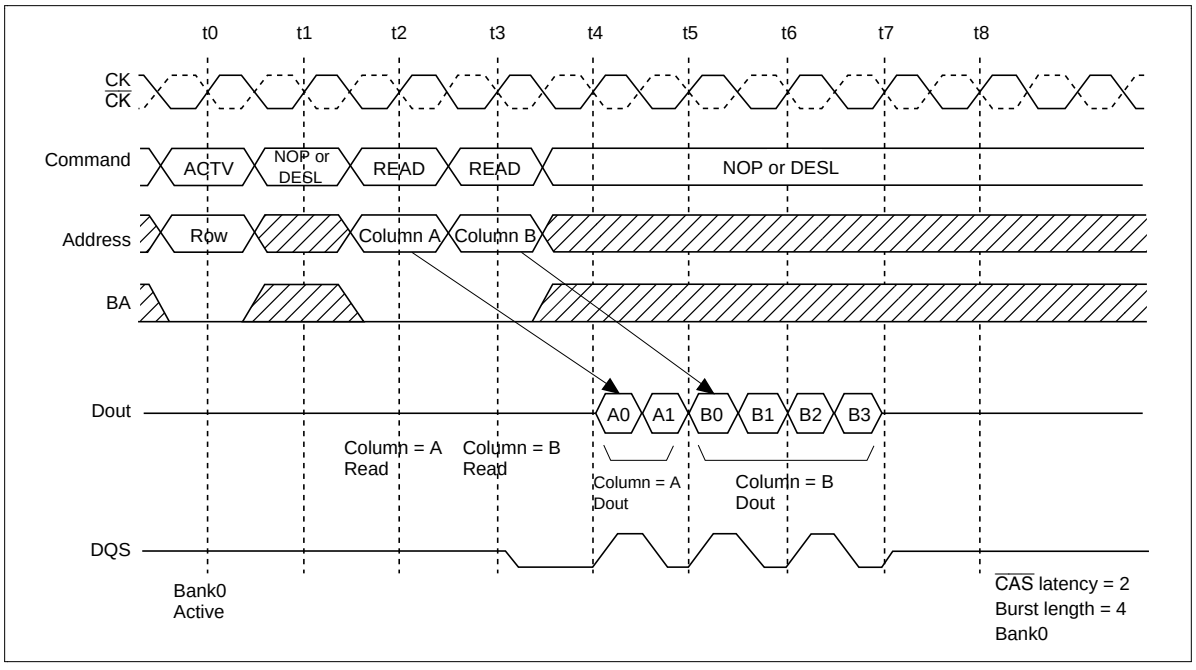
Note: Internal auto-precharge starts at the timing indicated by "↓".

Command Intervals

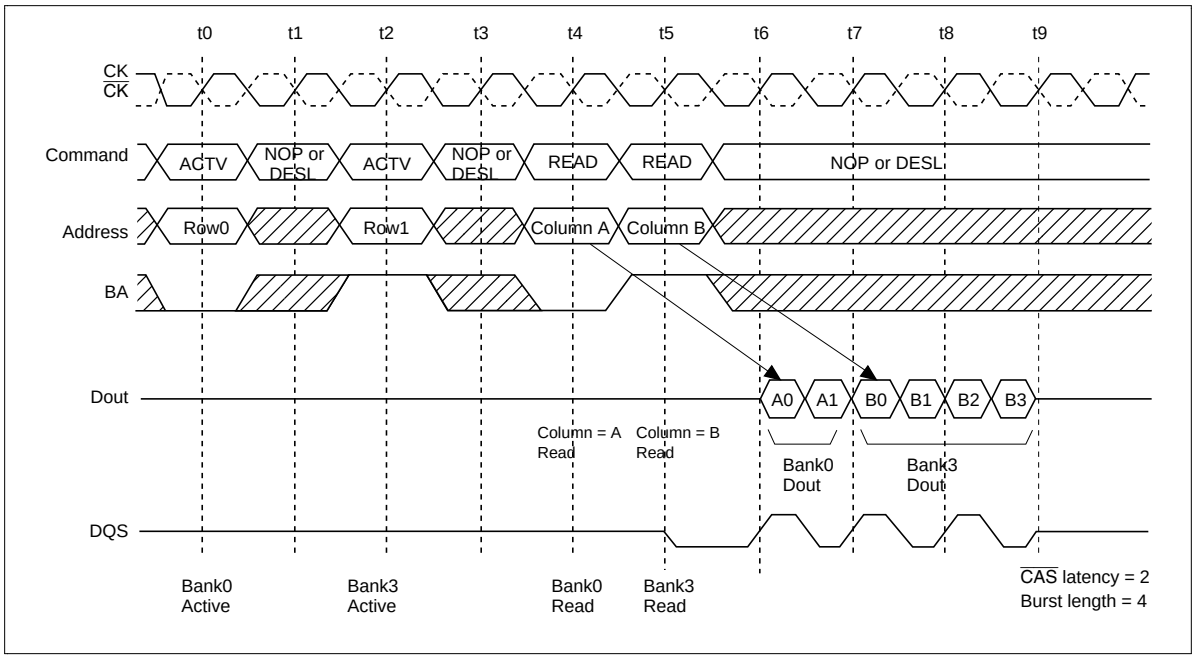
A Read command to the consecutive Read command Interval

	Destination row of the consecutive read command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Same	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
2.	Same	Other	—	Precharge the bank to interrupt the preceding read operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Other	Any	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
			IDLE	Precharge the bank without interrupting the preceding read operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive read command can be issued.

READ to READ Command Interval (same ROW address in same bank)



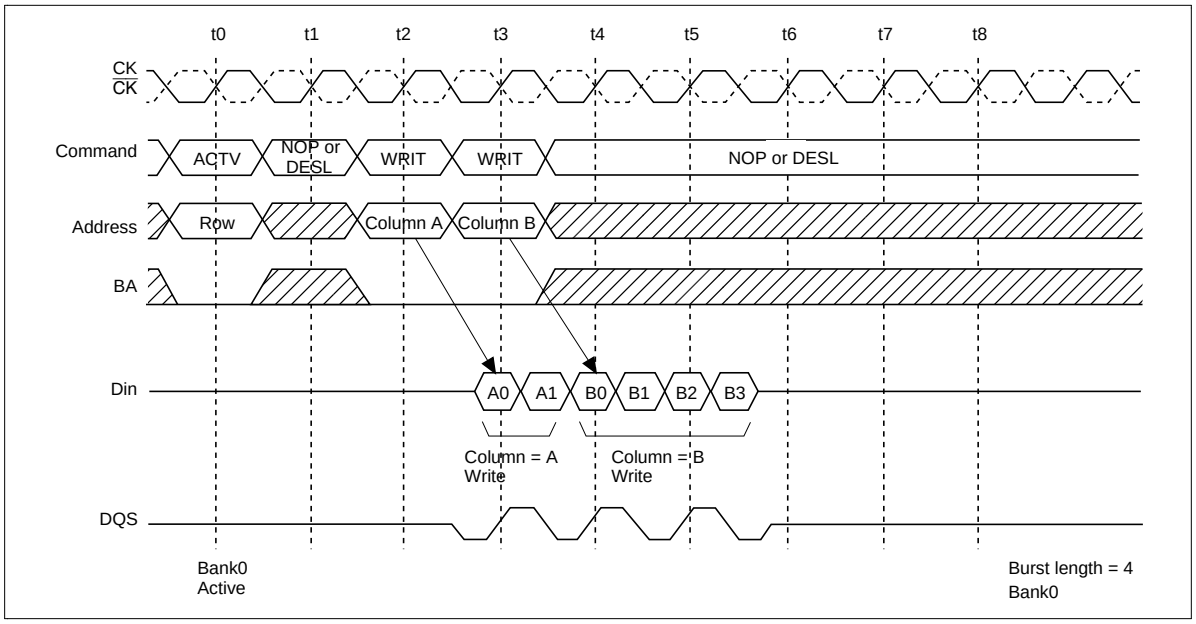
READ to READ Command Interval (different bank)



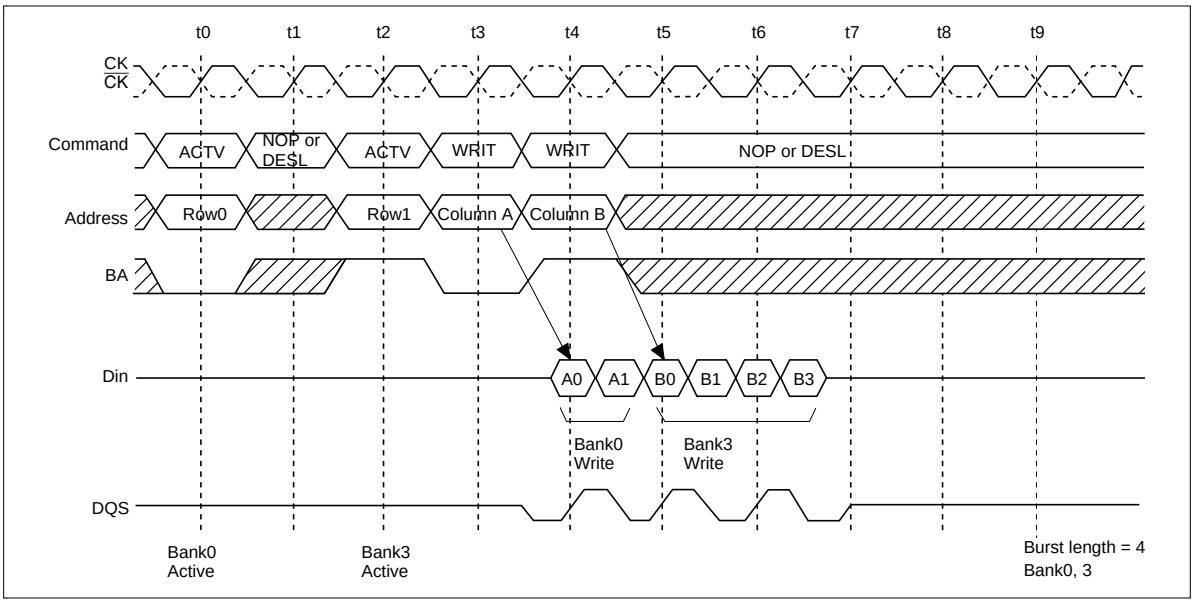
A Write command to the consecutive Write command Interval:

	Destination row of the consecutive write command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Same	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
2.	Same	Other	—	Precharge the bank to interrupt the preceding write operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive write command can be issued. See 'A write command to the consecutive precharge interval' section.
3.	Other	Any	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
			IDLE	Precharge the bank without interrupting the preceding write operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive write command can be issued.

WRITE to WRITE Command Interval (same ROW address in same bank)



WRITE to WRITE Command Interval (different bank)



A Read command to the consecutive Write command interval with the BST command

	Destination row of the consecutive write command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Same	ACTIVE	Issue the BST command. L_{BSTW} ($\geq L_{BSTZ}$) after the BST command, the consecutive write command can be issued.
2.	Same	Other	—	Precharge the bank to interrupt the preceding read operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive write command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Other	Any	ACTIVE	Issue the BST command. L_{BSTW} ($\geq L_{BSTZ}$) after the BST command, the consecutive write command can be issued.
			IDLE	Precharge the bank without interrupting the preceding read operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive write command can be issued.

READ to WRITE Command Interval

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

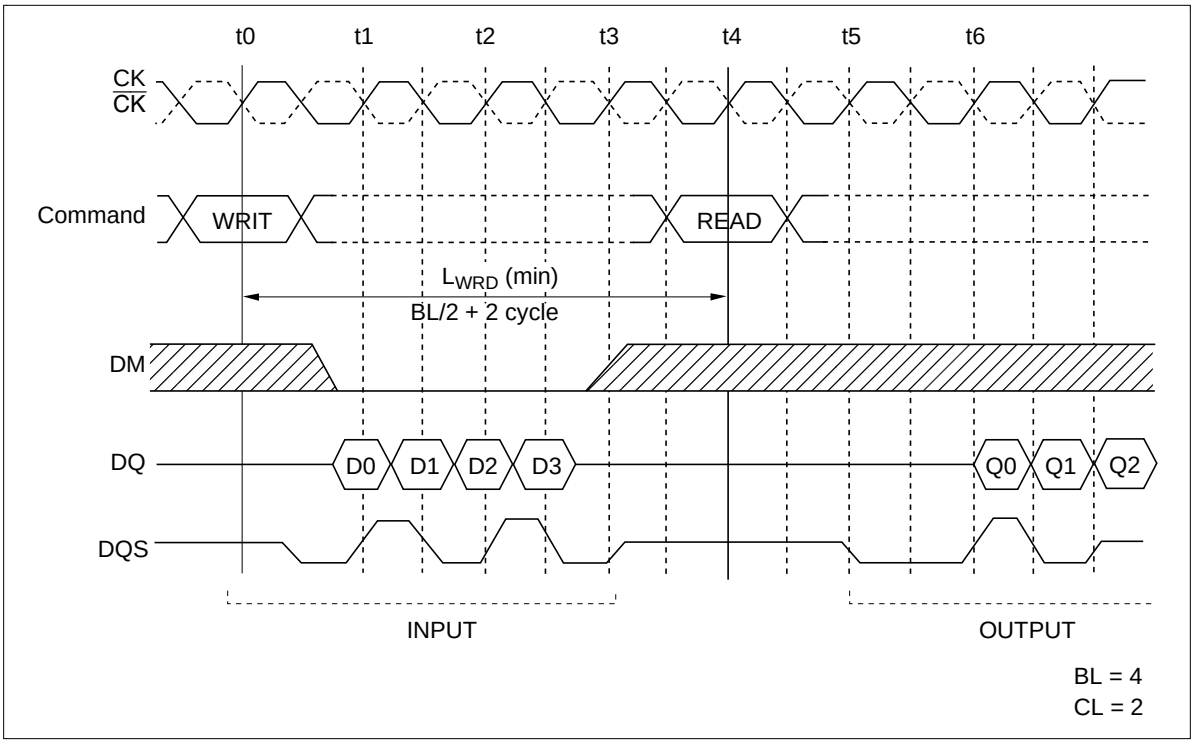
Burst length = 8

Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

A Write command to the consecutive Read command interval: To complete the burst operation

	Destination row of the consecutive read command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Same	ACTIVE	To complete a burst operation, the consecutive read command should be performed L_{WRD} (= BL/ 2 + 2) after the write command.
2.	Same	Other	—	Precharge the bank L_{WRD} after the preceding write command. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Other	Any	ACTIVE	To complete a burst operation, the consecutive read command should be performed L_{WRD} (= BL/ 2 + 2) after the write command.
			IDLE	Precharge the bank without interrupting the preceding write operation. t_{RP} after the precharge command, issue the ACTV command. t_{RCD} after the ACTV command, the consecutive read command can be issued.

WRITE to READ Command Interval

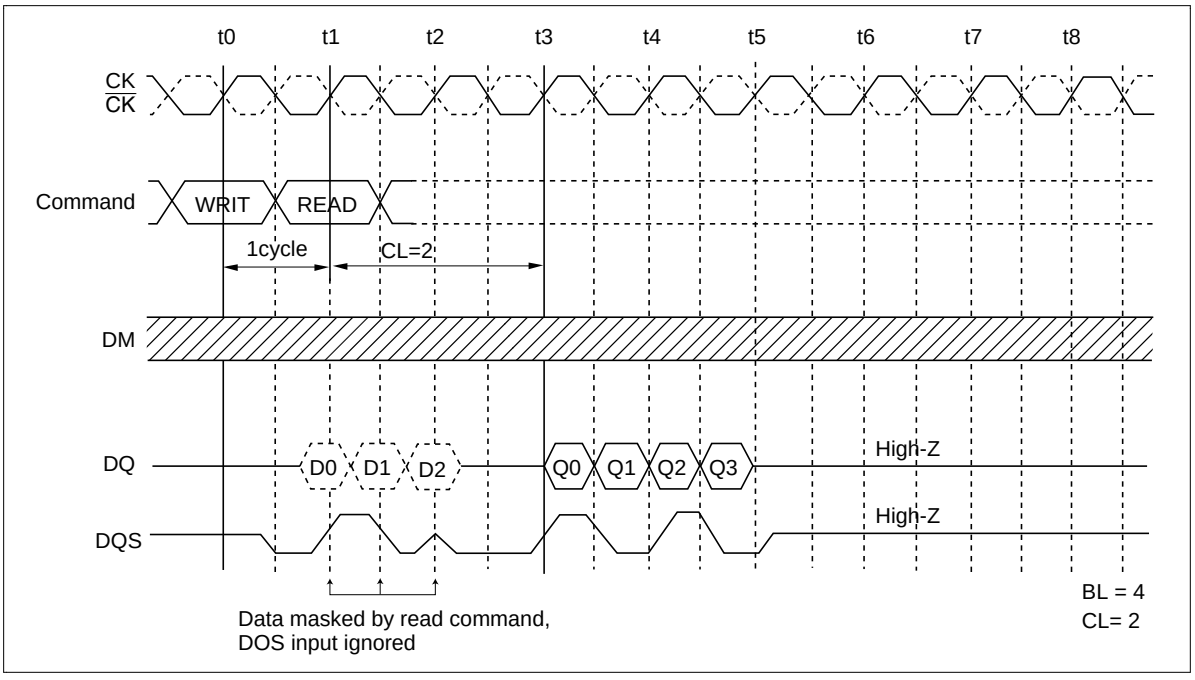


A Write command to the consecutive Read command interval: To interrupt the write operation.

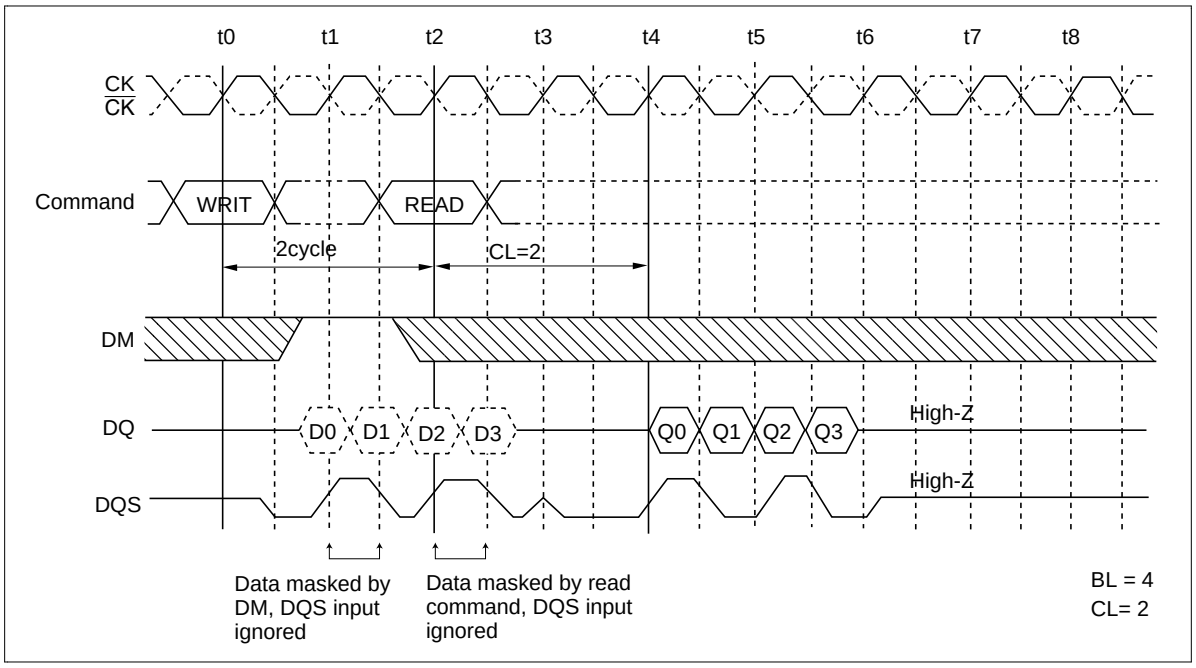
	Destination row of the consecutive read command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Same	ACTIVE	DM, DMU/DML must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM, DMU/DML is not necessary.
2.	Same	Other	—	—
3.	Other	Any	ACTIVE	DM, DMU/DML must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM, DMU/DML is not necessary.
			IDLE	—

WRITE to READ Command Interval (Samebank, same ROW address)

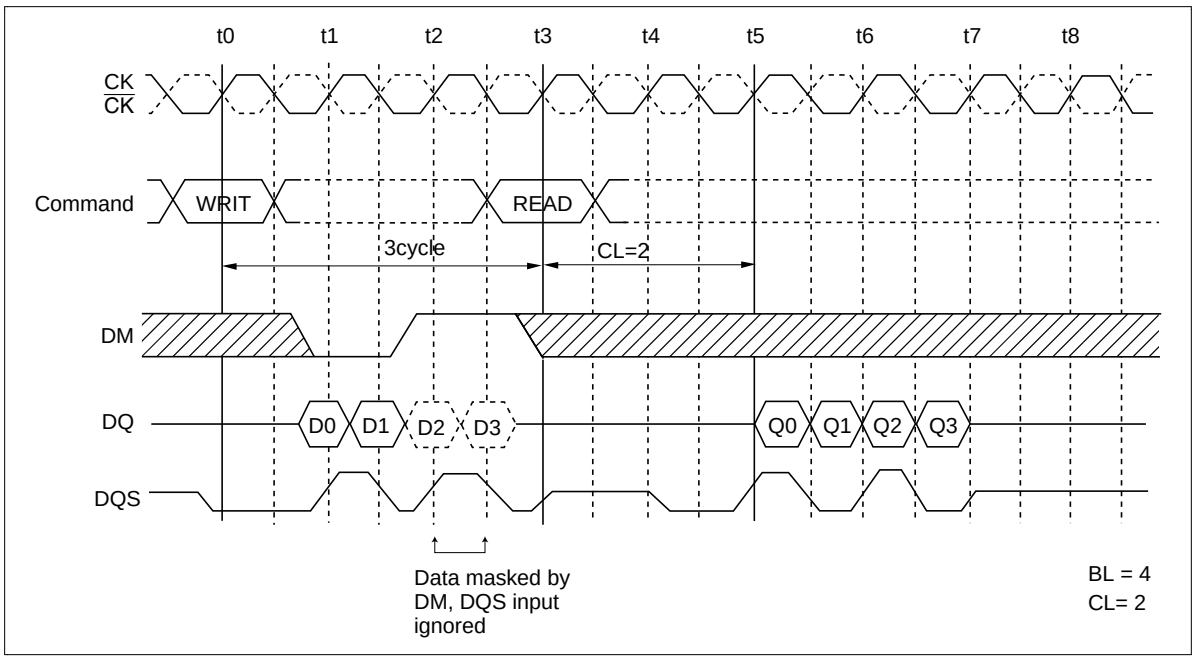
[WRITE to READ delay = 1 clock cycle]



[WRITE to READ delay = 2 clock cycle]



[WRITE to READ delay = 3 clock cycle]

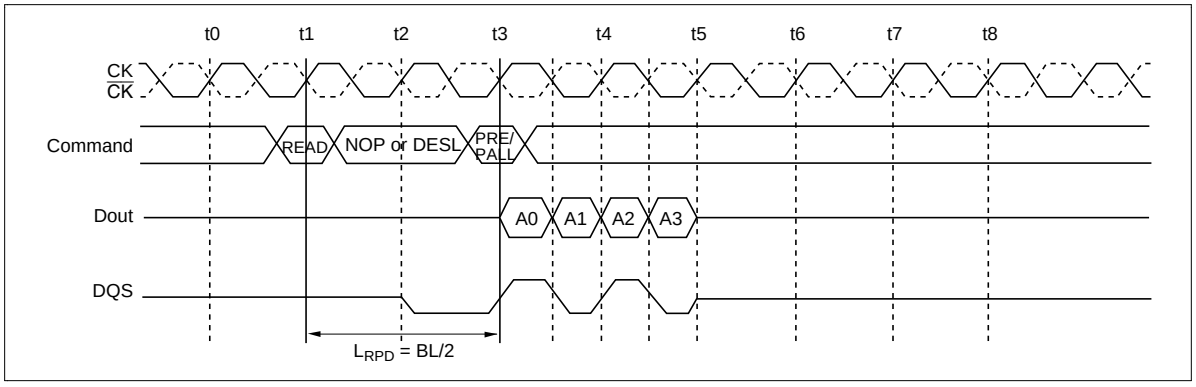


A Read command to the consecutive Precharge command interval (same bank):

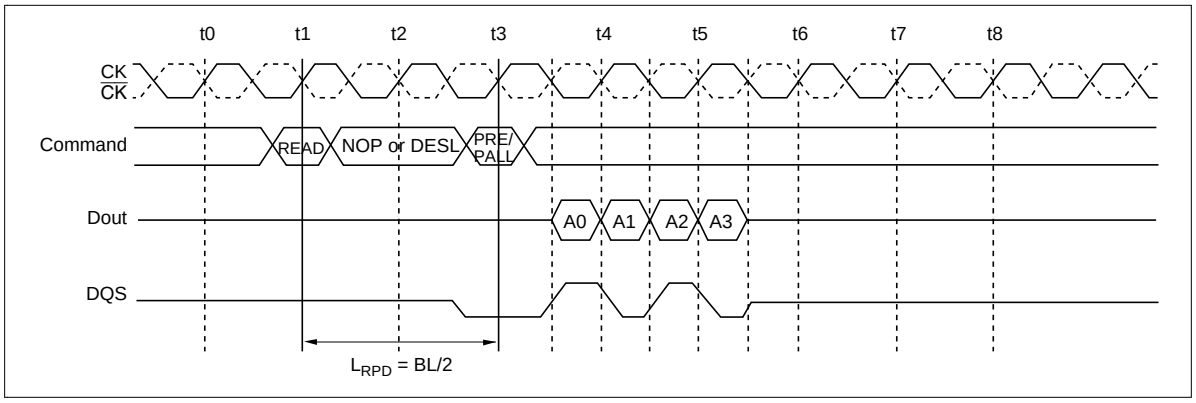
To output all data: To complete a burst read operation and get a burst length, programmed, of data, the consecutive precharge command must be issued L_{RPD} (= BL/ 2 cycles) after the read command is issued.

READ to PRECHARGE Command Interval (same bank): To output all data

$\overline{CAS}$ Latency = 2, Burst Length = 4



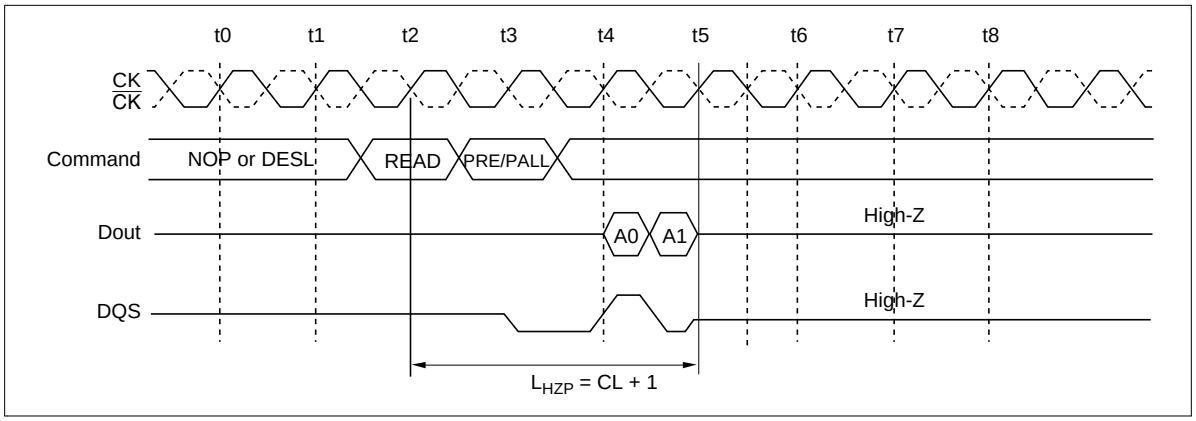
$\overline{CAS}$ Latency = 2.5, Burst Length = 4



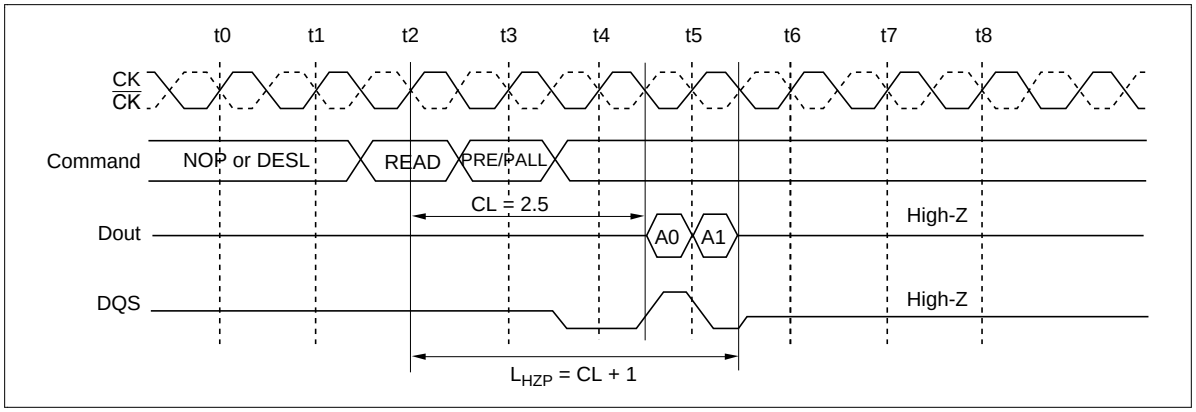
READ to PRECHARGE Command Interval (same bank): To stop output data

A burst data output can be interrupted with the precharge command. The output buffer becomes High-Z L_{HZP} (= CL) cycles after the precharge command.

$\overline{CAS}$ Latency = 2, Burst Length = 2, 4, 8



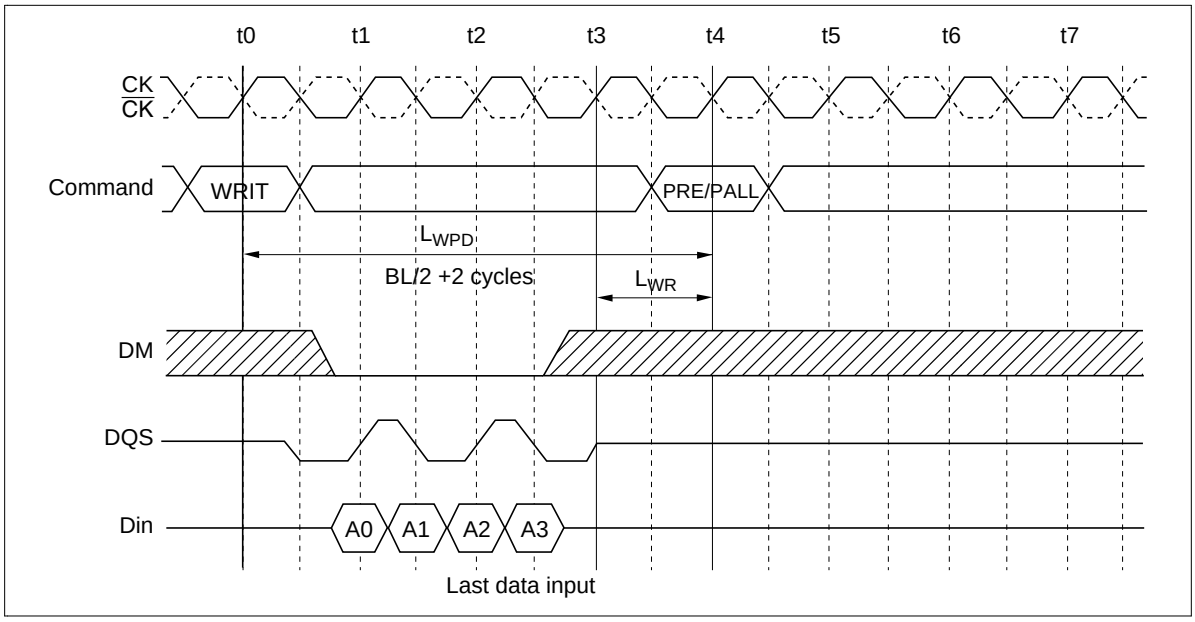
$\overline{CAS}$ Latency = 2.5, Burst Length = 2, 4, 8



Write command to Precharge command interval (same bank): The minimum interval L_{WPD} ((BL/ 2 + 2) cycles) is needed between the write command and the precharge command.

WRITE to PRECHARGE Command Interval (same bank)

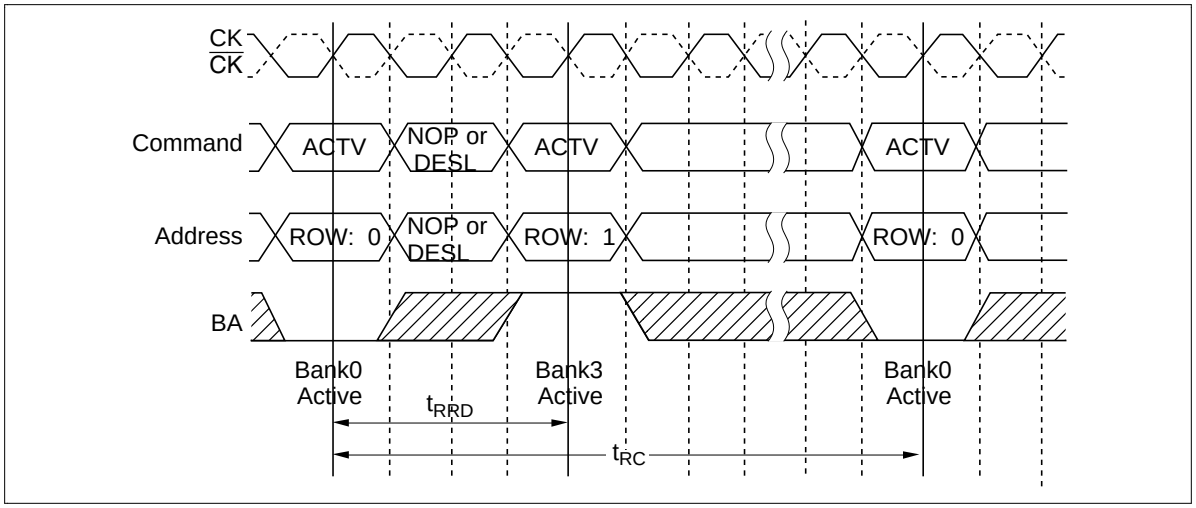
Burst Length = 4



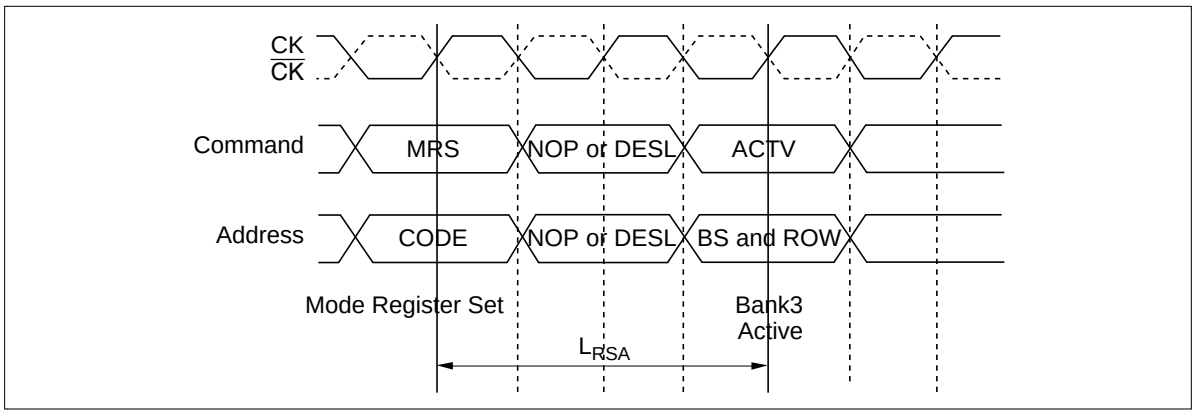
Bank active command interval:

	Destination row of the consecutive ACTV command			
	Bank address	**Row address**	**State**	**Operation**
1.	Same	Any	ACTIVE	t_{RC} after a ACTV command, the next ACTV command can be issued.
2.	Other	Any	ACTIVE	Precharge the bank. t_{RP} after the precharge command, the consecutive ACTV command can be issued.
			IDLE	t_{RRD} after a ACTV command, the next ACTV command can be issued.

Bank Active to Bank Active

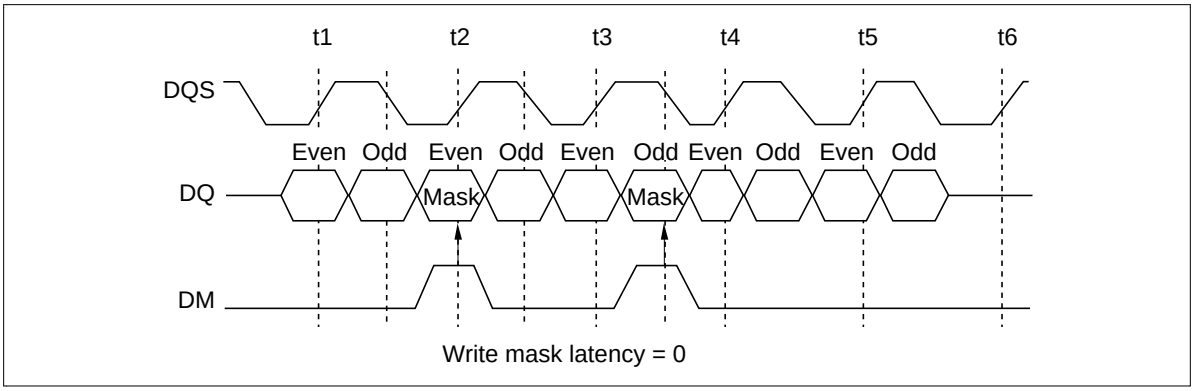


Mode register set to Bank-active command interval: The interval between setting the mode register and executing a bank-active command must be no less than t_{RSA}.



DM Control

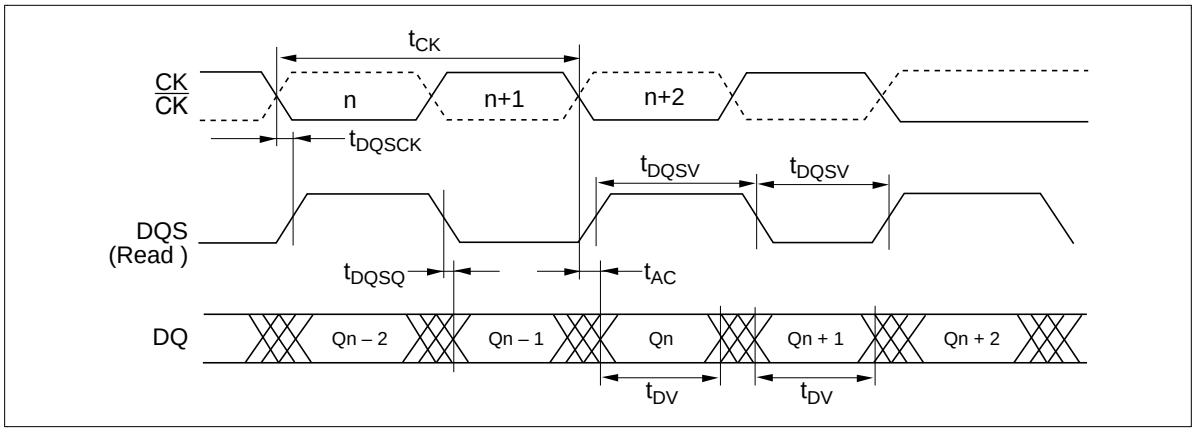
DM can mask input data. By setting DM to Low, data can be written. When DM is set to High, the corresponding data is not written, and the previous data is held. The latency between DM input and enabling/disabling mask function is 0. The set up and hold time of DM are referred to DQS.



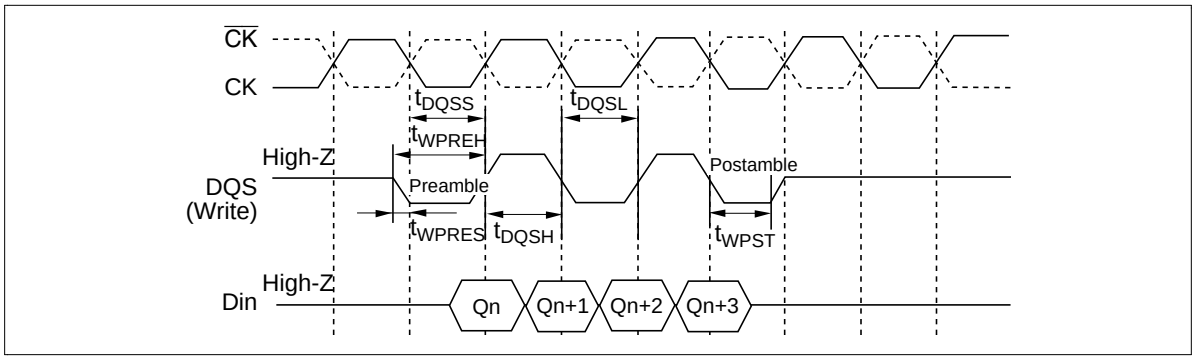
Timing Waveforms

Detailed Waveforms

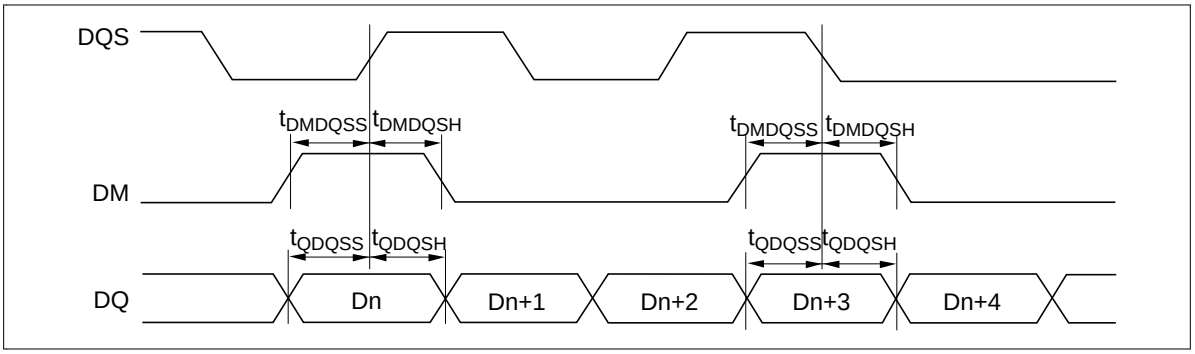
t_{DQSCK}, t_{AC}, t_{DQSQ}, t_{DQSV}, t_{DV}



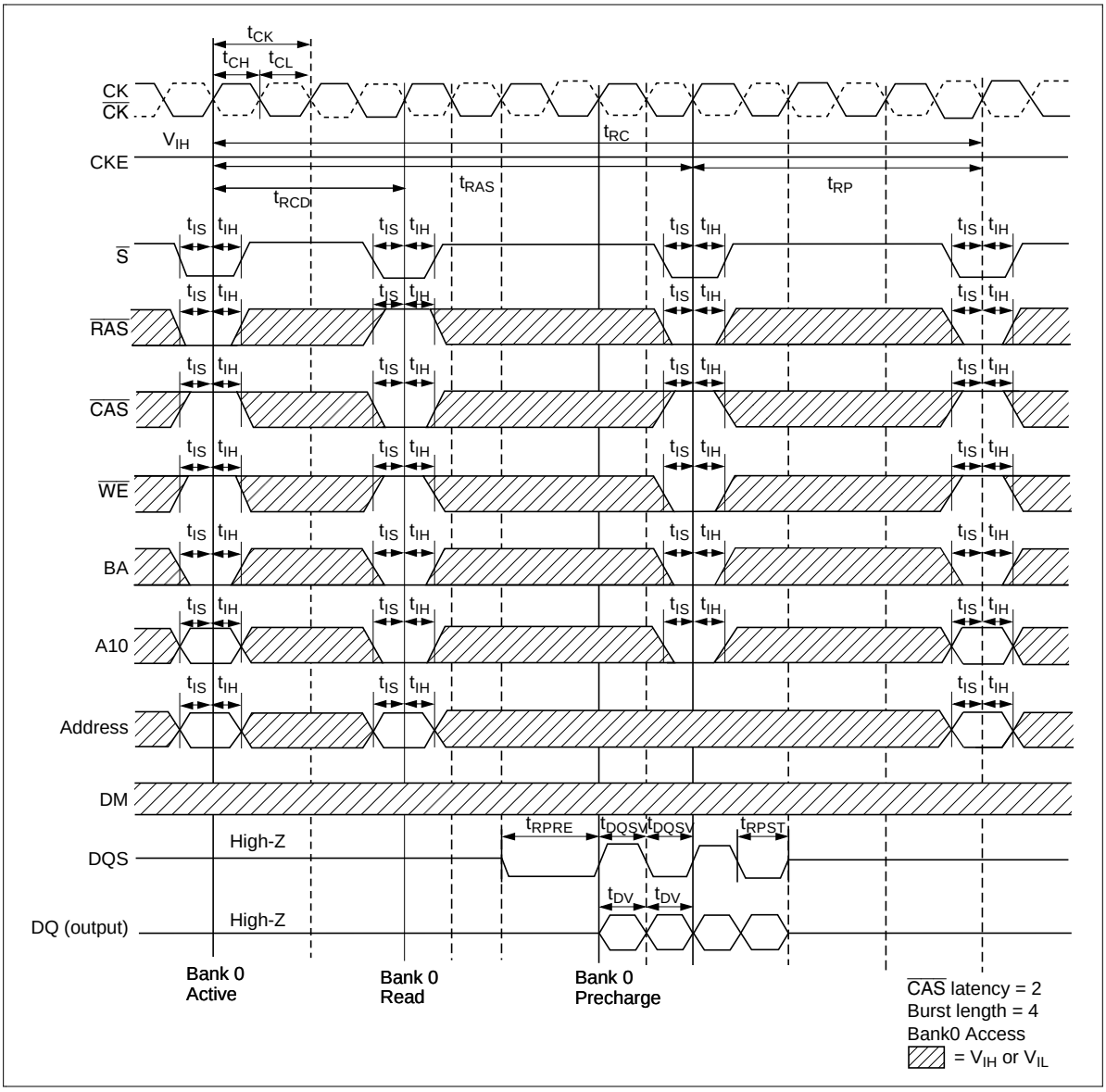
t_{DQSS}, t_{WPRES}, t_{WPREH}, t_{WPST}, t_{DQSH}, t_{DQSL}



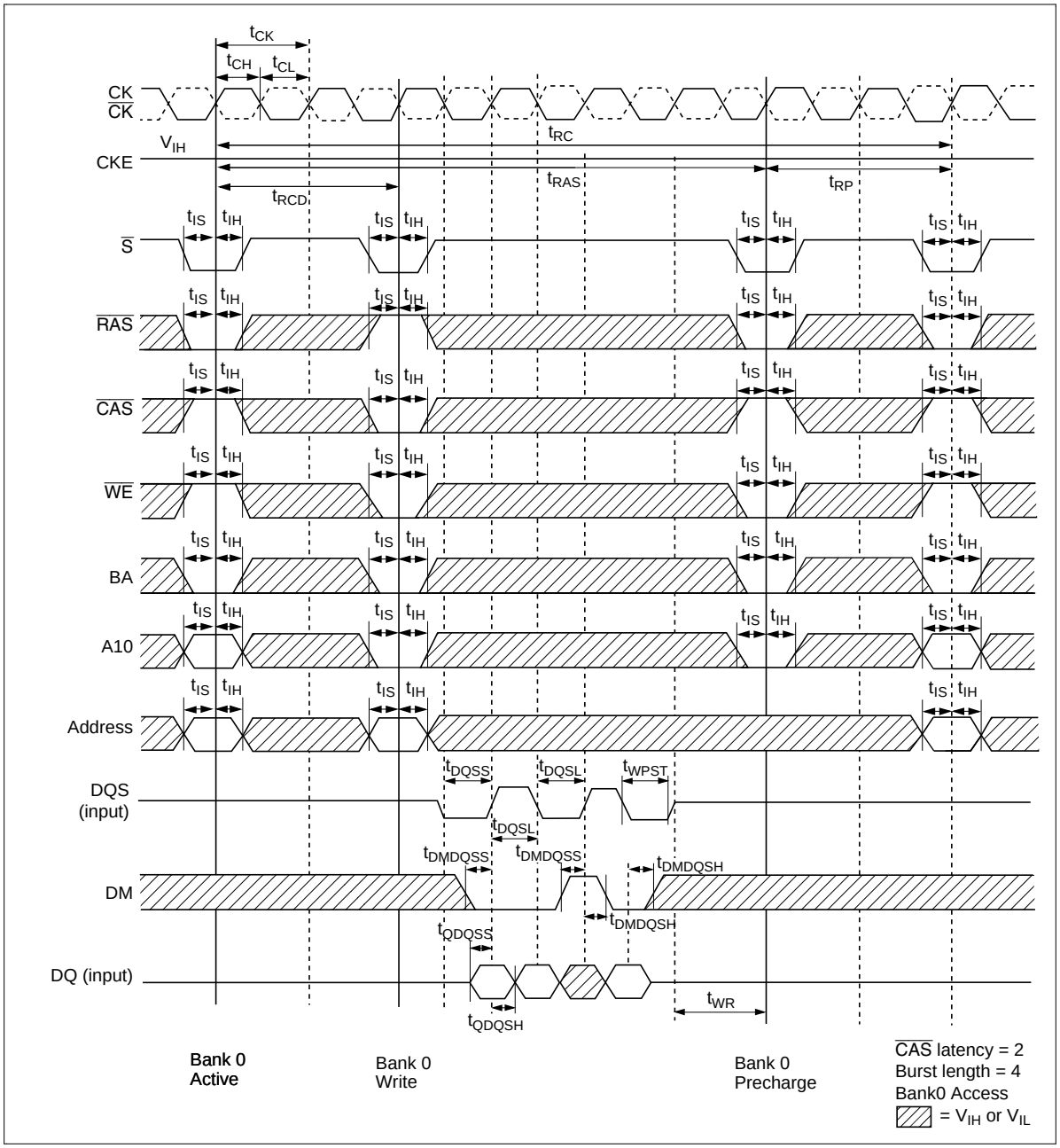
t_{DMDQSS}, t_{DMDQSH}, t_{QDQSS}, t_{QDQSH}



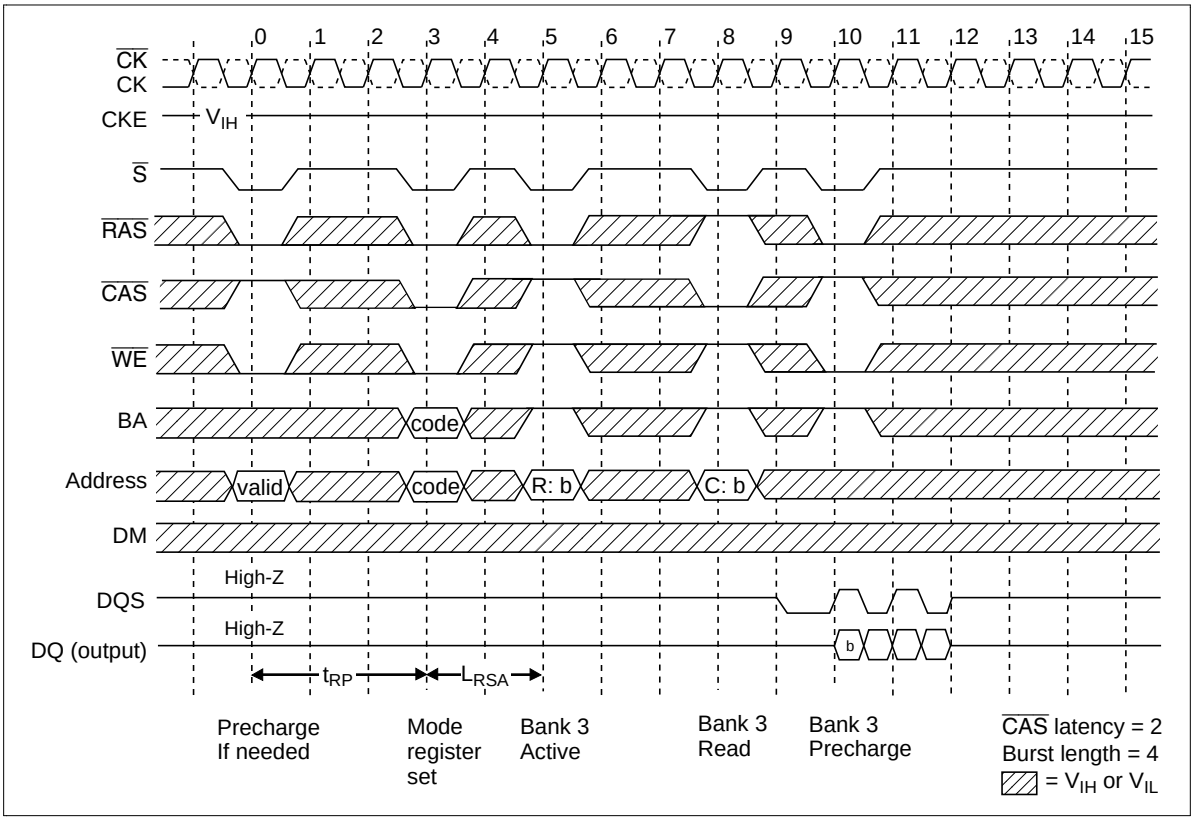
Read Cycle


tCK
tCH
tCL
CK
CK
VIH
tRC
CKE
tRAS
tRP
tRCD
tIS
tIH
S
RAS
CAS
WE
BA
A10
Address
DM
tRPRE
tDQSV
tDQSV
tRPST
High-Z
DQS
tDV
tDV
High-Z
DQ (output)
Bank 0
Active
Bank 0
Read
Bank 0
Precharge
CAS latency = 2
Burst length = 4
Bank0 Access
= VIH or VIL

Write Cycle

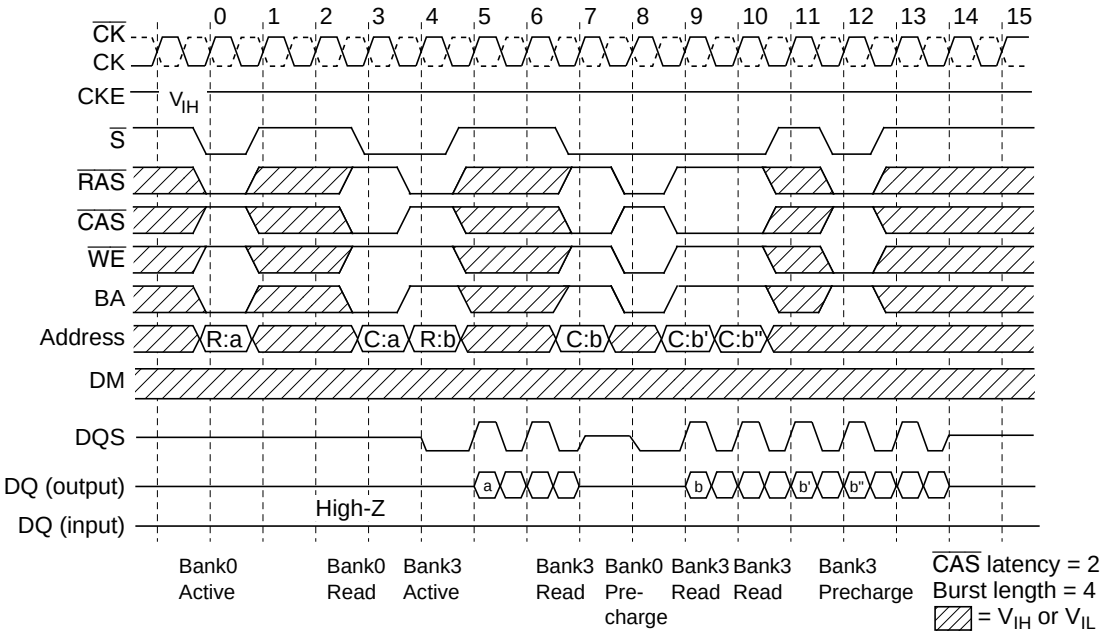

tCK
tCH
tCL
CK
CK
VIH
CKE
tRC
tRAS
tRP
tRCD
S
RAS
CAS
WE
BA
A10
Address
tIS
tIH
DQS
(input)
tDQSS
tDQSL
tWPST
DM
tDMDQSS
tDMDQSH
DQ (input)
tQDQSS
tQDQSH
tWR
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
CAS latency = 2
Burst length = 4
Bank0 Access
= VIH or VIL

Mode Register Set Cycle

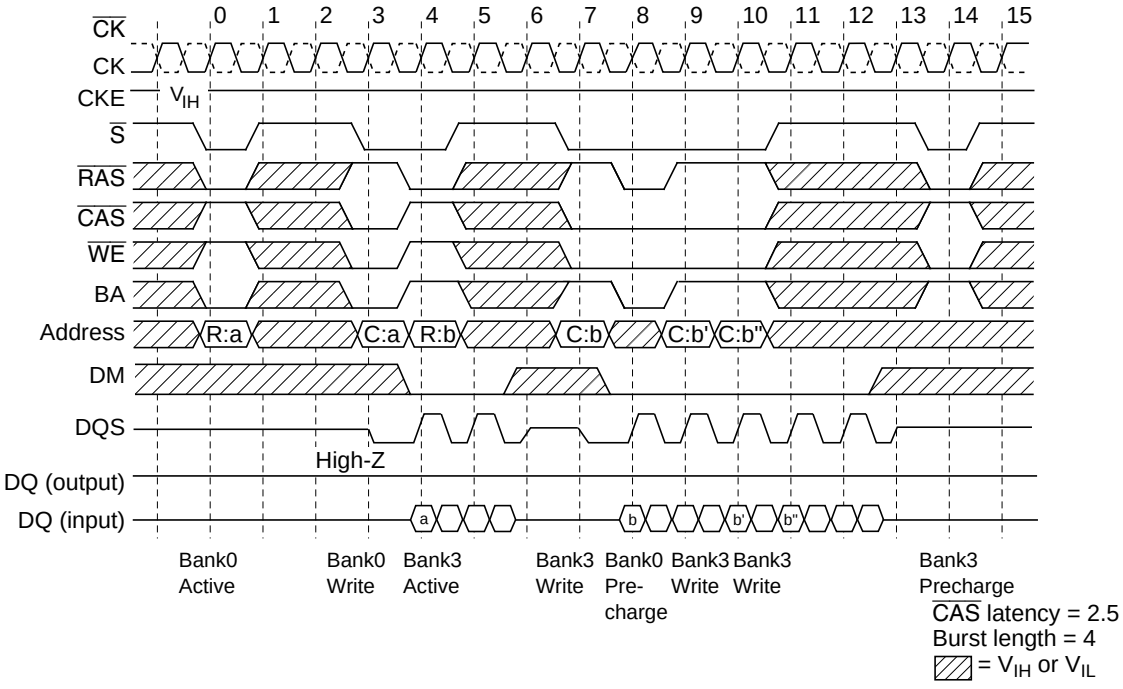


Read Cycle/Write Cycle

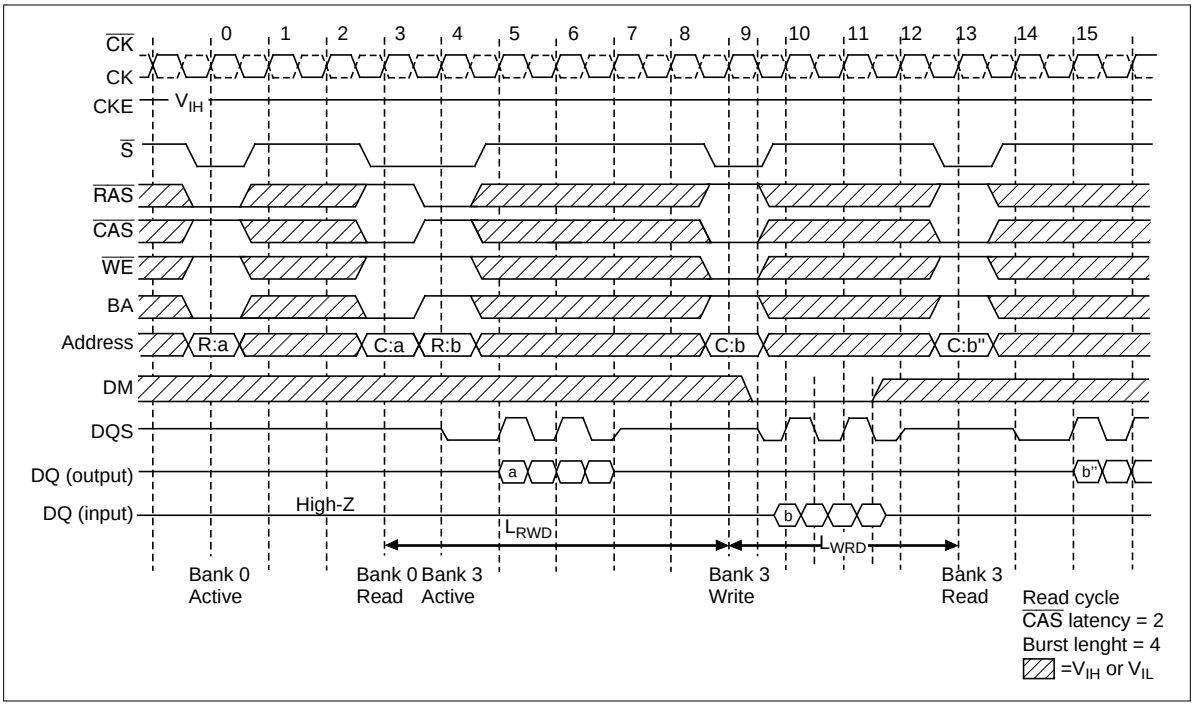
Read Cycle



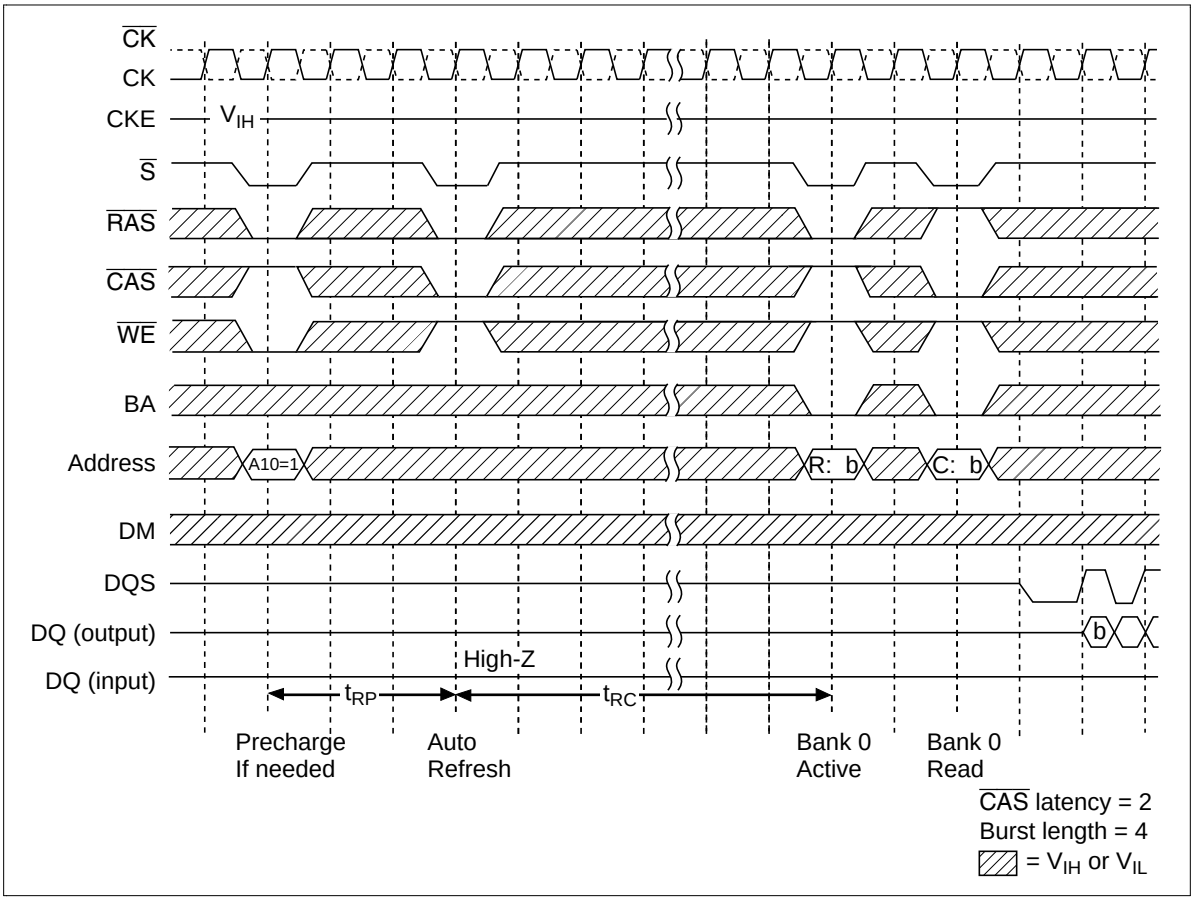
Write Cycle



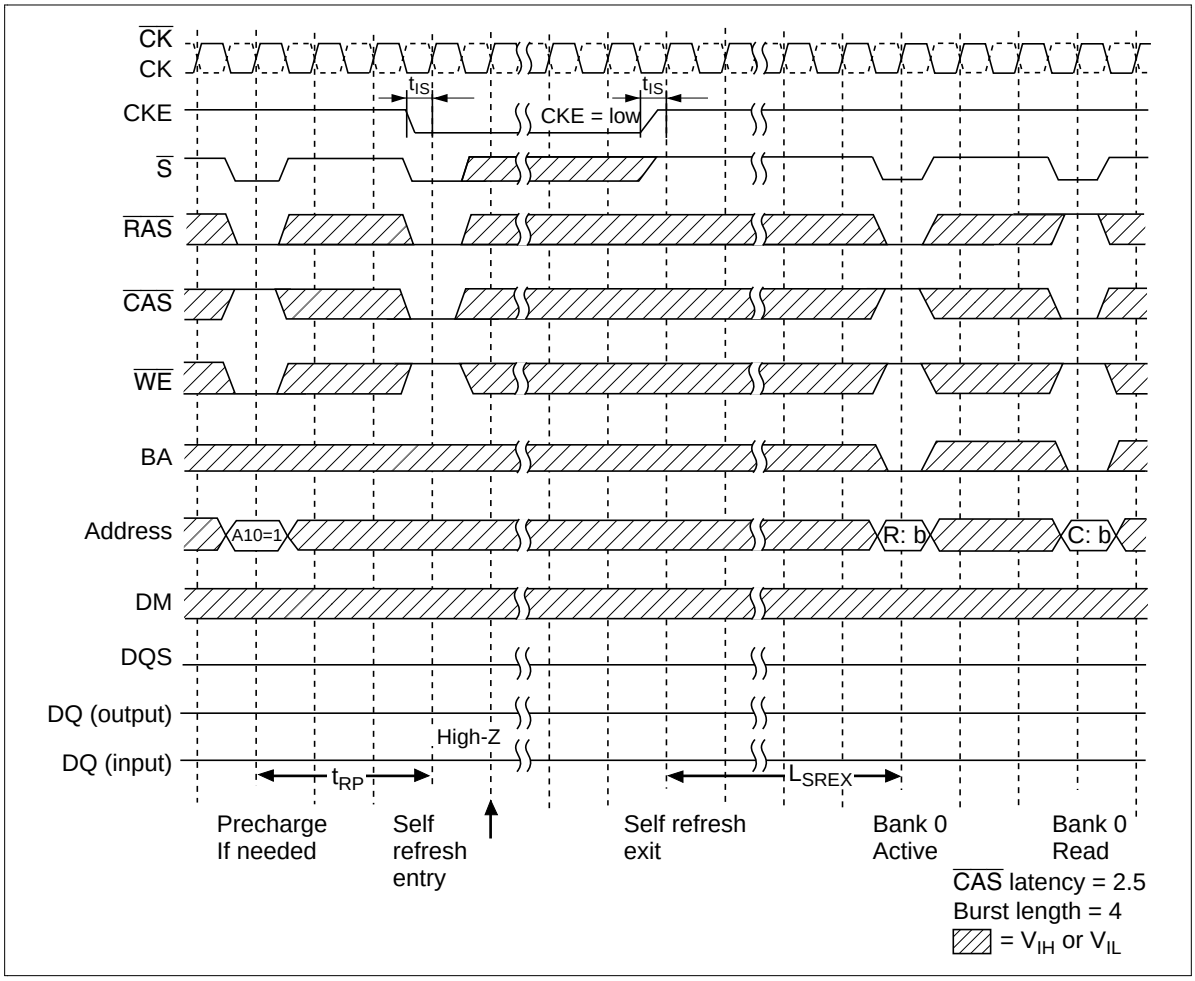
Read/Write Cycle



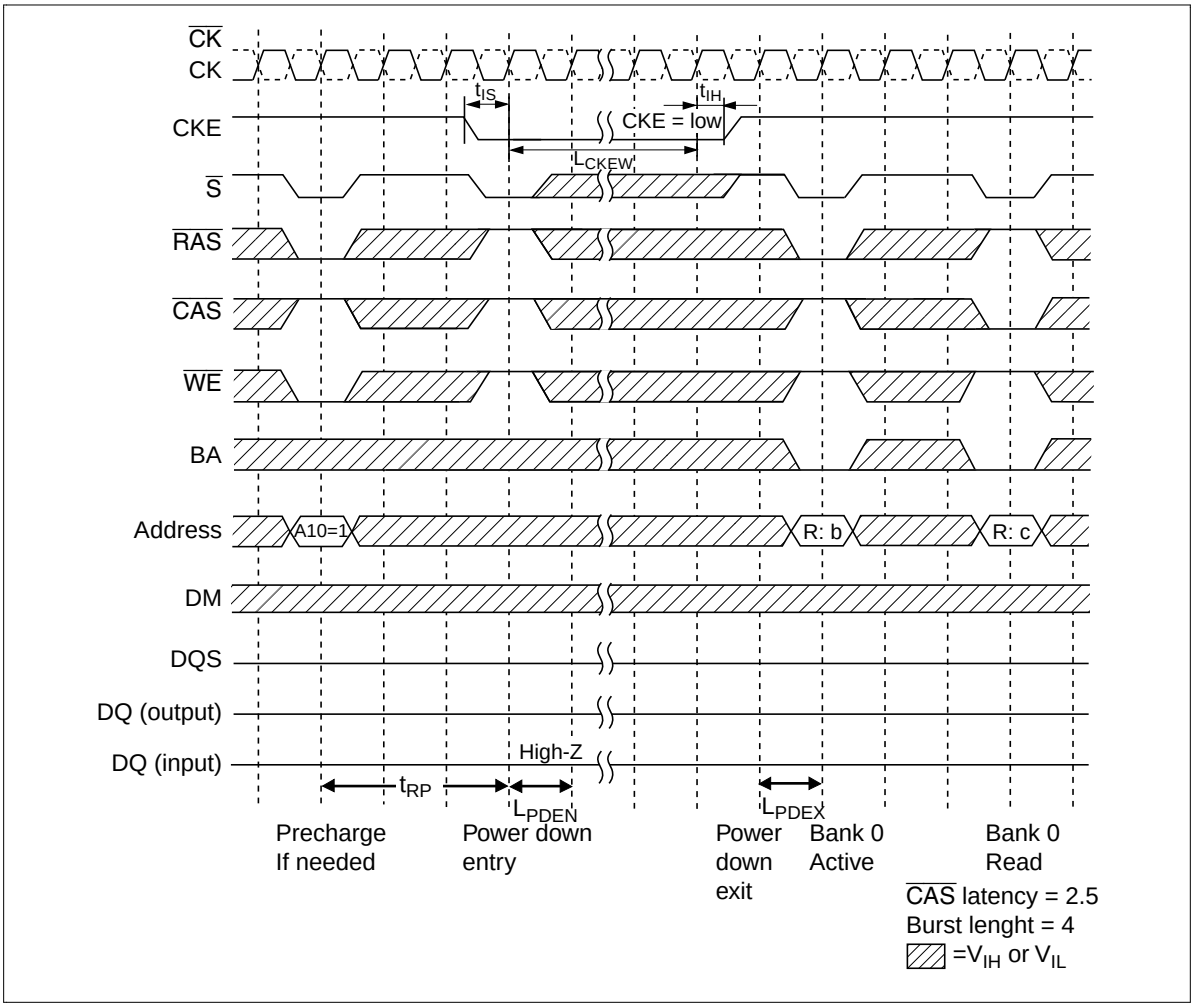
Auto Refresh Cycle



Self Refresh Cycle

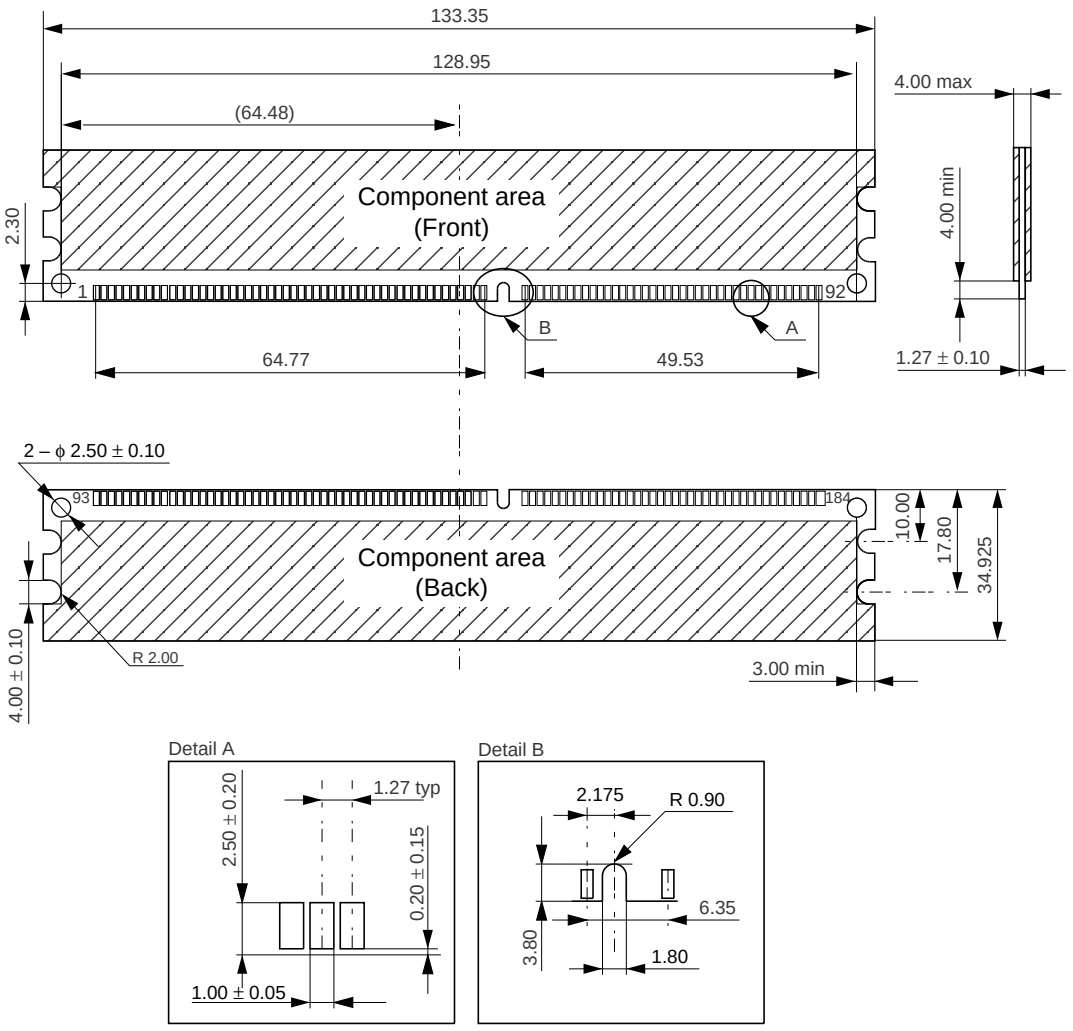


Power Down Mode



Physical Outline

Unit: mm



Note: Tolerance on all dimensions ± 0.13 unless otherwise specified.

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Aug. 7, 1998	Initial issue (referred to HM5464161D/HM5464801D/HM5464401D rev 0.1)		