HM5164160 Series
HM5165160 Series

64 M FP DRAM (4-Mword × 16-bit)
8 k Refresh/4 k Refresh

HITACHI

ADE-203-810B (Z)
Rev. 1.0
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Description

The Hitachi HM5164160 Series, HM5165160 Series are 64M-bit dynamic RAMs organized as 4,194,304-word × 16-bit. They have realized high performance and low power by employing CMOS process technology. HM5164160 Series, HM5165160 Series offer Fast Page Mode as a high speed access mode. They are packaged in standard 50-pin plastic TSOPII.

Features

- Single 3.3 V supply: 3.3 V ± 0.3 V
- Access time: 50 ns/60 ns (max)
- Power dissipation
  - Active: 432 mW/396 mW (max) (HM5164160 Series)
    : 504 mW/432 mW (max) (HM5165160 Series)
  - Standby: 1.8 mW (max) (CMOS interface)
    : 0.54 mW (max) (L-version)
- Fast page mode capability
- Refresh cycles
  - $\overline{\text{RAS}}$-only refresh
    8192 cycles /64 ms (HM5164160)
    /128 ms (HM5164160L) (L-version)
    4096 cycles /64 ms (HM5165160)
    /128 ms (HM5165160L) (L-version)
  - CBR/Hidden refresh
    4096 cycles /64 ms (HM5164160, HM5165160)
    /128 ms (HM5164160L, HM5165160L) (L-version)
-

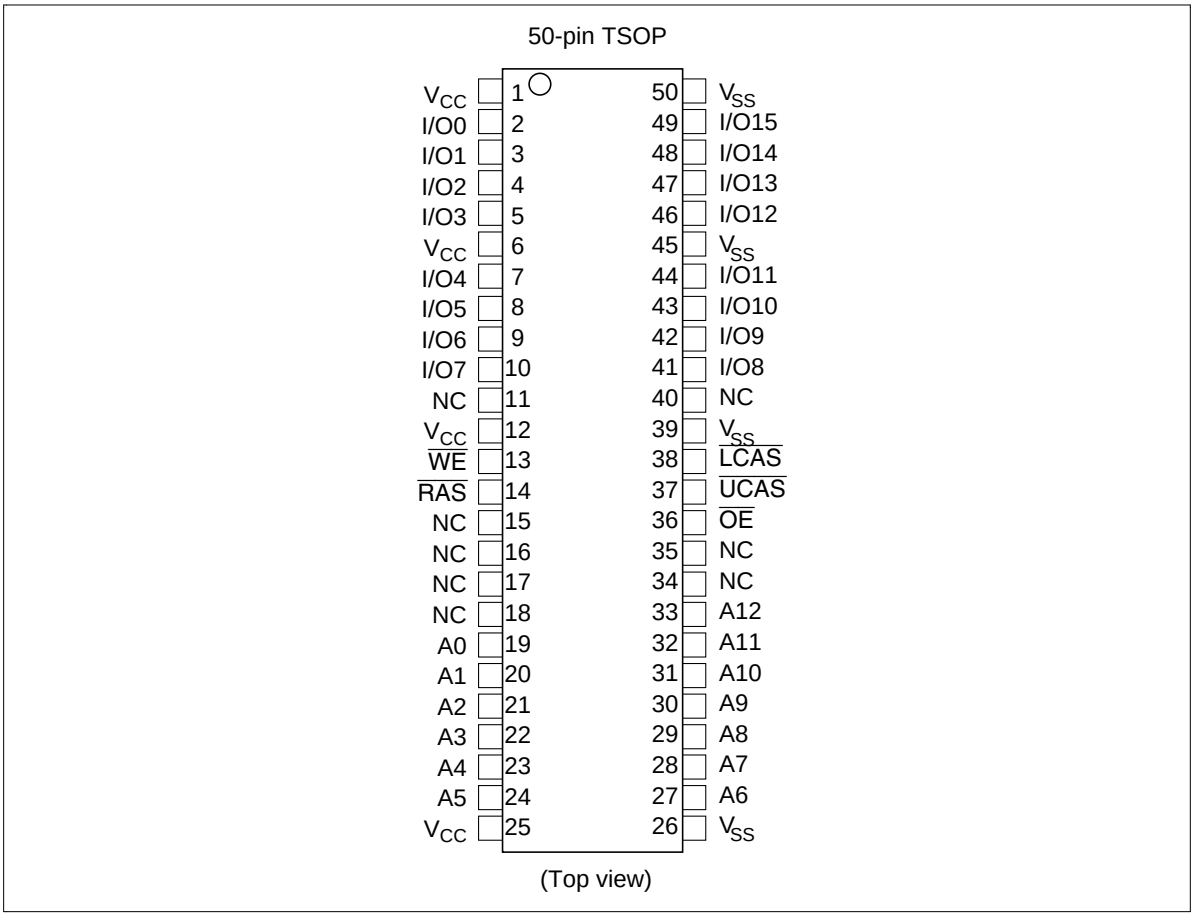
4 variations of refresh
- — $\overline{\text{RAS}}$-only refresh
- — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- — Hidden refresh
- — Self refresh (L-version)

- 2$\overline{\text{CAS}}$-byte control
- Battery backup operation (L-version)

Ordering Information

Type No.	Access time	Package
HM5164160TT-5	50 ns	400-mil 50-pin plastic TSOP II (TTP-50DB)
HM5164160TT-6	60 ns	
HM5164160LTT-5	50 ns	
HM5164160LTT-6	60 ns	
HM5165160TT-5	50 ns	
HM5165160TT-6	60 ns	
HM5165160LTT-5	50 ns	
HM5165160LTT-6	60 ns	

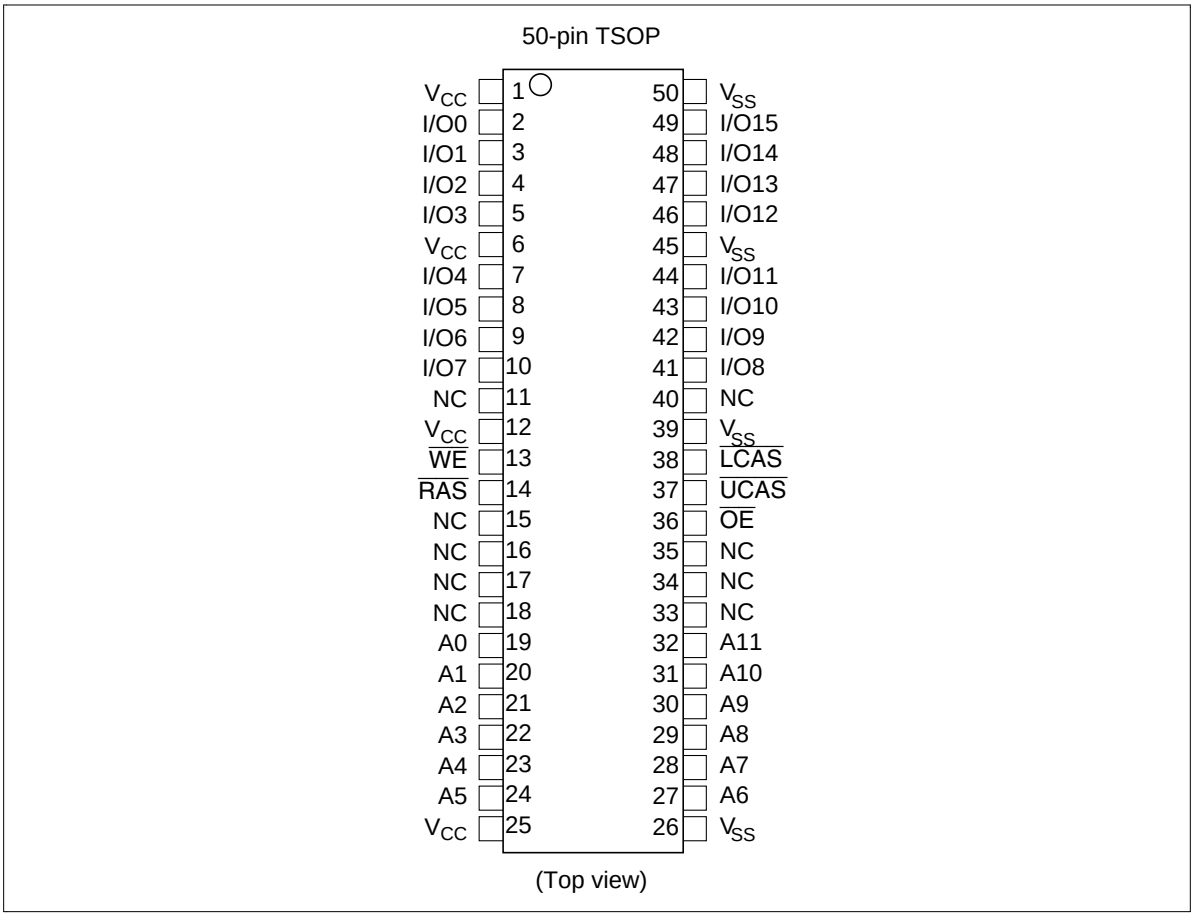
Pin Arrangement (HM5164160 Series)



Pin Description

Pin name	Function
A0 to A12	Address input — Row/Refresh address A0 to A12 — Column address A0 to A8
I/O0 to I/O15	Data input/output
$\overline{RAS}$	Row address strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{cc}	Power supply
V_{ss}	Ground
NC	No connection

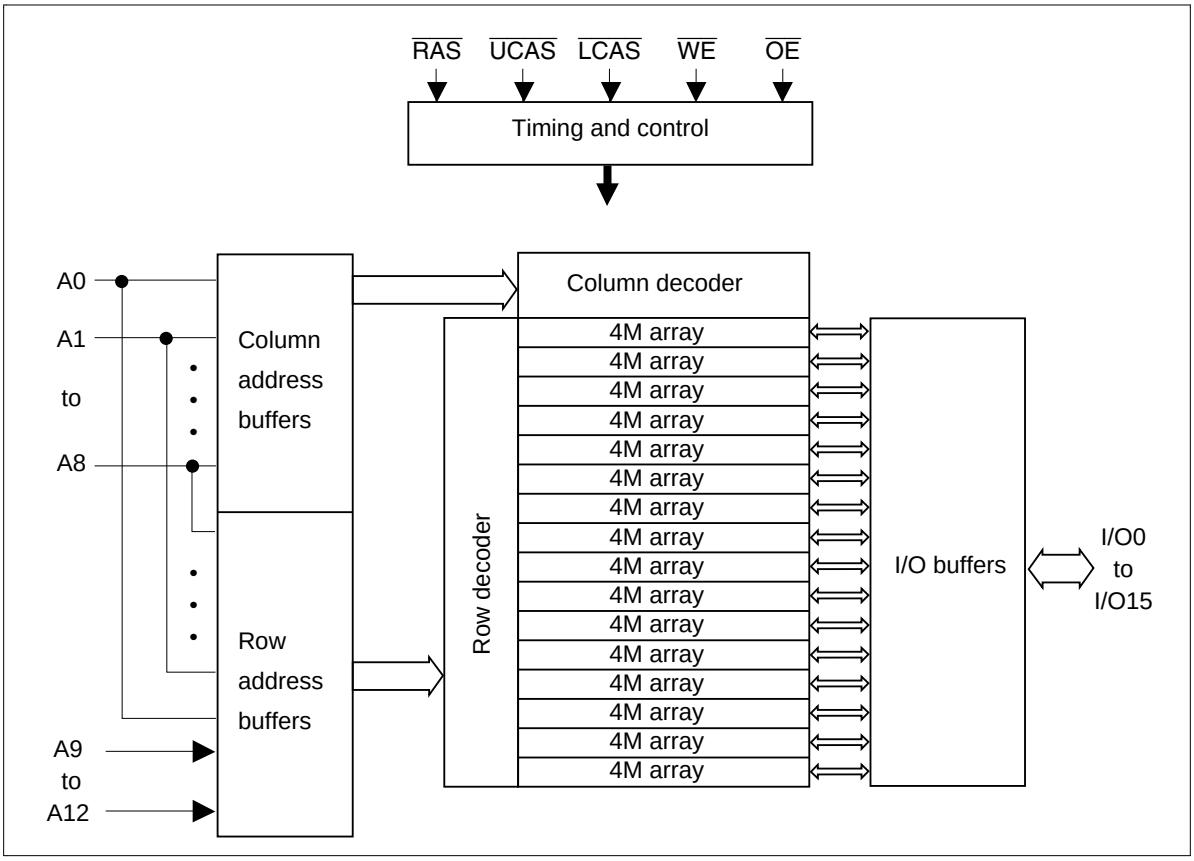
Pin Arrangement (HM5165160 Series)



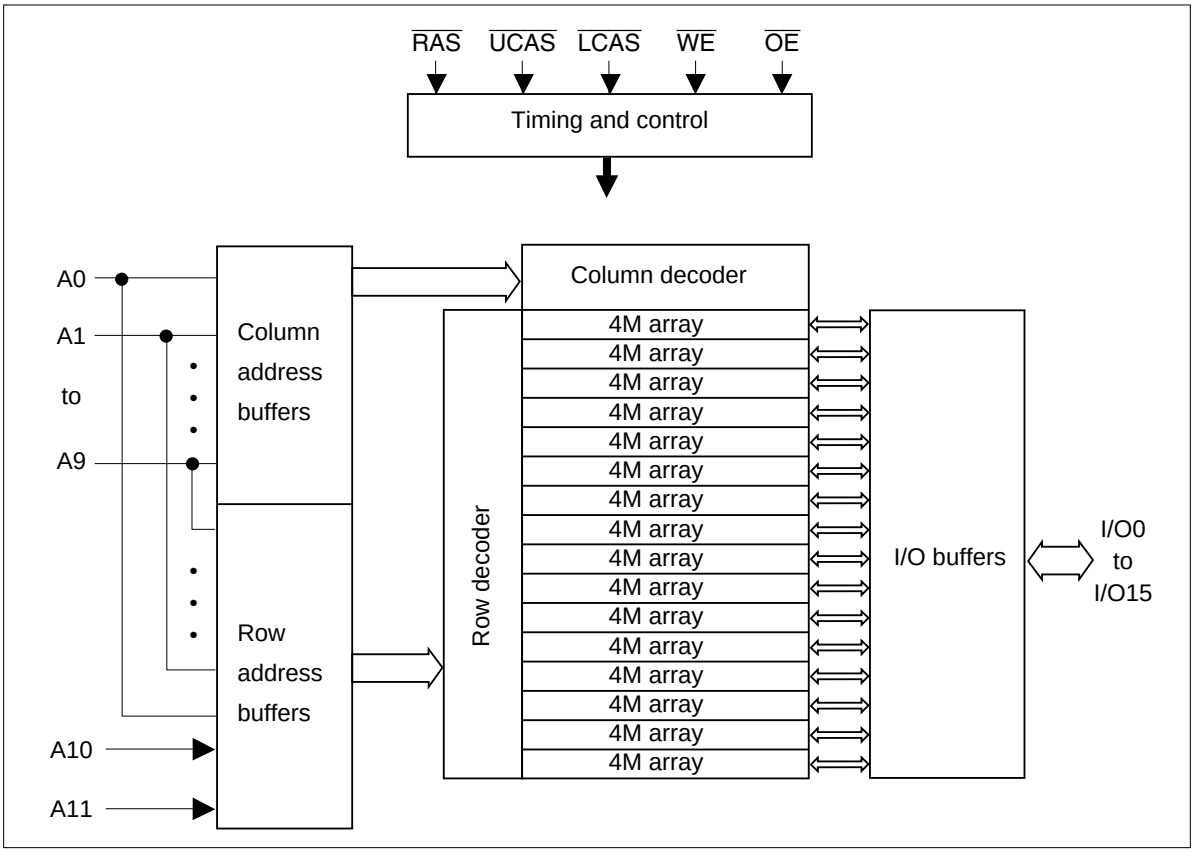
Pin Description

Pin name	Function
A0 to A11	Address input — Row/Refresh address A0 to A11 — Column address A0 to A9
I/O0 to I/O15	Data input/output
$\overline{RAS}$	Row address strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram (HM5164160 Series)



Block Diagram (HM5165160 Series)



Operation Table

RAS	LCAS	UCAS	WE	OE	I/O 0 to I/O 7	I/O 8 to I/O 15	Operation
H	×	×	×	×	High-Z	High-Z	Standby
L	L	H	H	L	Dout	High-Z	Read cycle
L	H	L	H	L	High-Z	Dout	
L	L	L	H	L	Dout	Dout	
L	L	H	L*[2]	×	Din	×	Early write cycle
L	H	L	L*[2]	×	×	Din	
L	L	L	L*[2]	×	Din	Din	
L	L	H	L*[2]	H	Din	×	Delayed write cycle
L	H	L	L*[2]	H	×	Din	
L	L	L	L*[2]	H	Din	Din	
L	L	H	H to L	L to H	Dout/Din	High-Z	Read-modify-write cycle
L	H	L	H to L	L to H	High-Z	Dout/Din	
L	L	L	H to L	L to H	Dout/Din	Dout/Din	
L	H	H	×	×	High-Z	High-Z	$\overline{\text{RAS}}$-only refresh cycle
H to L	H	L	H	×	High-Z	High-Z	$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle or
H to L	L	H	H	×	High-Z	High-Z	Self refresh cycle (L-version)
H to L	L	L	H	×	High-Z	High-Z	
L	L	L	H	H	High-Z	High-Z	Read cycle (Output disabled)

Notes: 1. H: V_{IH} (inactive) L: V_{IL} (active) ×: V_{IH} or V_{IL}

2. $t_{WCS} \geq 0$ ns: Early write cycle
   $t_{WCS} < 0$ ns: Delayed write cycle
3. Mode is determined by the OR function of the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$. (Mode is set by the earliest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ active edge and reset by the latest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ inactive edge.) However write operation and output High-Z control are done independently by each $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$.
   ex. if $\overline{\text{RAS}}$ = H to L, $\overline{\text{LCAS}}$ = L, $\overline{\text{UCAS}}$ = H, then $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle is selected.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5 to V_{CC} + 0.5 (≤ 4.6 V (max))	V
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Storage temperature	Tstg	–55 to +125	°C

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
	V_{SS}	0	0	0	V	2
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1
Ambient temperature range	Ta	0	—	70	˚C	

Notes: 1. All voltage referred to V_{SS}.

2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (HM5164160 Series)

		HM5164160					
		–5		–6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	120	—	110	mA	t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IH} Dout = High-Z
		—	0.5	—	0.5	mA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	150	—	150	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	120	—	110	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{UCAS}$, $\overline{LCAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	120	—	110	mA	t_{RC} = min
Fast page mode current*1, *3	I_{CC7}	—	100	—	90	mA	$\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycle, t_{PC} = t_{PC} min
Battery backup current*4 (Standby with CBR refresh) (L-version)	I_{CC10}	—	500	—	500	µA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 31.3 µs t_{RAS} ≤ 0.3 µs
Self refresh mode current (L-version)	I_{CC11}	—	400	—	400	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≤ 0.2 V Dout = High-Z
Input leakage current	I_{LI}	–5	5	–5	5	µA	0 V ≤ Vin ≤ V_{CC} + 0.3 V
Output leakage current	I_{LO}	–5	5	–5	5	µA	0 V ≤ Vout ≤ V_{CC} Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Measured with one sequential address change per fast page mode cycle, t_{PC}.
4. V_{IH} ≥ V_{CC} – 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

DC Characteristics (HM5165160 Series)

		HM5165160					
		–5		–6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	140	—	120	mA	t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IH} Dout = High-Z
		—	0.5	—	0.5	mA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	150	—	150	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	140	—	120	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{UCAS}$, $\overline{LCAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	140	—	120	mA	t_{RC} = min
Fast page mode current*1, *3	I_{CC7}	—	100	—	90	mA	$\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycle, t_{PC} = t_{PC} min
Battery backup current*4 (Standby with CBR refresh) (L-version)	I_{CC10}	—	500	—	500	µA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 31.3 µs t_{RAS} ≤ 0.3 µs
Self refresh mode current (L-version)	I_{CC11}	—	400	—	400	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≤ 0.2 V Dout = High-Z
Input leakage current	I_{LI}	–5	5	–5	5	µA	0 V ≤ Vin ≤ V_{CC} + 0.3 V
Output leakage current	I_{LO}	–5	5	–5	5	µA	0 V ≤ Vout ≤ V_{CC} Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Measured with one sequential address change per fast page mode cycle, t_{PC}.
4. V_{IH} ≥ V_{CC} – 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	—	7	pF	1, 2

Notes :1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{RAS}$, $\overline{UCAS}$ and $\overline{LCAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) *1, *2, *19, *24

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5164160/HM5165160					
		–5		–6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	90	—	110	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	—	10	—	ns	28
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10000	15	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	25
Column address hold time	t_{CAH}	8	—	10	—	ns	25
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	37	20	45	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	15	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	50	—	60	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	26
$\overline{OE}$ to Din delay time	t_{OED}	13	—	15	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	7

Read Cycle

		HM5164160/HM5165160					
		–5		–6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	15	ns	9, 10, 17
Access time from address	t_{AA}	—	25	—	30	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	13	—	15	ns	9
Read command setup time	t_{RCS}	0	—	0	—	ns	25
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	12, 26
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	—	30	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	25	—	30	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	ns	13
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	13	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	13	—	15	—	ns	5

Write Cycle

		HM5164160/HM5165160					
		–5		–6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	14, 25
Write command hold time	t_{WCH}	8	—	10	—	ns	25
Write command pulse width	t_{WP}	8	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	—	15	—	ns	27
Data-in setup time	t_{DS}	0	—	0	—	ns	15, 27
Data-in hold time	t_{DH}	8	—	10	—	ns	15, 27

Read-Modify-Write Cycle

		HM5164160/HM5165160					
		–5		–6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	131	—	155	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	73	—	85	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	36	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	48	—	55	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	13	—	15	—	ns	

Refresh Cycle

		HM5164160/HM5165160					
		–5		–6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	25
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	8	—	10	—	ns	26
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	8	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	ns	25

Fast Page Mode Cycle

		HM5164160/HM5165160					
		–5		–6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode cycle time	t_{PC}	35	—	40	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	30	—	35	ns	9, 17, 26
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	30	—	35	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HM5164160/HM5165160					
		–5		–6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode read-modify-write cycle time	t_{PRWC}	76	—	85	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	53	—	60	—	ns	14, 26

Refresh (HM5164160 Series)

Parameter	**Symbol**	**Max**	**Unit**	**Note**
Refresh period	t_{REF}	64	ms	8192 cycles
Refresh period (L-version)	t_{REF}	128	ms	8192 cycles

Refresh (HM5165160 Series)

Parameter	**Symbol**	**Max**	**Unit**	**Note**
Refresh period	t_{REF}	64	ms	4096 cycles
Refresh period (L-version)	t_{REF}	128	ms	4096 cycles

Self Refresh Mode (L-version)

		HM5164160L/HM5165160L					
		–5		–6			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	µs	23
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	90	—	110	—	ns	23
$\overline{CAS}$ hold time (self refresh)	t_{CHS}	–50	—	–50	—	ns	27

Notes: 1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.

7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{DS}, t_{DH} are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
20. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64 ms period on the condition a and b below.
    a. Enter self refresh mode within 15.6 µs after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
    b. Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6µs after exiting from self refresh mode.
21. In case of entering from $\overline{RAS}$-only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 20.
22. For L-version, it is available to apply each 128 ms and 31.2 µs instead of 64 ms and 15.6 µs at note 20.
23 At t_{RASS} > 100 µs, self refresh mode is activated, and not activated at t_{RASS} < 10 µs. It is undefined within the range of 10 µs $\leq t_{RASS} \leq$ 100 µs. For $t_{RASS} \geq$ 10 µs, it is necessary to satisfy t_{RPS}.
24. When both $\overline{UCAS}$ and $\overline{LCAS}$ go low at the same time, all 16-bit data are written into the device. $\overline{UCAS}$ and $\overline{LCAS}$ cannot be staggered within the same write/read cycles.
25. t_{ASC}, t_{CAH}, t_{RCS}, t_{WCS}, t_{WCH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
26. t_{CRP}, t_{CHR}, t_{RCH}, t_{CPA} and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
27. t_{CWL}, t_{DH}, t_{DS} and t_{CHS} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
28. t_{CP} is determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
29. XXX: H or L (H: V_{IH} (min) $\leq V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) $\leq V_{IN} \leq V_{IL}$ (max))

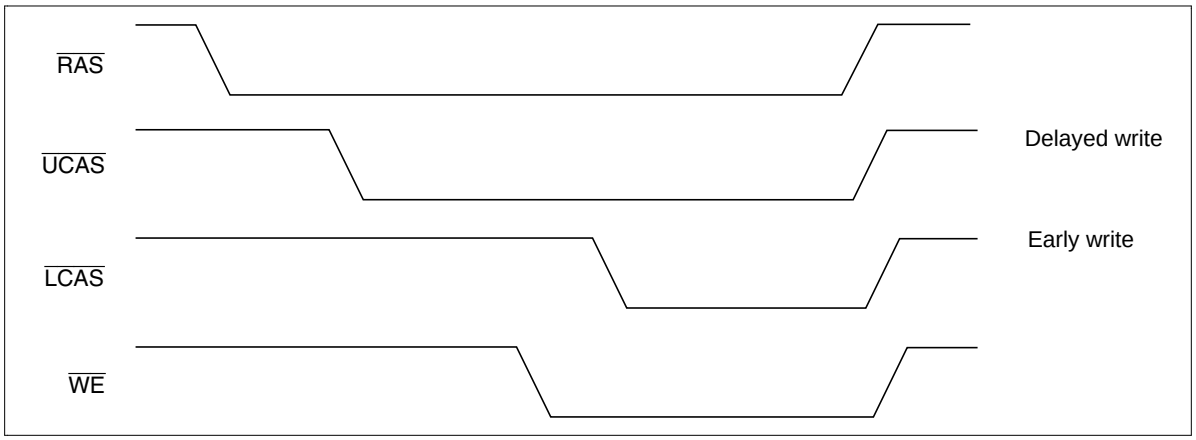
    ///////: Invalid Dout

    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

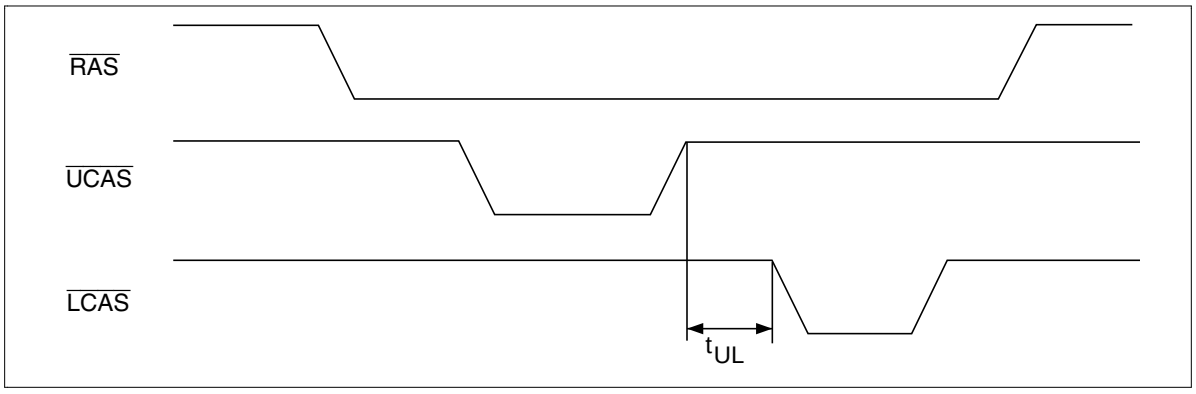
Notes concerning 2$\overline{CAS}$ control

Please do not separate the $\overline{UCAS}$/$\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}$/$\overline{LCAS}$ are allowed under the following conditions.

1. Each of the $\overline{UCAS}$/$\overline{LCAS}$ should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.



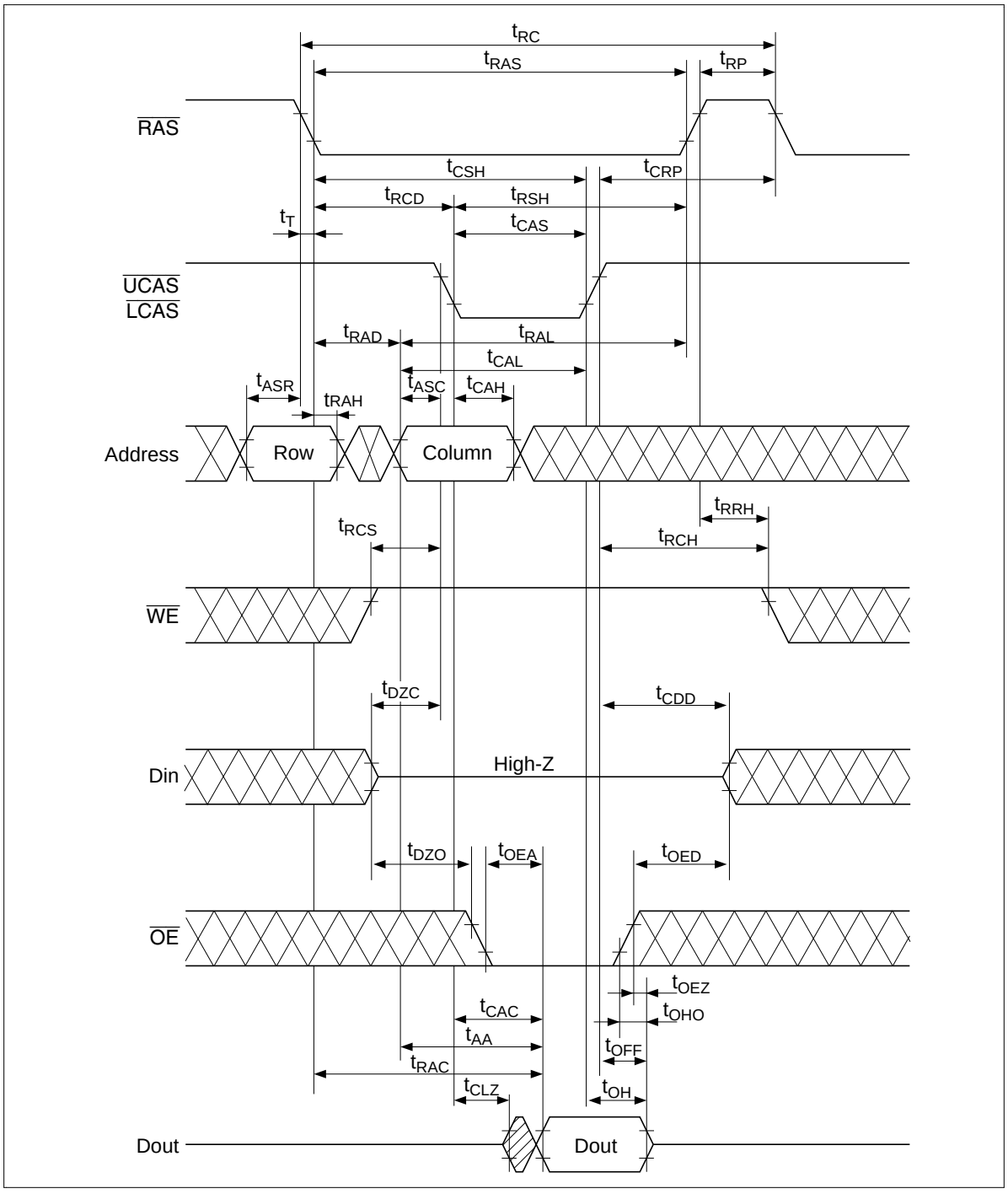
3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, Fast page mode can be performed.



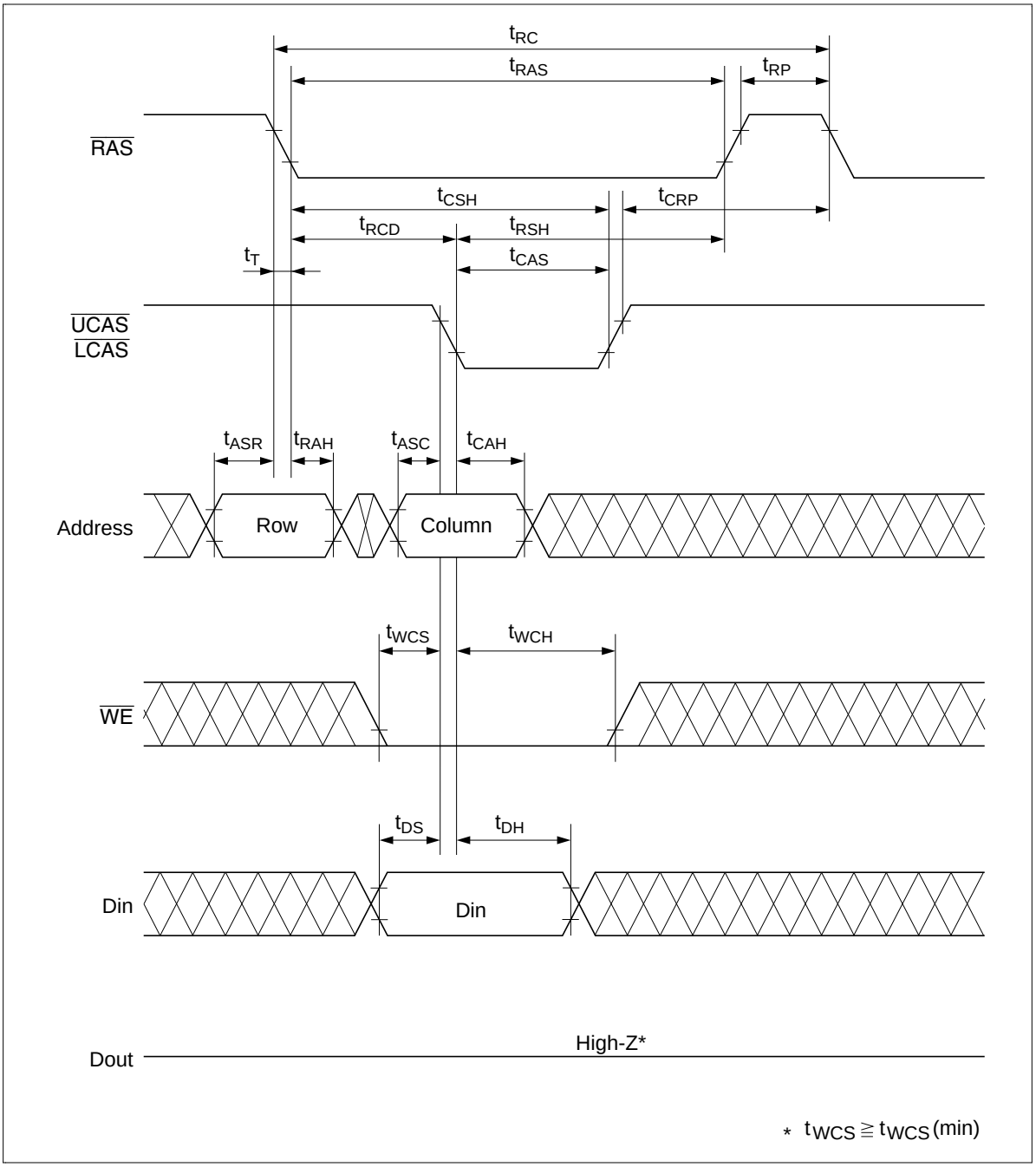
4. Byte control operation by remaining $\overline{UCAS}$ or $\overline{LCAS}$ high is guaranteed.

Timing Waveforms*[29]

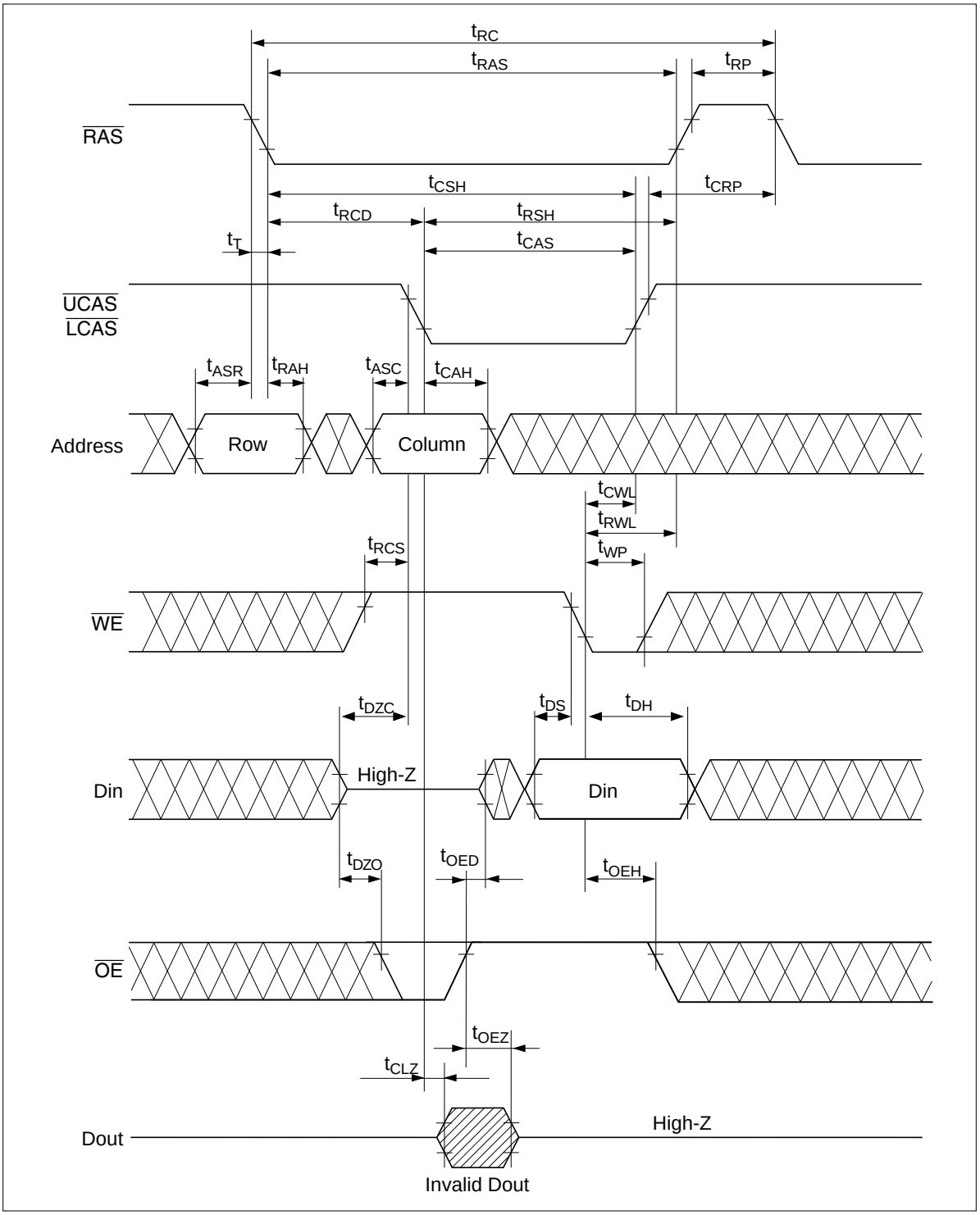
Read Cycle



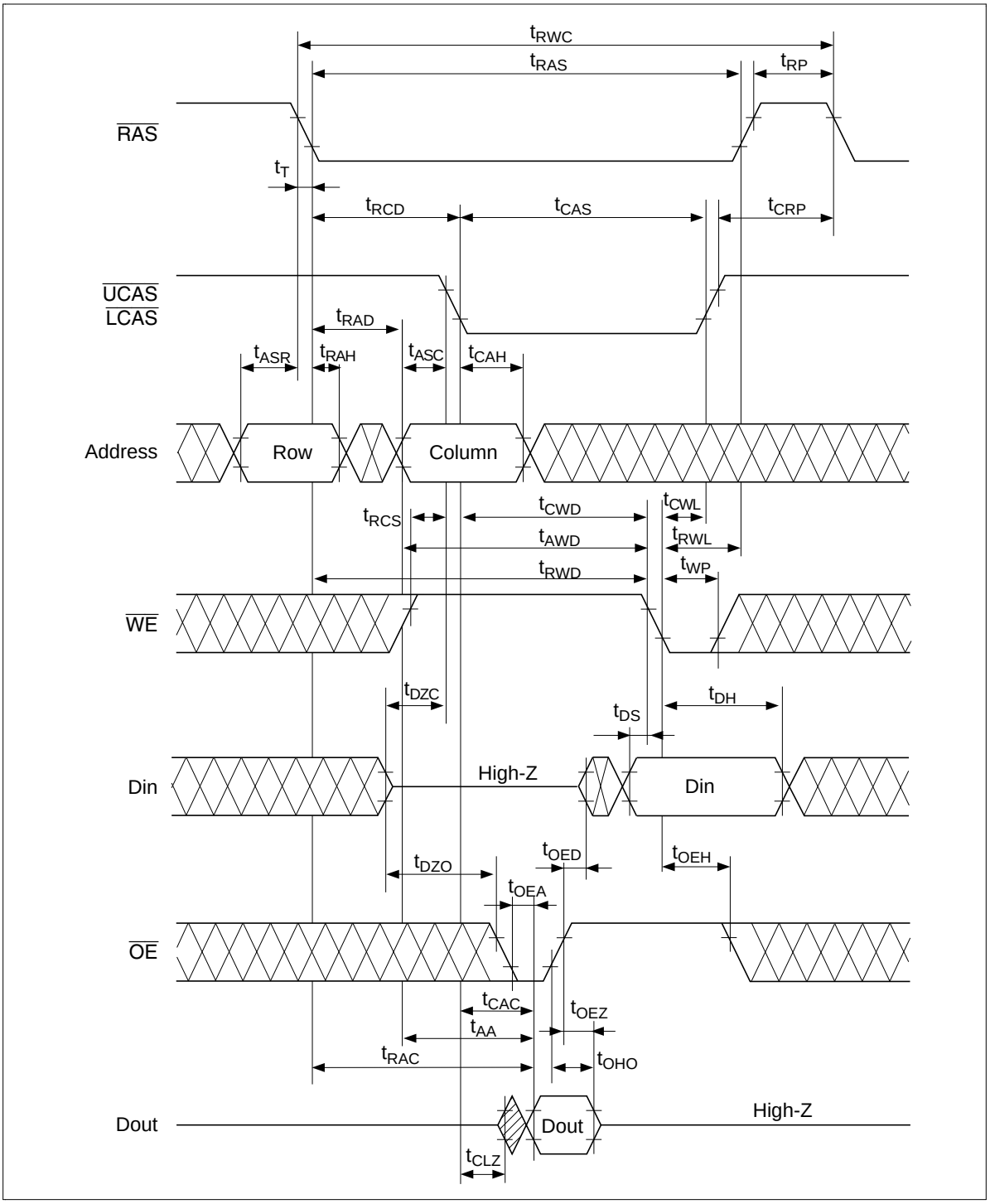
Early Write Cycle



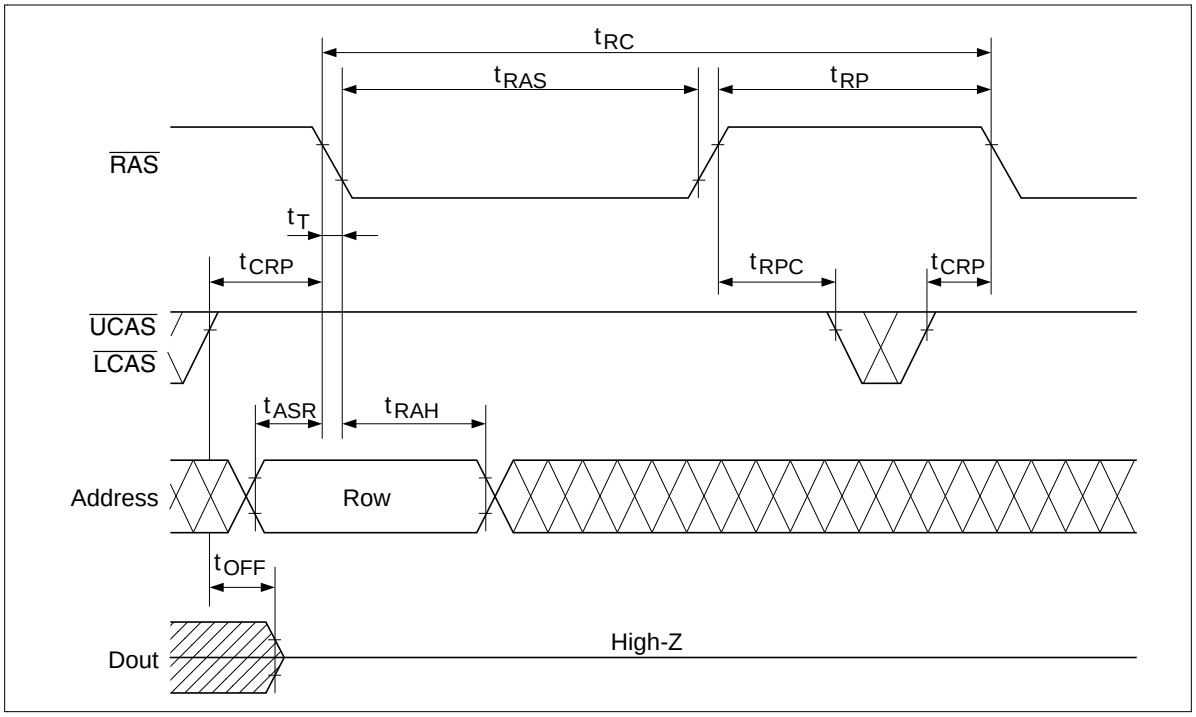
Delayed Write Cycle*[18]



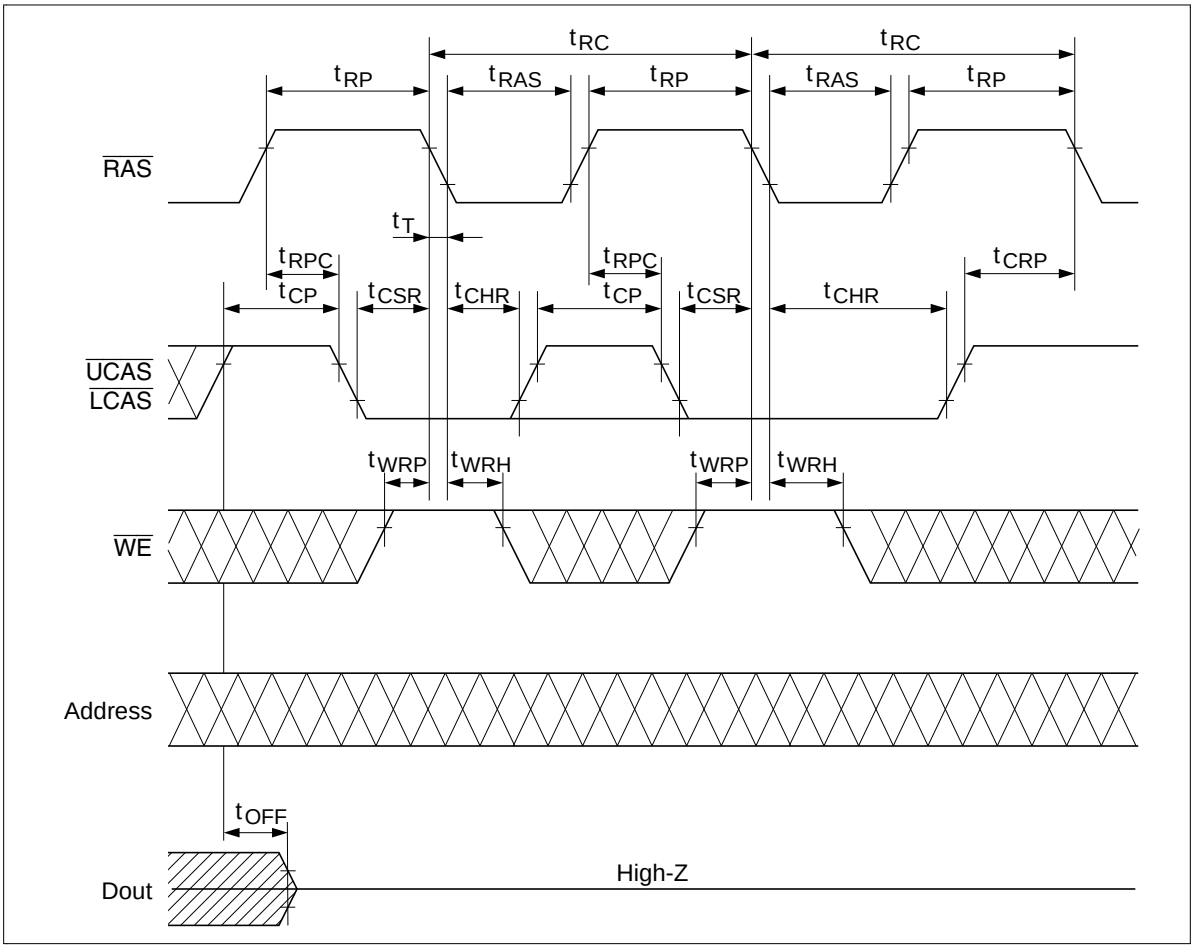
Read-Modify-Write Cycle*[18]



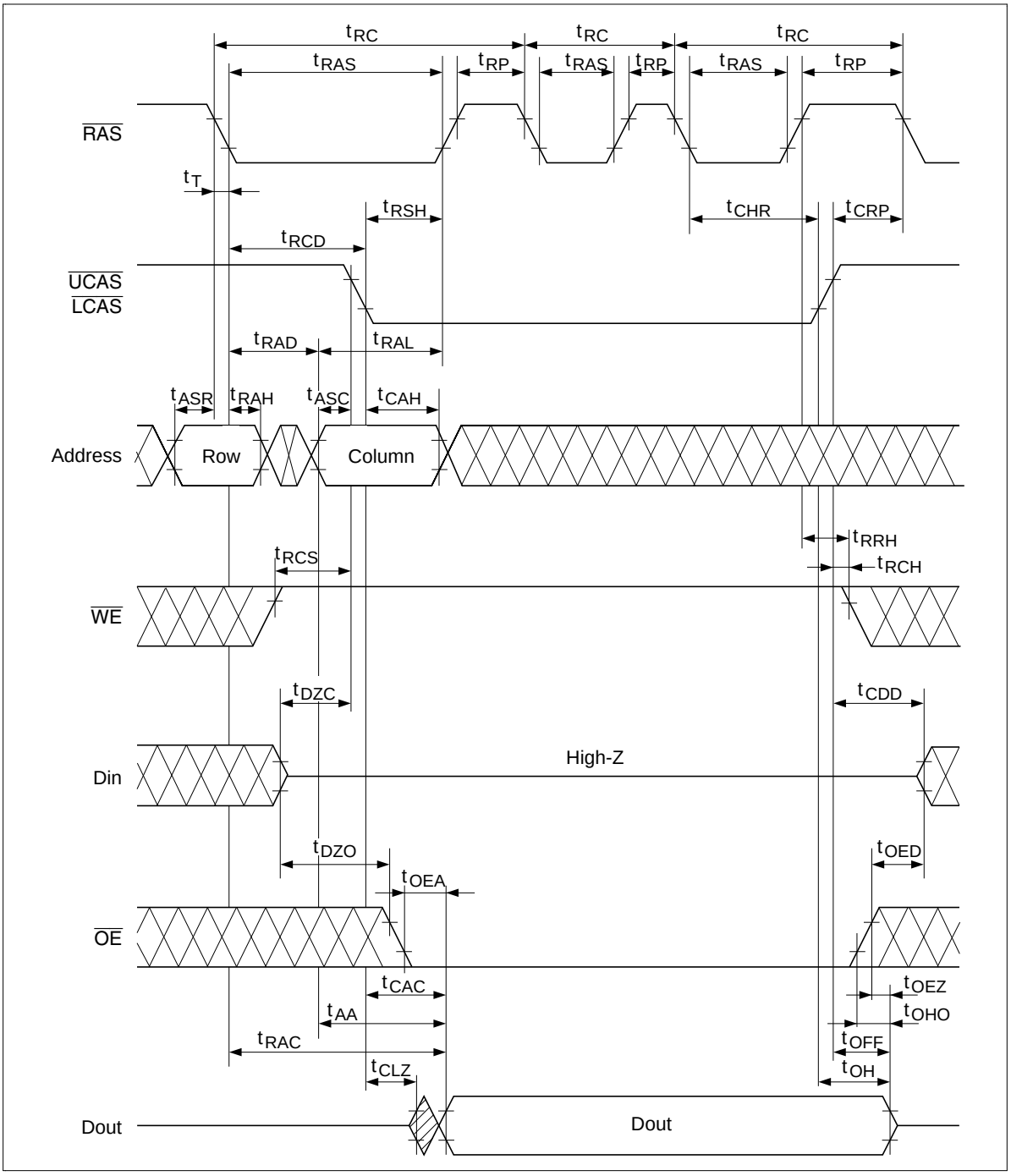
$\overline{\text{RAS}}$-Only Refresh Cycle



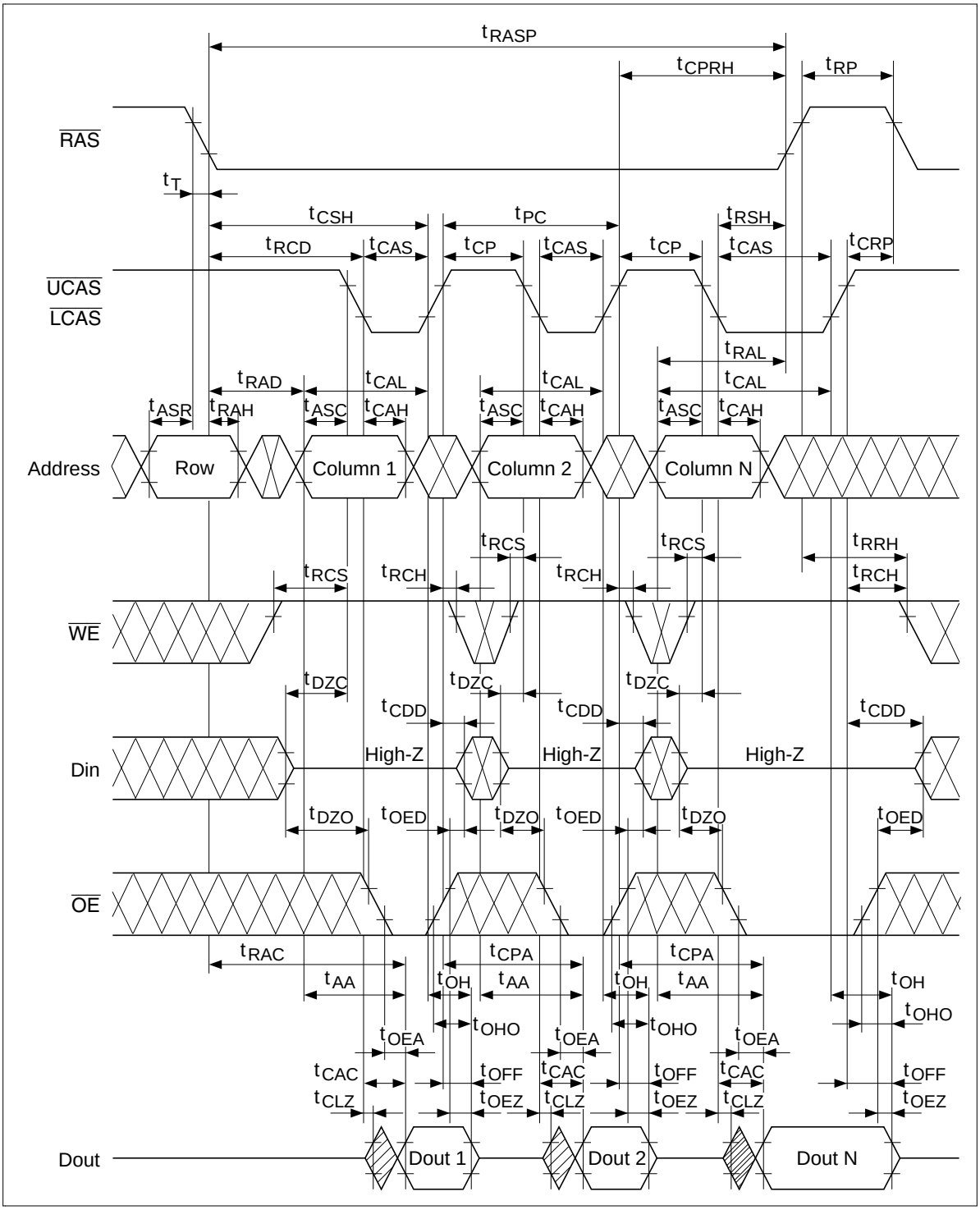
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



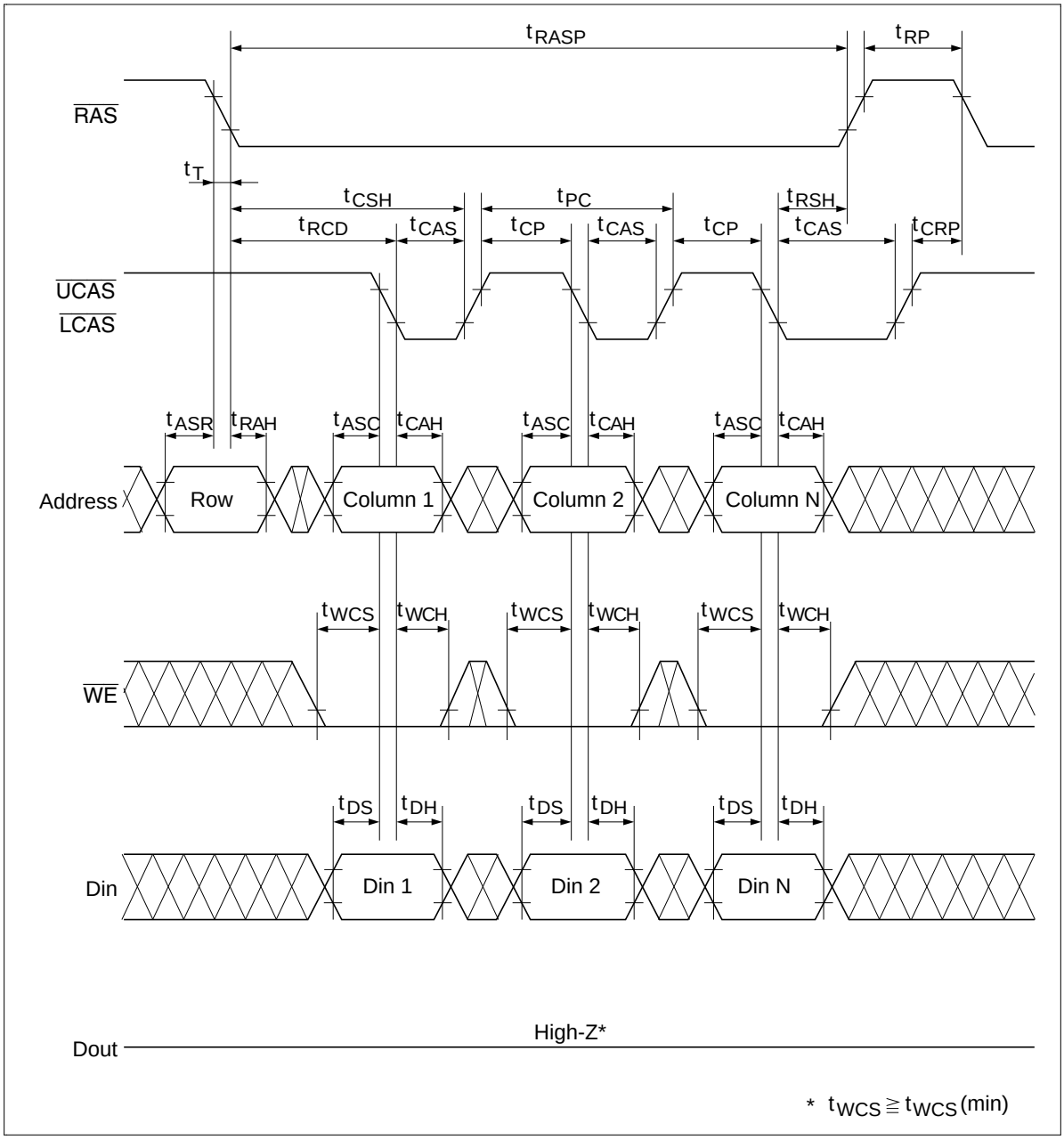
Hidden Refresh Cycle



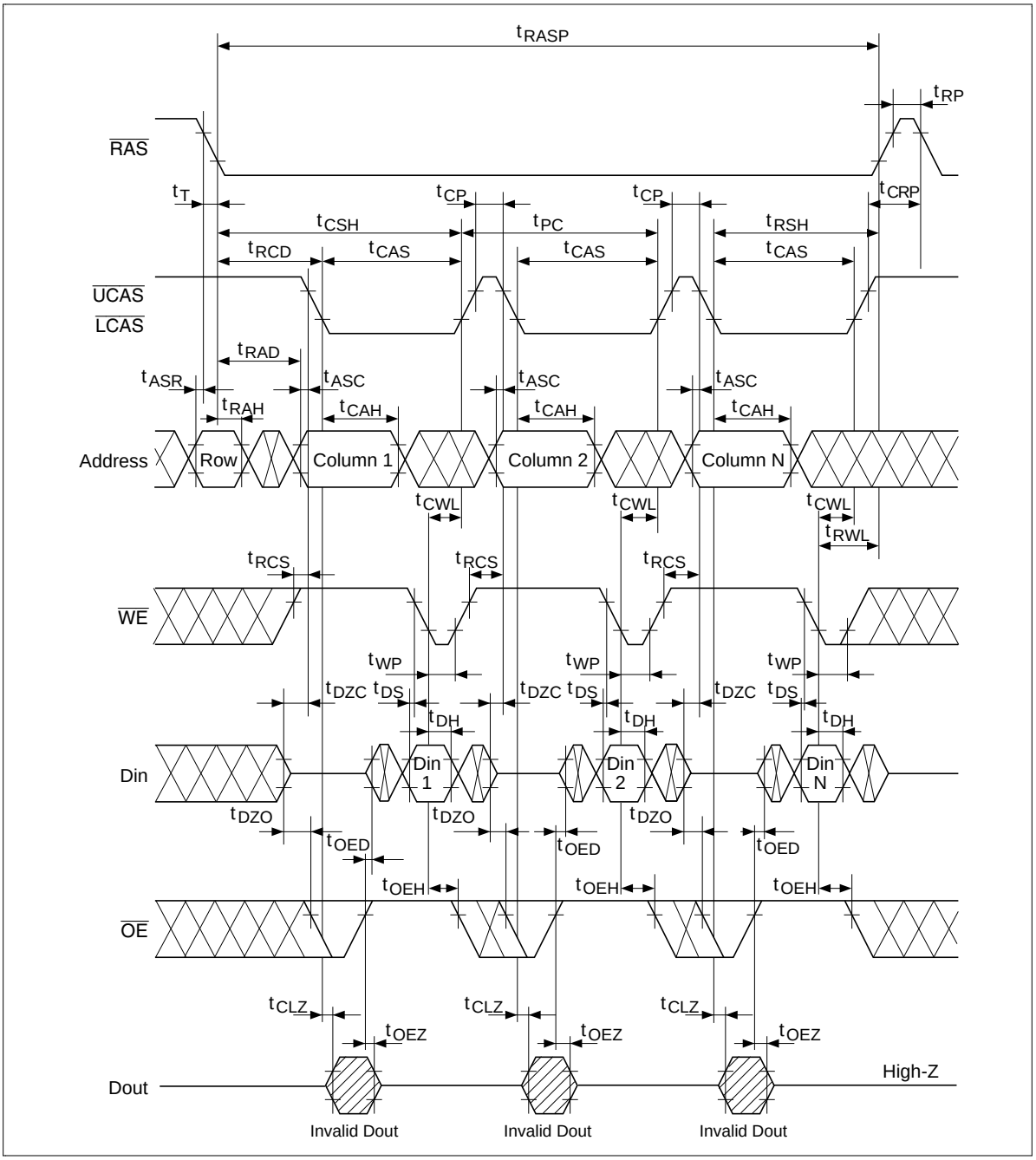
Fast Page Mode Read Cycle



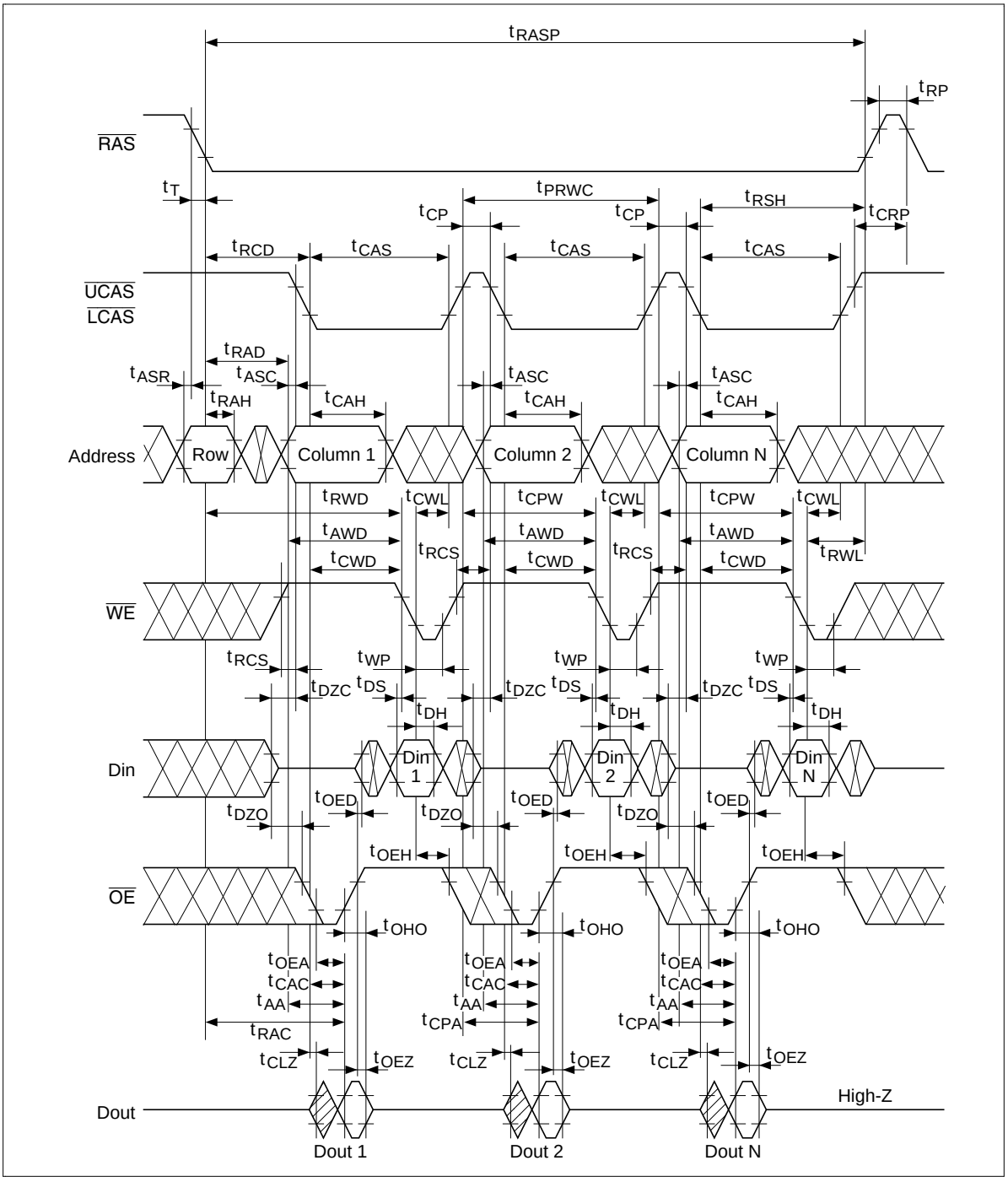
Fast Page Mode Early Write Cycle



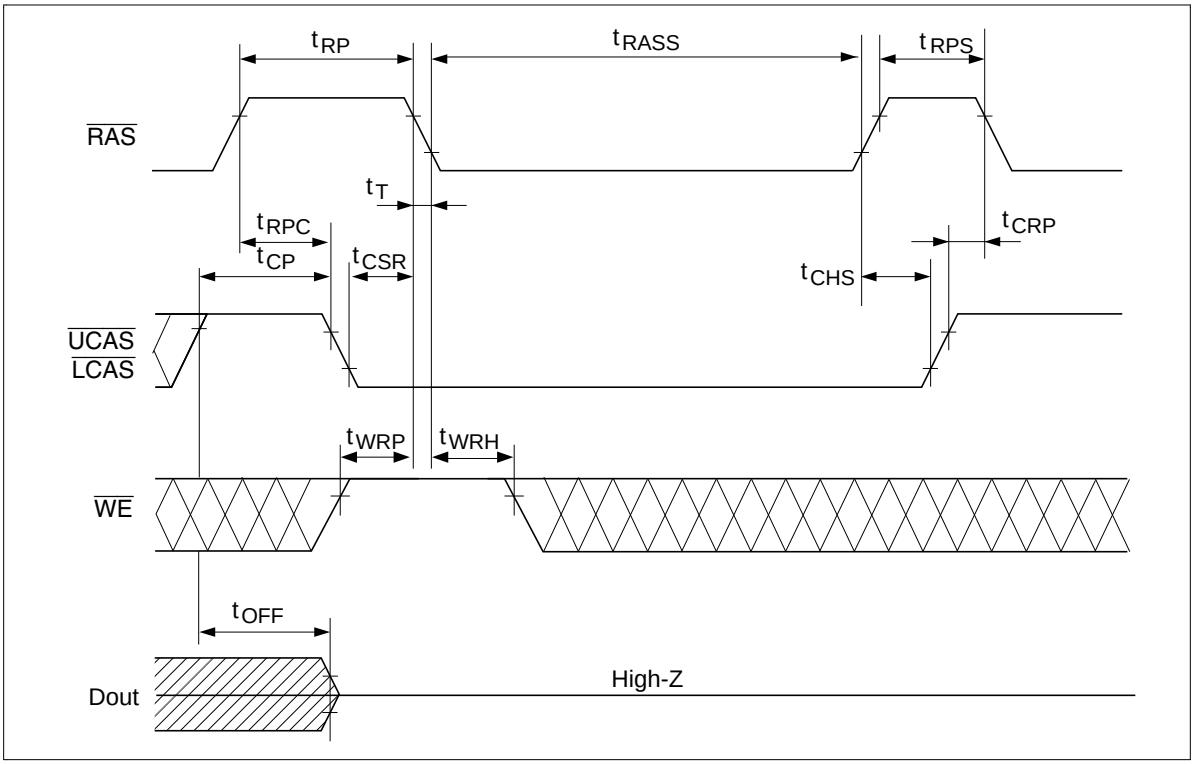
Fast Page Mode Delayed Write Cycle*[18]



Fast Page Mode Read-Modify-Write Cycle*[18]



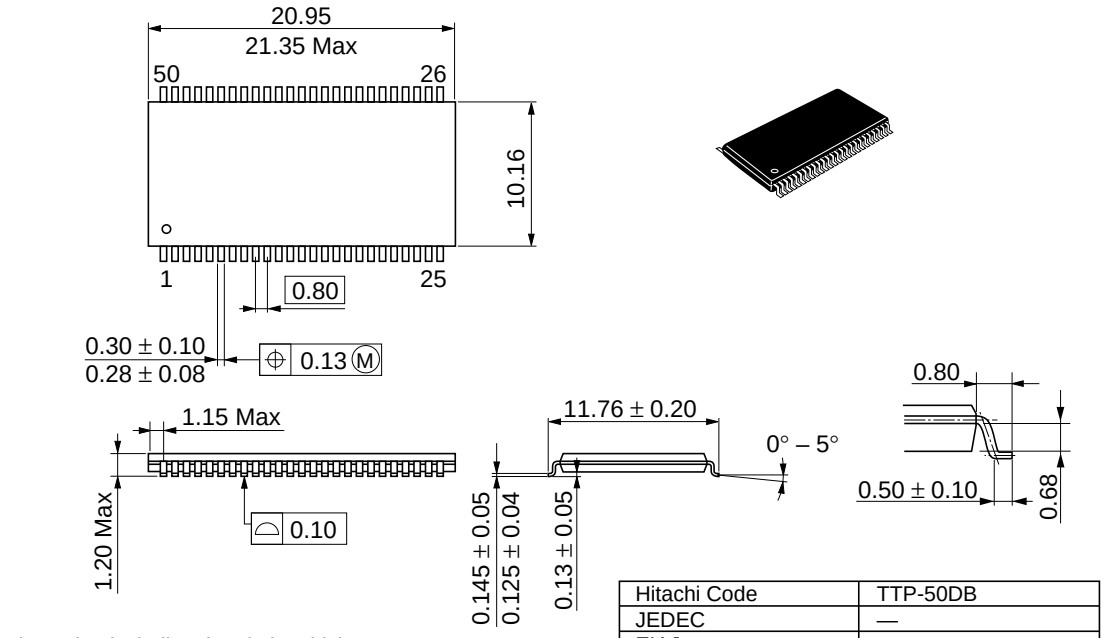
Self Refresh Cycle (L-version)*[20, 21, 22, 23]



Package Dimensions

HM5164160TT/LTT Series
HM5165160TT/LTT Series (TTP-50DB)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-50DB
JEDEC	—
EIAJ	—
Weight (reference value)	0.51 g

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HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi Semiconductor
(America) Inc.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1897
U S A
Tel: 800-285-1601
Fax:303-297-0447

Hitachi Europe GmbH
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30-00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 01628-585000
Fax: 01628-585160

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jul. 23, 1997	Initial issue	J. Miyake	M. Saeki
0.1	Nov. 1997	Change of Subtitle	J. Miyake	Y. Takahashi
1.0	Mar. 18, 1998	Deletion of Preliminary Deletion of HM5164160J/LJ, HM5165160J/LJ Series (CP-50DA) AC Characteristics Change order of notes Change note numbers of tables		