
HM5116400 Series, HM5117400 Series

16 M FP DRAM (4-Mword $\times$ 4-bit)
4 k Refresh/2 k Refresh

HITACHI

ADE-203-648E (Z)

Rev. 5.0

Nov. 1997

Description

The Hitachi HM5116400 Series, HM5117400 Series are CMOS dynamic RAMs organized 4,194,304-word $\times$ 4-bit. They employ the most advanced 0.5 μ m CMOS technology for high performance and low power. The HM5116400 Series, HM5117400 Series offer Fast Page Mode as a high speed access mode. They have package variations of standard 300-mil 26-pin plastic SOJ and standard 300-mil 26-pin plastic TSOP.

Features

- Single 5 V ($\pm 10\%$)
- Access time: 60 ns/70 ns (max)
- Power dissipation
 - Active mode : 440 mW/385 mW (max) (HM5116400 Series)
: 495 mW/440 mW (max) (HM5117400 Series)
 - Standby mode : 11 mW (max)
: 0.83 mW (max) (L-version)
- Fast page mode capability
- Long refresh period
 - 4096 refresh cycles : 64 ms (HM5116400 Series)
: 128 ms (L-version)
 - 2048 refresh cycles : 32 ms (HM5117400 Series)
: 128 ms (L-version)
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- Battery backup operation (L-version)
- Test function
 - 16-bit parallel test mode

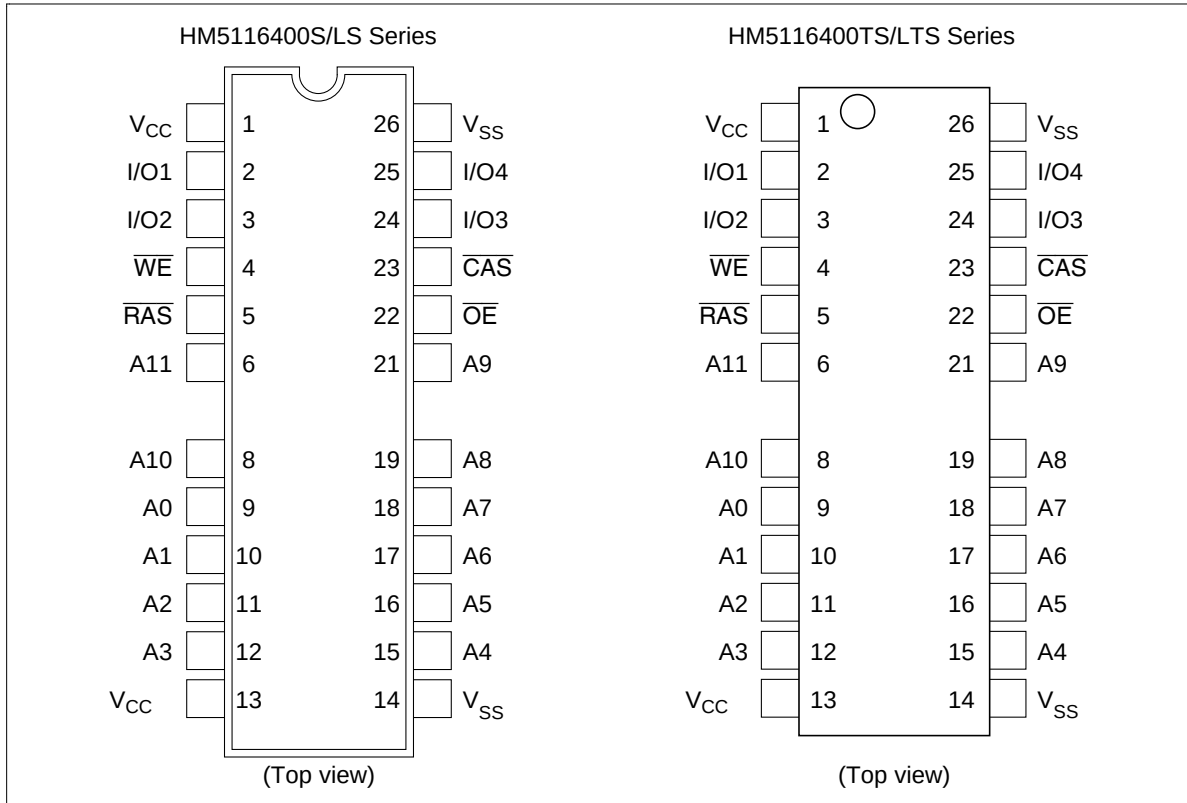
HM5116400 Series, HM5117400 Series

Ordering Information

Type No.	Access time	Package
HM5116400S-6	60 ns	300-mil 26-pin plastic SOJ (CP-26/24DB)
HM5116400S-7	70 ns	
HM5116400LS-6	60 ns	
HM5116400LS-7	70 ns	
HM5117400S-6	60 ns	
HM5117400S-7	70 ns	
HM5117400LS-6	60 ns	
HM5117400LS-7	70 ns	
HM5116400TS-6	60 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM5116400TS-7	70 ns	
HM5116400LTS-6	60 ns	
HM5116400LTS-7	70 ns	
HM5117400TS-6	60 ns	
HM5117400TS-7	70 ns	
HM5117400LTS-6	60 ns	
HM5117400LTS-7	70 ns	

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Pin Arrangement

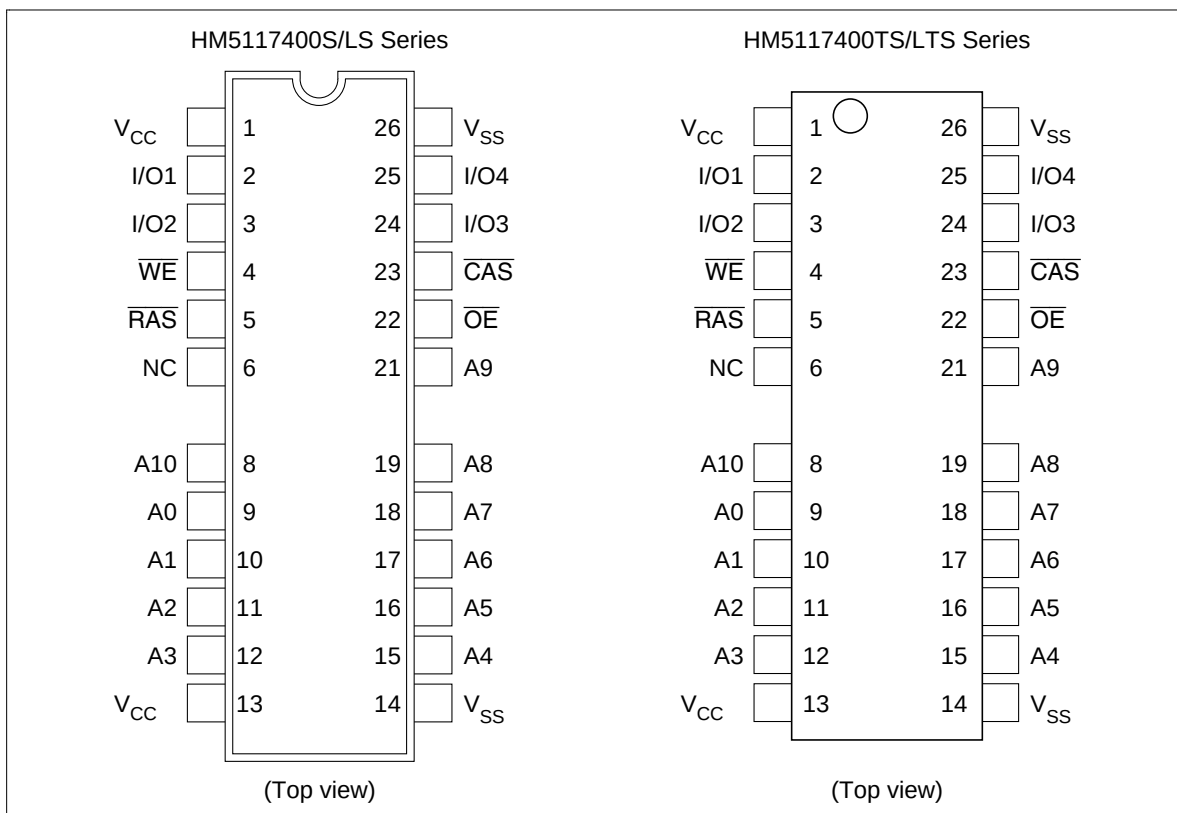


Pin Description

Pin name	Function
A0 to A11	Address input Row/Refresh address A0 to A11 Column address A0 to A9
I/O1 to I/O4	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

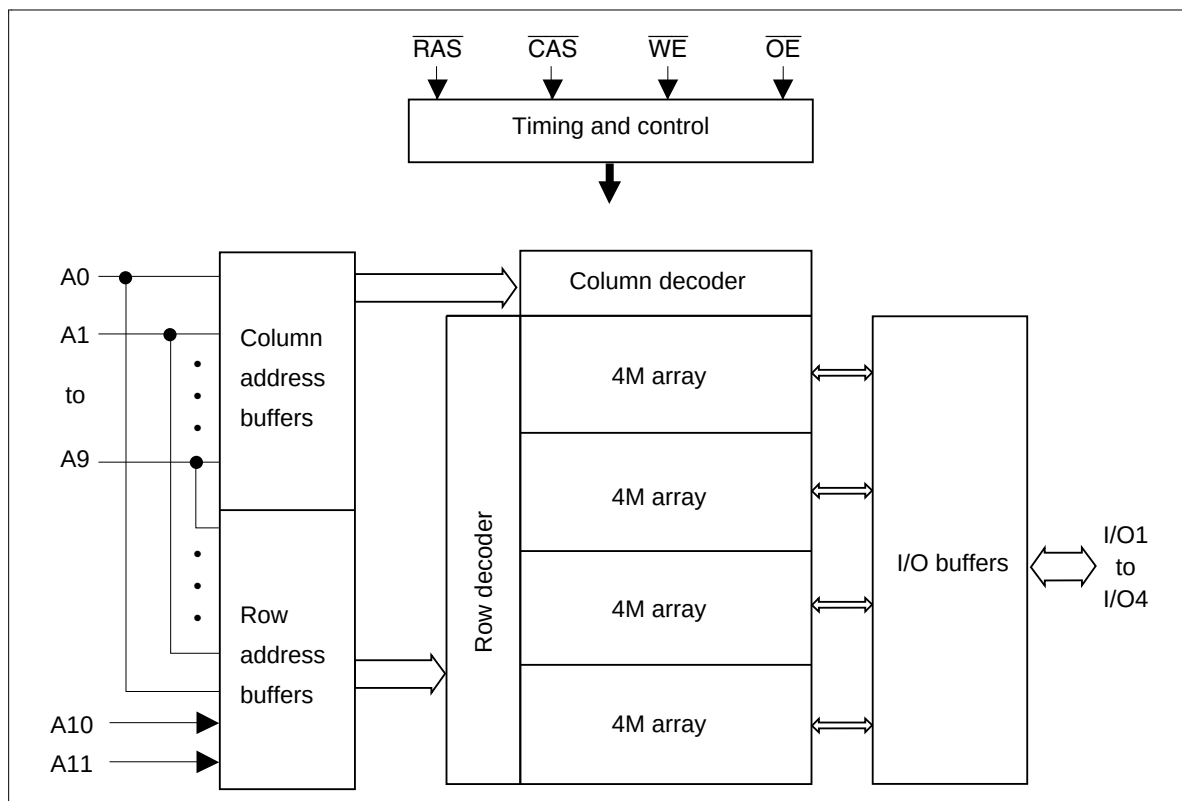
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Pin Arrangement



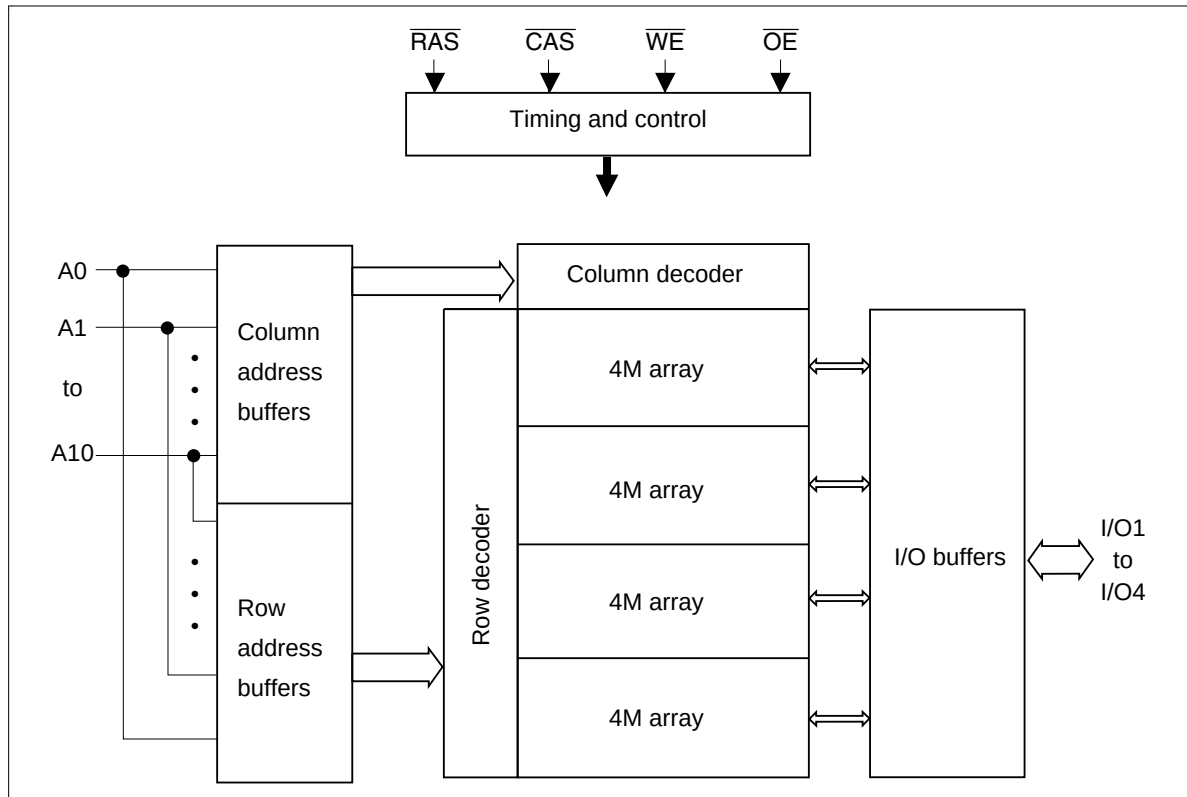
Pin Description

Pin name	Function
A0 to A10	Address input Row/Refresh address A0 to A10 Column address A0 to A10
I/O1 to I/O4	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram (HM5116400 Series)

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Block Diagram (HM5117400 Series)



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (HM5116400 Series)

		HM5116400					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Operating current* ¹ , * ²	I _{CC1}	—	80	—	70	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z
		—	1	—	1	mA	CMOS interface RAS, CAS ≥ V _{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	150	—	150	μA	CMOS interface RAS, CAS ≥ V _{CC} – 0.2 V Dout = High-Z
RAS-only refresh current* ²	I _{CC3}	—	80	—	70	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	5	—	5	mA	RAS = V _{IH} CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	80	—	70	mA	t _{RC} = min
Fast page mode current* ¹ , * ³	I _{CC7}	—	70	—	60	mA	t _{PC} = min
Battery backup current (Standby with CBR refresh) (L-version)	I _{CC10}	—	350	—	350	μA	CMOS interface Dout = High-Z, CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs
Input leakage current	I _{LI}	–10	10	–10	10	μA	0 V ≤ Vin ≤ 7 V
Output leakage current	I _{LO}	–10	10	–10	10	μA	0 V ≤ Vin ≤ 7 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = –5 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while R_{AS} = V_{IL}.

3. Address can be changed once or less while C_{AS} = V_{IH}.

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DC Characteristics

($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) (HM5117400 Series)

HM5117400							
Parameter	Symbol	-6		-7		Unit	Test conditions
		Min	Max	Min	Max		
Operating current* ¹ , * ²	I _{CC1}	—	90	—	80	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z
		—	1	—	1	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	150	—	150	μA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current* ²	I _{CC3}	—	90	—	80	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	5	—	5	mA	RAS = V _{IH} CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	90	—	80	mA	t _{RC} = min
Fast page mode current* ¹ , * ³	I _{CC7}	—	80	—	70	mA	t _{PC} = min
Battery backup current (Standby with CBR refresh) (L-version)	I _{CC10}	—	350	—	350	μA	CMOS interface Dout = High-Z, CBR refresh: t _{RC} = 62.5 μs t _{RAS} ≤ 0.3 μs
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 7 V
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 7 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −5 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.

3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *1, *2, *18, *19

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

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Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5116400/HM5117400					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	110	—	130	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	40	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	60	10000	70	10000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	15	10000	18	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	ns	
Column address hold time	t _{CAH}	10	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	45	20	52	ns	3
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	30	15	35	ns	4
$\overline{\text{RAS}}$ hold time	t _{RSH}	15	—	18	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5	—	5	—	ns	
$\overline{\text{OE}}$ to Din delay time	t _{OED}	15	—	18	—	ns	5
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	t _{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	3	50	3	50	ns	7

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Read Cycle

		HM5116400/HM5117400					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	8, 9, 20
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	ns	9, 10, 17, 20
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 17, 20
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	ns	9, 20
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	30	—	35	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	ns	5

Write Cycle

		HM5116400/HM5117400					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t _{WCS}	0	—	0	—	ns	14
Write command hold time	t _{WCH}	10	—	15	—	ns	
Write command pulse width	t _{WP}	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	15	—	18	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	15	—	18	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	ns	15
Data-in hold time	t _{DH}	10	—	15	—	ns	15

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Read-Modify-Write Cycle

		HM5116400/HM5117400					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t _{RWC}	155	—	181	—	ns	
RAS to $\overline{WE}$ delay time	t _{RWD}	85	—	98	—	ns	14
CAS to $\overline{WE}$ delay time	t _{CWD}	40	—	46	—	ns	14
Column address to $\overline{WE}$ delay time	t _{AWD}	55	—	63	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t _{OEH}	15	—	18	—	ns	

Refresh Cycle

		HM5116400/HM5117400					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
CAS setup time (CBR refresh cycle)	t _{CSR}	5	—	5	—	ns	
CAS hold time (CBR refresh cycle)	t _{CHR}	10	—	10	—	ns	
WE setup time (CBR refresh cycle)	t _{WRP}	0	—	0	—	ns	
WE hold time (CBR refresh cycle)	t _{WRH}	10	—	10	—	ns	
RAS precharge to CAS hold time	t _{RPC}	5	—	5	—	ns	

Fast Page Mode Cycle

		HM5116400/HM5117400					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t _{PC}	40	—	45	—	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	t _{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	35	—	40	ns	9, 17, 20
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{CPRH}	35	—	40	—	ns	

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Fast Page Mode Read-Modify-Write Cycle

		HM5116400/HM5117400					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	t _{PRWC}	85	—	96	—	ns	
WE delay time from $\overline{\text{CAS}}$ precharge	t _{CPW}	60	—	68	—	ns	14

Test Mode Cycle *19

		HM5116400/HM5117400					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Test mode $\overline{\text{WE}}$ setup time	t_{WTS}	0	—	0	—	ns	
Test mode $\overline{\text{WE}}$ hold time	t_{WTH}	10	—	10	—	ns	

Refresh (HM5116400 Series)

Parameter	Symbol	Max	Unit	Notes
Refresh	t_{REF}	64	ms	4096 cycles
Refresh (L-version)	t_{REF}	128	ms	4096 cycles

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Refresh (HM5117400 Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	32	ms	2048 cycles
Refresh period (L-version)	t_{REF}	128	ms	2048 cycles

Notes: 1. AC measurements assume $t_T = 5$ ns.

- An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ -only refresh or $\overline{CAS}$ -before- $\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles are required.
- Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
- Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
- Either t_{OED} or t_{CDD} must be satisfied.
- Either t_{DZO} or t_{DZC} must be satisfied.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
- Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
- Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
- Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
- t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
- t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
- t_{RASP} defines $\overline{RAS}$ pulse width in Fast page mode cycles.
- Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
- In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
- The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M $\times$ 4 are don't care during test mode. Test mode is set by performing a $\overline{WE}$ -and- $\overline{CAS}$ -before- $\overline{RAS}$ (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O.
If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed.

Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.

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To get out of test mode and enter a normal operation mode, perform either a regular $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle or $\overline{\text{RAS}}$ -only refresh cycle.

20. In a test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

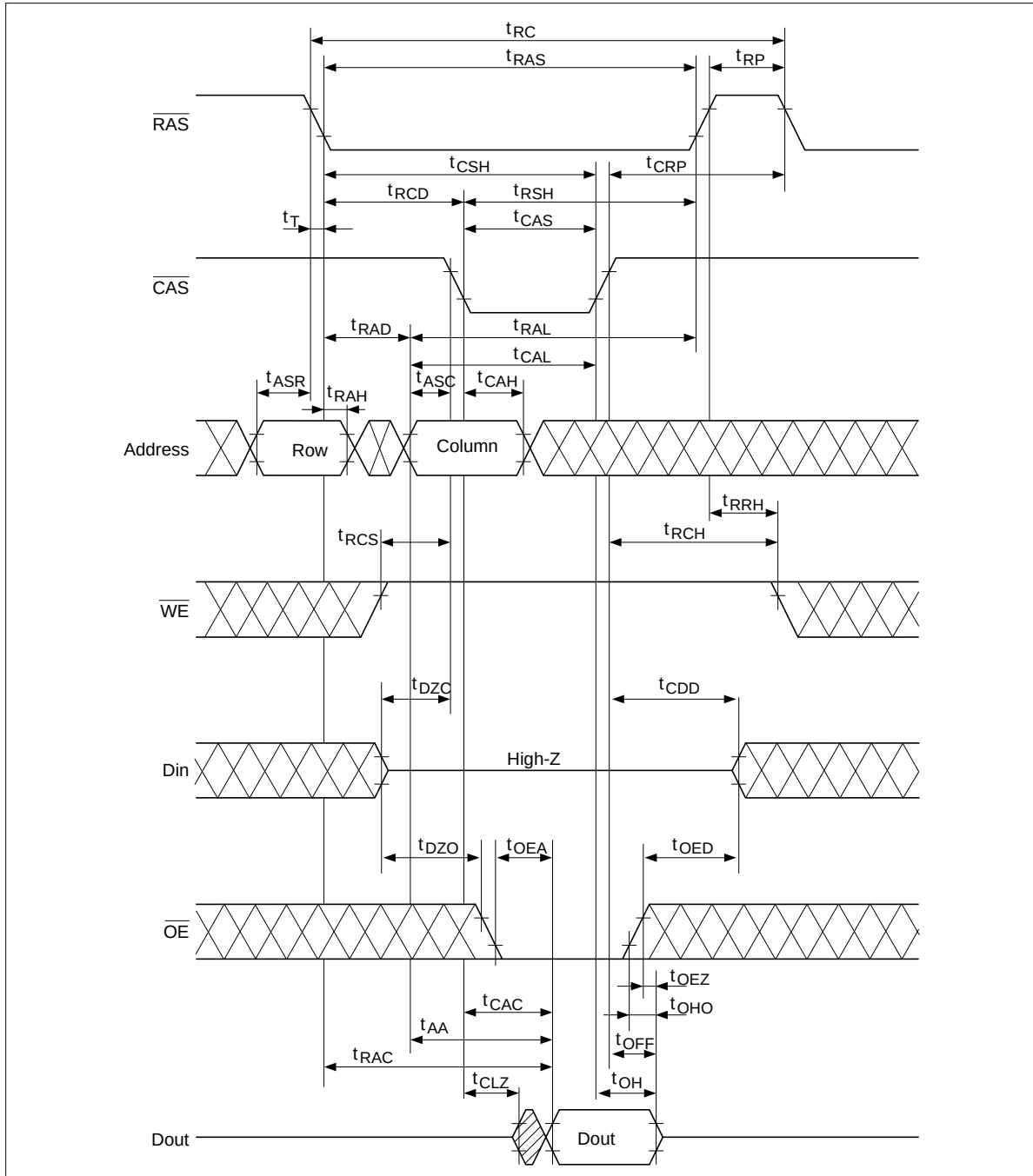
21. XXX: H or L (H: $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$, L: $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$)

///////: Invalid Dout

When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

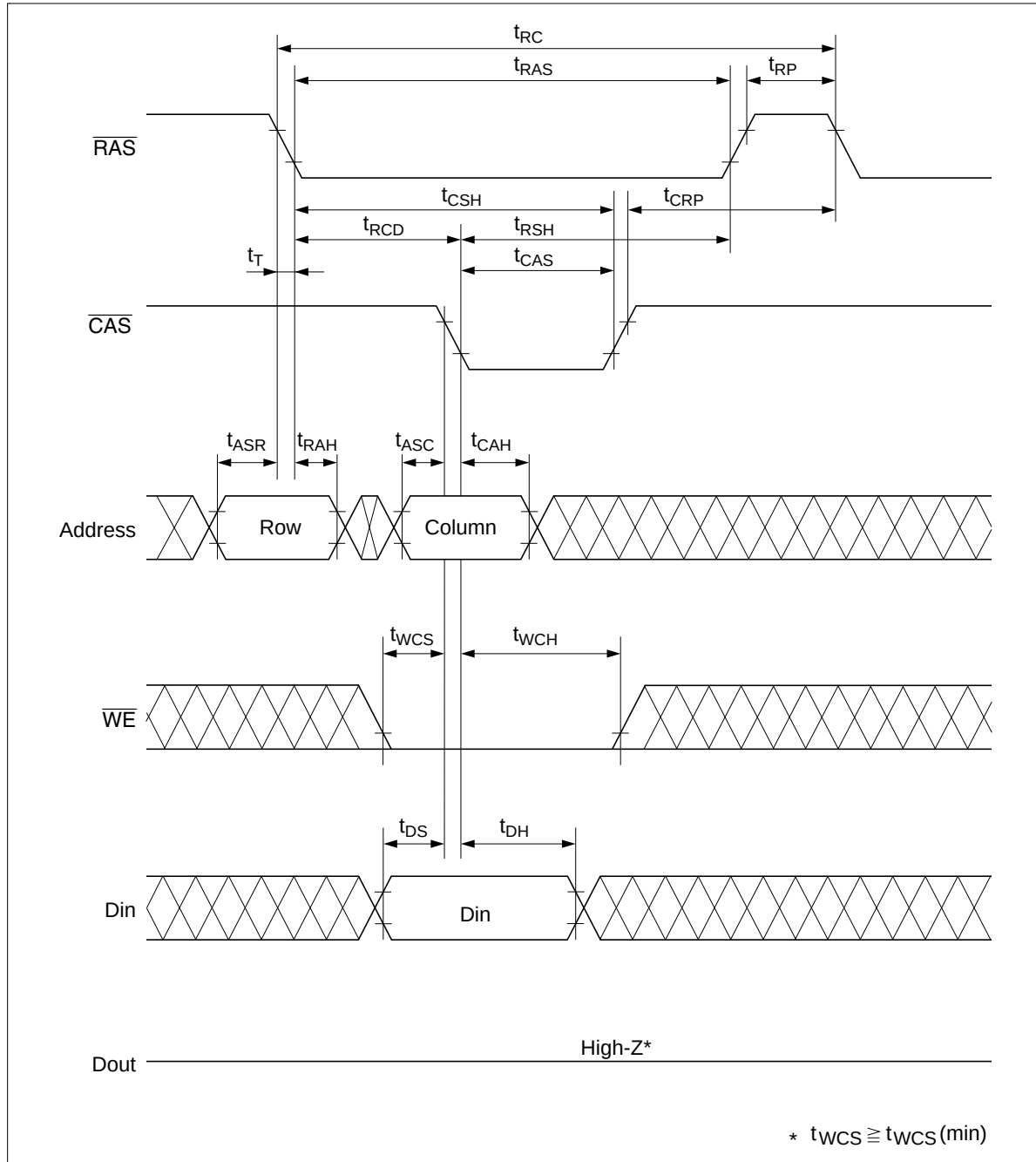
Timing Waveforms*21

Read Cycle



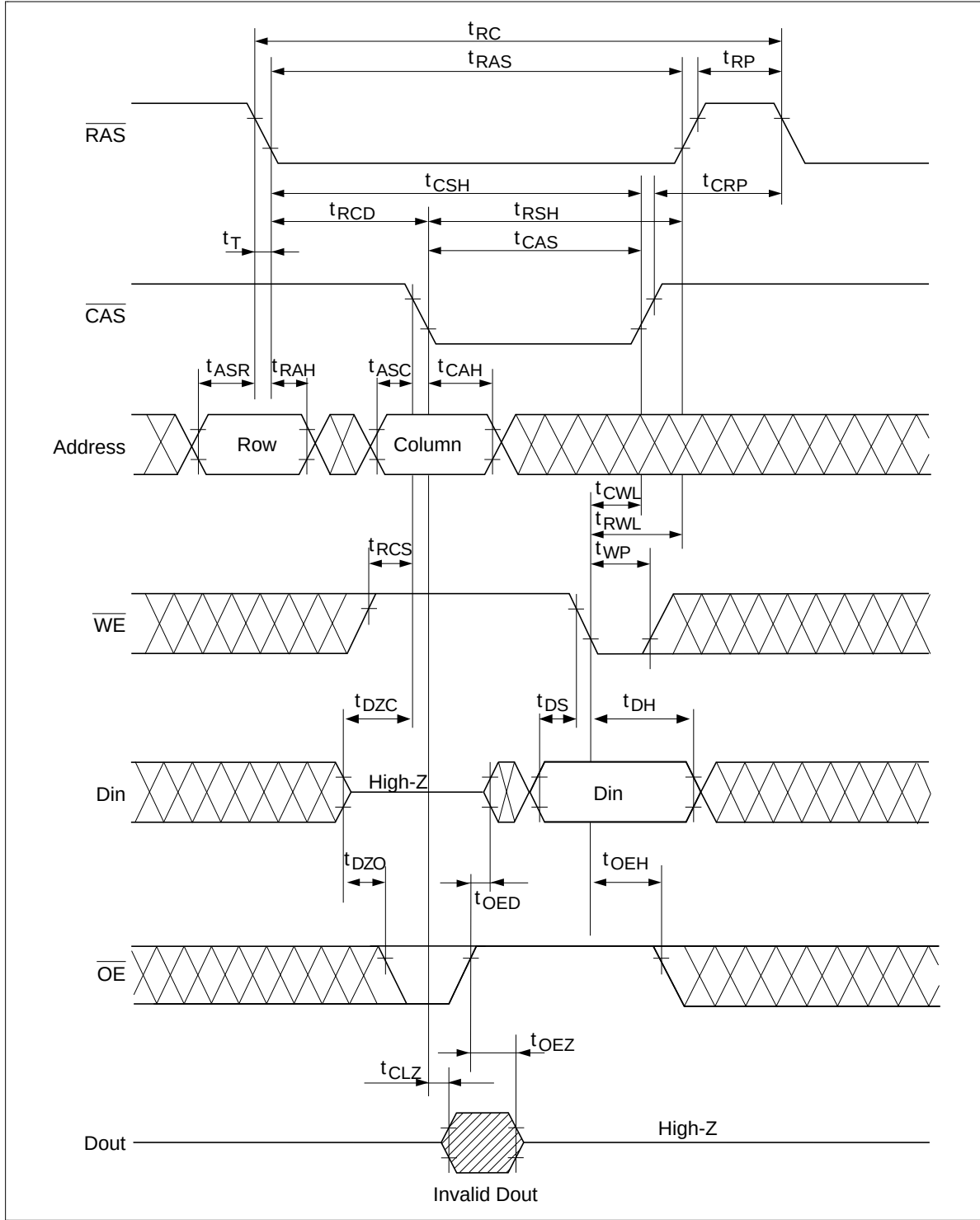
HM5116400 Series, HM5117400 Series

Early Write Cycle



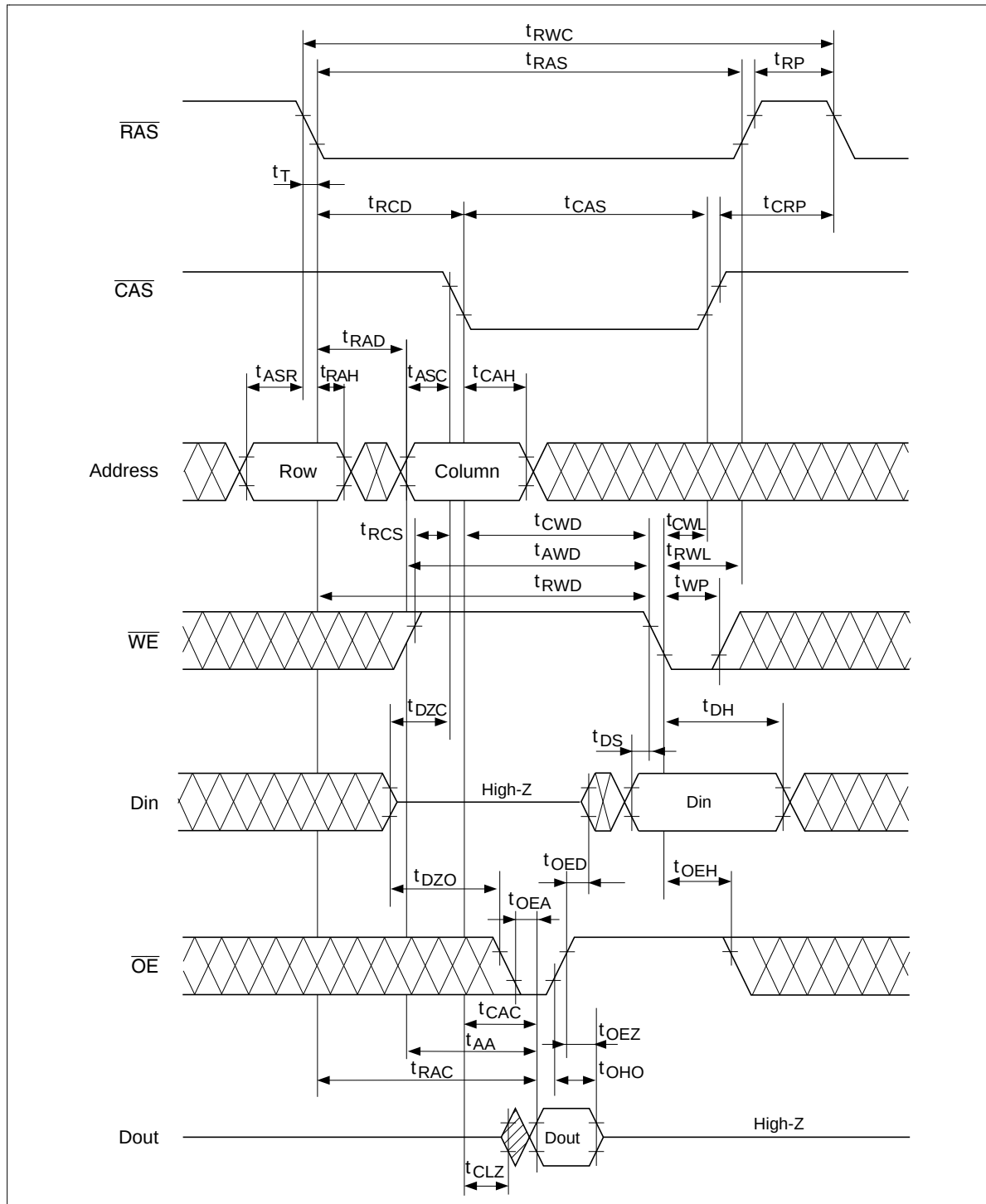
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Delayed Write Cycle*¹⁸

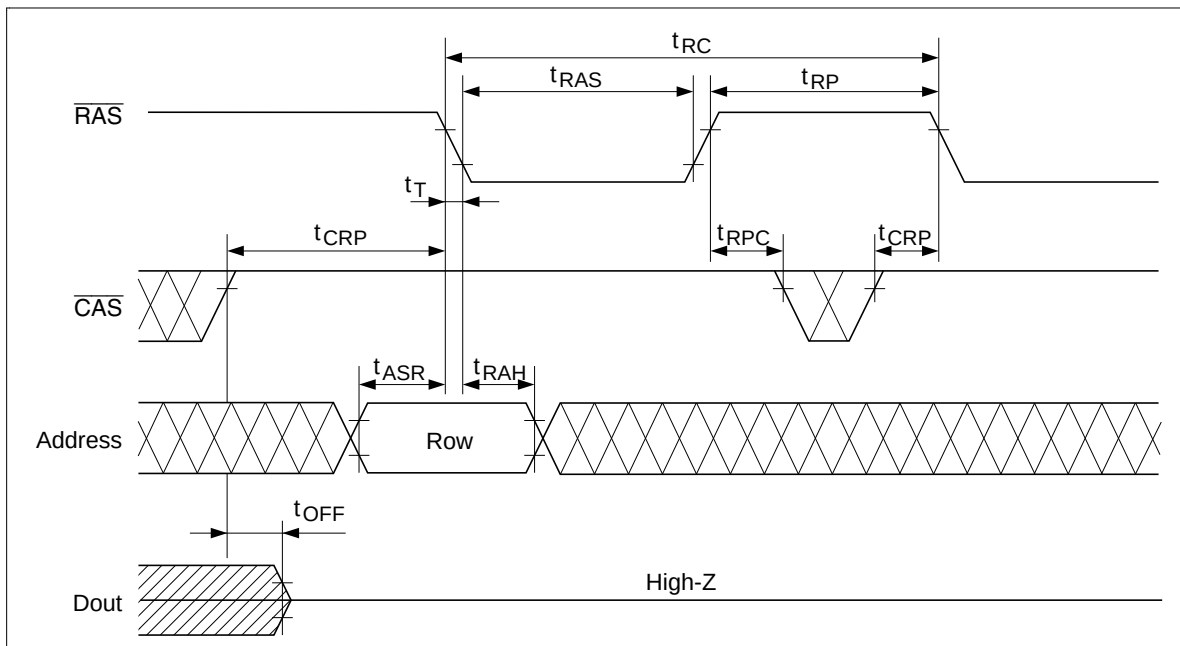


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Read-Modify-Write Cycle*18

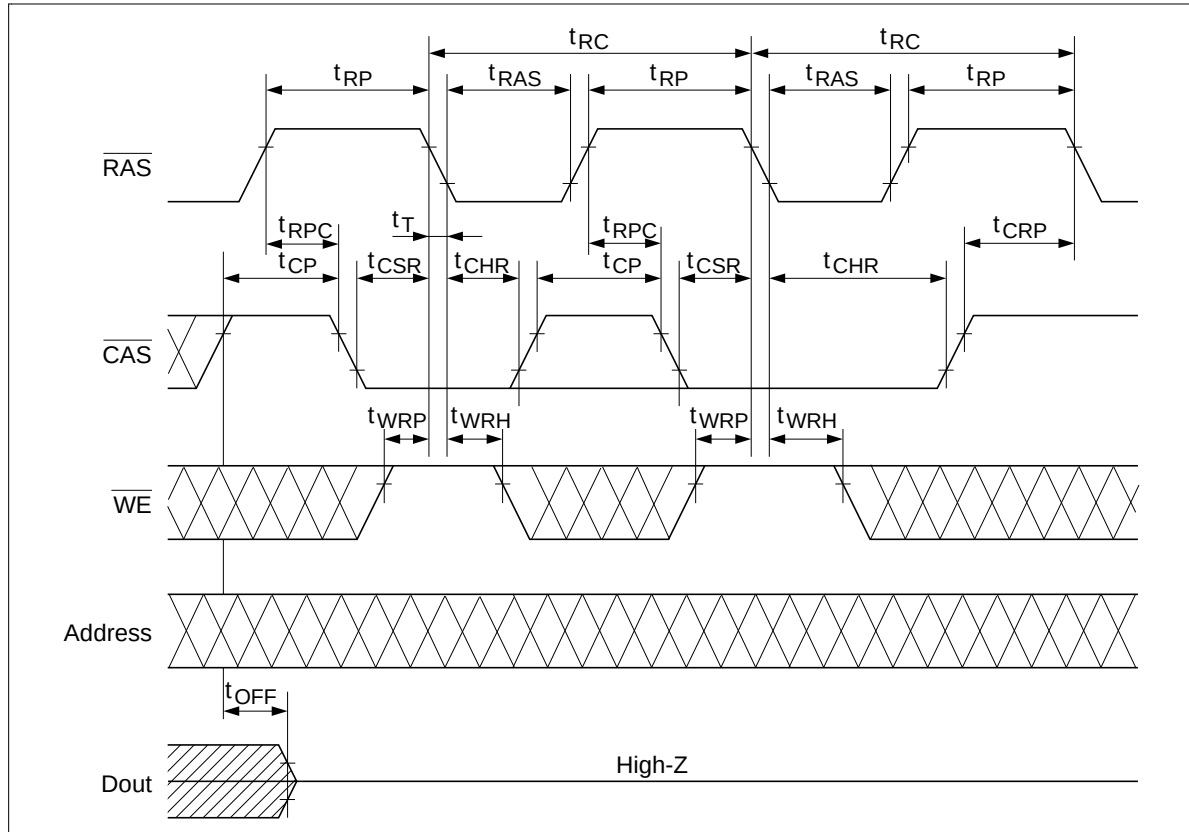


$\overline{\text{RAS}}$ -Only Refresh Cycle

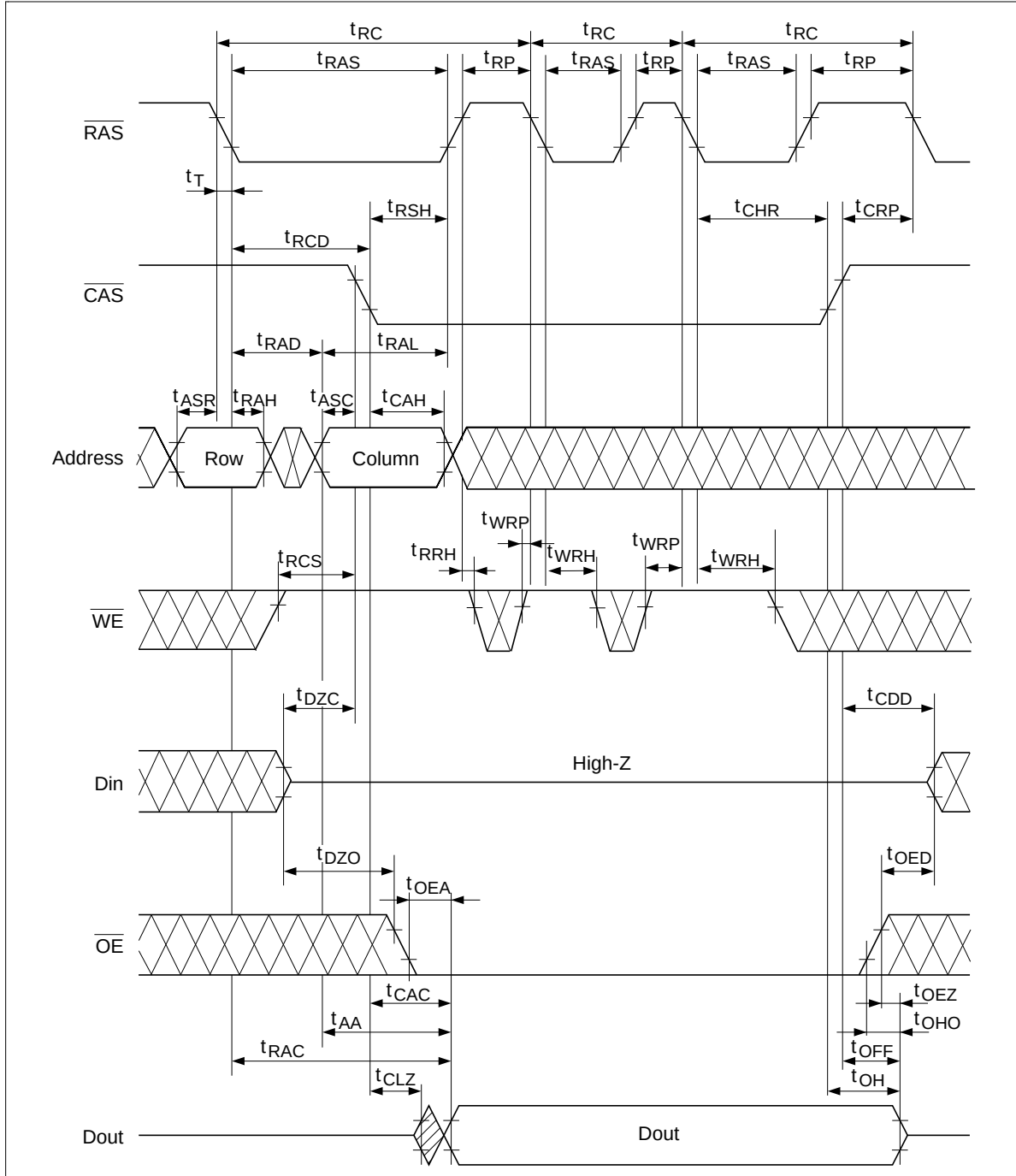


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$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

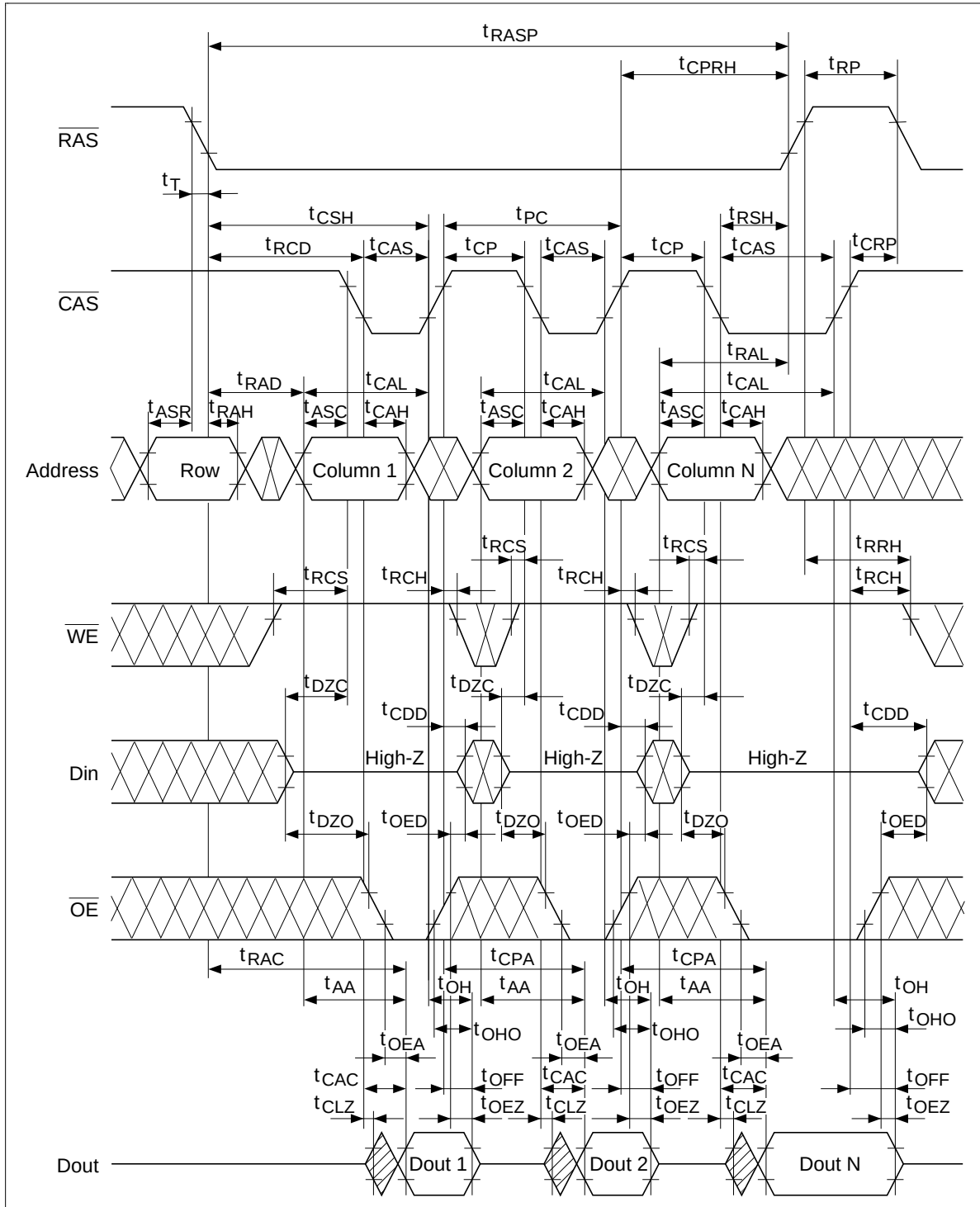


Hidden Refresh Cycle

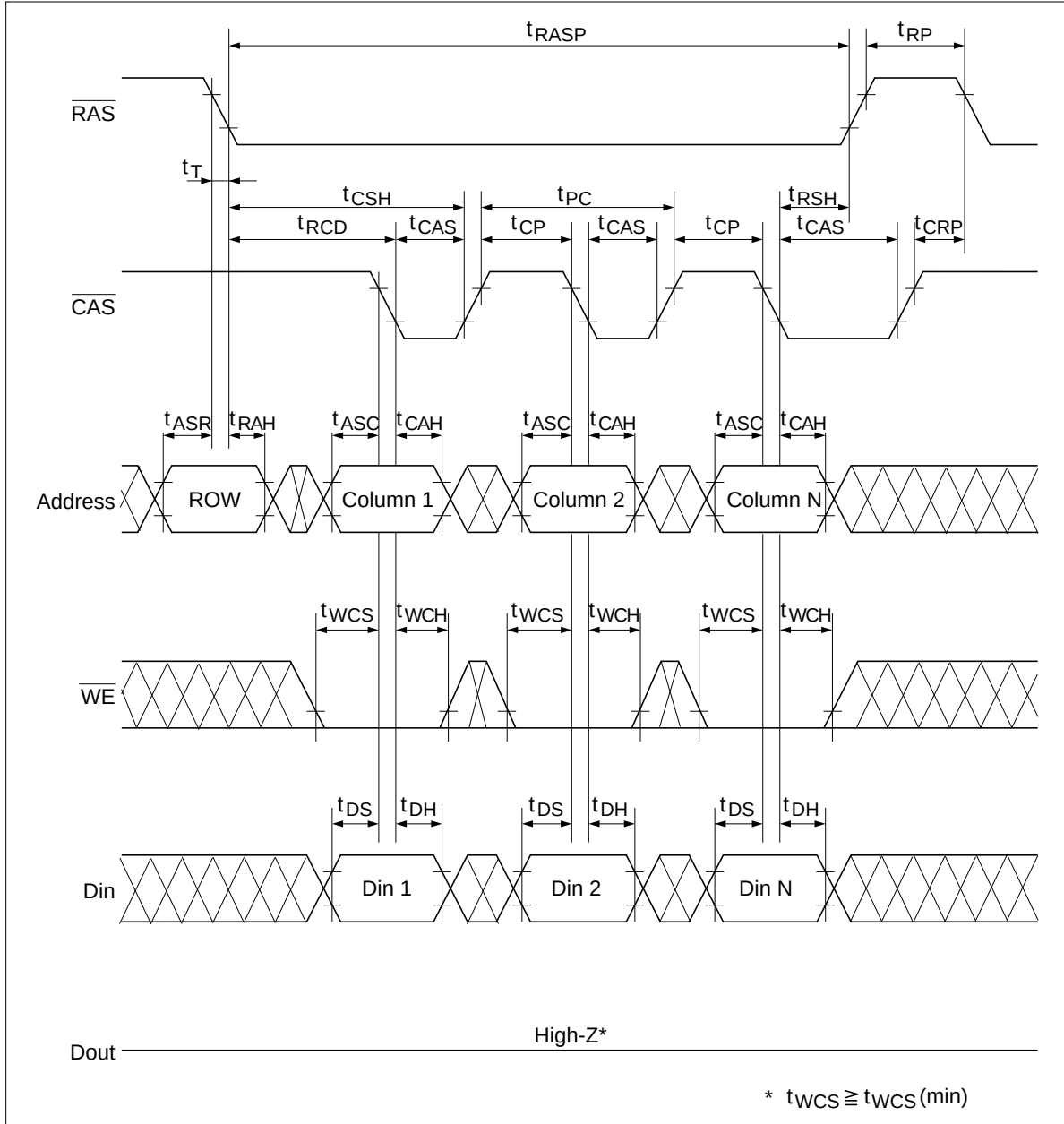


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Fast Page Mode Read Cycle

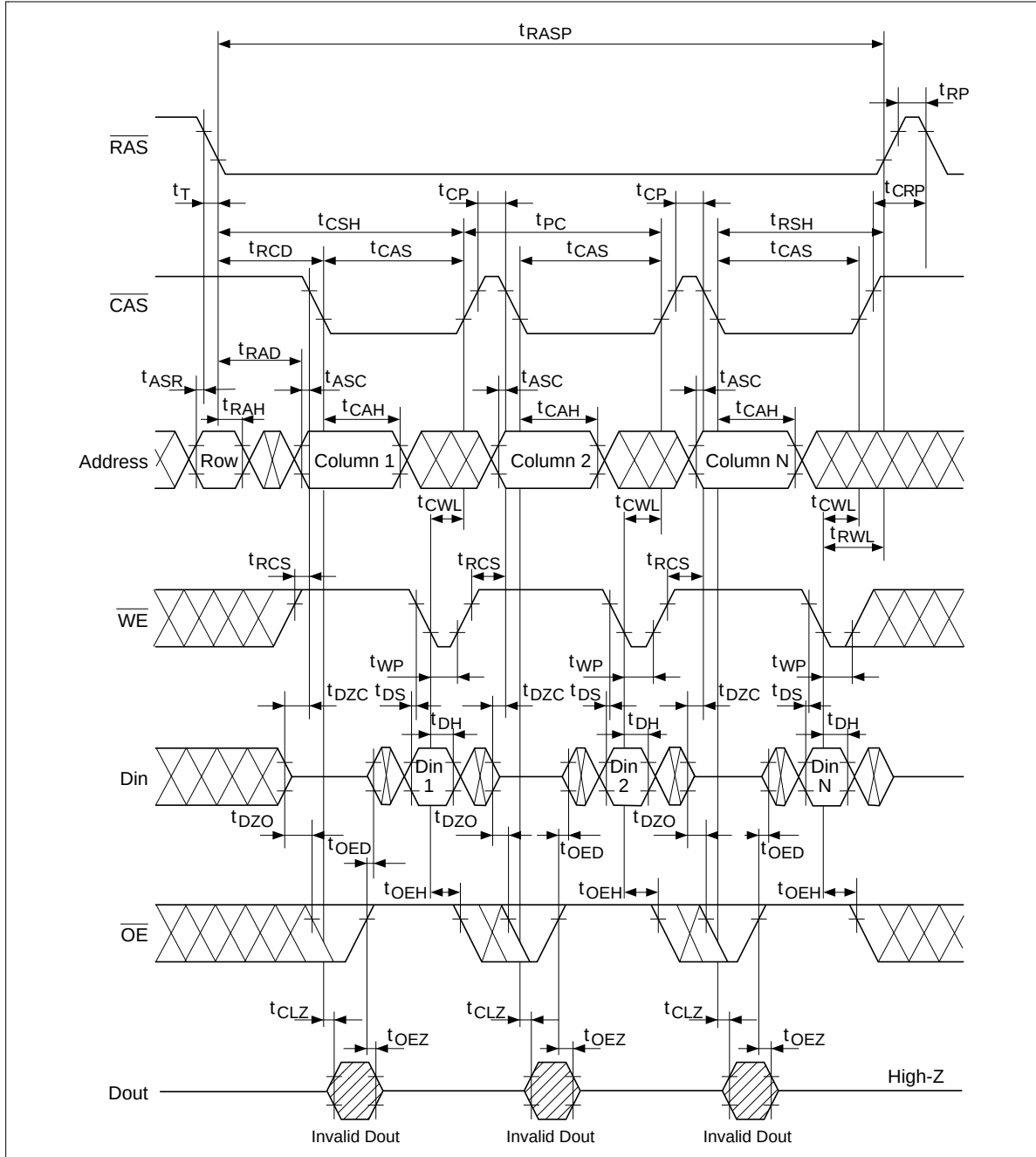


Fast Page Mode Early Write Cycle



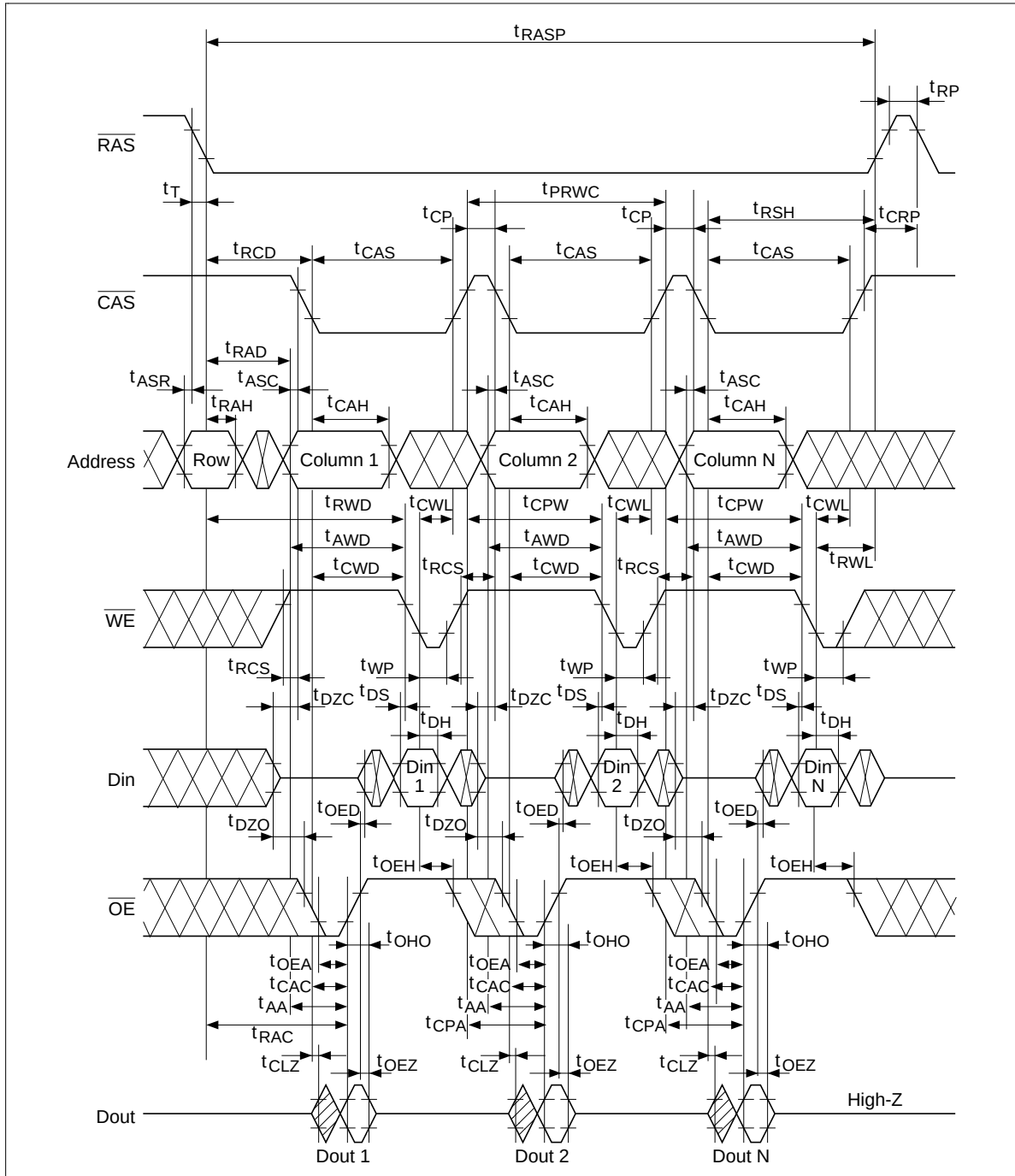
HM5116400 Series, HM5117400 Series

Fast Page Mode Delayed Write Cycle*¹⁸



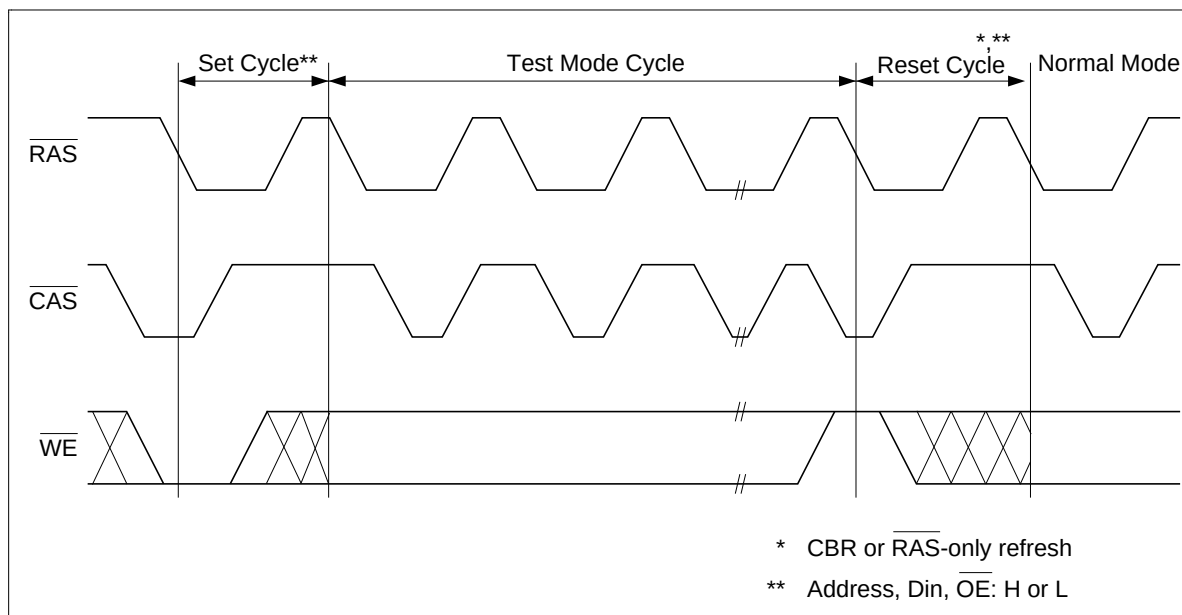
HM5116400 Series, HM5117400 Series

Fast Page Mode Read-Modify-Write Cycle*18



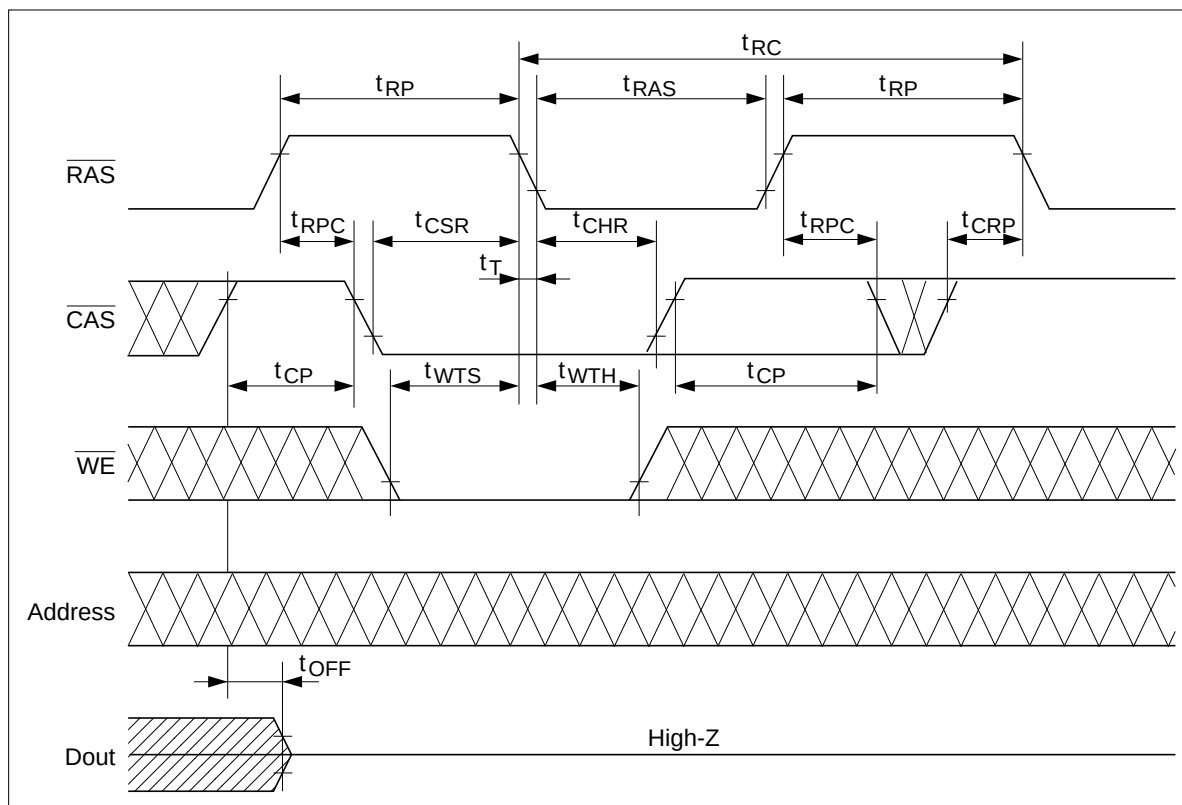
HM5116400 Series, HM5117400 Series

Test Mode Cycle*¹⁹



HM5116400 Series, HM5117400 Series

Test Mode Set Cycle



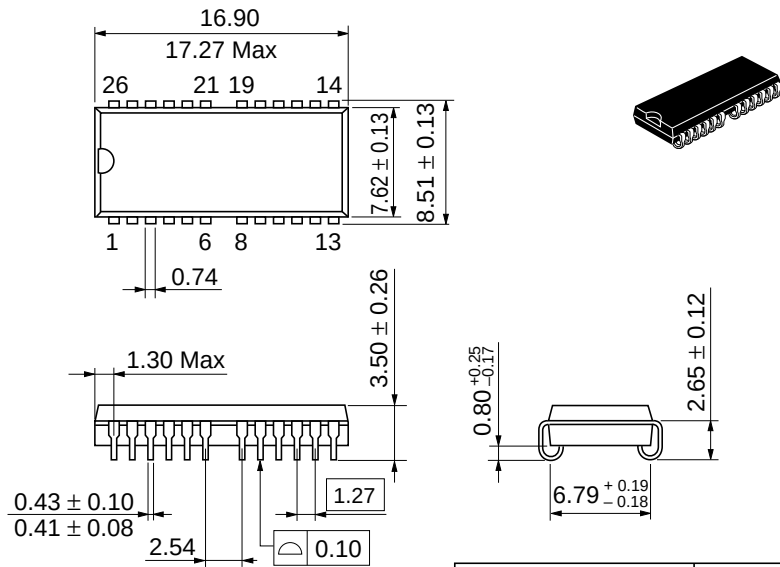
HM5116400 Series, HM5117400 Series

Package Dimensions

HM5116400S/LS Series

HM5117400S/LS Series (CP-26/24DB)

Unit: mm



Dimension including the plating thickness
Base material dimension

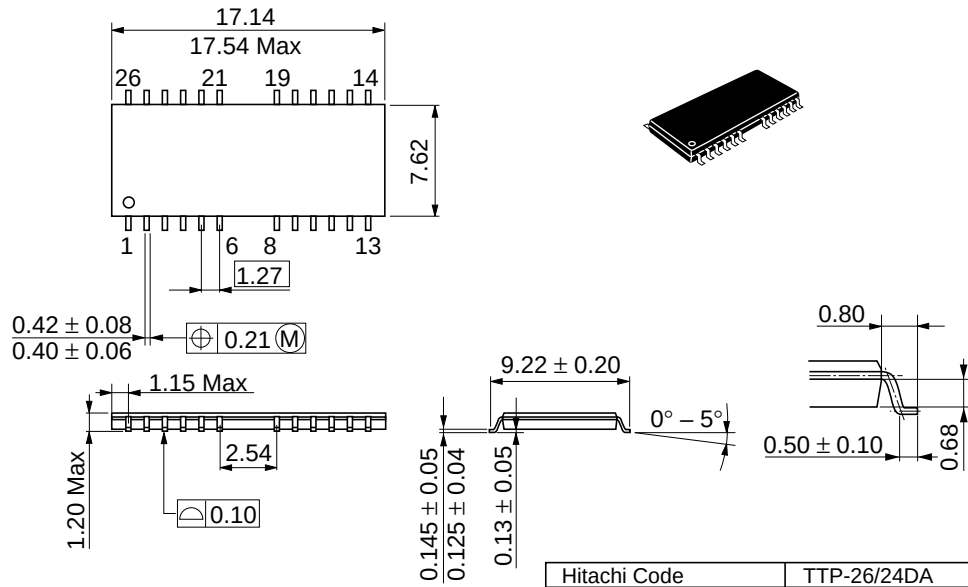
Hitachi Code	CP-26/24DB
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.8 g

HM5116400 Series, HM5117400 Series

HM5116400TS/LTS Series

HM5117400TS/LTS Series (TTP-26/24DA)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-26/24DA
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.30 g

HM5116400 Series, HM5117400 Series

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HM5116400 Series, HM5117400 Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Oct. 14, 1996	Initial issue	Y. Kasama	M. Mishima
2.0	Nov. 14, 1996	Addition of HM5116400-5 Series Addition of HM5117400-5 Series Power dissipation (active) 605/550 mW(max) to 550/495/440 mW (max) (HM5117400 Series) DC Characteristics (HM5117400 Series) I_{CC1} max: 110/100 mA to 100/90/80 mA I_{CC3} max: 110/100 mA to 100/90/80 mA I_{CC6} max: 110/100 mA to 100/90/80 mA	Y. Kasama	Y. Matsuno
3.0	Feb. 27, 1997	AC Characteristics t_{RRH} min: 5/5/5 ns to 0/0/0 ns	Y. Kasama	Y. Matsuno
4.0	Jun. 12, 1997	Deletion of HM5116400/HM5117400-5 Series	Y. Kasama	Y. Matsuno
5.0	Nov. 1997	Change of Subtitle		