HM51W4265C Series

262,144-word × 16-bit Dynamic Random Access Memory

HITACHI

ADE-203-477B (Z)
Rev. 2.0
Jul. 10, 1997

Description

The Hitachi HM51W4265C Series is a CMOS dynamic RAM organized as 262,144-word × 16-bit. HM51W4265C Series has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM51W4265C Series offers Extended Data Out (EDO) Page Mode as a high speed access mode. It is packaged in standard 44-pin plastic TSOPII.

Features

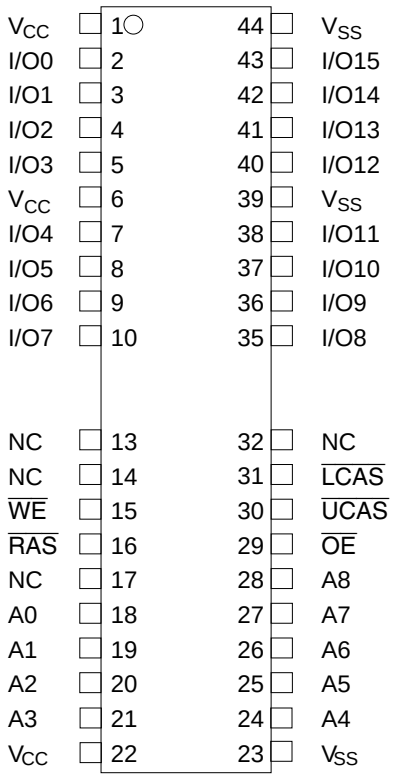
- Single 3.3 V supply: 3.3 V ±0.15 V (HM51W4265C-6R)
- 3.3 V ±0.3 V (HM51W4265C-6R)
- Access time: 60 ns/70 ns/80 ns (max)
- Power dissipation
  - Active mode: 576 mW/552 mW/468 mW/396 mW (max)
  - Standby mode: 6.9 mW (max) (HM51W4265C-6R)
    7.2 mW (max) (HM51W4265C-6/7/8)
    0.69 mW (max)(L-version) (HM51W4265CL-6R)
    0.72 mW (max) (L-version) (HM51W4265CL-6/7/8)
- EDO page mode capability
- Refresh cycles
  - 512 refresh cycles: 8 ms
    128 ms (L-version)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Self refresh
- 2$\overline{\text{CAS}}$-byte control
- Battery backup operation (L-version)

Ordering Information

Type No.	Access time	Package
HM51W4265CTT-6	60 ns	400-mil 44-pin plastic TSOPII (TTP-44/40DB)
HM51W4265CTT-6R	60 ns	
HM51W4265CTT-7	70 ns	
HM51W4265CTT-8	80 ns	
HM51W4265CLTT-6	60 ns	
HM51W4265CLTT-6R	60 ns	
HM51W4265CLTT-7	70 ns	
HM51W4265CLTT-8	80 ns	

Pin Arrangement

HM51W4265CTT/CLTTSeries

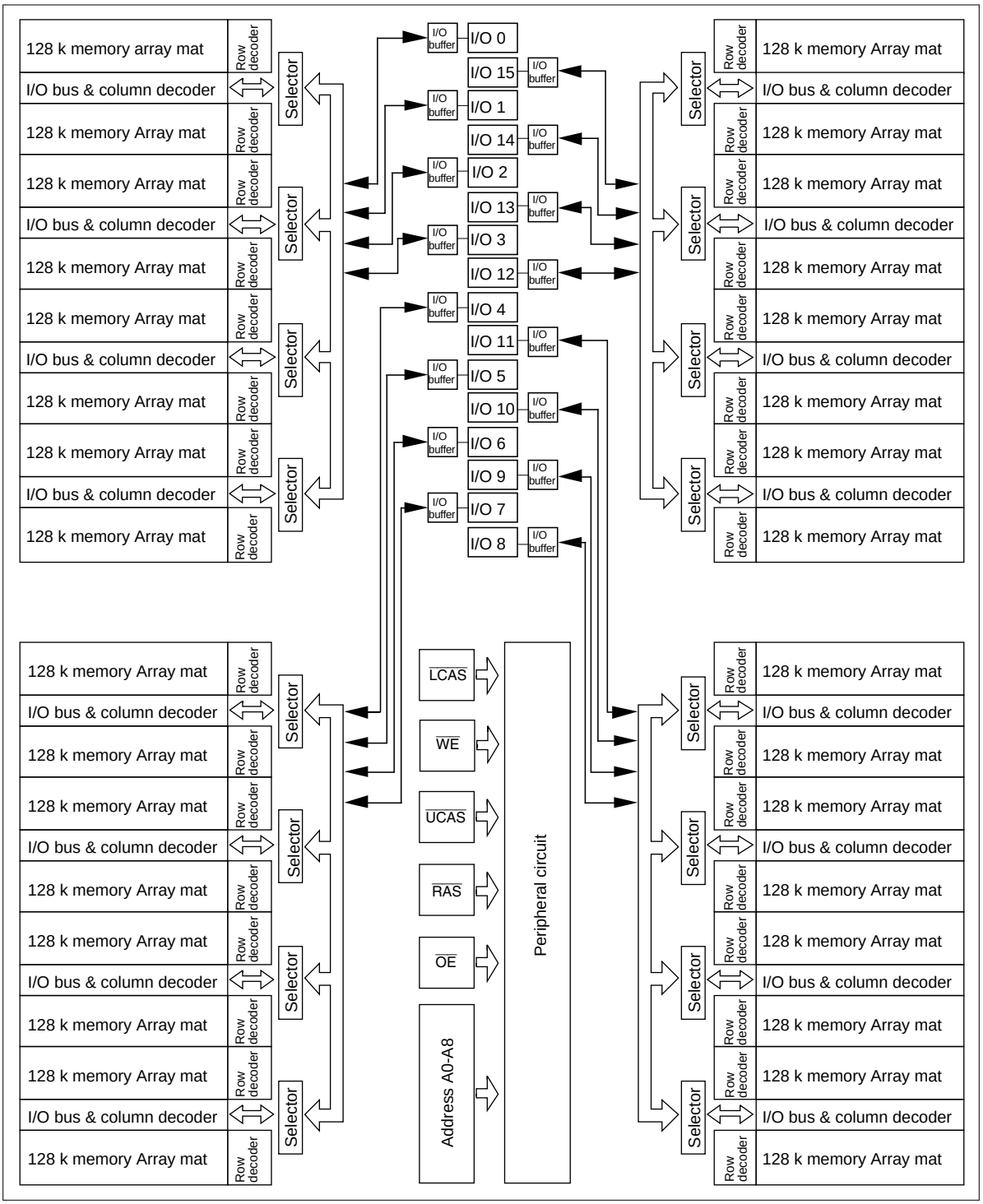


(Top view)

Pin Description

Pin name	Function	
A0 to A8	Address input	
	– Row address	A0 to A8
	– Column address	A0 to A8
	– Refresh address	A0 to A8
I/O0 to I/O15	Data input/output	
$\overline{RAS}$	Row address strobe	
$\overline{UCAS}$, $\overline{LCAS}$	Column address strobe	
$\overline{WE}$	Read/write enable	
$\overline{OE}$	Output enable	
V_{CC}	Power supply	
V_{SS}	Ground	
NC	No connection	

Block Diagram



Operation Table

The HM51W4265C series has the following 11 operation modes.

1. Read cycle
2. Early write cycle
3. Delayed write cycle
4. Read-modify-write cycle
5. $\overline{\text{RAS}}$-only refresh cycle
6. $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle
7. Self refresh cycle
8. EDO page mode read cycle
9. EDO page mode early write cycle
10. EDO page mode delayed write cycle
11. EDO page mode read-modify-write cycle

Inputs

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Output	Operation
H	H	H	D	D	Open	Standby
H	L	L	H	L	Valid	Standby
L	L	L	H	L	Valid	Read cycle
L	L	L	L*[2]	D	Open	Early write cycle
L	L	L	L*[2]	H	Undefined	Delayed write cycle
L	L	L	H to L	L to H	Valid	Read-modify-write cycle
L	H	H	D	D	Open	$\overline{\text{RAS}}$-only refresh cycle
H to L	H	L	D	D	Open	$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle
	L	H				Self refresh cycle
	L	L				
L	H to L	H to L	H	L	Valid	EDO page mode read cycle
L	H to L	H to L	L*[2]	D	Open	EDO page mode early write cycle
L	H to L	H to L	L*[2]	H	Undefined	EDO page mode delayed write cycle
L	H to L	H to L	H to L	L to H	Valid	EDO page mode read-modify-write cycle
L	L	L	H	H	Open	Read cycle (Output disabled)

Notes: 1. H: High(inactive) L: Low(active) D: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

2. $t_{WCS} \geq 0$ ns: Early write cycle
   $t_{WCS} < 0$ ns: Delayed write cycle
3. Mode is determined by the OR function of the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$. (Mode is set by the earliest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ active edge and reset by the latest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ inactive edge.) However write operation and output High-Z control are done independently by each $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$.

ex. if $\overline{\text{RAS}}$ = H to L, $\overline{\text{LCAS}}$ = L, $\overline{\text{UCAS}}$ = H, then $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle is selected.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	2
	V_{CC} (HM51W4265C-6R)	3.15	3.3	3.45	V	1, 2
	V_{CC} (HM51W4265C-6/7/8)	3.0	3.3	3.6	V	1, 2
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Notes: 1. All voltage referred to V_{SS}.
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ±0.15 V, V_{SS} = 0 V) (HM51W4265C-6R)*[5]
(Ta = 0 to +70°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V) (HM51W4265C-6/7/8) *[5]

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*[1, 2]	I_{CC1}	—	120	—	110	—	95	mA	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ cycling t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ $\overline{WE}$, $\overline{OE}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	200	—	200	—	200	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*[2]	I_{CC3}	—	120	—	105	—	92	mA	t_{RC} = min
Standby current*[1]	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current*[2]	I_{CC6}	—	120	—	105	—	92	mA	t_{RC} = min
EDO page mode current*[1, 3]	I_{CC4}	—	160	—	130	—	110	mA	t_{HPC} = min
Battery backup current*[4] (Standby with CBR refresh) (L-version)	I_{CC10}	—	200	—	200	—	200	µA	Standby: CMOS interface Dout = High-Z CBR refresh: t_{RC} = 250 µs t_{RAS} ≤ 1 µs, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IL} $\overline{WE}$, $\overline{OE}$ = V_{IH}
Self-refresh mode current	I_{CC11}	—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≤ 0.2 V Dout = High-Z
Self-refresh mode current (L-version)	I_{CC11}	—	200	—	200	—	200	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≤ 0.2 V Dout = High-Z
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less within one EDO page cycle.
4. $V_{IH} \geq V_{CC} - 0.2$ V, $0 \leq V_{IL} \leq 0.2$ V, Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
5. All the V_{CC} pins should be supplied with the same voltage. And all the V_{SS} pins should be supplied with the same voltage.

Capacitance

(Ta = +25°C, V_{CC} = 3.3 V ±0.15 V) (HM51W4265C-6R)
(Ta = +25°C, V_{CC} = 3.3 V ±0.3 V) (HM51W4265C-6/7/8)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{UCAS}$ and $\overline{LCAS}$ = V_{IH} to disable Dout.

AC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.15 V, V_{SS} = 0 V) (HM51W4265C-6R)*1, *14, *15, *17, *18
(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HM51W4265C-6/7/8)*1, *14, *15, *17, *18

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: V_{IL} = 0 V, V_{IH} = 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (50 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	104	—	124	—	144	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	27
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	15	10000	ns	28
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	19
Column address hold time	t_{CAH}	10	—	13	—	15	—	ns	19
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	9
$\overline{RAS}$ hold time	t_{RSH}	15	—	18	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	48	—	58	—	68	—	ns	29
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	20
$\overline{OE}$ to Din delay time	t_{ODD}	15	—	18	—	20	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	7
Refresh period	t_{REF}	—	8	—	8	—	8	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	ns	3, 4, 13
Access time from address	t_{AA}	—	30	—	35	—	40	ns	3, 5, 13
Access time from $\overline{OE}$	t_{OAC}	—	15	—	20	—	20	ns	3, 23
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	19
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	16, 20
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	16
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	18	—	23	—	28	—	ns	
Output buffer turn-off time	t_{OFF1}	—	15	—	15	—	15	ns	6, 25
Output buffer turn-off time to $\overline{OE}$	t_{OFF2}	—	15	—	15	—	15	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	18	—	20	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	15	—	18	—	20	—	ns	
$\overline{WE}$ to Din delay time	t_{WDD}	15	—	18	—	20	—	ns	
$\overline{OE}$ pulse width	t_{OEP}	15	—	20	—	20	—	ns	23
Turn-off to $\overline{RAS}$	t_{OFR}	—	15	—	15	—	15	ns	6, 25
Turn-off to $\overline{WE}$	t_{WEZ}	—	15	—	15	—	15	ns	6
Output data hold time	t_{OH}	5	—	5	—	5	—	ns	25
Output data hold time from $\overline{RAS}$	t_{OHR}	5	—	5	—	5	—	ns	25
Read command hold time from $\overline{RAS}$	t_{RCHR}	60	—	70	—	80	—	ns	
Read command hold time from $\overline{CAS}$	t_{RCHC}	15	—	18	—	20	—	ns	
Read command hold time from column address	t_{RCHA}	30	—	35	—	40	—	ns	

Write Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10, 19
Write command hold time	t_{WCH}	10	—	13	—	15	—	ns	19
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	15	—	ns	21
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11, 21
Data-in hold time	t_{DH}	10	—	13	—	15	—	ns	11, 21

Read-Modify-Write Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	133	—	159	—	183	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	—	90	—	102	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	—	38	—	42	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	47	—	55	—	62	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	18	—	20	—	ns	

Refresh Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	19
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	19
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	13	—	15	—	ns	22

EDO Page Mode Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t_{HPC}	25	—	30	—	35	—	ns	24
EDO page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	15	—	ns	22
EDO page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	35	—	40	—	45	ns	3, 13, 20
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	—	40	—	45	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	3	—	ns	26
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	10	—	13	—	20	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHP}	35	—	40	—	45	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode read-modify-write cycle time	t_{HPCM}	66	—	77	—	86	—	ns	
EDO page mode read-modify-write cycle $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	52	—	60	—	67	—	ns	10, 20

Self Refresh Mode

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	100	—	µs	30, 31, 32, 33
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	110	—	130	—	150	—	ns	
$\overline{CAS}$ hold time (self refresh)	t_{CHS}	–50	—	–50	—	–50	—	ns	21

Notes:
1. AC measurements assume t_T = 2 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL loads and 50 pF. (V_{OH} = 2.0 V, V_{OL} = 0.8 V)
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF1} (max), t_{OFF2} (max), t_{OFR} (max) and t_{WEZ} (max) define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in EDO mode cycles.
13. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{ACP}.
14. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
17. When both $\overline{UCAS}$ and $\overline{LCAS}$ go low at the same time, all 16-bit data are written into the device. $\overline{UCAS}$ and $\overline{LCAS}$ cannot be staggered within the same write/read cycles.
18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
19. t_{ASC}, t_{CAH}, t_{RCS}, t_{WCS}, t_{WCH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
20. t_{CRP}, t_{CHR}, t_{ACP}, t_{CPW} and t_{RCH} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
21. t_{CWL}, t_{DH}, t_{DS} and t_{CHS} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
22. t_{CPN} and t_{CP} are determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.

23. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
24. t_{HPC} (min) can be achieved during a series of EDO page mode early write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle t_{HPC} ($t_{CAS} + t_{CP} + 2t_T$) becomes greater than the specified t_{HPC} (min) value.
25. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF1}.
26. t_{DOH} defines the time at which the output level satisfied the output timing reference levels. Measured with the test conditions.
27. t_{RAS} (min) = t_{RWD} (min) + t_{RWL} (min) + t_T in read-modify-write cycle.
28. t_{CAS} (min) = t_{CWD} (min) + t_{CWL} (min) + t_T in read-modify-write cycle.
29. t_{CSH} (min) can be achieved when $t_{RCD} \leq t_{CSH}$ (min) – t_{CAS} (min).
30. Please do not use t_{RASS} timing, 10 µs ≤ t_{RASS} ≤ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq$ 100 µs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
31. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
32. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
33. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
34. XXX: H or L (H: V_{IH} (min) ≤ $V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) ≤ $V_{IN} \leq V_{IL}$ (max))

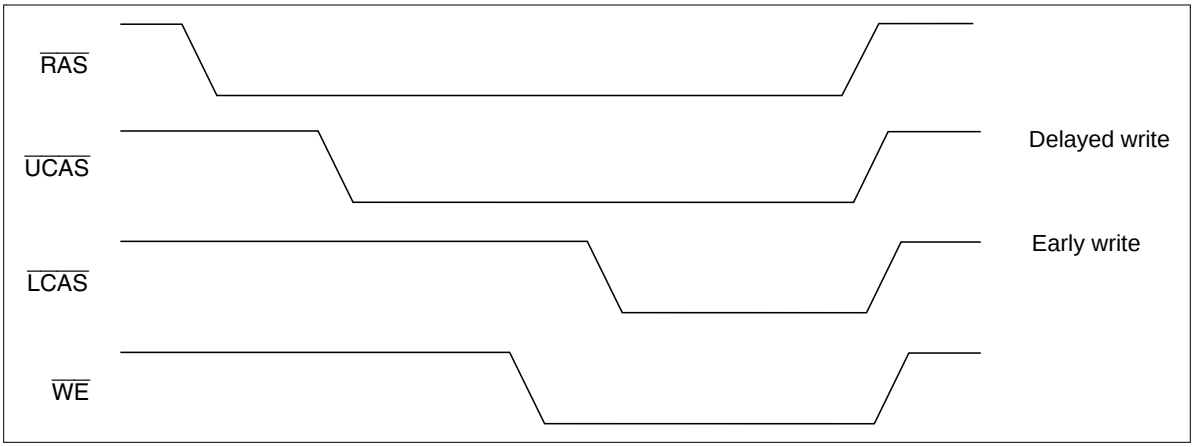
    ///////: Invalid Dout

    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

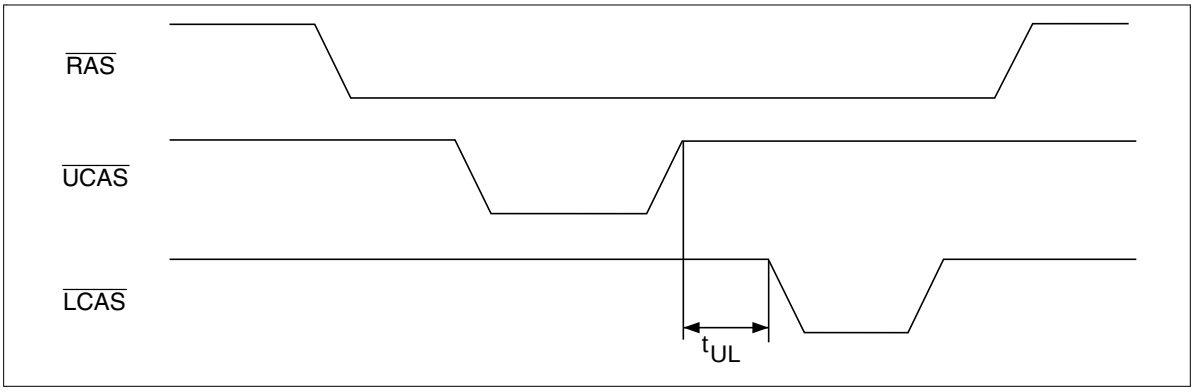
Notes concerning 2$\overline{CAS}$ control

Please do not separate the $\overline{UCAS}$/$\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}$/$\overline{LCAS}$ are allowed under the following conditions.

1. Each of the $\overline{UCAS}$/$\overline{LCAS}$ should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.



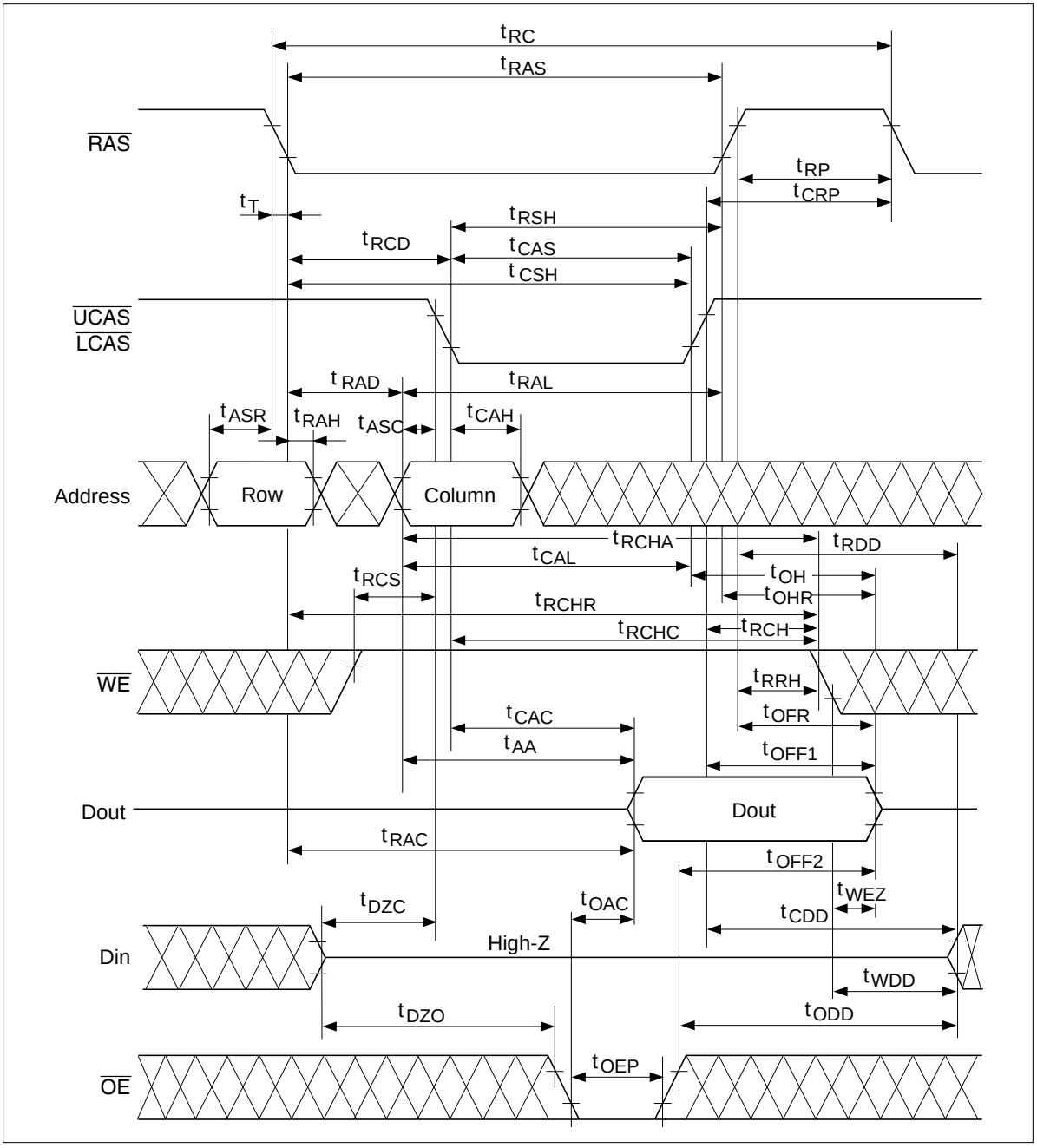
3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, EDO page mode can be performed.



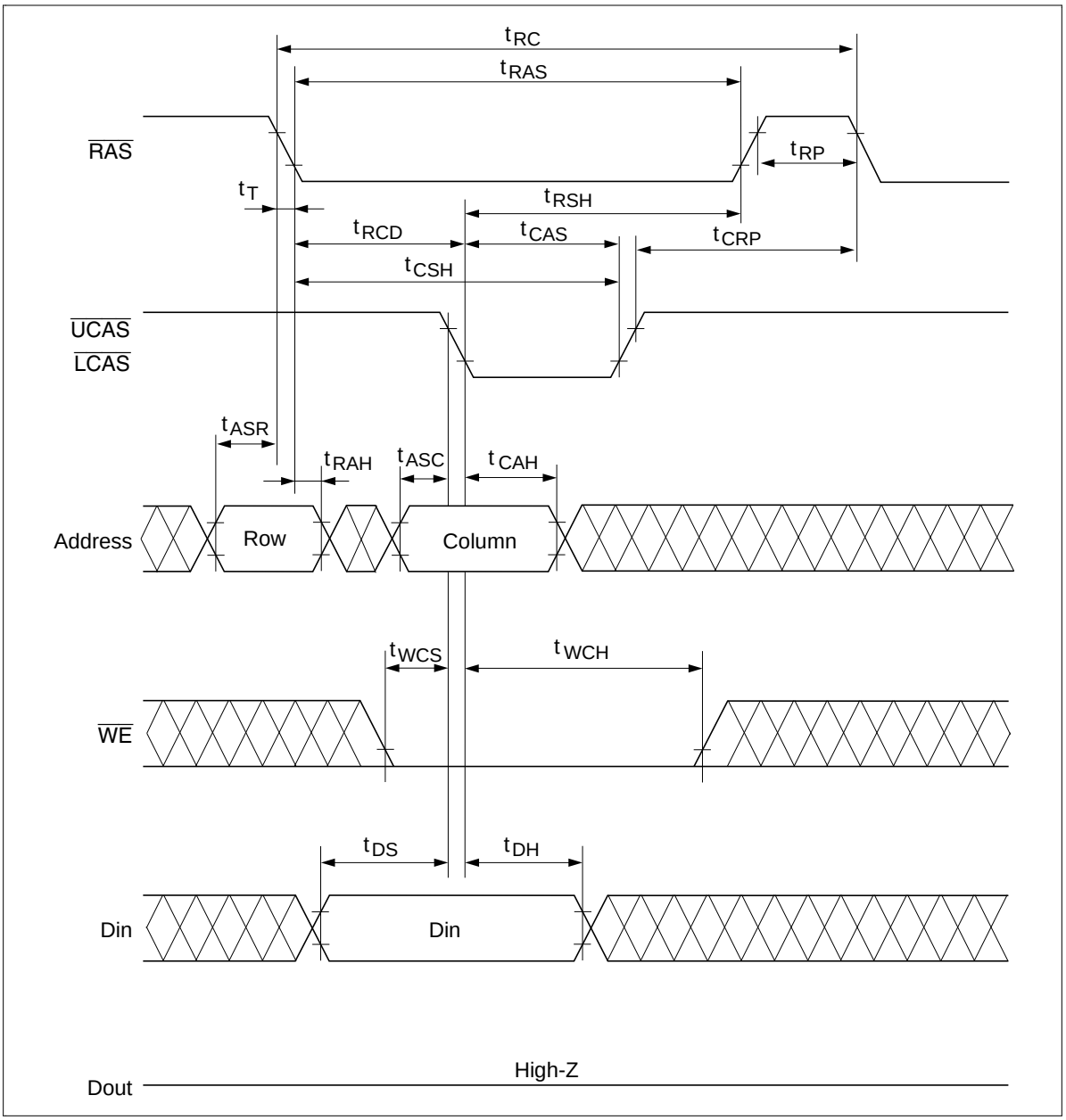
4. Byte control operation by remaining $\overline{UCAS}$ or $\overline{LCAS}$ high is guaranteed.

Timing Waveforms*[34]

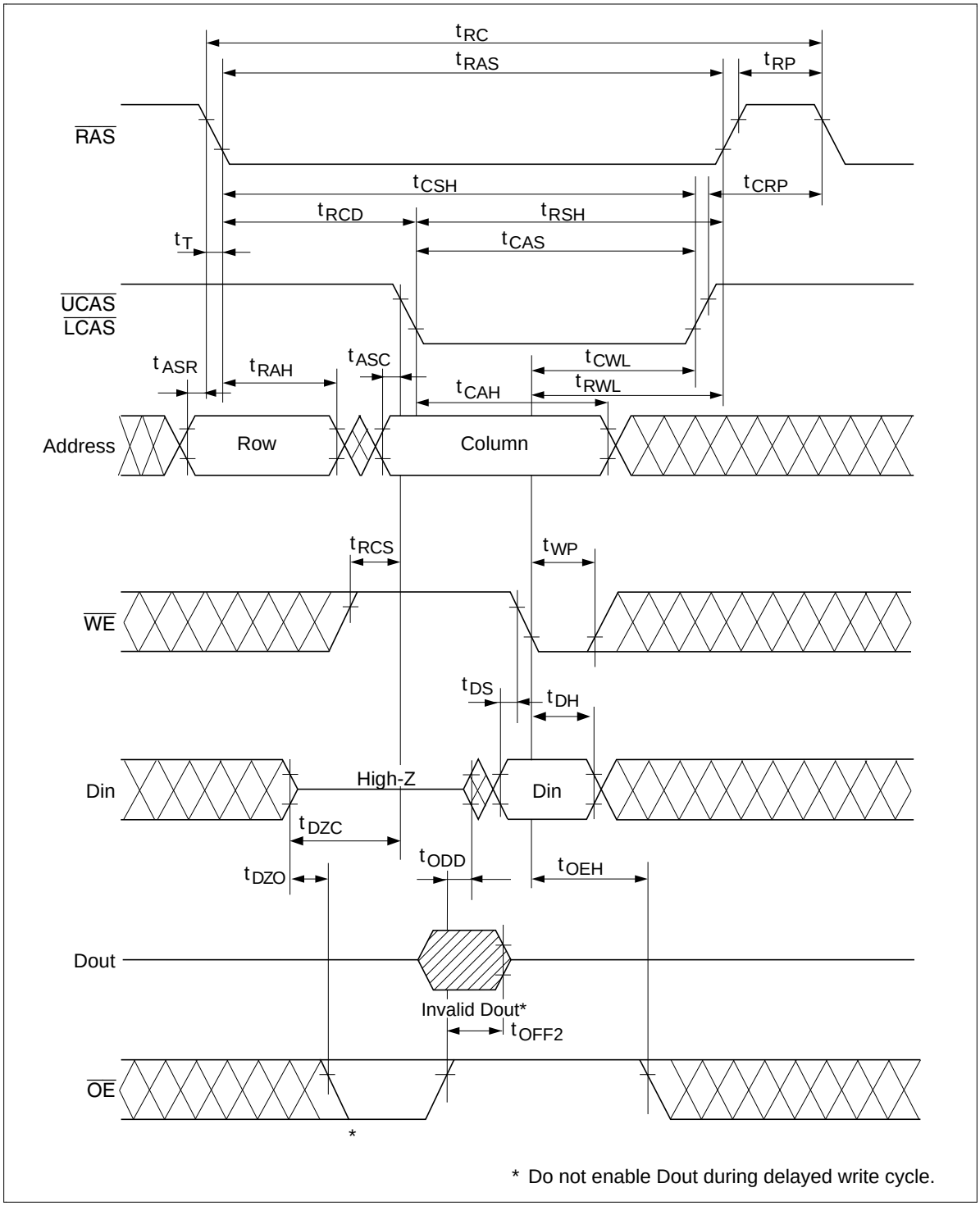
Read Cycle



Early Write Cycle

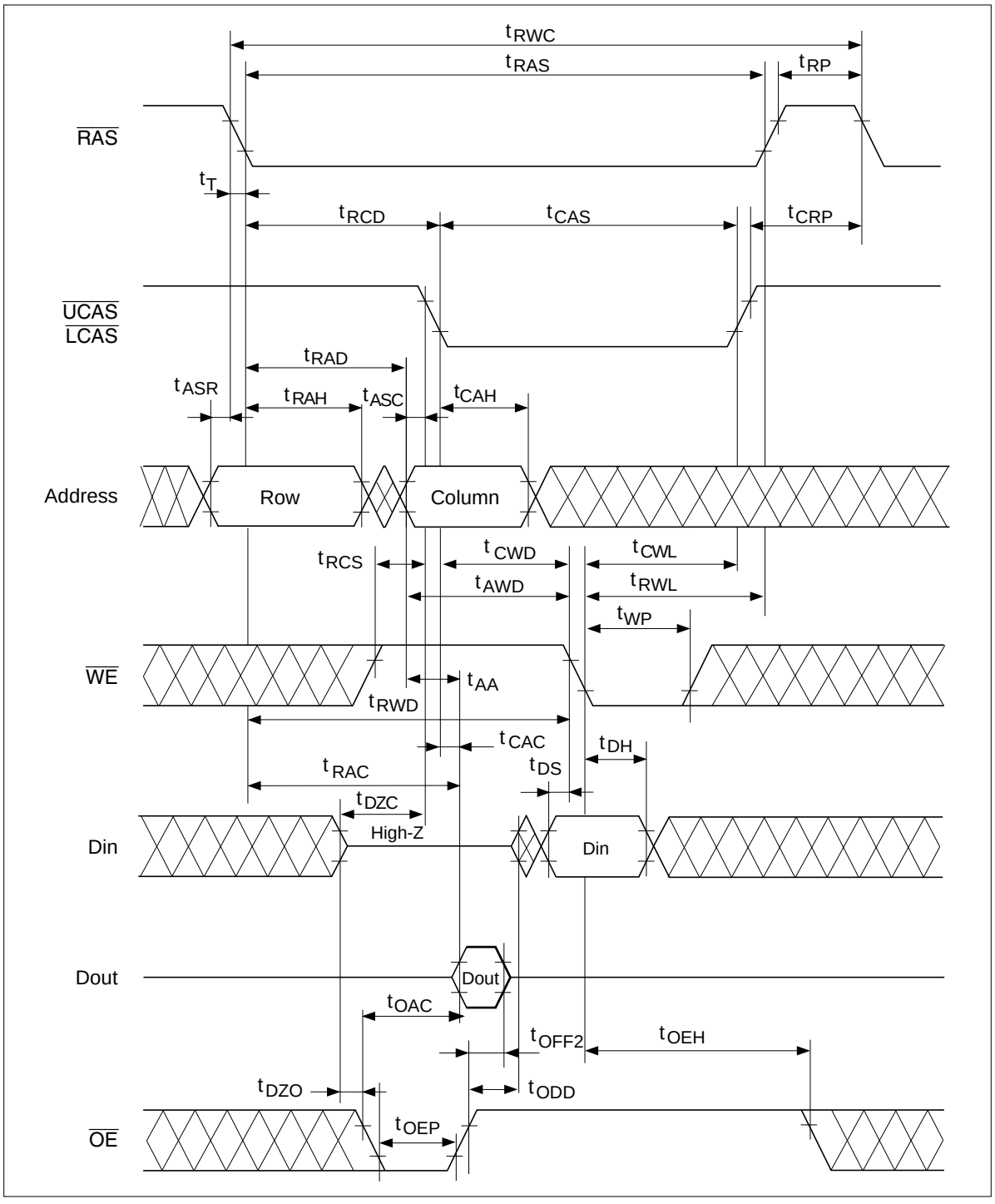


Delayed Write Cycle

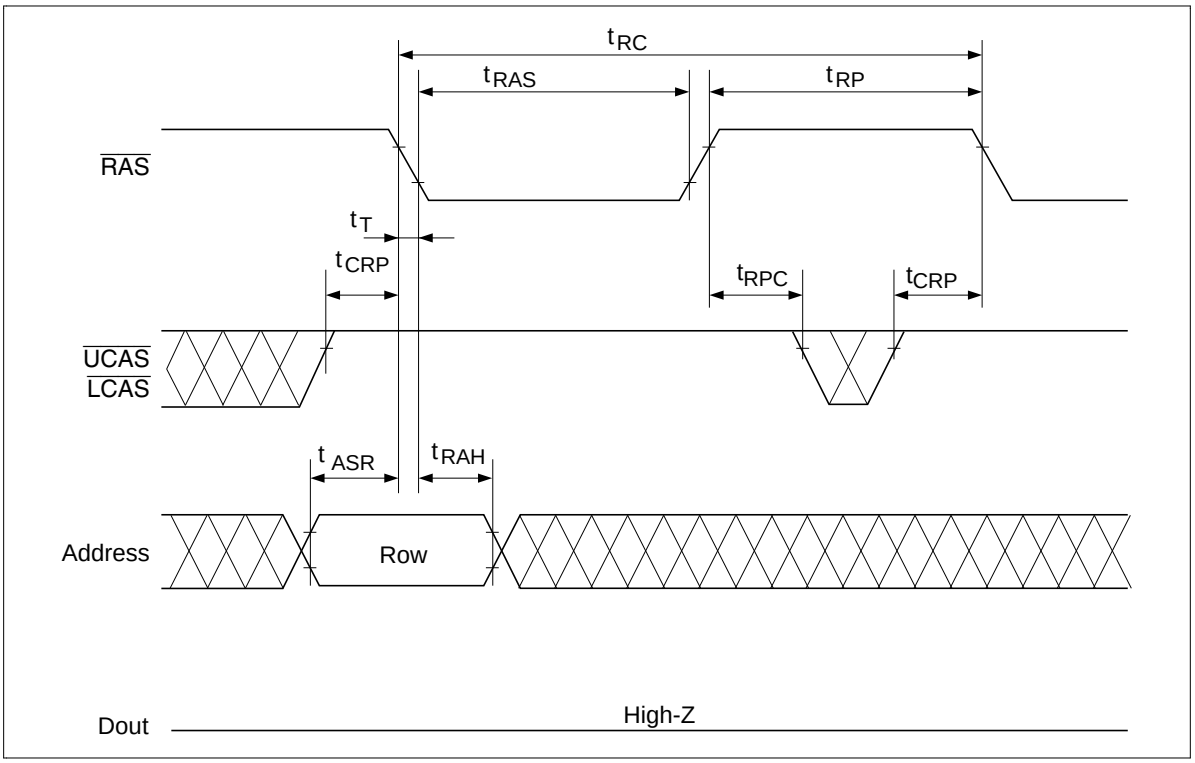


* Do not enable Dout during delayed write cycle.

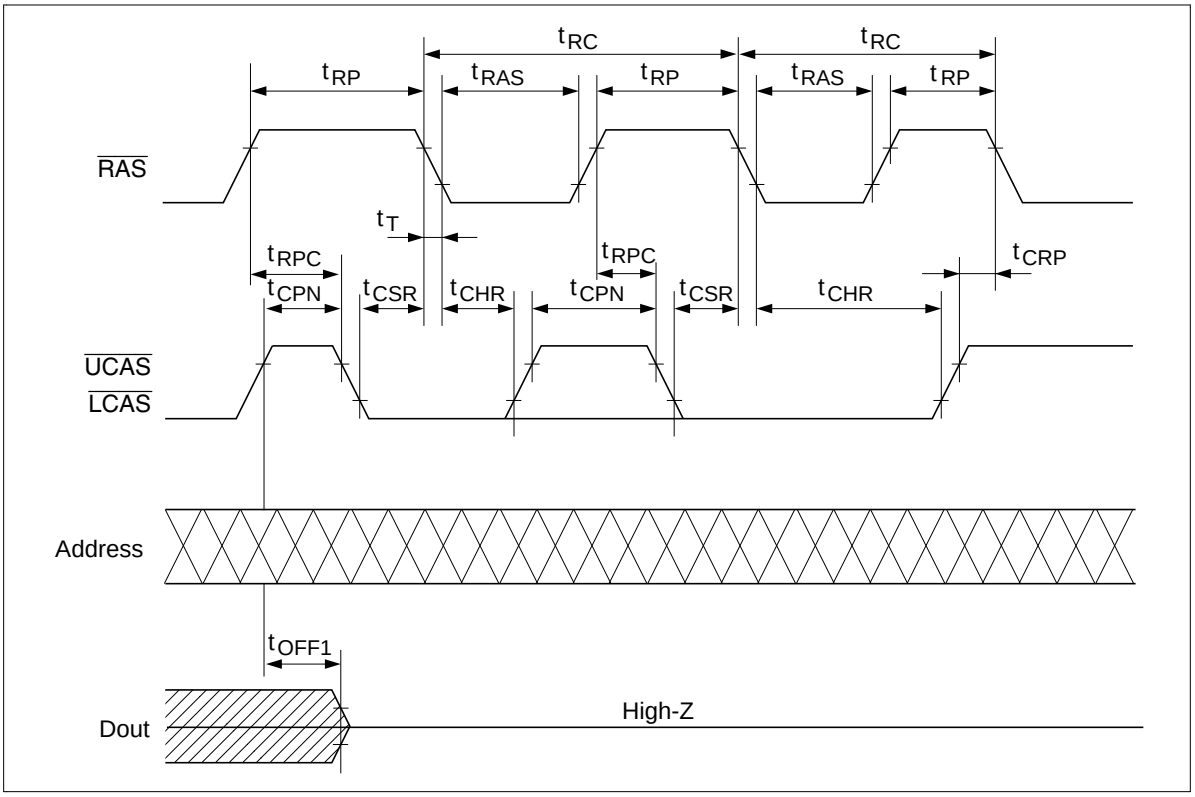
Read-Modify-Write Cycle



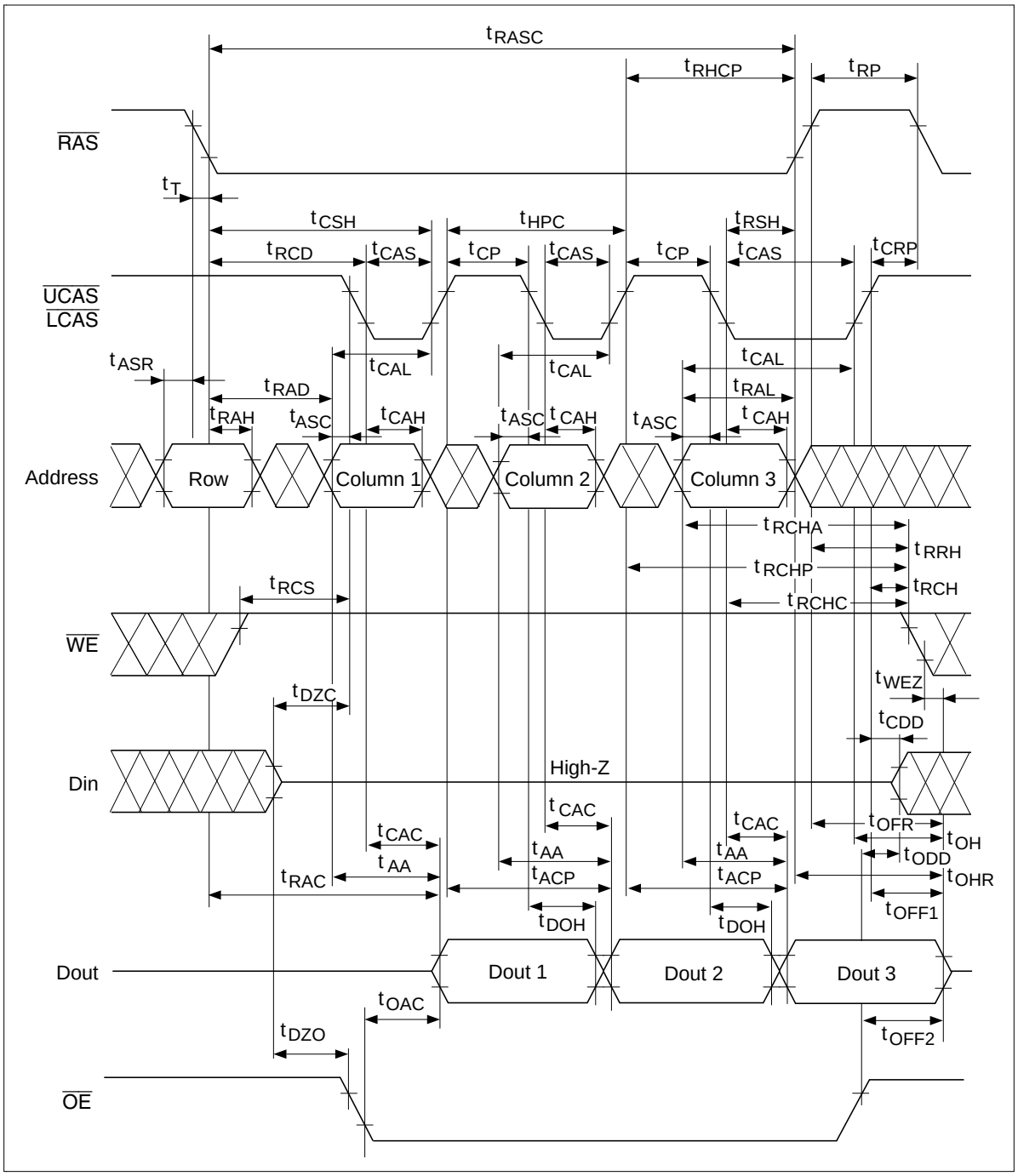
$\overline{\text{RAS}}$-Only Refresh Cycle



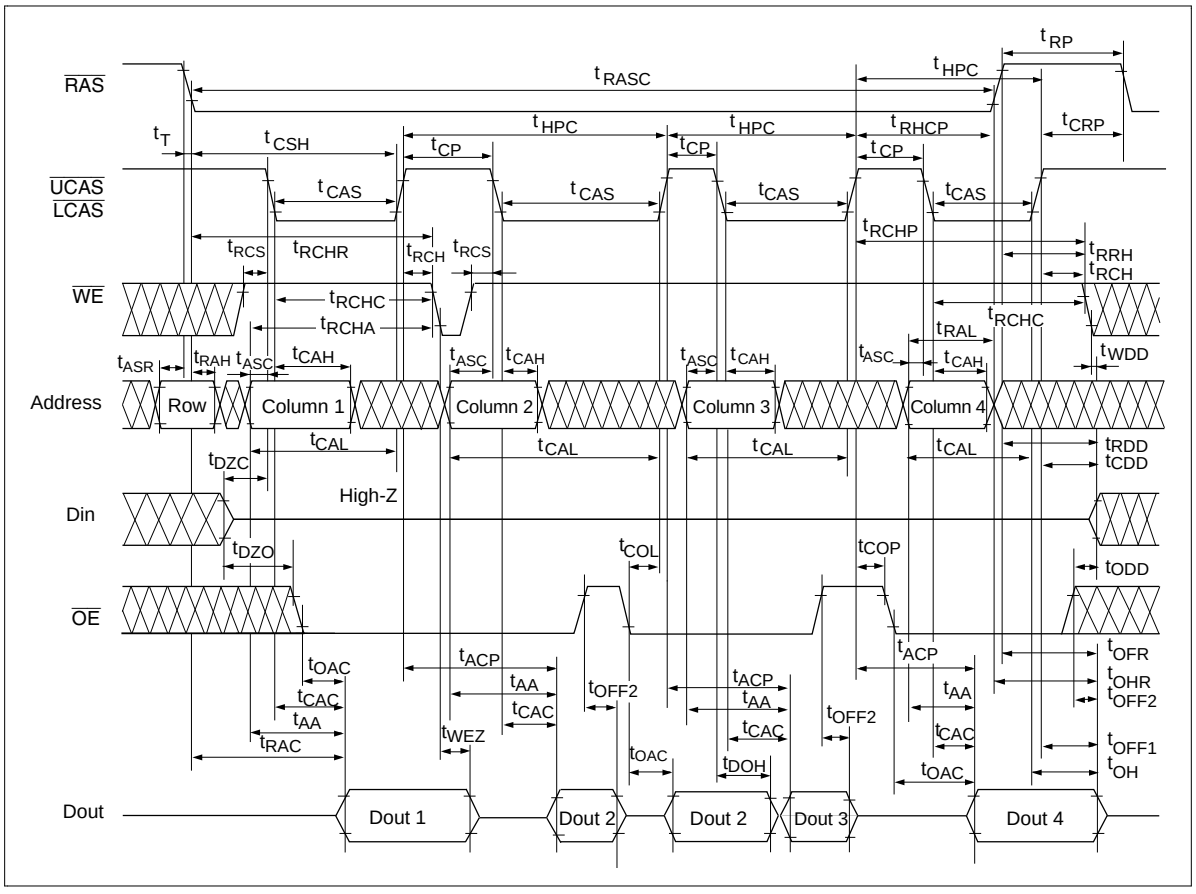
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



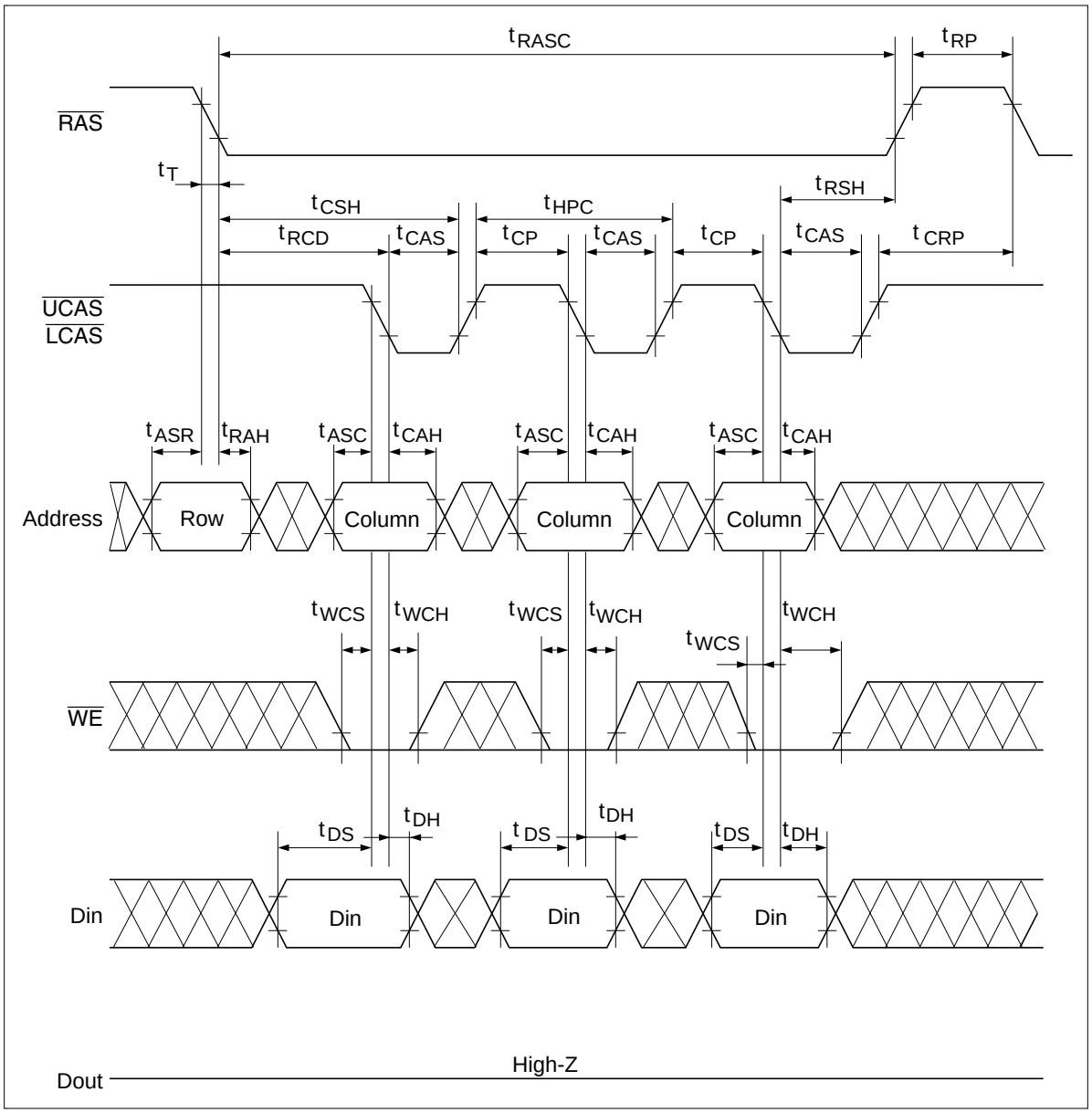
EDO Page Mode Read Cycle (t_{HPC} minimum cycle operation)



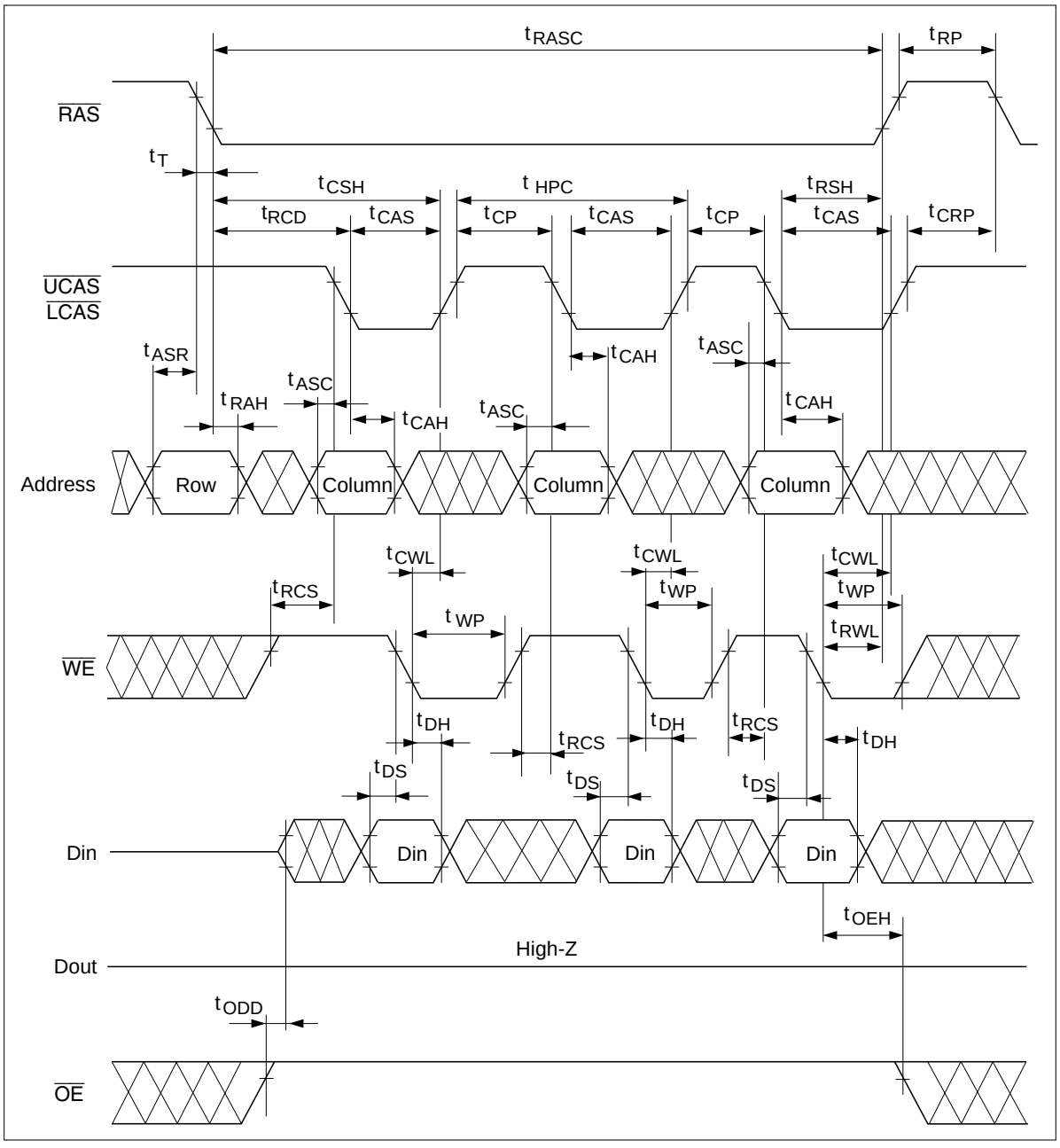
EDO Page Mode Read Cycle (High-Z control by $\overline{WE}$ and $\overline{OE}$)



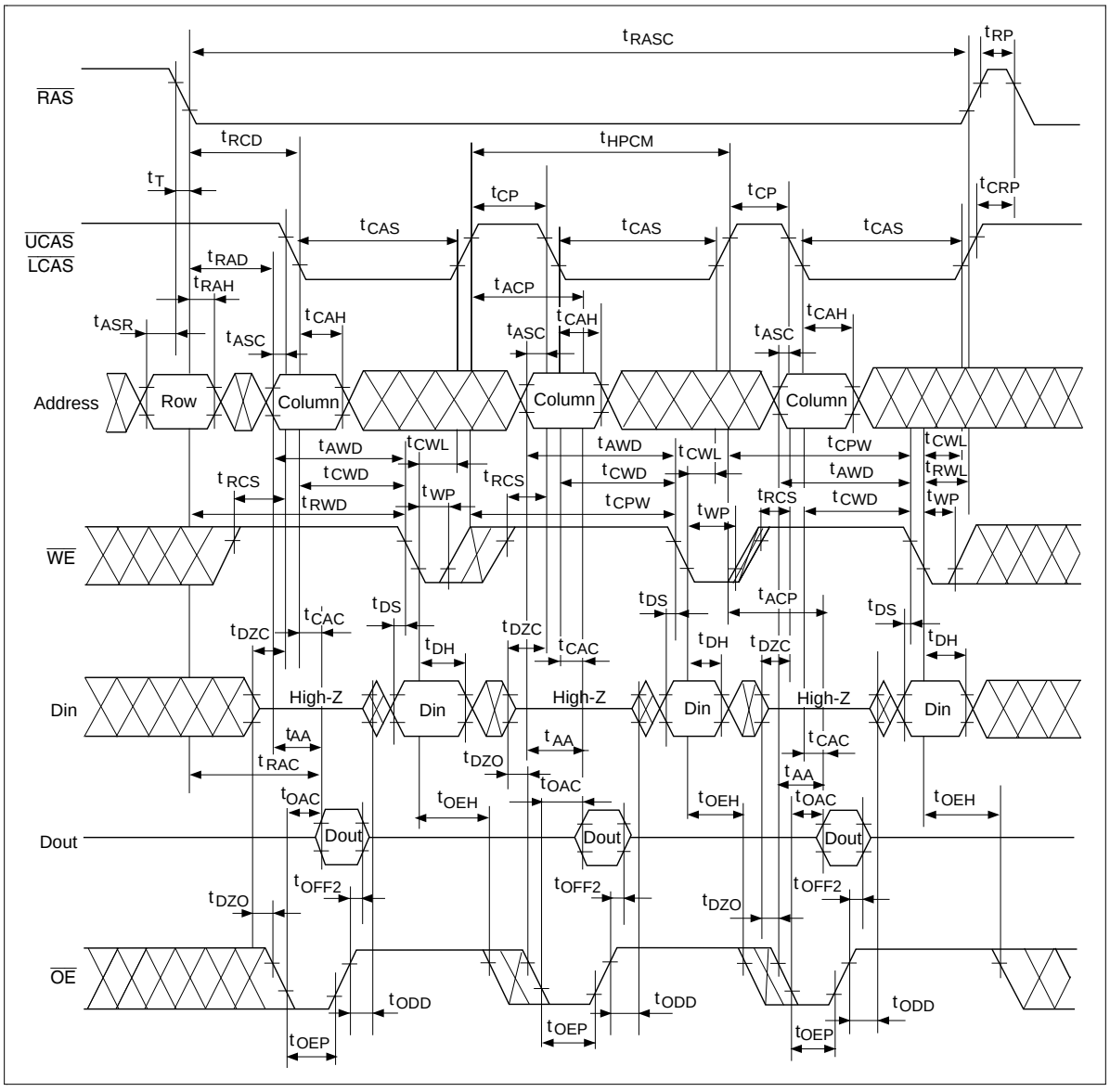
EDO Page Mode Early Write Cycle (t_{HPC} minimum cycle operation)



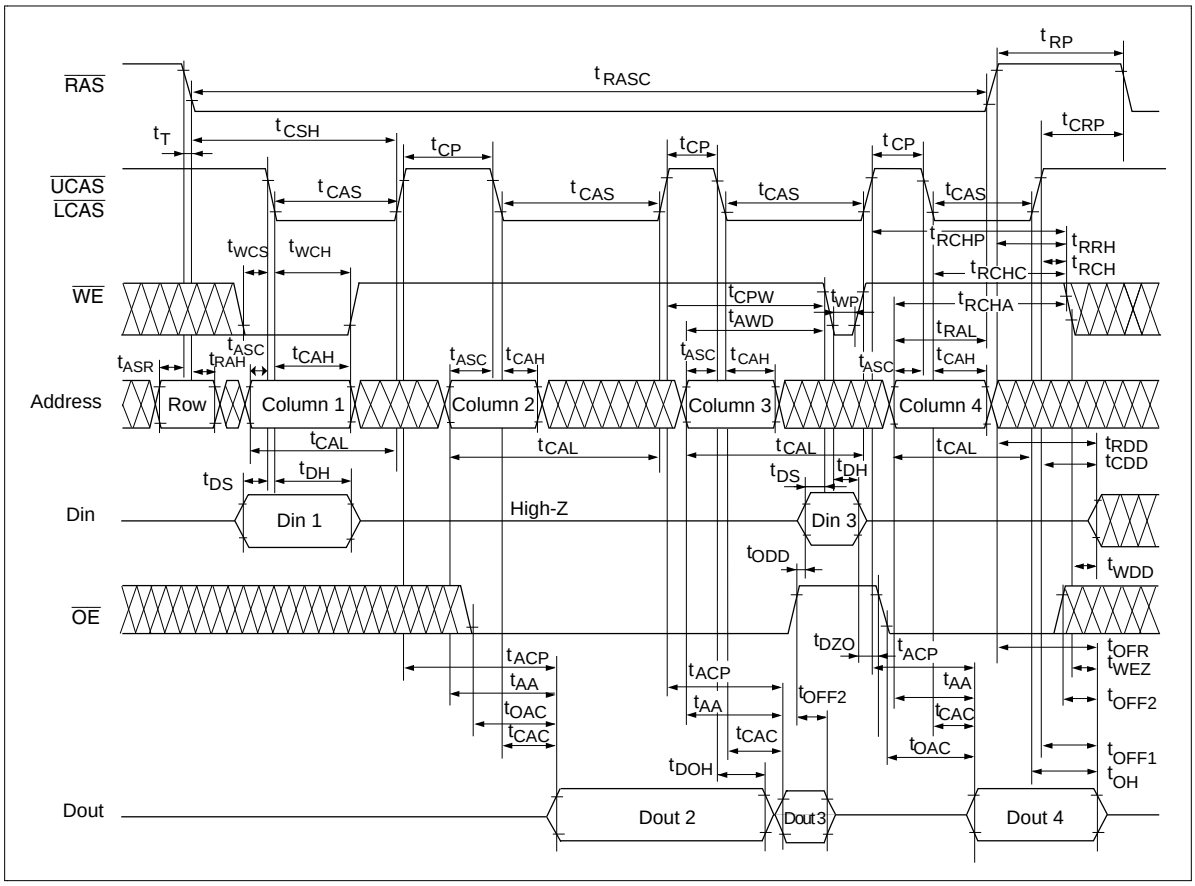
EDO Page Mode Delayed Write Cycle



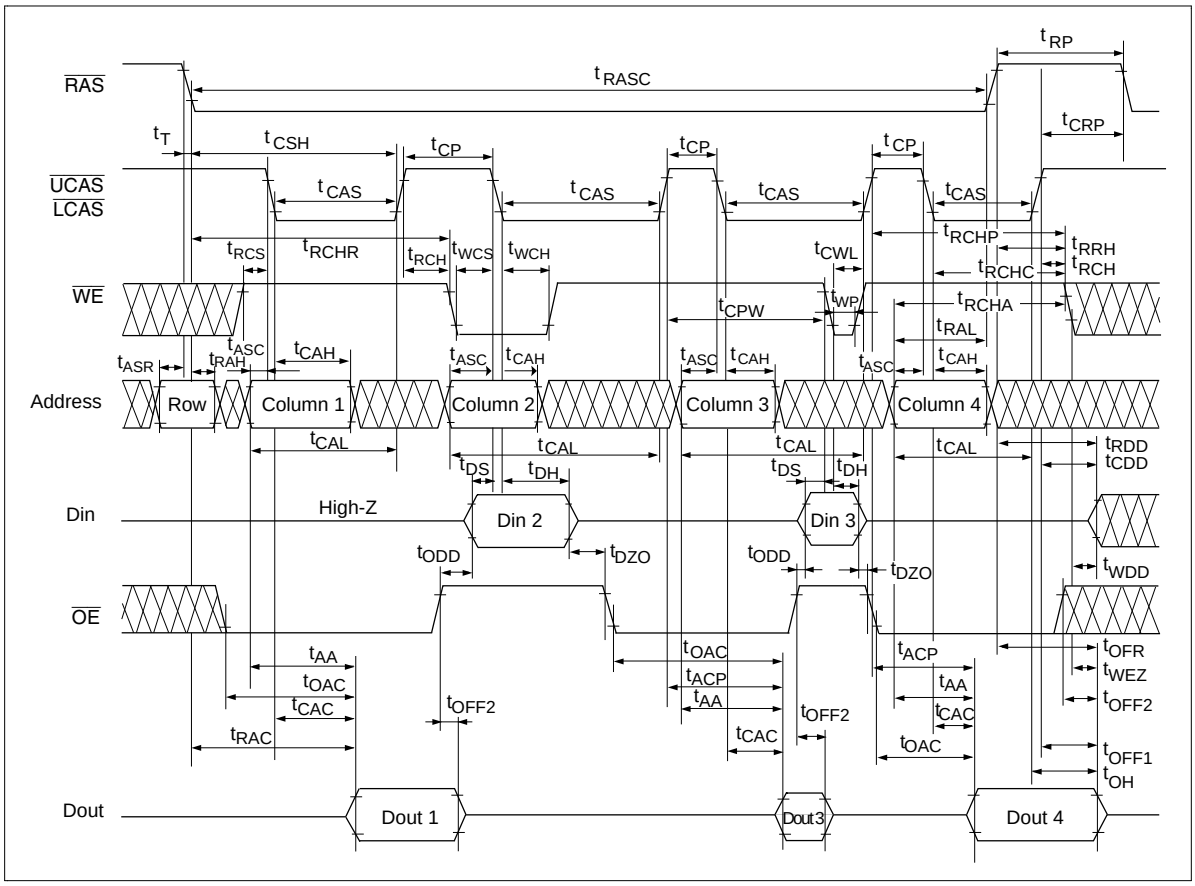
EDO Page Mode Read-Modify-Write Cycle



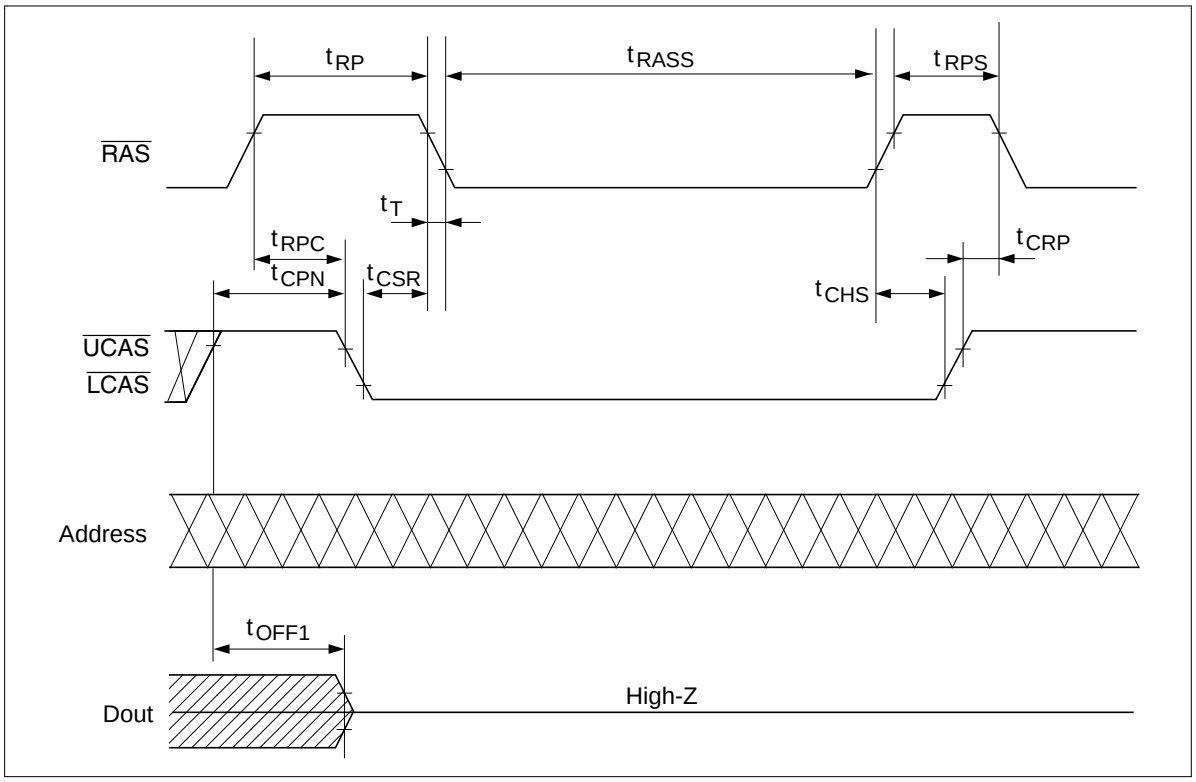
EDO Page Mode Mix Cycle (1)*[24]



EDO Page Mode Mix Cycle (2)*[24]

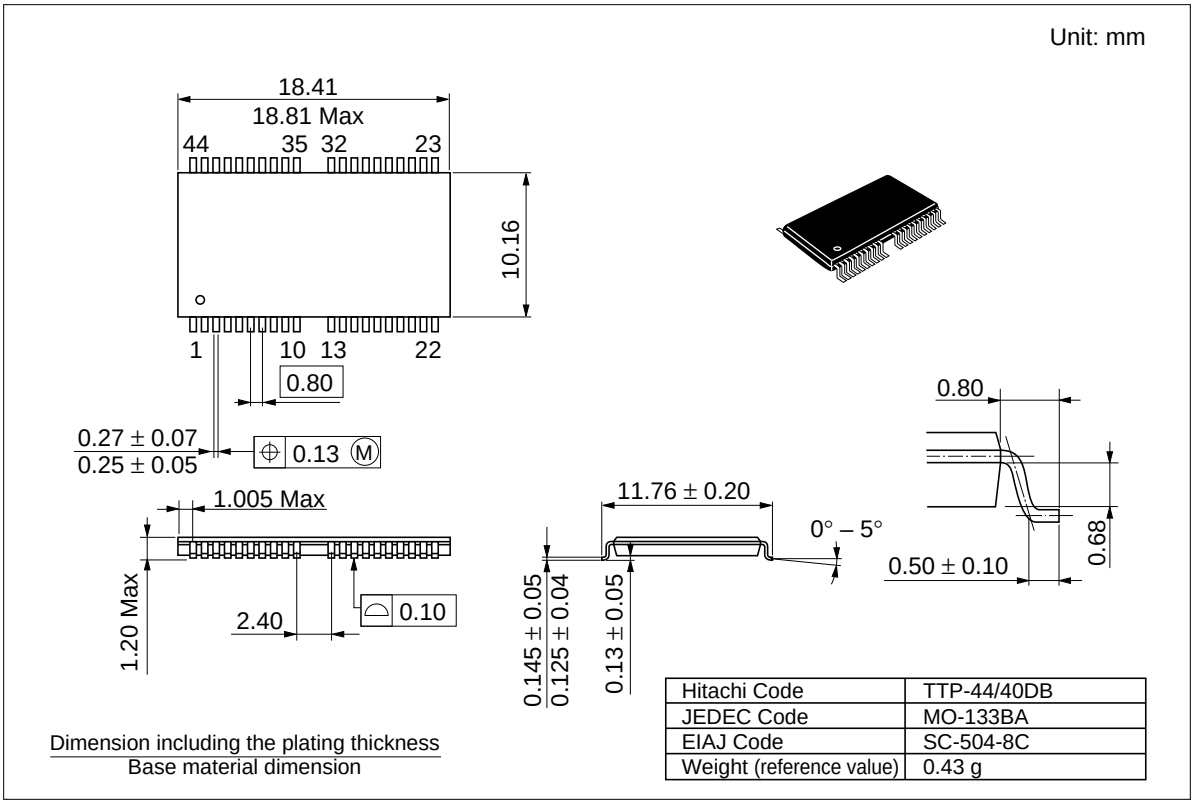


Self Refresh Cycle*[30, 31, 32, 33]



Package Dimensions

HM51W4265CTT/CLTT Series (TTP-44/40DB) Unit: mm



Hitachi Code	TTP-44/40DB
JEDEC Code	MO-133BA
EIAJ Code	SC-504-8C
Weight (reference value)	0.43 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Dec. 1, 1995	Initial issue	T. Oono	S. Suzuki
1.0	Jul. 31, 1996	Addition of HM51W4265C-6 Series AC Characteristics Change of note 25, 34 Addition of note 30 Notes concerning 2$\overline{CAS}$ control Addition of note 4 Timing waveforms Deletion of notes about undefined pins. Early write cycle. EDO pagemode early write cycle. $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{RAS}$- only refresh cycle. Self refresh cycle.	M. Tsunozaki	S. Suzuki
2.0	Jul. 10, 1997	Correct errors DC Characteristics Test conditions of I_{CC1}, I_{CC5}: $\overline{UCAS}$ or ... to $\overline{UCAS}$, ... Addition of note 5 AC Characteristics Correct numbers on tables t_{RPS} max: 130/130/130 ns to 110/130/150 ns Notes concerning 2$\overline{CAS}$ control Addition of description Timing waveforms Change order of waveforms $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle Read-modify-write cycle		