OMC942723078

H8 HITACHI SINGLE-CHIP MICROCOMPUTER
H8/300L Series

HITACHI

The Hitachi H8 Series of single-chip microcomputers consists of the H8/500 Series, the H8/300H Series, the H8/300 Series, and the H8/300L Series. These series have the following features.

H8/500: Highly orthogonal instructions, with an instruction set geared for high level languages
General register architecture
Up to 16-Mbyte address space

H8/300H: 16-Mbyte linear address space
16-bit general register architecture CPU that is upwardly compatible with the H8/300 family.
Concise instruction set
Powerful word-size and longword size arithmetic instructions

H8/300: Simple instruction (2- and 4-byte opcodes)
General register architecture
Concise instruction set
Power bit manipulation instructions
64-kbyte address space

H8/300L: Same CPU as the H8/300 Series
On-chip support functions geared for consumer applications
Low-voltage/low-power operation

This overview document describes all the products in the H8/300L series, briefly presenting their features, a functional overview, and the microcomputer development environment system.

The H8/300L Series are built around the H8/300L CPU core, and provide on chip a wealth of supporting functions for use in various application systems. These include ROM, RAM, timers, 14-bit PWM, serial communication interfaces, A/D converters, I/O ports, vacuum fluorescent display (VFD) controller/drivers, liquid crystal display (LCD) controller/ drivers, dual tone multi frequency (DTMF) generators, and multi-tone generators. These peripheral modules support the implementation of compact multi-function applications.

Introduction

The H8/300L Series are available in either mask ROM or ZTAT™* versions, the latter providing an on-chip PROM that can be programmed by the user.

Hitachi is working to provide a full, efficient development environment for a microcomputer application system. In addition to support software, the environment includes a stand-alone emulator that can be connected to a general purpose computer.

Note: * ZTAT™ is a trademark of Hitachi, Ltd.

Contents

Contents

1. Application Areas

Today, a wide range of electronic equipment, including TVs, VCRs, audio systems, telephones, refrigerators, washing machines, microwave ovens, and air conditioners, surrounds us in our daily life. Since the seventies these home appliances have seen continuous progress in terms of increased functionality and improved performance due to the use of 4-bit microcomputers with superlative cost-performance. During this period 4-bit microcomputers have seen both increased integration of memory and peripherals as well as cost reduction due to increased CPU performance and revolutions in semiconductor precision manufacturing technologies. As a result, 4-bit microcomputers have come to play a major role in supporting the development of new consumer products. However, the market has come to demand increased entertainment value and product satisfaction in consumer products. Simplified VCR programmability, powerful tape editing functions in audio equipment, neuro-fuzzy control of microwave ovens and washing machines, and improved man-machine interfaces (such as display functions) in all types of equipment are examples of this trend.

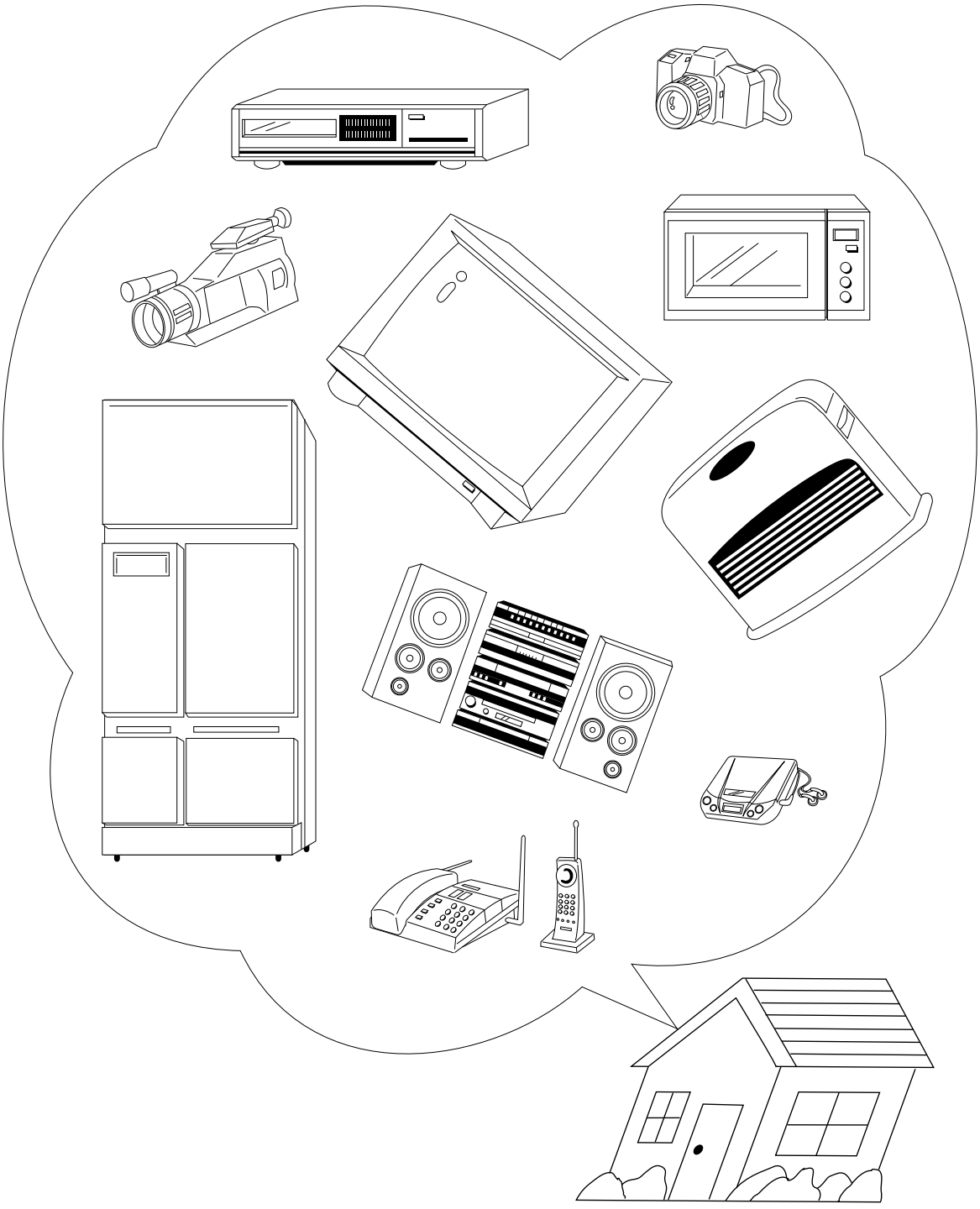
Microcomputers with a large scale program ROM (at least 16 kbytes), superlative arithmetic performance, and high processing speed are required to realize these new functions. From the implementors' standpoint, programming languages that support the efficient development of large-scale programs are required. However, from an architectural standpoint, the 4-bit microcomputer is limited both in arithmetic abilities and in software productivity. Now, the 8-bit CPU in the H8/300L Series has made its appearance to support improved functionality and performance in consumer equipment. The H8/300L CPU provides a 64-kbyte address space and the high speed performance of a 0.4 µs minimum instruction execution time. Furthermore, this CPU realizes high software productivity, since it supports standard (IEEE conforming) mnemonics and the highly efficient C programming language.

The H8/300L Series is a product line of microcomputers that takes this H8/300L CPU as their core and inherits and extends the consumer product oriented peripheral functions that were supported by Hitachi's 4-bit microcomputers. Peripheral functions provided by this series include vacuum fluorescent display (VFD) controller/drivers, liquid crystal display (LCD) controller/drivers, A/D converters, D/A converters, synchronous and asynchronous serial communication interfaces (SCI), tone generators for telephone and radio equipment, PWM, and a wide variety of timers. The H8/300L Series product line consists of products that combine sets of these modules appropriate for particular applications.

What is the H8/300L Series?

The Significance of Lower Voltage and Lower Power

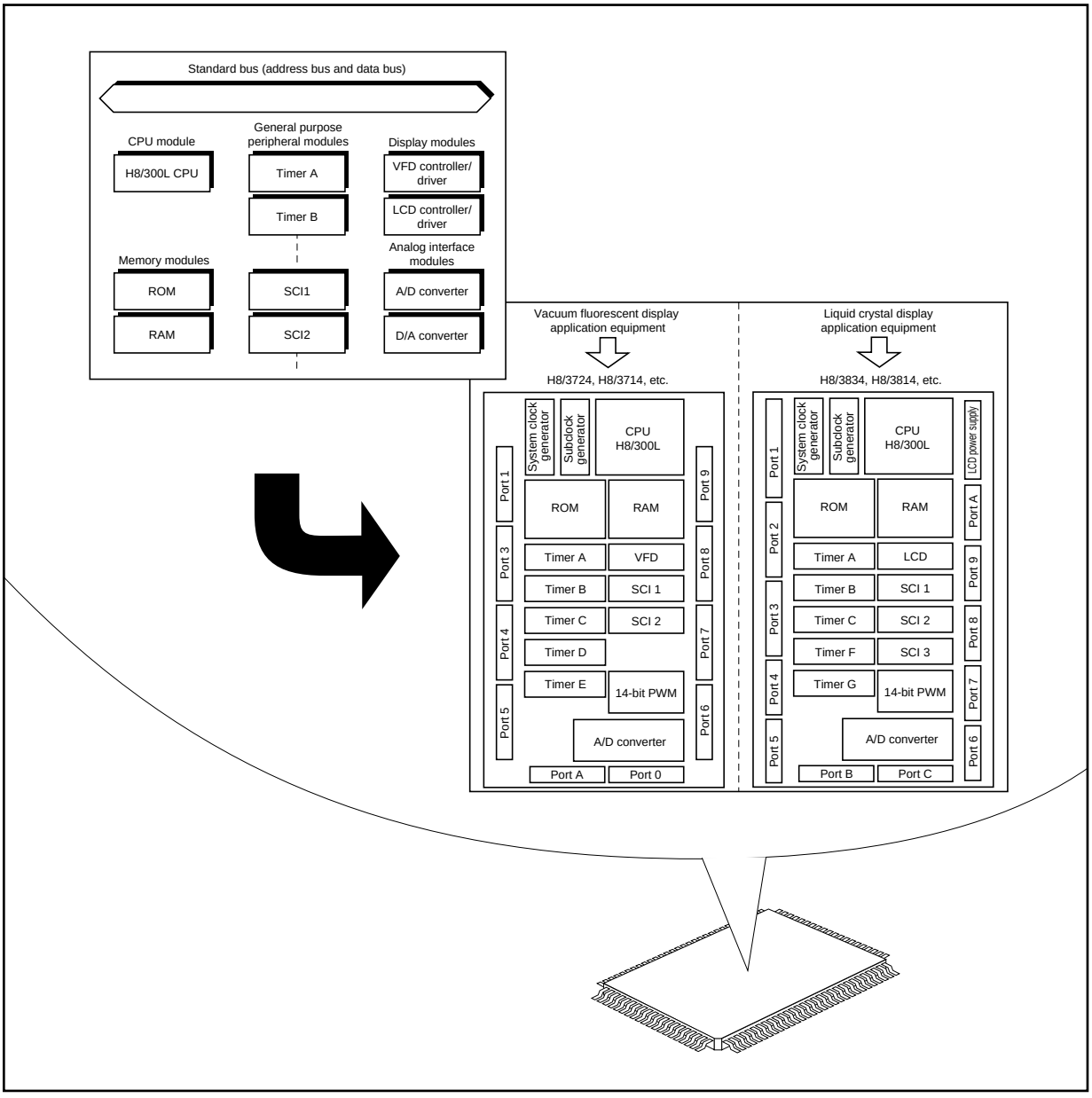
In addition to the increased performance discussed above, contemporary consumer and portable electronic equipment also requires lower voltage and lower power operation. This is because increased battery life is desired in portable equipment such as cordless telephones, and extended backup operating periods are desired in equipment that uses line power. Since the H8/300L Series microcomputers not only support operation at 2.7 V, but also support a rich variety of low power modes, including 32-kHz subclock based operation, they can contribute to reduced voltage and lower power application systems.



2. ASSP Based Approach

The members of the H8/300L Series include on-chip peripheral functions that are optimal for particular applications.

The microcomputers in the H8/300L Series consist of an H8/300L CPU module, a standard bus to which the on-chip modules are connected, and some number of modules, such as ROM/RAM, VFD/LCD controller/driver, A/D and D/A converter, and I/O port including general purpose I/O ports and high current I/O ports. Thus each product in this series integrates the modules required to form that product. This approach allows us to develop products that are optimal for a particular application area.



3. ZTAT™ Microcomputers

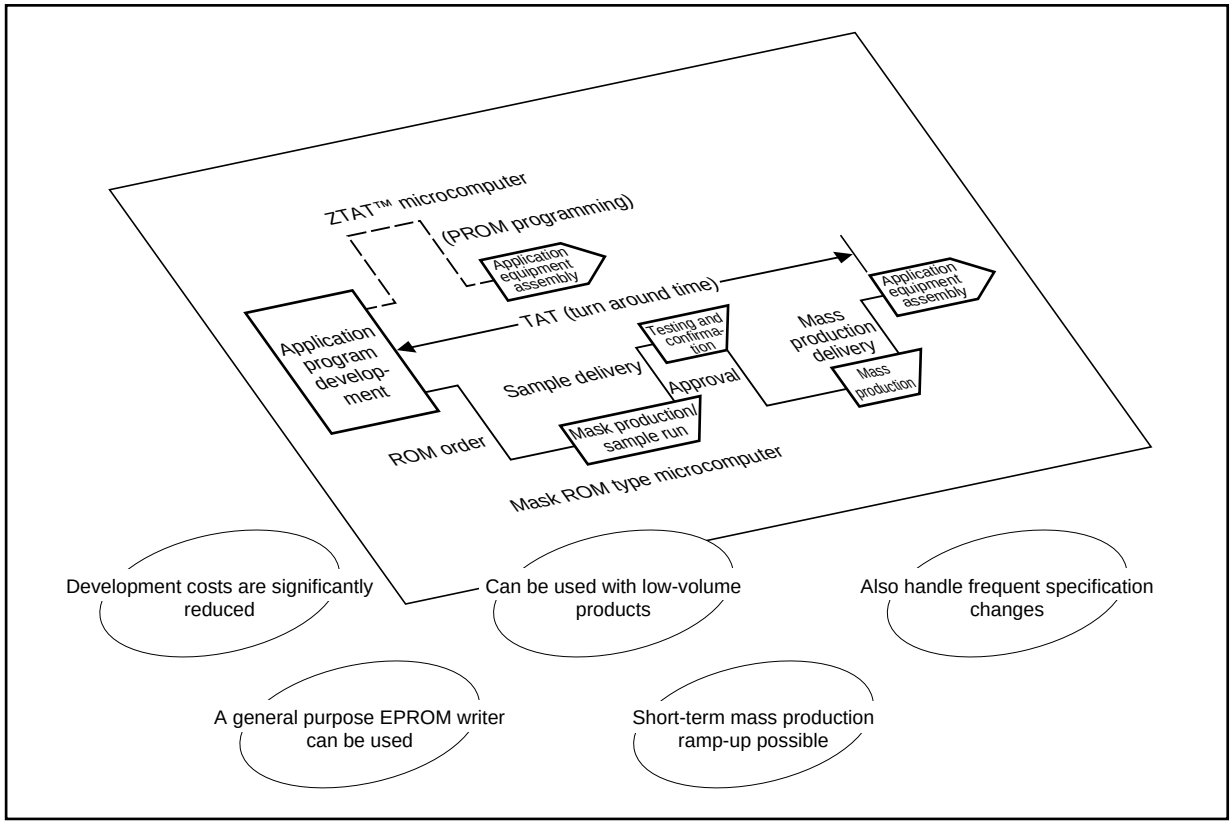
Hitachi proposed the new concept of the ZTAT™ (zero turn around time) microcomputer in 1984, and began shipping ZTAT™ products that year.

ZTAT™ microcomputers are microcomputers that include user-programmable PROM on-chip. Since these microcomputers allow completed programs to be written to PROM at the user's site, the waiting time until a completed LSI is obtained, which had previously been required in the development process, was reduced to zero. This allows rapid and flexible handling of the customer's product development.

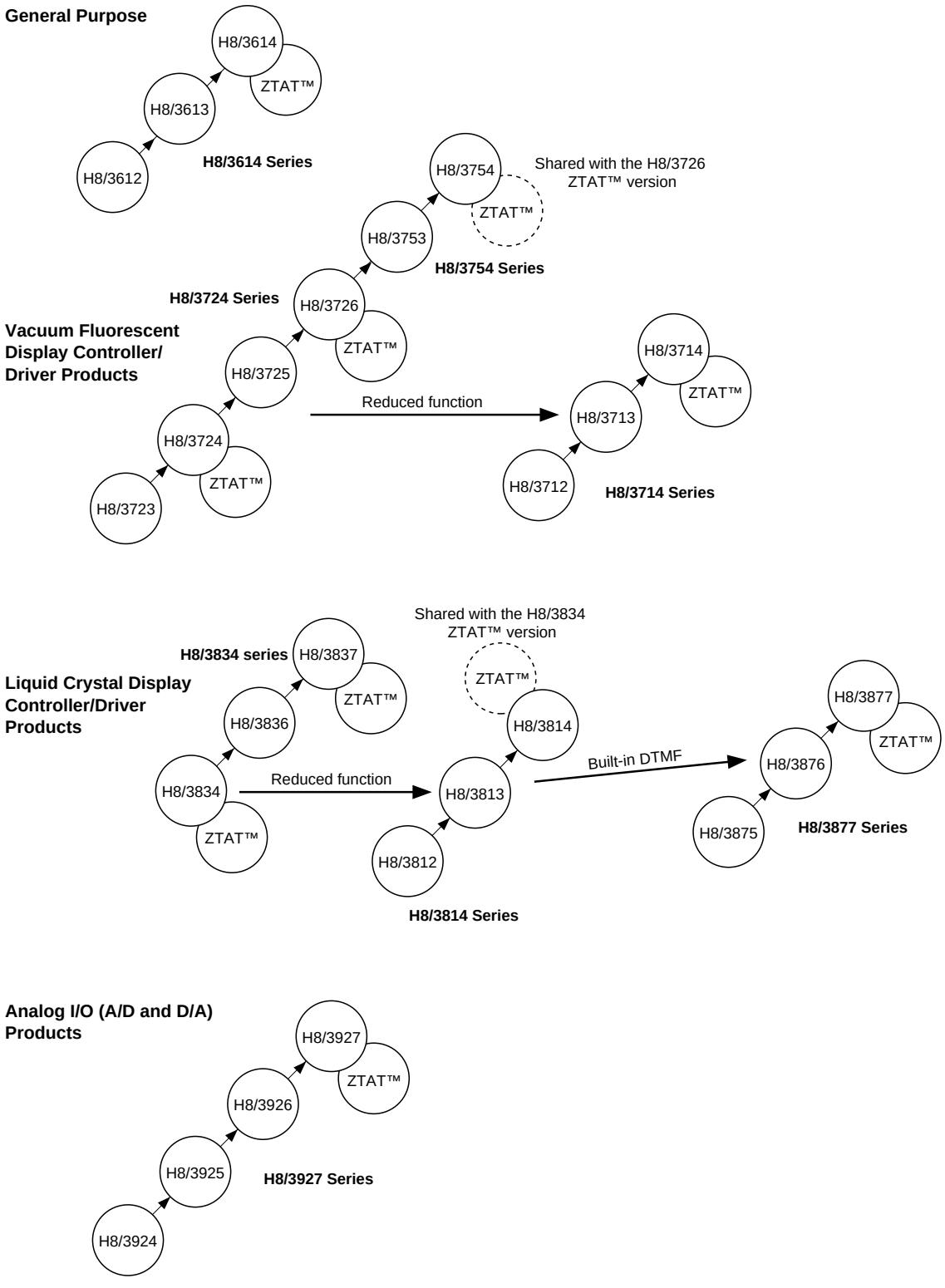
ZTAT™ microcomputers provide an ideal response to the demands of markets in which new product development competition is accelerating and that require reduced development times and value added functions not available from other companies.

A Large Reduction in TAT is Possible

The ZTAT™ microcomputers do away with the time required for mark production, testing, and confirmation required by earlier microcomputers. Furthermore, ZTAT™ microcomputers can quickly handle situations where the program changes occur during the process.



Product Line



<Notation>
DTMF: Dual tone multi frequency

Product	ROM						RAM						ZTAT™	Timers*							14-Bit PWM	SCI			8-Bit A/D Converter	8-Bit D/A Converter	Vacuum Fluorescent Display Controller/Driver	Liquid Crystal Display Controller/Driver	Dual Tone Multi Frequency Generator	Multi-Tone Generator	Package						Reference Page
	16 kbytes	24 kbytes	32 kbytes	40 kbytes	48 kbytes	60 kbytes	256 bytes	384 bytes	512 bytes	640 bytes	1 kbyte	2 kbytes		Clock Timer	Reload Timer	Event Counter	Up/Down Counter	Output Compare Function	Input Capture Function	Watchdog Timer		Synchronous Type	32-Byte Data Transfer	Synchronous/Asynchronous							DP-64S	FP-64A	FP-80A	FP-80B	FP-100A	FP-100B	
H8/3612	●								●					●	●	●	●				●	●	●		●						●	●					55
H8/3613		●									●			●	●	●	●				●	●	●		●						●	●					55
H8/3614			●								●		●	●	●	●	●				●	●	●		●						●	●					55
H8/3712	●							●						●	●	●	●				●	●	●		●		●				●	●					58
H8/3713		●						●						●	●	●	●				●	●	●		●		●				●	●					58
H8/3714			●						●				●	●	●	●	●				●	●	●		●		●				●	●					58
H8/3723		●						●						●	●	●	●				●	●	●		●		●						●	●			61
H8/3724			●						●				●	●	●	●	●				●	●	●		●		●						●	●			61
H8/3725				●						●				●	●	●	●				●	●	●		●		●						●	●			61
H8/3726					●						●		●	●	●	●	●				●	●	●		●		●						●	●			61
H8/3753		●									●			●	●	●	●				●	●	●		●		●						●	●			64
H8/3754			●								●			●	●	●	●				●	●	●		●		●						●	●			64
H8/3812	●								●					●		●		●	●			●		●	●			●							●	●	67
H8/3813		●							●					●		●		●	●			●		●	●			●							●	●	67
H8/3814			●						●					●		●		●	●			●		●	●			●							●	●	67
H8/3834			●								●		●	●	●	●	●	●	●		●	●	●	●	●			●							●	●	70
H8/3836					●							●		●	●	●	●	●	●		●	●	●	●	●			●							●	●	70
H8/3837						●						●	●	●	●	●	●	●	●		●	●	●	●	●			●							●	●	70
H8/3875				●								●		●		●		●	●			●		●	●			●	●	●						●	73
H8/3876					●							●		●		●		●	●			●		●	●			●	●	●						●	73
H8/3877						●						●	●	●		●		●	●			●		●	●			●	●	●						●	73
H8/3924			●								●			●	●	●	●	●	●	●	●	●			●	●								●			76
H8/3925				●							●			●	●	●	●	●	●	●	●	●			●	●								●			76
H8/3926					●						●			●	●	●	●	●	●	●	●	●			●	●								●			76
H8/3927						●					●		●	●	●	●	●	●	●	●	●	●			●	●								●			76

Note: * Refer to the function table for the number of timers.

Function Table

			H8/3612	H8/3613	H8/3614	H8/3712	H8/3713	H8/3714	H8/3723	H8/3724	H8/3725	H8/3726	H8/3753	H8/3754
Memory	ROM	Mask ROM	16 kbytes	24 kbytes	32 kbytes	16 kbytes	24 kbytes	32 kbytes	24 kbytes	32 kbytes	40 kbytes	48 kbytes	24 kbytes	32 kbytes
		ZTAT™	—	—	●	—	—	●	—	●	—	●	—	—
	RAM		512 bytes	1 kbyte		384 bytes	384 bytes	512 bytes	384 bytes	512 bytes	640 bytes	1 kbyte	1 kbyte	1 kbyte
Timers	Clock timer		1 channel			1 channel			1 channel					
	Reload timer		3 channels			3 channels			3 channels					
	Event counter		3 channels (of which 2 also function as reload timers)			3 channels (of which 2 also function as reload timers)			3 channels (of which 2 also function as reload timers)					
	Up/down counter		1 channel (also functions as an event counter)			1 channel (also functions as an event counter)			1 channel (also functions as an event counter)					
	Output compare function		—			—			—					
	Input capture function		—			—			—					
	Watchdog timer		—			—			—					
14-bit PWM			—	1 channel		1 channel			1 channel					
SCI	Synchronous		2 channels			2 channels			2 channels					
	Multi-byte data transfer		1 channel[*1] (however, also functions as the synchronous interface)			1 channel[*1] (however, also functions as the synchronous interface)			1 channel[*1] (however, also functions as the synchronous interface)					
	Asynchronous/ synchronous		—			—			—					
8-bit A/D converter			8 channels			8 channels			8 channels					
8-bit D/A converter			—			—			—					
Vacuum fluorescent display controller/driver function			—			Built-in VFD controller/driver 16 segments × 16 digits[*2]			Built-in VFD controller/driver 20 segments × 16 digits[*2]					
Liquid crystal display controller/driver function			—			—			—					
High current drive pins			6 lines			32 lines			36 lines					
Dual tone multi frequency generator			—			—			—					
Multi-tone generator			—			—			—					
Package			DP-64S/FP-64A			DP-64S/FP-64A			FP-80A/FP-80B					
Minimum instruction execution time			0.48 µsec			0.48 µsec			0.48 µsec					
Maximum operating frequency			4.19 MHz			4.19 MHz			4.19 MHz					
Operating voltage			2.7 V to 5.5 V			2.7 V to 5.5 V			2.7 V to 5.5 V					
Target applications			General purpose			AV equipment such as VCRs and CD players, home appliances such as microwave ovens			AV equipment such as VCRs, LD players and CD players, communication equipment such as telephones					

Notes: 1. Automatic transfer of up to 32 bytes of data.
2. Of the digit lines, 8 can also be used as segments.

	H8/3812	H8/3813	H8/3814	H8/3834	H83836	H8/3837	H8/3875	H8/3876	H8/3877	H8/3924	H8/3925	H8/3926	H8/3927
	16 kbytes	24 kbytes	32 kbytes	32 kbytes	48 kbytes	60 kbytes	40 kbytes	48 kbytes	60 kbytes	32 kbytes	40 kbytes	48 kbytes	60 kbytes
	—	—	—	●	—	●	—	—	●	—	—	—	●
	512 bytes	512 bytes	512 bytes	1 kbyte	2 kbytes	2 kbytes	2 kbytes	2 kbytes	2 kbytes	1 kbyte	1 kbyte	1 kbyte	1 kbyte
	1 channel			1 channel			1 channel			1 channel			
	—			2 channels			—			4 channels			
	1 channel (16-bit or 8-bit, also functions as output-compare channel)			3 channels (also function as reload timers, and as output-compare channels)			1 channel (16-bit or 8-bit, also functions as output-compare channel)			2 channels (also function as reload timers)			
	—			1 channel (also functions as an event counter)			—			1 channel (also functions as an event counter)			
	16 bits × 1 channel (or 8 bits × 2 channels)			16 bits × 1 channel (or 8 bits × 2 channels)			16 bits × 1 channel (or 8 bits × 2 channels)			16 bits × 2 channels, 8 bits × 2 channels			
	8 bits × 2 channels			8 bits × 2 channels			8 bits × 2 channels			16 bits × 4 channels			
	—			—			—			1 channel			
	—			1 channel			—			1 channel			
	1 channel			2 channels			1 channel			2 channels			
	—			1 channel*1 (however, also functions as the synchronous interface)			—			1 channel*1 (however, also functions as the synchronous interface)			
	1 channel			1 channel			1 channel			—			
	12 channels			12 channels			8 channels			8 channels			
	—			—			—			4 channels			
	—			—			—			—			
	Built-in LCD controller/driver 4 common lines × 40 segments			Built-in LCD controller/driver 4 common lines × 40 segments			Built-in LCD controller/driver 4 common lines × 52 segments			—			
	16 lines			16 lines			16 lines			8 lines			
	—			—			1.2 MHz to 10 MHz in 400 kHz increments			—			
	—			—			40 Hz to 4000 Hz			—			
	FP-100A/FP-100B			FP-100A/FP-100B			FP-100B			FP-80B			
	0.4 µsec			0.4 µsec			0.4 µsec			0.4 µsec			
	5 MHz			5 MHz			5 MHz			5 MHz			
	2.7 V to 5.5 V			2.7 V to 5.5 V			2.7 V to 5.5 V			2.7 V to 5.5 V			
	Portable electronic equipment, SLRs, compact cameras, cordless telephones			Portable electronic equipment, SLRs, compact cameras, cordless telephones			Communication equipment and other similar applications			VCRs and similar equipment			

1. Vacuum Fluorescent Display Controller/Driver (H8/3714 Series, H8/3724 Series, and H8/3754 Series)

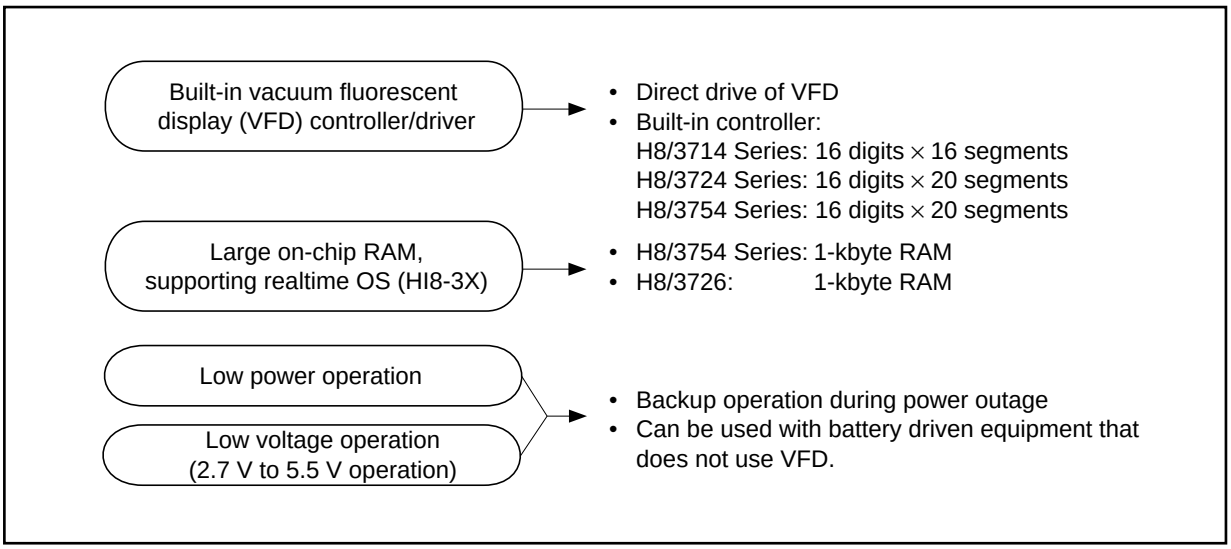
Features

Hitachi, Ltd. provides the 64-pin package H8/3714 Series and the 80-pin package H8/3724 Series and H8/3754 Series as built-in vacuum fluorescent display (VFD) controller/driver microcomputers for use with applications incorporating fluorescent display. The H8/3714 Series provides 16 kbytes to 32 kbytes of on-chip ROM, H8/3724 Series provides 24 kbytes to 48 kbytes, and the H8/3754 Series provides 24 kbytes to 32 kbytes.

The VFD controller/driver consists of display RAM, a display control circuit, and 40 V high breakdown voltage drivers. Vacuum fluorescent display can be driven directly by simply storing data corresponding to the segments to be driven in display RAM.

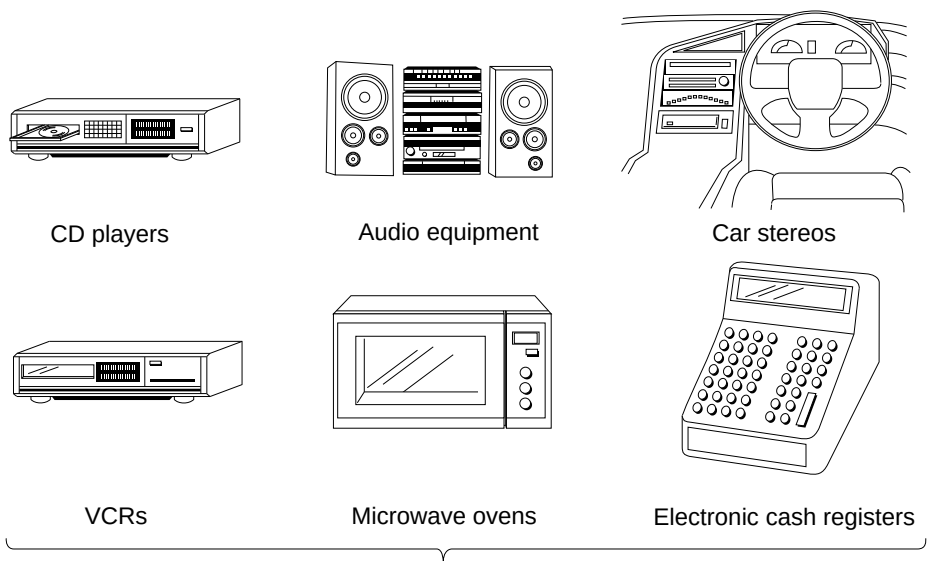
These microcomputers provide on-chip five types of timer, a 14-bit PWM, two serial communication interface channels, and an 8-channel A/D converter as additional peripheral functions.

Furthermore, these microcomputers support low voltage operation (2.7 V) and a rich set of low power modes including microcomputer operation from a 32 kHz subclock making these products optimal for applications which require backup operation during power outages or battery operation.



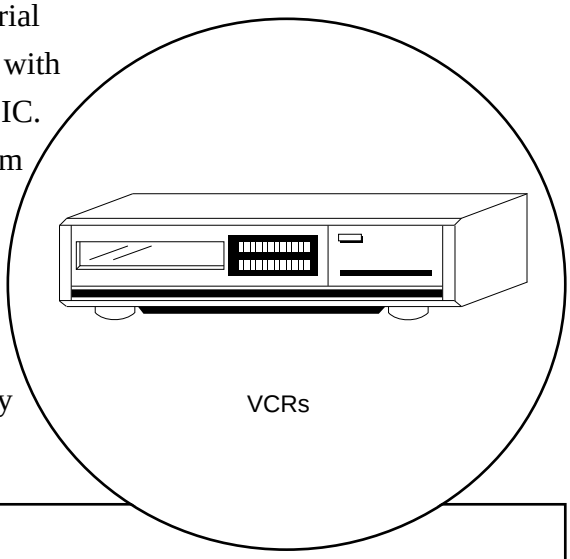
Possible Applications

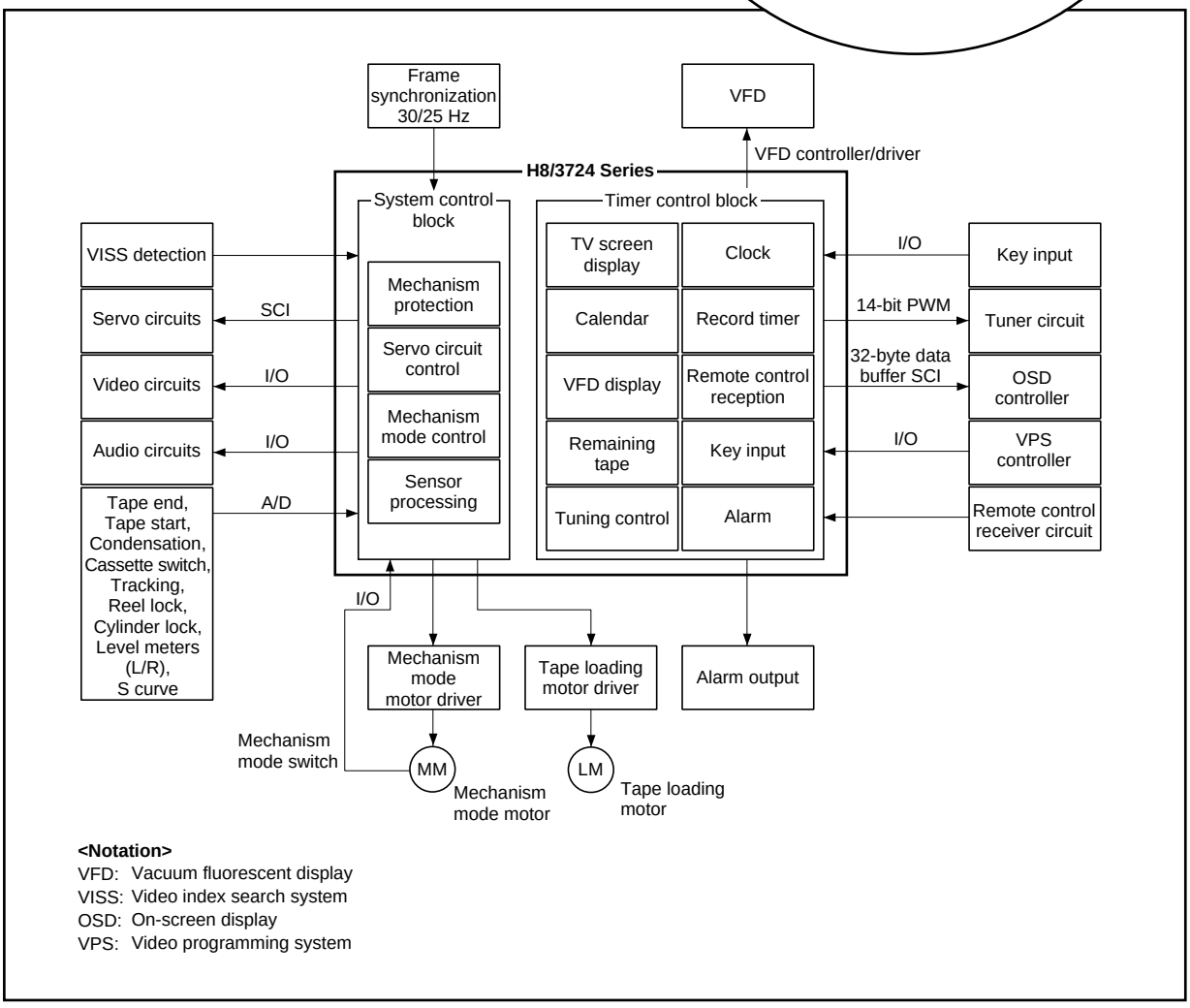
The H8/3714 Series, the H8/3724 Series, and the H8/3754 Series are optimal for applications that use vacuum fluorescent display. Typical products that incorporate vacuum fluorescent display include VCR and laser disk players, audio equipment such as CD players, home appliances such as microwave ranges, and electronic cash registers (ECRs). Furthermore, since these microcomputers support low voltage operation (2.7 V) and a rich set of low power modes, they can be used in portable equipment such as cordless telephones and camcorders.



Application Example

This section describes the use of the H8/3724 Series in VCR units. The VFD controller/driver directly drives the VCR front panel vacuum fluorescent display. The built-in timers, of which there are five types, are used to generate the basic timing for system control and for the clock/calendar function, remote control reception control, the frame synchronization counter, the alarm, and other functions. The two-channel serial communication interface (SCI) forms the interface with servo ICs and the on screen display control (OSD) IC. Finally, the A/D converter acquires analog data from various sensors for the microcomputer. Since the H8/3724 Series provides a large capacity on-chip ROM (24 kbytes to 48 kbytes), in addition to these powerful peripheral functions it is possible to implement VCR system control, timers, and display control with a single microcomputer chip.





<Notation>
VFD: Vacuum fluorescent display
VISS: Video index search system
OSD: On-screen display
VPS: Video programming system

2. Liquid Crystal Display Controller/Driver (H8/3814 Series, H8/3834 Series)

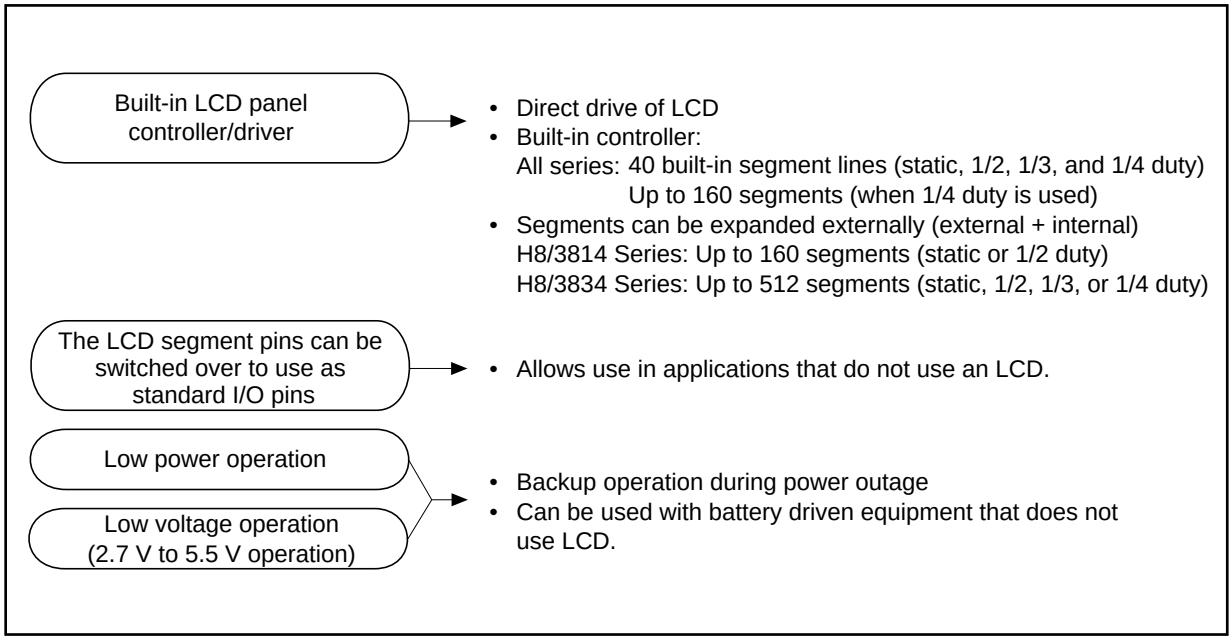
Features

Hitachi, Ltd. provides the H8/3814 Series and the H8/3834 Series (all in 100-pin packages) as built-in liquid crystal display (LCD) controller/driver microcomputers for use with applications incorporating liquid crystal displays. The H8/3814 Series provides 16 kbytes to 32 kbytes of on-chip ROM, and the H8/3834 Series provides 32 kbytes to 60 kbytes.

Since the LCD controller/driver provides 40 built-in segment lines and duty ratios of 1/4, 1/3, 1/2, and static, displays of up to 160 segments can be used. Furthermore, displays with up to 512 segments can be driven if an external expansion LCD driver (such as the HD66100) is used.

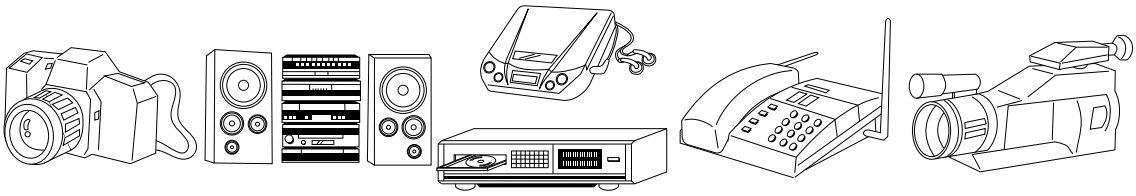
As for additional peripheral functions, the H8/3834 Series provides on-chip five types of timers and three serial communication interface channels. The H8/3814 Series provides on-chip three types of timers and two serial communication interface channels. These microcomputers also include a 12-channel A/D converter.

Furthermore, these microcomputers support low voltage operation (2.7 V) and a rich set of low power modes including microcomputer operation from a 32 kHz subclock making these products optimal for applications which require backup operation during power outages or battery operation.



Possible Applications

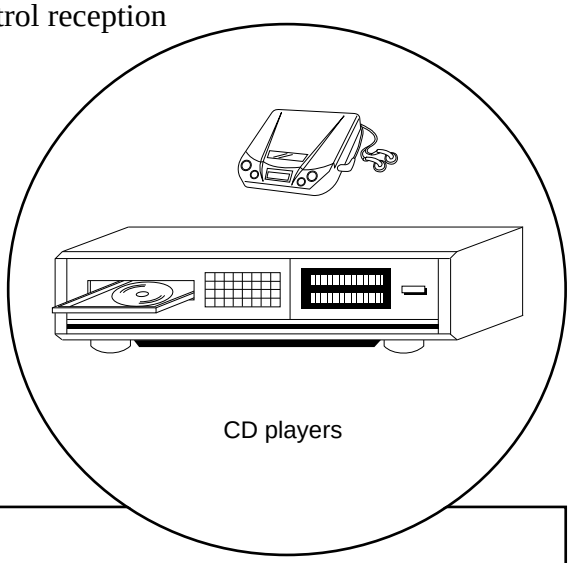
The H8/3814 Series and H8/3834 Series are optimal for use in applications that use liquid crystal display (LCD). Typical products that incorporate LCD include cameras, audio components, and CD players. Furthermore, since the LCD segment pins can be switched over to function as standard I/O pins, these microcomputers can also be used for system control in applications that do not require an LCD, such as cordless telephones and camcorders.

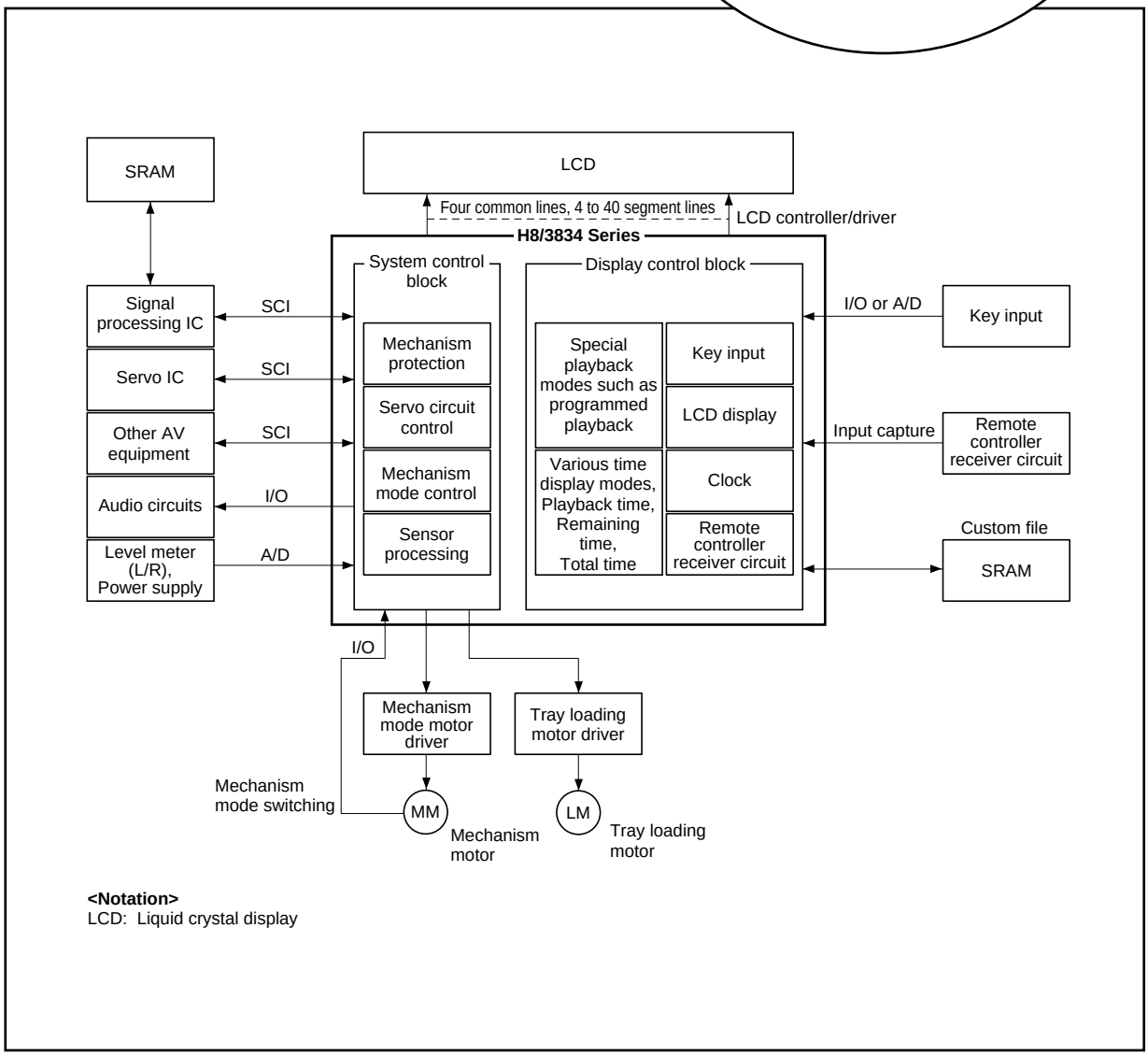


Man-machine interface and system controller in equipment using liquid crystal display

Application Example

This section describes the use of the H8/3834 Series in CD players. The liquid crystal display (LCD) controller/driver drives the LCD directly. The built-in timers, of which there are five types, are used to implement clock and remote control reception functions. The three-channel serial communication interface (SCI) forms the interface with signal processing and servo ICs and can also be used for the interface with other equipment. Finally, the 12-channel A/D converter can be used for data acquisition from the various sensors, such as the audio level control.





<Notation>
LCD: Liquid crystal display

3. Tone Generator + LCD (H8/3877 Series)

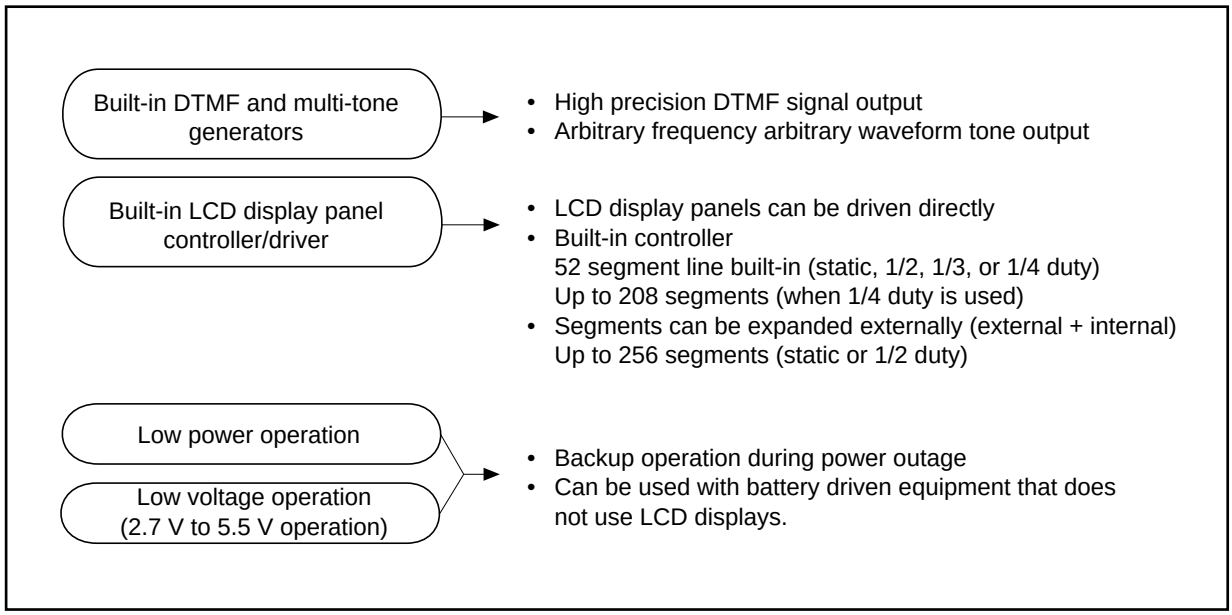
Features

Hitachi, Ltd. provides the H8/3877 Series as microcomputers that include on-chip high precision dual tone multi frequency (DTMF) and multi-tone generator circuits. The H8/3877 Series microcomputers include 40 kbytes to 60 kbytes of ROM and a 2-kbyte large capacity RAM on chip.

The DTMF generator circuit provides high precision DTMF signal output and the multi-tone generator circuit provides arbitrary tone outputs at arbitrary frequencies.

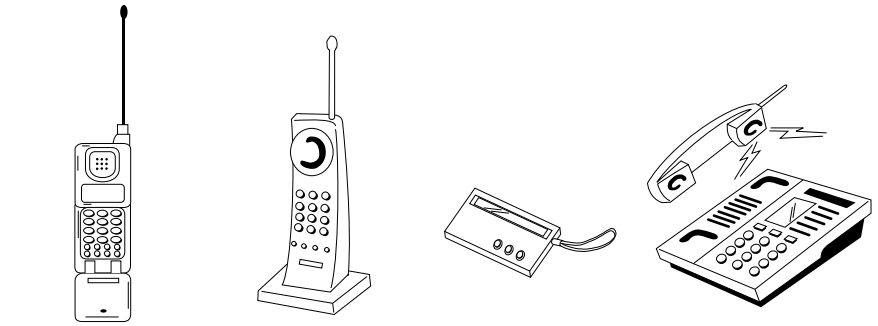
These microcomputers provide on-chip an LCD controller/driver (52 segment lines × 4 common lines), three types of timers, two serial communication interface (SCI) channels, and an 8-channel A/D converter as additional peripheral functions.

Furthermore, these microcomputers support low voltage operation (2.7 V) and a rich set of low power modes including microcomputer operation from a 32 kHz subclock making these products optimal for applications which require backup operation during power outages or battery operation.



Possible Applications

The H8/3877 Series microcomputers are optimal for use in applications that require tone generators and LCD displays. Typical products that require tone generators and LCD displays include portable equipment such as portable telephones and radio transceivers, cordless telephone hand sets, and pagers, as well as multi-function telephones.

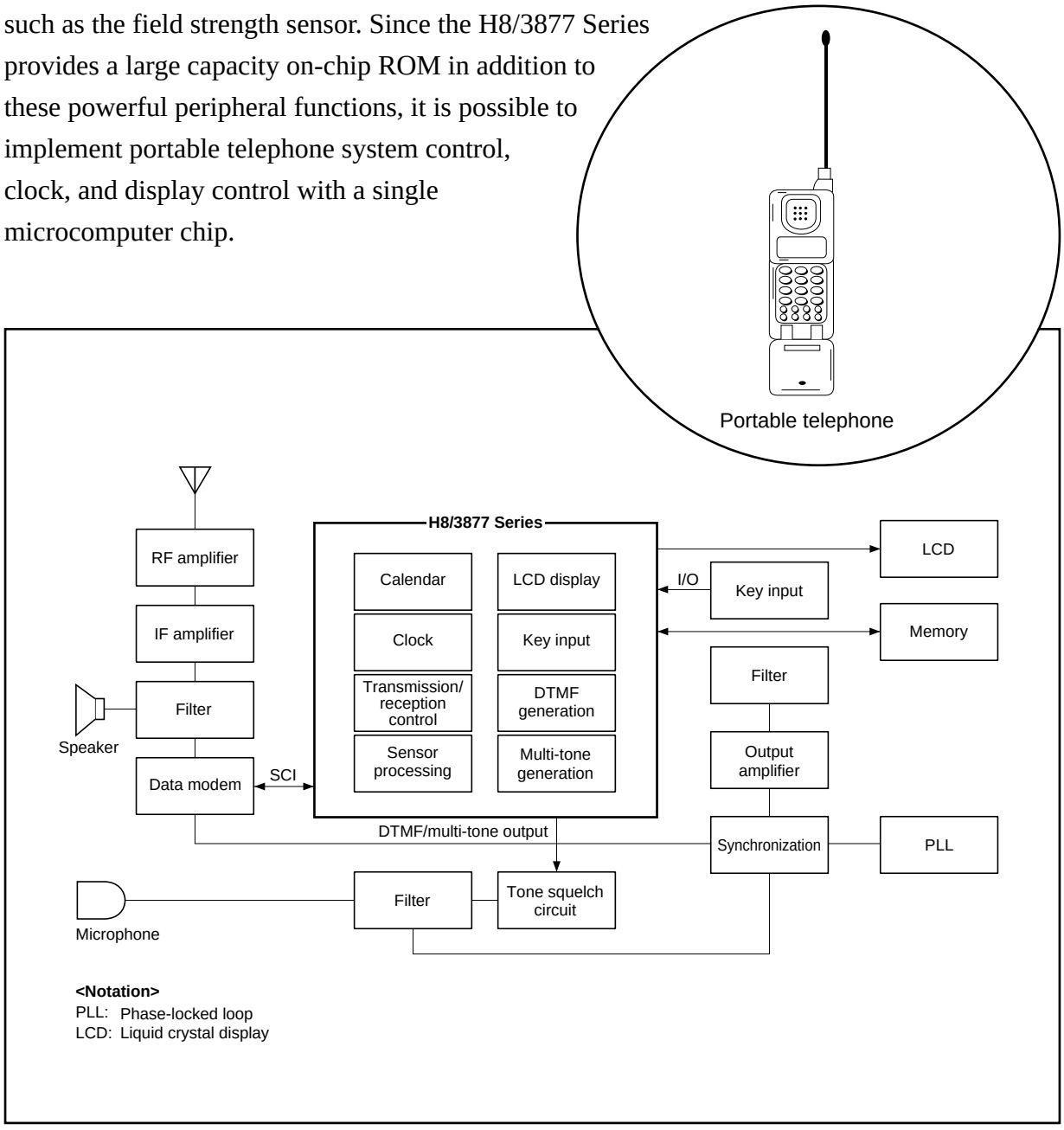


Portable telephones and radio transceivers | Cordless telephones (hand sets) | Pagers | Multi-function telephones

Man-machine interface and system controller in equipment using dual tone multi frequency and other tone generators and liquid crystal displays

Application Example

This section describes the use of the H8/3877 Series in portable telephones. The LCD controller/driver drives the LCD panel directly. Since the tone generators can output DTMF signals and arbitrary tones simultaneously, the external components previously required for optional functions, such as tone squelch, can be eliminated. This can allow overall system costs to be significantly reduced. The built-in timers, of which there are three types, are used to generate the basic timing for system control, for the clock and calendar functions, for the transmission/reception control function, and for the alarm function. The two-channel serial communication interface (SCI) is used for, e.g., radio control protocols. Finally, the A/D converter is used for acquisition of analog data from sensors such as the field strength sensor. Since the H8/3877 Series provides a large capacity on-chip ROM in addition to these powerful peripheral functions, it is possible to implement portable telephone system control, clock, and display control with a single microcomputer chip.



4. A/D and D/A Converters (H8/3927 Series)

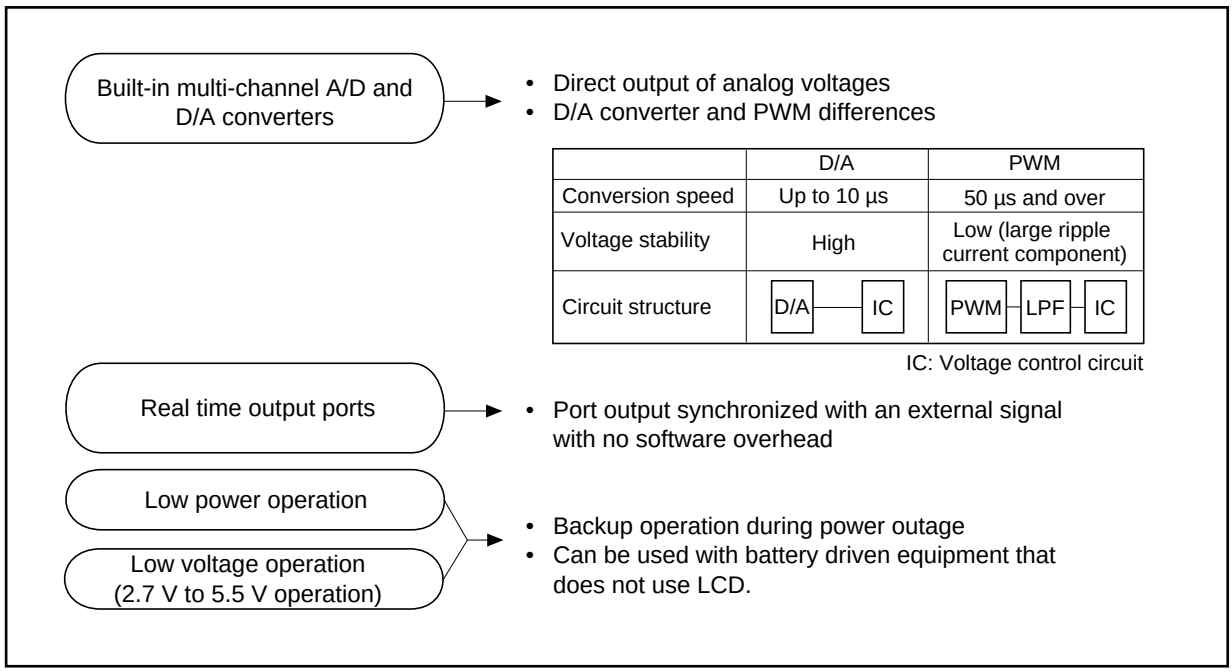
Features

Hitachi, Ltd. provides the H8/3927 Series, which includes built-in 8-bit A/D and D/A converters, as microcomputers for use in analog signal interface applications. The H8/3927 Series microcomputers include 32 kbytes to 60 kbytes of ROM and 1 kbyte of RAM on chip.

Since the D/A converter can directly output analog signals, analog output signals can be directly controlled without the use of the external PWM generator and low pass filter components that were previously required to form the D/A converter. Furthermore, eight A/D converter channels are built in.

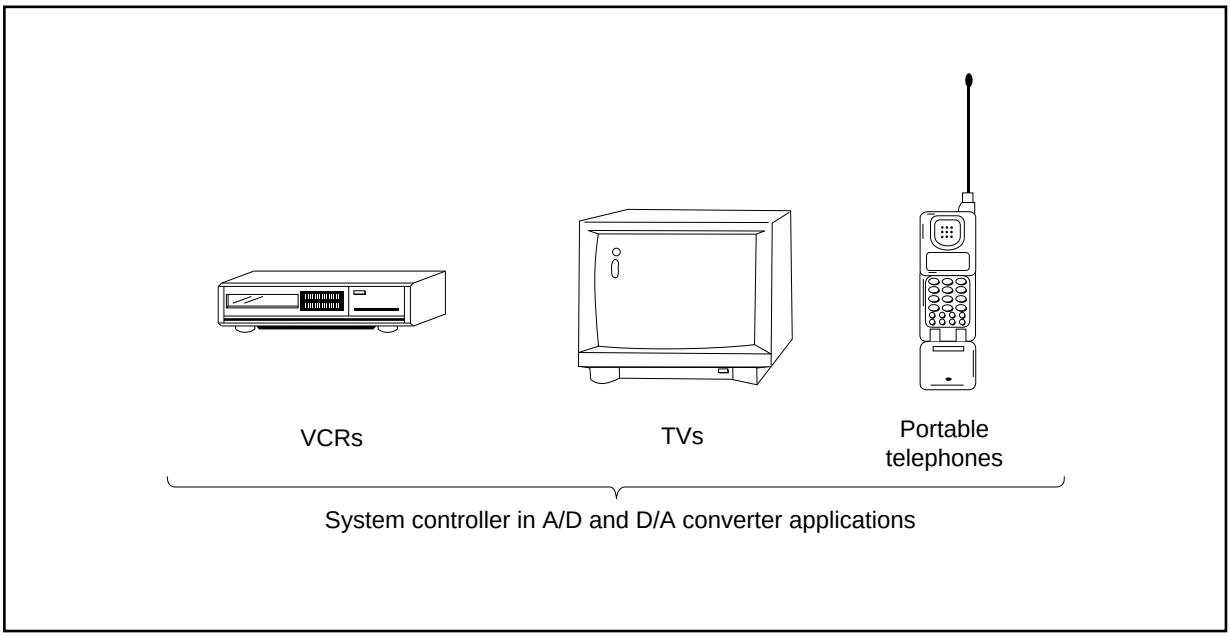
These microcomputers provide on-chip ten types of timer (including a watchdog timer), real-time output ports, a 14-bit PWM, and two serial communication interface channels as additional peripheral functions.

Furthermore, these microcomputers support low voltage operation (2.7 V) and a rich set of low power modes including microcomputer operation from a 32 kHz subclock making these products optimal for applications which require backup operation during power outages or battery operation.



Possible Applications

The H8/3927 Series microcomputers are optimal for use in applications that control analog signals. Typical products that require A/D and D/A converters include video applications such as VCRs and TVs. Furthermore, since the H8/3927 Series microcomputers support low power and low voltage (2.7 V) operation, they can be used in portable equipment such as portable telephones.



1. Features

The H8/300L CPU provides sixteen 8-bit general registers and a concise optimized instruction set that is geared for high speed operation. The general register set can also be used as eight 16-bit registers. Arithmetic, data transfer, and other operations are executed rapidly due to operating frequencies of up to 5 MHz. Furthermore, the H8/300L CPU instruction set is compatible with the H8/300 CPU instruction set.

H8/300L High Speed CPU

- **General register architecture**
  — Register set of sixteen 8-bit registers; also accessible as eight 16-bit registers

- **High speed operations**
  — Maximum operating frequency of 5 MHz (ø clock)
  — High speed operations
  8 or 16 bit register to register add: 0.4 µs (5 MHz clock)
  8 × 8 bit multiply: 2.8 µs (5 MHz clock)
  16 ÷ 8 bit division: 2.8 µs (5 MHz clock)

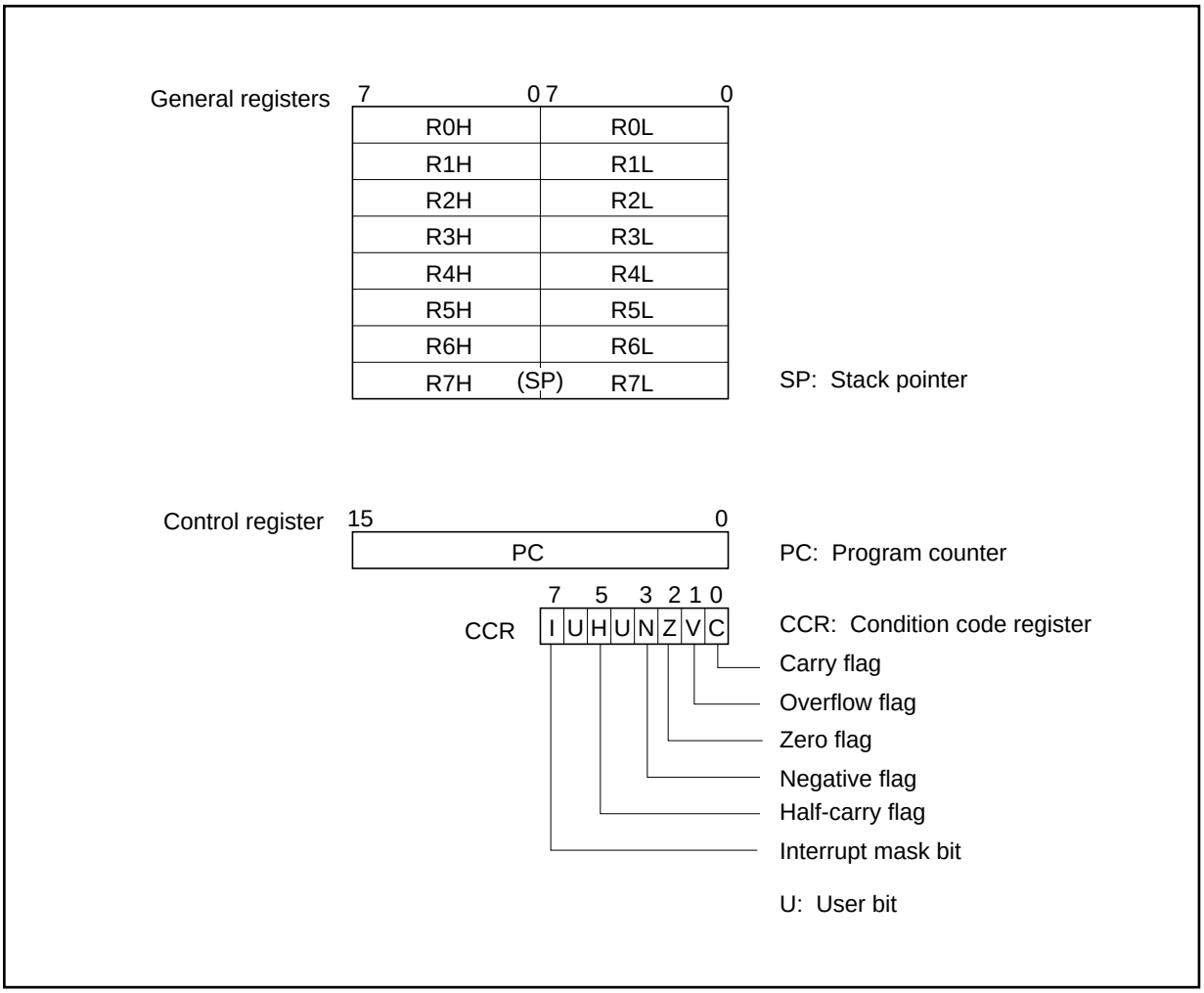
- **Instruction set suited for high speed operation**
  — 55 basic instruction types
  — Two and four byte instruction lengths
  — High speed multiply and divide instructions and powerful bit manipulation instructions

- **64 kbyte address space**

2. Register Structure

The H8/300L CPU register set consists of sixteen 8-bit general registers (referred to as R0H/R0L through R7H/R7L), a 16-bit program counter (PC) used as a control register, and an 8-bit condition code register (CCR).

CPU Internal Organization



General Registers

The sixteen 8-bit registers all have the same structure and can be used without distinguishing data registers from address registers. They can also be used as eight 16-bit registers. When used as data registers, the general registers can be used as either 8-bit registers, in which case they are referred to as upper (H) and lower (L) byte registers, or as 16-bit registers. When used as address registers, they are used as 16-bit registers. These usages differ depending on the instruction.

In addition to its function as a general register, register R7 is also allocated for use as the stack pointer (SP). It is used implicitly in subroutine calls and exception processing.

Control Registers

Program Counter (PC): The program counter is a 16-bit register that holds the address of the next instruction to be executed by the H8/300L CPU.

Condition Code Register (CCR): This 8-bit register contains internal status information, including the carry (C), overflow (V), zero (Z), negative (N), and half-carry (H) flags and the interrupt mask bit (I). The CCR can be manipulated with the CCR manipulation instructions.

Bit 7 (I): Interrupt mask bit
This bit masks interrupts when set to 1. It is set to 1 at the start of exception handling.

Bit 6 (U): User bit
This bit can be read and written by user software using the LCD, STC, ANDC, ORC, and XORC instructions.

Bit 5 (H): Half-carry flag
This bit is set to 1 when an ADD.B, ADDX.B, SUB.B, SUBX.B, CMP.B, or NEG.B causes a carry into or borrow from bit 3, and is cleared to 0 when the execution of one of those instructions does not cause a carry or borrow. Similarly, it is set to 1 when an ADD.W, SUB.W, or CMP.W instruction causes a carry into or borrow from bit 11, and is cleared to 0 when the execution of one of those instructions does not cause a carry or borrow. It is used implicitly by the DAA and DAS instructions.

Bit 4 (U): User bit
This bit can be read and written by user software using the LCD, STC, ANDC, ORC, and XORC instructions.

Bit 3 (N): Negative flag
This bit indicates the most significant bit (the sign bit) of the result of an instruction.

Bit 2 (Z): Zero flag
This bit is set to 1 to indicate a zero result and cleared to 0 to indicate a non-zero result.

Bit 1 (V): Overflow flag
This bit is set to 1 when an arithmetic overflow occurs and cleared to 0 when no overflow occurs during an arithmetic operation.

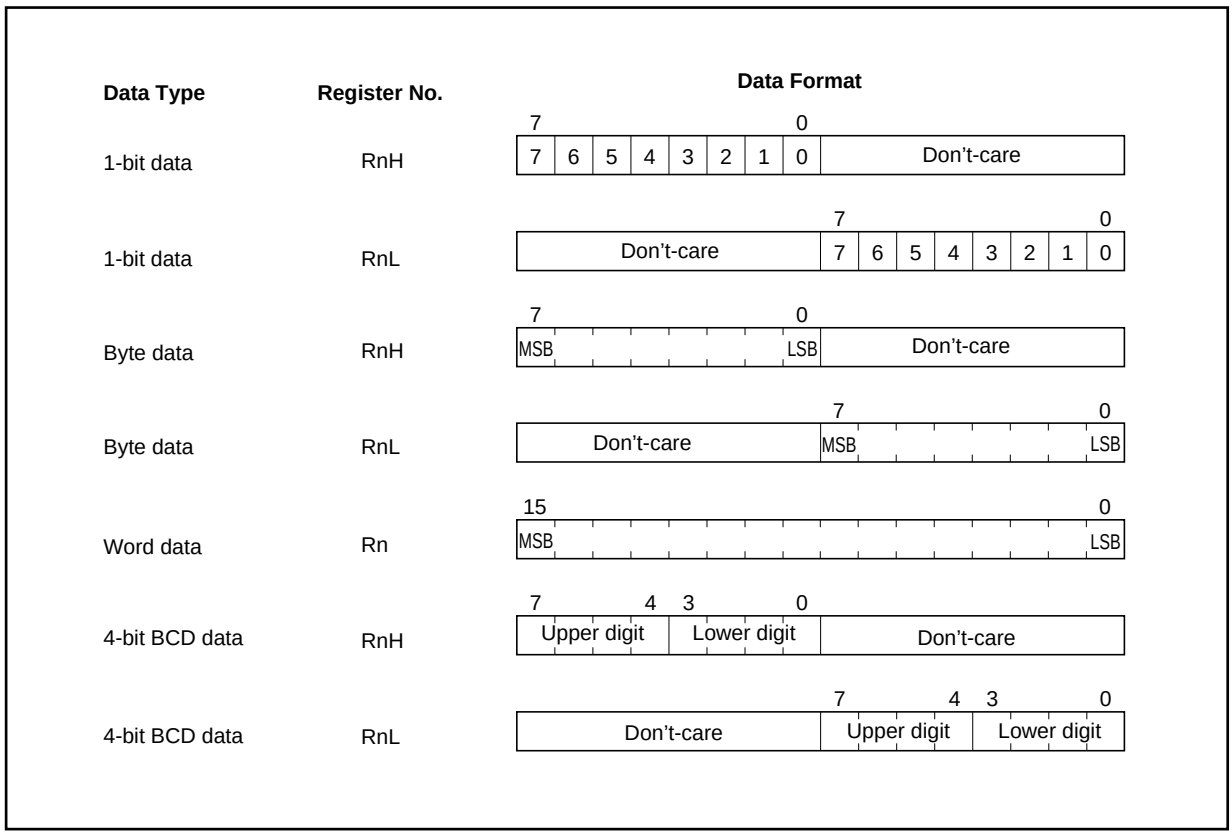
Bit 0 (C): Carry flag
This bit is set to 1 when a carry occurs and cleared to 0 when no carry occurs.
A carry can occur due to a carry from an add instruction, a borrow from a subtract instruction, or a shift or rotate instruction.
The carry flag also has a bit accumulator function that is used by bit operation and bit transfer instructions.

3. Data Formats

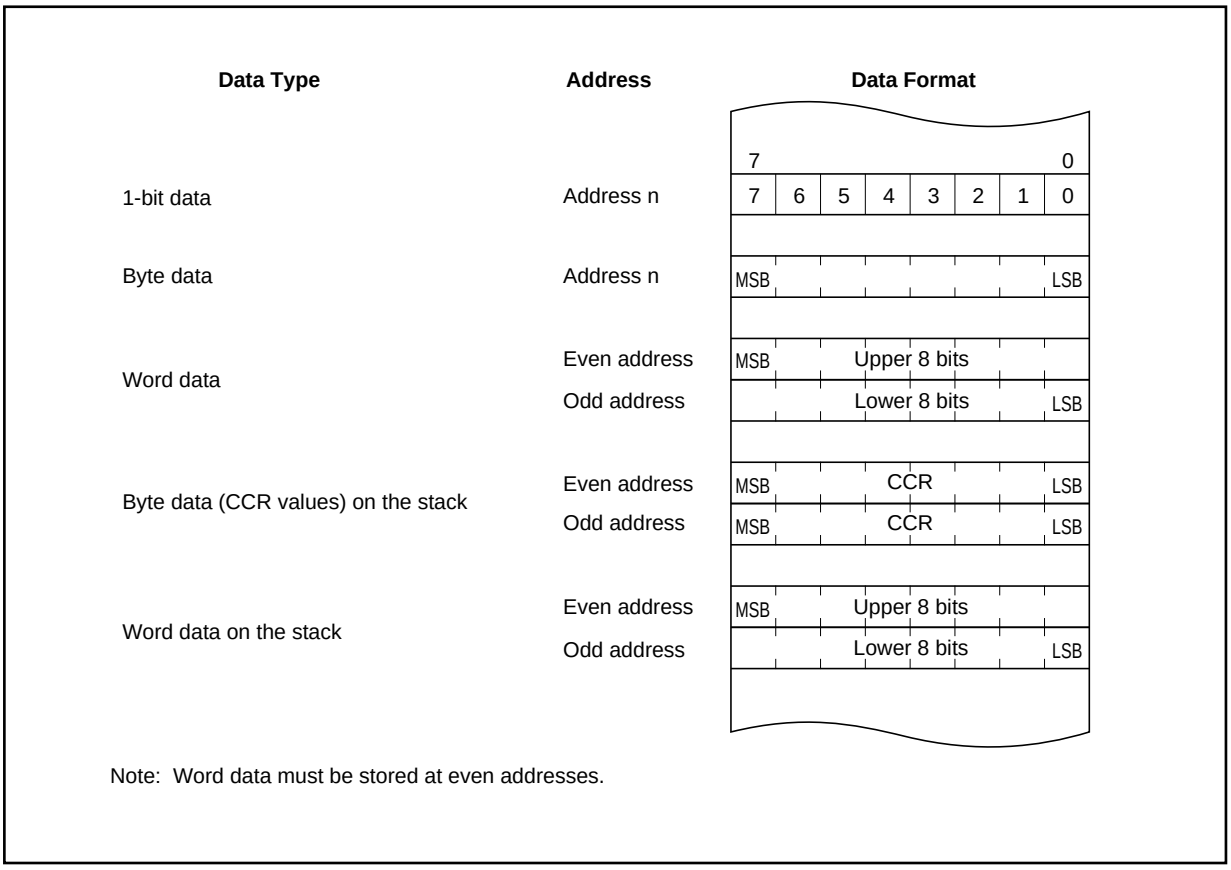
The H8/300L CPU can process 1-bit data, 4-bit (BCD) data, 8-bit (byte) data, and 16-bit (word) data. Essentially all instructions can process byte data. The bit manipulation instructions process 1-bit data and certain data transfer and arithmetic instructions process word data. The decimal adjust instructions process 4-bit BCD data.

The figures below show the formats in which data is stored in general registers and memory.

General Register Data Formats



Memory Data Formats



Note: Word data must be stored at even addresses.

4. Addressing Modes

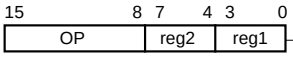
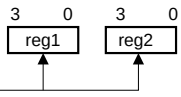
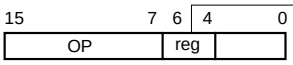
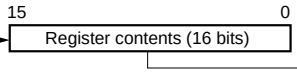
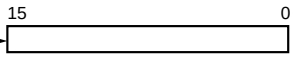
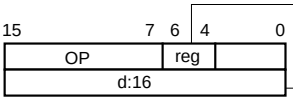
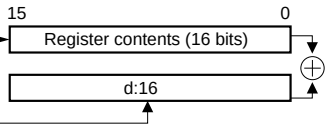
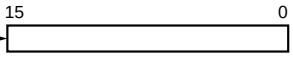
The H8/300L CPU supports the following eight addressing modes.

Addressing Modes

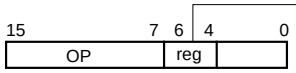
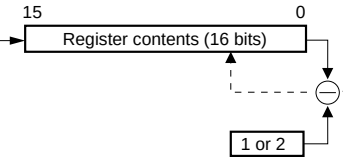
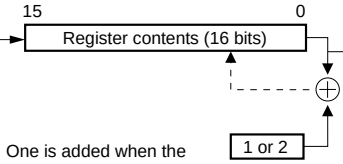
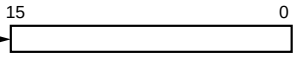
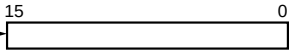
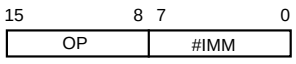
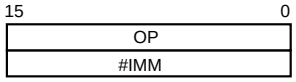
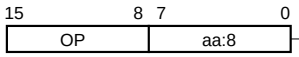
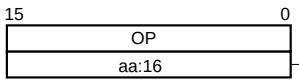
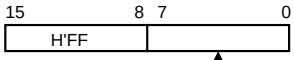
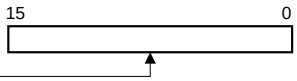
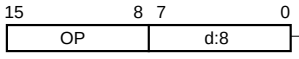
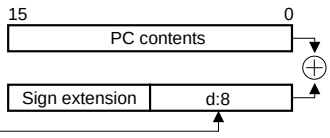
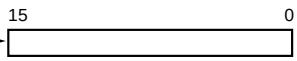
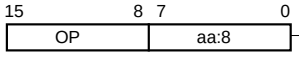
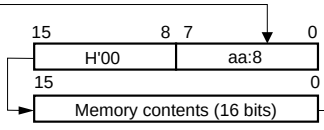
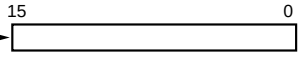
No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@Rn
3	Register indirect with displacement	@(d:16, Rn)
4	Register indirect with pre-decrement	@–Rn
	Register indirect with post-increment	@Rn+
5	Immediate	#xx:8/#xx:16
6	Absolute address	@aa:8/@aa:16
7	PC-relative	@(d:8, PC)
8	Memory indirect	@@aa:8

Note: Data transfer instructions can use modes 1 through 6.

Effective Address Calculation

No.	Addressing Mode, Instruction Format	Effective Address Calculation	EA
1	Register direct Rn 		 The operands are the contents of registers reg1 and reg2.
2	Register indirect @Rn 		
3	Register indirect with displacement @(d:16,Rn) 		

(Continued on following page.)

No.	Addressing Mode, Instruction Format	Effective Address Calculation	EA
4	Register indirect with pre-decrement @–Rn  Register indirect with post-decrement @Rn+ 	  One is added when the operand size is byte, and 2 is added when the operand size is word.	 
5	Immediate #xx:8 		The operand is the single byte of immediate data.
	Immediate #xx:16 		The operand is the two bytes of immediate data.
6	Absolute address @aa:8  Absolute address @aa:16 		 
7	PC-relative @(d:8,PC) 		
8	Memory indirect @@aa:8 		

<Notation>

reg: General register
#IMM: Immediate data
d: Displacement
aa: Absolute address
OP: Op-code
PC: Program counter

5. Instruction Set

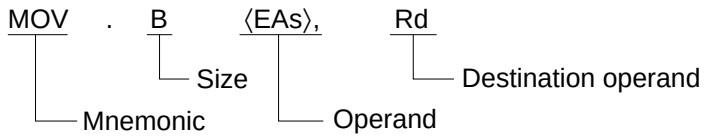
The H8/300L CPU supports 55 basic instructions with the following features.

Features

- **Concise instruction set geared to high-speed performance**
  — All instructions are 2 or 4 bytes long.
- **High speed**
  — All frequently executed instructions execute in 2 to 4 states.
- **General register architecture**
- **Powerful bit-manipulation instructions**
- **Standard H8/300 Series mnemonics**

Assembly Language Format

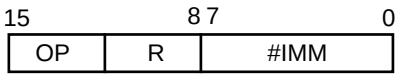
The example below uses the MOV instruction. The letter B (byte) or W (word) designates the operand size. Note that certain instructions only allow one of these sizes to be used.



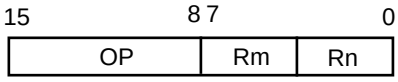
Main Instruction Formats

The figure below shows the main instruction formats supported by the H8/300L CPU.

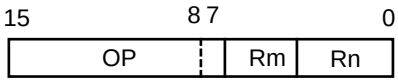
- Arithmetic or logic operation on immediate data and register contents



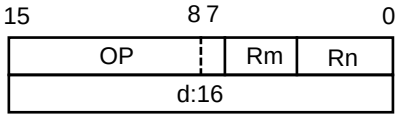
- Register-register arithmetic or logic operation



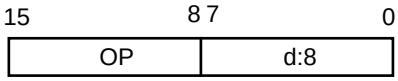
- Data transfer instruction [@Rm↔Rn]



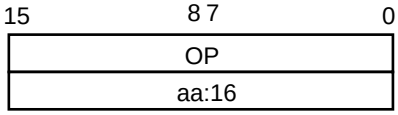
- Data transfer instruction [@(d:16,Rm)↔Rn]



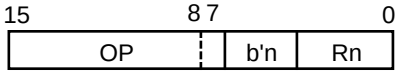
- Branch instruction [@(d:8,PC)]



- Branch instruction [@aa:16]



- Bit manipulation instruction (with direct specification of bit position)



<Notation>

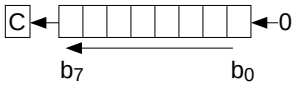
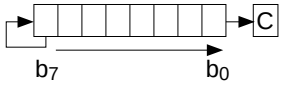
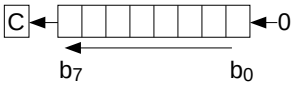
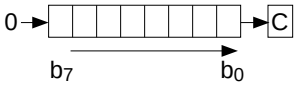
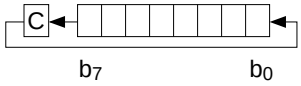
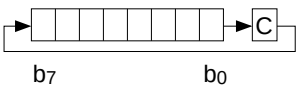
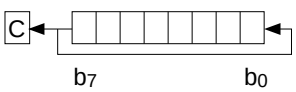
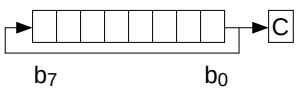
OP:	Op-code
Rn,Rm:	General register
#IMM:	Immediate data
d:	Displacement
aa:	Absolute address
b’n:	Bit number

Instruction Set

Mnemonic		Operand Size	Operation	Addressing Mode/ Instruction Length									Condition Code						No. of States
				#xx:	Rn	@Rn	@(d:16,Rn)	@–Rn/@Rn+	@aa:	@(d:8,PC)	@@aa	Implied	I	H	N	Z	V	C	
Data transfer instructions	MOV.B Rs,Rd	B	Rs8 → Rd8		2								—	—	↕	↕	0	—	2
	MOV.B #xx:8,Rd	B	#xx:8 → Rd8	2									—	—	↕	↕	0	—	2
	MOV.B @Rs,Rd	B	@Rs16 → Rd8			2							—	—	↕	↕	0	—	4
	MOV.B @(d:16,Rs),Rd	B	@(d:16,Rs16)→ Rd8				4						—	—	↕	↕	0	—	6
	MOV.B @Rs+,Rd	B	@Rs16 → Rd8 Rs16+1 → Rs16					2					—	—	↕	↕	0	—	6
	MOV.B @aa:8,Rd	B	@aa:8 → Rd8						2				—	—	↕	↕	0	—	4
	MOV.B @aa:16,Rd	B	@aa:16 → Rd8						4				—	—	↕	↕	0	—	6
	MOV.B Rs,@Rd	B	Rs8 → @Rd16			2							—	—	↕	↕	0	—	4
	MOV.B Rs,@(d:16,Rd)	B	Rs8 → @(d:16,Rd16)				4						—	—	↕	↕	0	—	6
	MOV.B Rs,@–Rd	B	Rd16–1 → Rd16 Rs8 → @Rd16					2					—	—	↕	↕	0	—	6
	MOV.B Rs,@aa:8	B	Rs8 → @aa:8						2				—	—	↕	↕	0	—	4
	MOV.B Rs,@aa:16	B	Rs8 → @aa:16						4				—	—	↕	↕	0	—	6
	MOV.W Rs,Rd	W	Rs16 → Rd16		2								—	—	↕	↕	0	—	2
	MOV.W @Rs,Rd	W	@Rs16 → Rd16			2							—	—	↕	↕	0	—	4
	MOV.W @(d:16,Rs),Rd	W	@(d:16,Rs16) → Rd16				4						—	—	↕	↕	0	—	6
	MOV.W @Rs+,Rd	W	@Rs16 → Rd16 Rs16+2 → Rs16					2					—	—	↕	↕	0	—	6
	MOV.W @aa:16,Rd	W	@aa:16 → Rd16						4				—	—	↕	↕	0	—	6
	MOV.W Rs,@Rd	W	Rs16 → @Rd16			2							—	—	↕	↕	0	—	4
	MOV.W Rs,@(d:16,Rd)	W	Rs16 → @(d:16,Rd16)				4						—	—	↕	↕	0	—	6
	MOV.W Rs,@–Rd	W	Rd16–2 → Rd16 Rs16 → @Rd16					2					—	—	↕	↕	0	—	6
	MOV.W Rs, @aa:16	W	Rs16 → @aa:16						4				—	—	↕	↕	0	—	6
	MOV.W #xx:16,Rd	W	#xx:16 → Rd	4									—	—	↕	↕	0	—	4
	POP Rd	W	@SP+ → Rd					2					—	—	↕	↕	0	—	6
	PUSH Rs	W	Rs → @–SP					2					—	—	↕	↕	0	—	6
	EEPMOV	B	if R4L≠0, Repeat @R5 → @R6 R5+1 → R5,R6+1 → R6 R4L–1 → R4L Until R4L=0 else next									4	—	—	—	—	—	—	4
Arithmetic instructions	ADD.B #xx:8,Rd	B	Rd8+#xx:8 → Rd8	2									—	↕	↕	↕	↕	↕	2
	ADD.B Rs,Rd	B	Rs8+Rd8 → Rd8		2								—	↕	↕	↕	↕	↕	2
	ADD.W Rs,Rd	W	Rs16+Rd16 → Rd16		2								—	1	↕	↕	↕	↕	2
	ADDX.B #xx:8,Rd	B	Rd8+#xx:8 +C → Rd8	2									—	↕	↕	2	↕	↕	2
	ADDX.B Rs,Rd	B	Rd8+Rs8 +C → Rd8		2								—	↕	↕	2	↕	↕	2
	ADDS.W #1,Rd	W	Rd16+1 → Rd16		2								—	—	—	—	—	—	2
	ADDS.W #2,Rd	W	Rd16+2 → Rd16		2								—	—	—	—	—	—	2
	INC.B Rd	B	Rd8+1 → Rd8		2								—	—	↕	↕	↕	—	2
	DAA.B Rd	B	Rd8 10 decimal correction → Rd8		2								—	*	↕	↕	*	3	2
	NEG.B Rd	B	0–Rd → Rd		2								—	↕	↕	↕	↕	↕	2
	SUB.B Rs,Rd	B	Rd8–Rs8 → Rd8		2								—	↕	↕	↕	↕	↕	2
	SUB.W Rs,Rd	W	Rd16–Rs16 → Rd16		2								—	1	↕	↕	↕	↕	2
	SUBX.B #xx:8,Rd	B	Rd8–#xx:8 –C → Rd8	2									—	↕	↕	2	↕	↕	2
	SUBX.B Rs,Rd	B	Rd8–Rs8 → Rd8		2								—	↕	↕	2	↕	↕	2
	SUBS.W #1,Rd	W	Rd16–1 → Rd16		2								—	—	—	—	—	—	2
	SUBS.W #2,Rd	W	Rd16–2 → Rd16		2								—	—	—	—	—	—	2
	DEC.B Rd	B	Rd8–1 → Rd8		2								—	—	↕	↕	↕	—	2
	DAS.B Rd	B	Rd8 10 decimal correction → Rd8		2								—	*	↕	↕	*	—	2

(Continued on following page.)

Instruction Set (cont)

Mnemonic		Operand Size	Operation	Addressing Mode/ Instruction Length									Condition Code						No. of States
				#xx:	Rn	@Rn	@(d:16,Rn)	@–Rn/@Rn+	@aa:	@(d:8,PC)	@@aa	Implied	I	H	N	Z	V	C	
Arithmetic instructions	CMP.B #xx:8,Rd	B	Rd8–#xx:8	2									—	↕	↕	↕	↕	↕	2
	CMP.B Rs,Rd	B	Rd8–Rs8		2								—	↕	↕	↕	↕	↕	2
	CMP.W Rs,Rd	W	Rd16–Rs16		2								—	1	↕	↕	↕	↕	2
	MULXU.B Rs,Rd	B	Rd8×Rs8 → Rd16		2								—	—	—	—	—	—	14
	DIVXU.B Rs,Rd	B	Rd16÷Rs8 → Rd16 (RdH: Remainder, RdL: Quotient)		2								—	—	5	6	—	—	14
Logic instructions	AND.B #xx:8,Rd	B	Rd8∧#xx:8 → Rd8	2									—	—	↕	↕	0	—	2
	AND.B Rs,Rd	B	Rd8∧Rs8 → Rd8		2								—	—	↕	↕	0	—	2
	OR.B #xx:8,Rd	B	Rd8∨#xx:8 → Rd8	2									—	—	↕	↕	0	—	2
	OR.B Rs,Rd	B	Rd8∨Rs8 → Rd8		2								—	—	↕	↕	0	—	2
	XOR.B #xx:8,Rd	B	Rd8⊕#xx:8 → Rd8	2									—	—	↕	↕	0	—	2
	XOR.B Rs,Rd	B	Rd8⊕Rs8 → Rd8		2								—	—	↕	↕	0	—	2
	NOT.B Rd	B	Rd → Rd		2								—	—	↕	↕	0	—	2
Shift instructions	SHAL.B Rd	B			2								—	—	↕	↕	↕	↕	2
	SHAR.B Rd	B			2								—	—	↕	↕	0	↕	2
	SHLL.B Rd	B			2								—	—	↕	↕	0	↕	2
	SHLR.B Rd	B			2								—	—	↕	↕	0	↕	2
	ROTXL.B Rd	B			2								—	—	↕	↕	0	↕	2
	ROTXR.B Rd	B			2								—	—	↕	↕	0	↕	2
	ROTL.B Rd	B			2								—	—	↕	↕	0	↕	2
	ROTR.B Rd	B			2								—	—	↕	↕	0	↕	2

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Instruction Set (cont)

Mnemonic		Operand Size	Operation	Addressing Mode/ Instruction Length									Condition Code						No. of States
				#xx:	Rn	@Rn	@(d:16,Rn)	@–Rn/@Rn+	@aa:	@(d:8,PC)	@@aa	Implied	I	H	N	Z	V	C	
Bit manipulation instructions	BSET #xx:3,Rd	B	(#xx:3 of Rd8) ← 1		2								—	—	—	—	—	—	2
	BSET #xx:3,@Rd	B	(#xx:3 of @Rd16) ← 1			4							—	—	—	—	—	—	8
	BSET #xx:3,@aa:8	B	(#xx:3 of @aa:8) ← 1						4				—	—	—	—	—	—	8
	BSET Rn,Rd	B	(Rn8 of Rd8) ← 1		2								—	—	—	—	—	—	2
	BSET Rn,@Rd	B	(Rn8 of @Rd16) ← 1			4							—	—	—	—	—	—	8
	BSET Rn,@aa:8	B	(Rn8 of @aa:8) ← 1						4				—	—	—	—	—	—	8
	BCLR #xx:3,Rd	B	(#xx:3 of Rd8) ← 0		2								—	—	—	—	—	—	2
	BCLR #xx:3,@Rd	B	(#xx:3 of @Rd16) ← 0			4							—	—	—	—	—	—	8
	BCLR #xx:3,@aa:8	B	(#xx:3 of @aa:8) ← 0						4				—	—	—	—	—	—	8
	BCLR Rn,Rd	B	(Rn8 of Rd8) ← 0		2								—	—	—	—	—	—	2
	BCLR Rn,@Rd	B	(Rn8 of @Rd16) ← 0			4							—	—	—	—	—	—	8
	BCLR Rn,@aa:8	B	(Rn8 of @aa:8) ← 0						4				—	—	—	—	—	—	8
	BNOT #xx:3,Rd	B	(#xx:3 of Rd8)←($\overline{\text{#xx:3 of Rd8}}$)		2								—	—	—	—	—	—	2
	BNOT #xx:3,@Rd	B	(#xx:3 of @Rd16)←($\overline{\text{#xx:3 of @Rd16}}$)			4							—	—	—	—	—	—	8
	BNOT #xx:3,@aa:8	B	(#xx:3 of @aa:8)←($\overline{\text{#xx:3 of @aa:8}}$)						4				—	—	—	—	—	—	8
	BNOT Rn,Rd	B	(Rn8 of Rd8) ← ($\overline{\text{Rn8 of Rd8}}$)		2								—	—	—	—	—	—	2
	BNOT Rn,@Rd	B	(Rn8 of @Rd16)←($\overline{\text{Rn8 of @Rd16}}$)			4							—	—	—	—	—	—	8
	BNOT Rn,@aa:8	B	(Rn8 of @aa:8)← ($\overline{\text{Rn8 of @aa:8}}$)						4				—	—	—	—	—	—	8
	BTST #xx:3,Rd	B	($\overline{\text{#xx:3 of Rd8}}$) → Z		2								—	—	—	↕	—	—	2
	BTST #xx:3,@Rd	B	($\overline{\text{#xx:3 of @Rd16}}$) → Z			4							—	—	—	↕	—	—	6
	BTST #xx:3,@aa:8	B	($\overline{\text{#xx:3 of @aa:8}}$) → Z						4				—	—	—	↕	—	—	6
	BTST Rn,Rd	B	($\overline{\text{Rn8 of Rd8}}$) → Z		2								—	—	—	↕	—	—	2
	BTST Rn,@Rd	B	($\overline{\text{Rn8 of @Rd16}}$) → Z			4							—	—	—	↕	—	—	6
	BTST Rn,@aa:8	B	($\overline{\text{Rn8 of @aa:8}}$) → Z						4				—	—	—	↕	—	—	6
	BLD #xx:3,Rd	B	(#xx:3 of Rd8) → C		2								—	—	—	—	—	↕	2
	BLD #xx:3,@Rd	B	(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↕	6
	BLD #xx:3,@aa:8	B	(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↕	6
	BILD #xx:3,Rd	B	($\overline{\text{#xx:3 of Rd8}}$) → C		2								—	—	—	—	—	↕	2
	BILD #xx:3,@Rd	B	($\overline{\text{#xx:3 of @Rd16}}$) → C			4							—	—	—	—	—	↕	6
	BILD #xx:3,@aa:8	B	($\overline{\text{#xx:3 of @aa:8}}$) → C						4				—	—	—	—	—	↕	6
	BST #xx:3,Rd	B	C → (#xx:3 of Rd8)		2								—	—	—	—	—	—	2
	BST #xx:3,@Rd	B	C → (#xx:3 of @Rd16)			4							—	—	—	—	—	—	8
	BST #xx:3,@aa:8	B	C → (#xx:3 of @aa:8)						4				—	—	—	—	—	—	8
	BIST #xx:3,Rd	B	$\overline{\text{C}}$ → (#xx:3 of Rd8)		2								—	—	—	—	—	—	2
	BIST #xx:3,@Rd	B	$\overline{\text{C}}$ → (#xx:3 of @Rd16)			4							—	—	—	—	—	—	8
	BIST #xx:3,@aa:8	B	$\overline{\text{C}}$ → (#xx:3 of @aa:8)						4				—	—	—	—	—	—	8
	BAND #xx:3,Rd	B	C∧(#xx:3 of Rd8) → C		2								—	—	—	—	—	↕	2
	BAND #xx:3,@Rd	B	C∧(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↕	6
	BAND #xx:3,@aa:8	B	C∧(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↕	6
	BIAND #xx:3,Rd	B	C∧($\overline{\text{#xx:3 of Rd8}}$) → C		2								—	—	—	—	—	↕	2
	BIAND #xx:3,@Rd	B	C∧($\overline{\text{#xx:3 of @Rd16}}$) → C			4							—	—	—	—	—	↕	6
	BIAND #xx:3, @aa:8	B	C∧($\overline{\text{#xx:3 of @aa:8}}$) → C						4				—	—	—	—	—	↕	6
	BOR #xx:3,Rd	B	C∨(#xx:3 of Rd8) → C		2								—	—	—	—	—	↕	2
	BOR #xx:3,@Rd	B	C∨(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↕	6
	BOR #xx:3, @aa:8	B	C∨(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↕	6
	BIOR #xx:3,Rd	B	C∨($\overline{\text{#xx:3 of Rd8}}$) → C		2								—	—	—	—	—	↕	2

(Continued on following page.)

Instruction Set (cont)

Mnemonic		Operand Size	Operation		Addressing Mode/ Instruction Length									Condition Code						No. of States
					#xx:	Rn	@Rn	@(d:16,Rn)	@–Rn/@Rn+	@aa:	@(d:8,PC)	@@aa	Implied	I	H	N	Z	V	C	
Bit manipulation instructions	BIOR #xx:3,@Rd	B	C∨(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
	BIOR #xx:3, @aa:8	B	C∨(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
	BXOR #xx:3,Rd	B	C⊕(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
	BXOR #xx:3,@Rd	B	C⊕(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
	BXOR #xx:3, @aa:8	B	C⊕(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
	BIXOR #xx:3,Rd	B	C⊕(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
	BIXOR #xx:3,@Rd	B	C⊕(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
	BIXOR #xx:3, @aa:8	B	C⊕(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
Branch instructions	BRA(BT)	—	PC ← PC+d:8								2			—	—	—	—	—	—	4
	BRN(BF)	—	PC ← PC+2								2			—	—	—	—	—	—	4
	BHI	—	If true then PC ← PC+d:8 else next	CVZ=0							2			—	—	—	—	—	—	4
	BLS	—		CVZ=1							2			—	—	—	—	—	—	4
	BCC(BHS)	—		C=0							2			—	—	—	—	—	—	4
	BCS(BLO)	—		C=1							2			—	—	—	—	—	—	4
	BNE	—		Z=0							2			—	—	—	—	—	—	4
	BEQ	—		Z=1							2			—	—	—	—	—	—	4
	BVC	—		V=0							2			—	—	—	—	—	—	4
	BVS	—		V=1							2			—	—	—	—	—	—	4
	BPL	—		N=0							2			—	—	—	—	—	—	4
	BMI	—		N=1							2			—	—	—	—	—	—	4
	BGE	—		N⊕V=0							2			—	—	—	—	—	—	4
	BLT	—		N⊕V=1							2			—	—	—	—	—	—	4
	BGT	—		ZV(N⊕V)=0							2			—	—	—	—	—	—	4
	BLE	—		ZV(N⊕V)=1							2			—	—	—	—	—	—	4
	JMP @Rn.	—	PC ← Rn16				2							—	—	—	—	—	—	4
	JMP @aa:16	—	PC ← aa:16							4				—	—	—	—	—	—	6
	JMP @@aa:8	—	PC ← @aa:8									2		—	—	—	—	—	—	8
	BSR	—	SP–2 → SP PC → @SP PC ← PC+d:8								2			—	—	—	—	—	—	6
	JSR @Rn	—	SP–2 → SP PC → @SP PC ← Rn16				2							—	—	—	—	—	—	6
	JSR @aa:16	—	SP–2 → SP PC → @SP PC ← aa:16							4				—	—	—	—	—	—	8
	JSR @@aa:8	—	SP–2 → SP PC → @SP PC ← @aa:8									2		—	—	—	—	—	—	8
	RTS	—	PC ← @SP SP+2 → SP										2	—	—	—	—	—	—	8

(Continued on following page.)

Instruction Set (cont)

Mnemonic		Operand Size	Operation	Addressing Mode/ Instruction Length									Condition Code						No. of States
				#xx:	Rn	@Rn	@(d:16,Rn)	@–Rn/@Rn+	@aa:	@(d:8,PC)	@@aa	Implied	I	H	N	Z	V	C	
System control instructions	RTE	—	CCR ← @SP SP+2 → SP PC ← @SP SP+2 → SP									2	↕	↕	↕	↕	↕	↕	10
	SLEEP	—	Switches to low power mode.									2	—	—	—	—	—	—	2
	LDC #xx:8,CCR	B	#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
	LDC Rs,CCR	B	Rs8 → CCR		2								↕	↕	↕	↕	↕	↕	2
	STC CCR,Rd	B	CCR → Rd8		2								—	—	—	—	—	—	2
	ANDC #xx:8,CCR	B	CCR∧#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
	ORC #xx:8,CCR	B	CCR∨#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
	XORC #xx:8,CCR	B	CCR⊕#xx:8 → CCR	2									↕	↕	↕	↕	↕	↕	2
	NOP	—	No operation									2	—	—	—	—	—	—	2

Notes: 1 Set to 1 when there is a carry to or borrow from bit 11; otherwise cleared to 0.
2 If the result is zero the previous value of the flag is retained; otherwise the flag is cleared to 0.
3 Set to 1 if decimal adjustment produces a carry; otherwise the previous value is retained.
4 The number of states required for execution is 4n + 9, where n is the value of register R4L.
5 Set to 1 if the divisor is negative; otherwise cleared to 0.
6 Set to 1 if the divisor is zero; otherwise cleared to 0.

CPU

Operating Notation

Symbol	Meaning
PC	Program counter
SP	Stack pointer (R7)
CCR	Condition code register
Z	CCR zero flag
C	CCR carry flag
Rs, Rd, Rn	General registers (8-bit: R0H/R0L to R7H/R7L; 16-bit: R0 to R7)
d:8, d:16	Displacement
#xx:3, #xx:8, #xx:16	3-bit, 8-bit, or 16-bit immediate data
→	The operand on the left side of the operator is transferred to the operand on the right.
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical exclusive OR
¬	Logical negation (one's complement)
( ) and < >	Contents of effective address

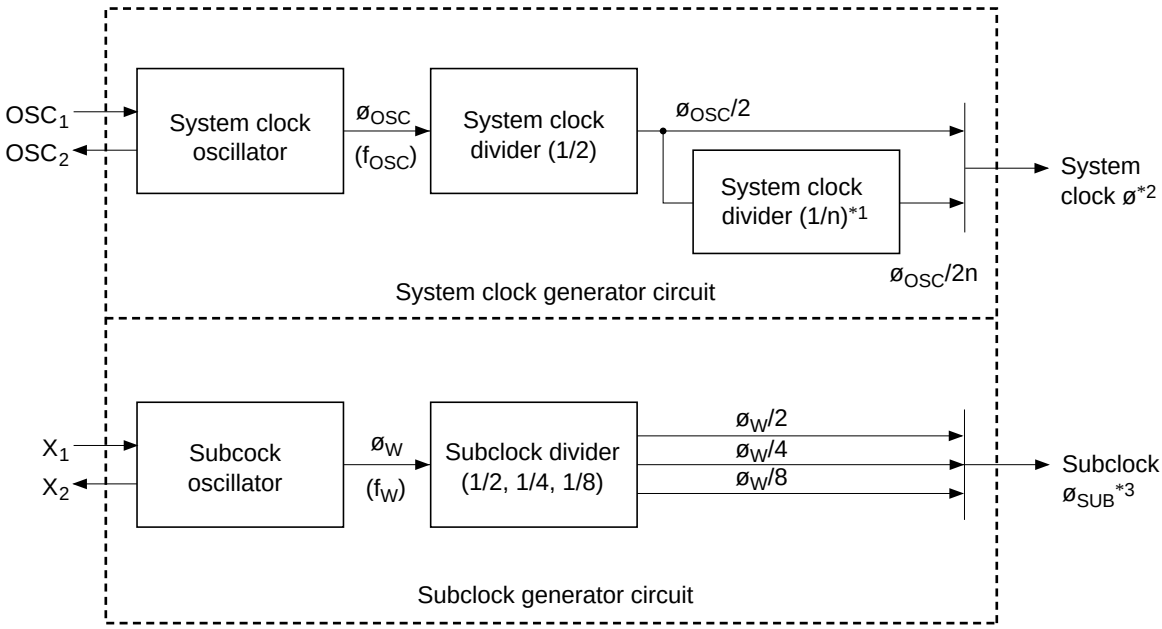
Condition Code Notation

Symbol	Meaning
↕	The flag is updated according to the result of the operation.
*	Indeterminate; the flag is left in an unpredictable state.
0	The flag is cleared to 0.
—	The flag is not changed.

6. Basic Bus Timing

The H8/300L CPU clock is generated either by the system clock generator circuit or the subclock generator circuit. The system clock generator circuit consists of the system clock oscillator and the system clock divider. The subclock generator circuit consists of the subclock oscillator and the system clock divider.

Clock Generator Circuits

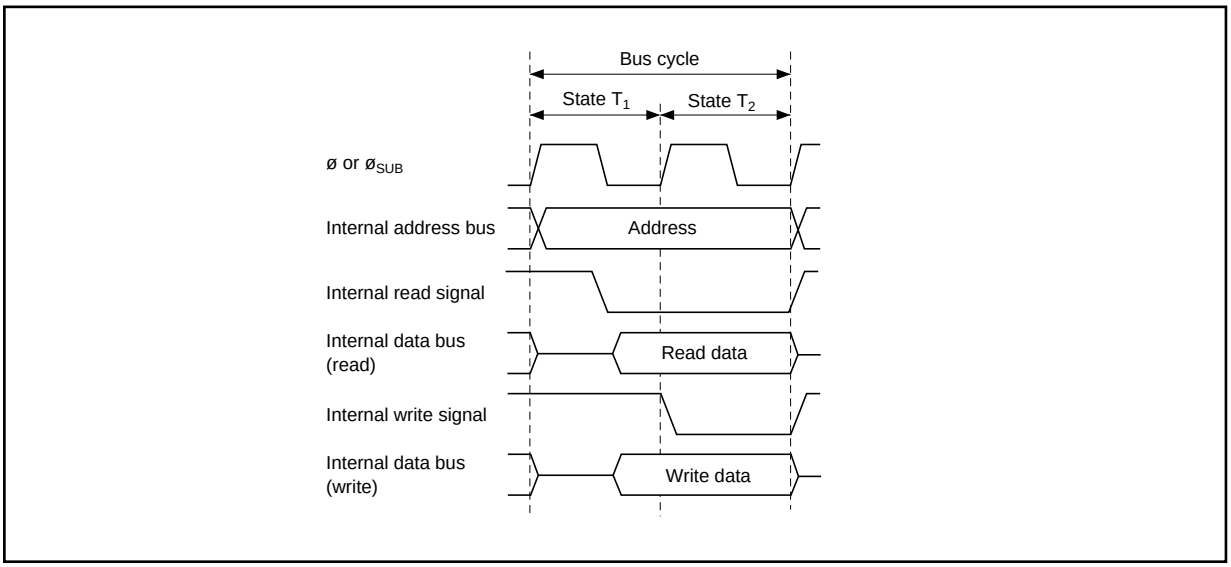


Notes: 1. The divisor n differs for each product in the series.
2. Only $ø_{OSC}/2$ is provided by the H8/3614 Series, H8/3714 Series, H8/3724 Series, and H8/3754 Series.
3. Only $ø_W/8$ is provided by the H8/3614 Series, H8/3714 Series, H8/3724 Series, and H8/3754 Series.

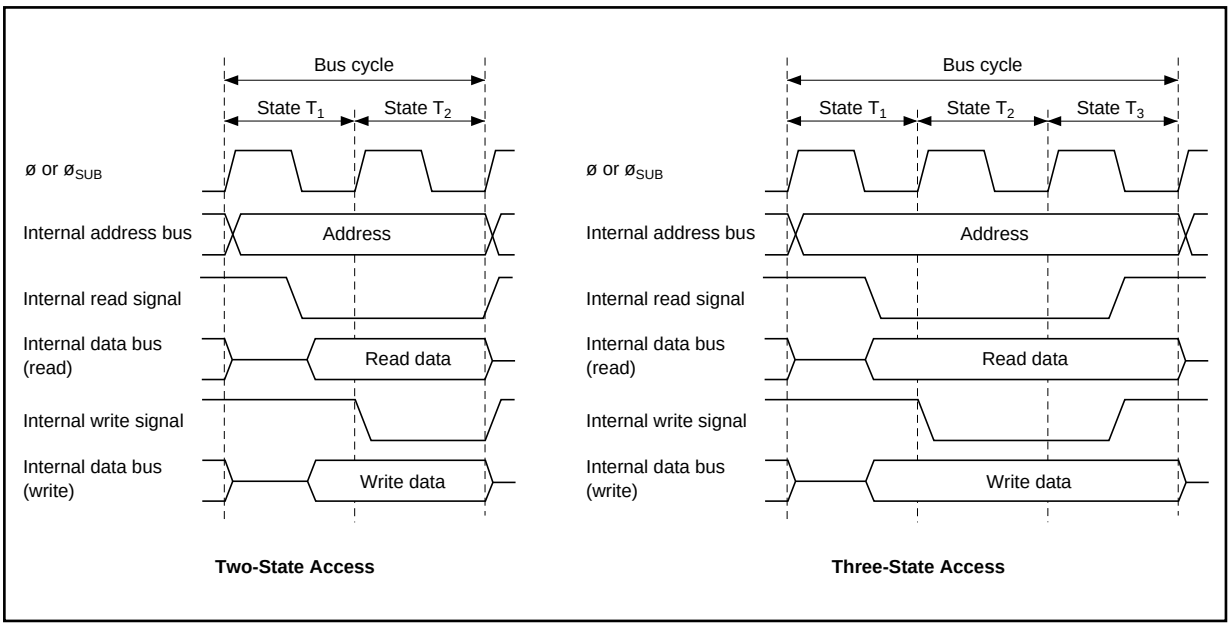
CPU Read/Write Cycle

The H8/300L CPU operates on either the system clock ø or the subclock $ø_{SUB}$, which are generated by the clock generator circuits. A single period of either the ø or $ø_{SUB}$ clock is called a state. Accesses, which differ for the on-chip memory and the on-chip peripheral modules, take place in basic bus cycles, which take either 2 or 3 states.

On-Chip Memory Access Timing (RAM and ROM): On-chip memory is accessed in two states. The data bus can be used in either 8-bit or 16-bit widths for byte or word accesses.



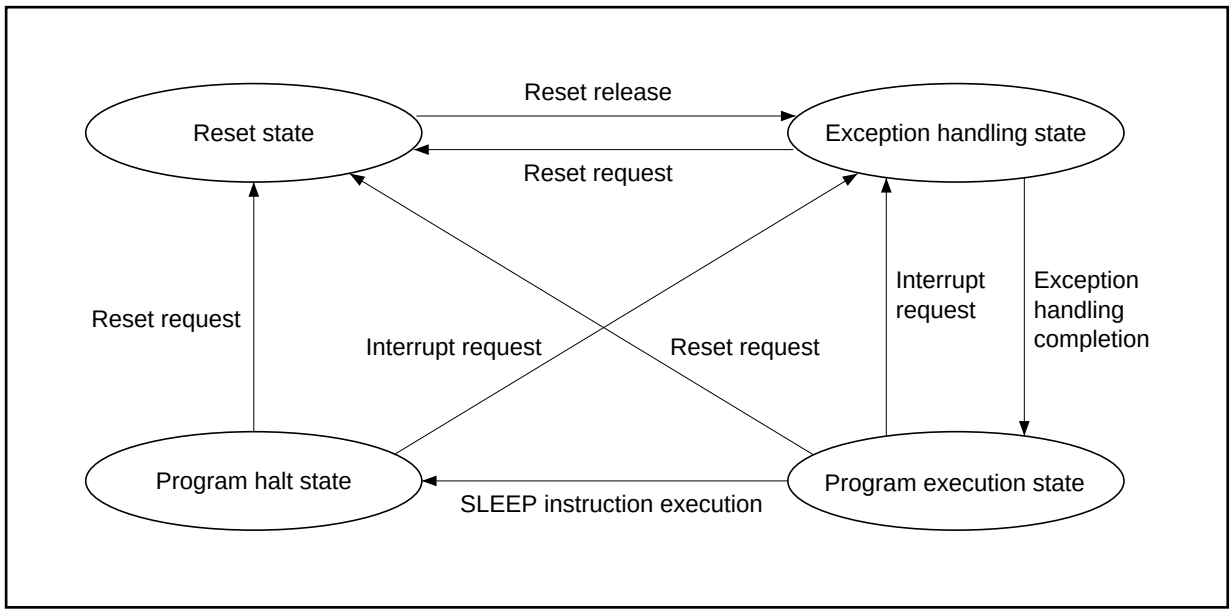
On-Chip Peripheral Module Access Timing: On-chip peripheral modules are accessed in two or three states. The data bus width in this case is 8 bits, so only byte access is possible.



7. CPU Operating States

The H8/300L CPU operates in four states, namely, program execution state, program halt state, exception handling state, and reset state. The figure below shows the transitions between these states.

State Transition Diagram



Reset State: The H8/300L CPU is reset in this state.

Program Execution State: In this state the H8/300L CPU executes instructions sequentially. The program execution state has two modes: active mode and subactive mode. In active mode the CPU operates on the system clock and in subactive mode the CPU operates according to the subclock. (For further details see the section titled “Low Power Modes” later in this document.)

Exception Handling State: This is a transient state that occurs when the H8/300L CPU execution state flow is changed by a reset, interrupt, or exception. The program counter and condition code register are saved on the stack using the stack pointer.

Program Halt State: The program halt state has three modes: sleep mode, standby mode, and watch mode. (For further details see the “Low Power Modes” section later in this document.)

8. Exception Handling

The H8/300L CPU supports two types of exceptions: resets and interrupts. When the H8/300L CPU starts interrupt exception handling, it saves the PC and CCR on the stack by referencing the SP. Then it sets the CCR I bit to 1 and fetches the starting address of the interrupt handling routine from the vector table.

Note that reset is the highest priority exception, and that when multiple interrupts occur at the same time they are processed according to their relative priorities. (See the description of the interrupt vector table.)

Priority	Exception Type	Activation Factors
1	Reset	Reset exception processing starts when the $\overline{\text{RES}}$ pin changes from low to high.
2	Interrupt	When an interrupt occurs, interrupt handling starts at the completion of the current instruction execution.*

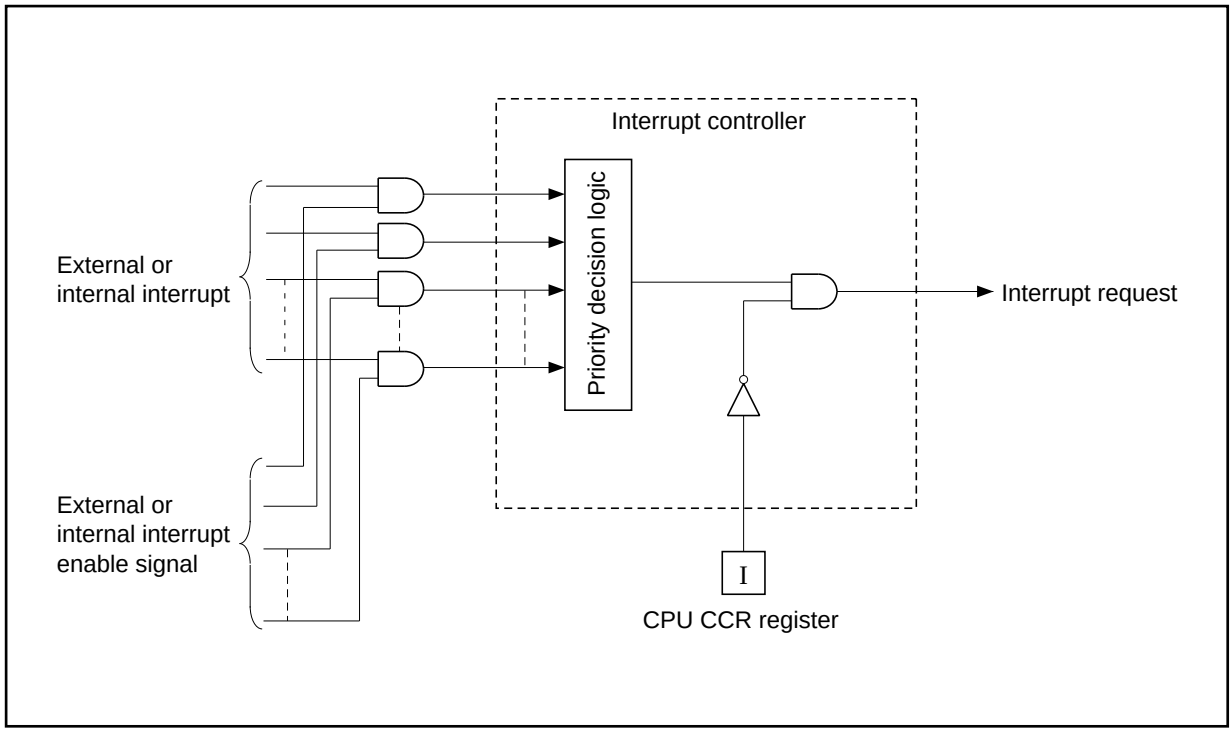
Note: * Not detected after the ANDC, ORC, XORC, and LDC instructions.

Interrupt Handling

Interrupt factors fall into two classes: external interrupts requested from external pins and internal interrupts requested by on-chip peripheral modules. Both external and internal interrupts are masked by the CCR I bit. That is, all interrupts are masked when the CCR I bit is set to 1. A unique vector address is allocated to each interrupt.

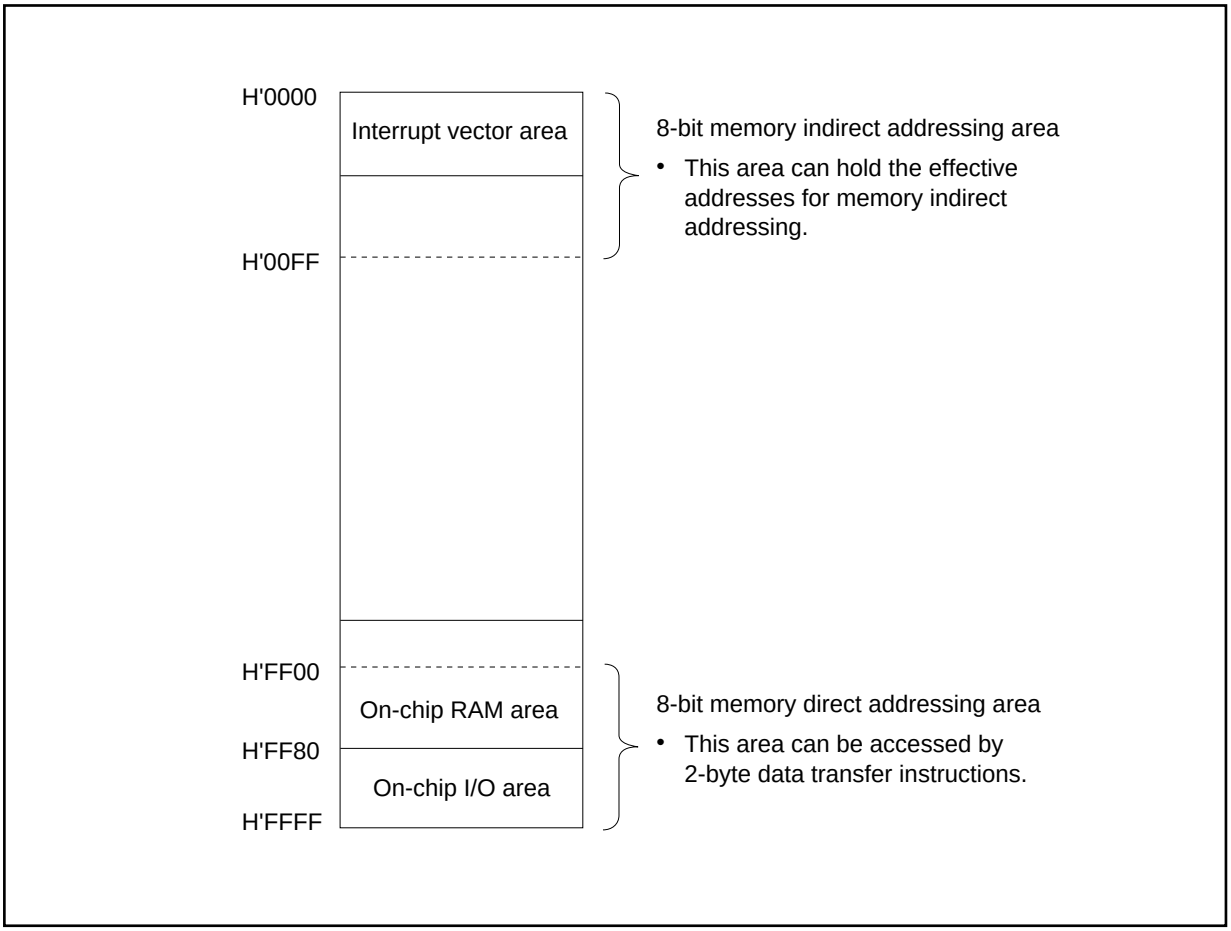
Interrupts are controlled by the interrupt controller. When multiple interrupts are requested at the same time, the interrupt controller selects the highest priority interrupt, and leaves the lower priority interrupts pending. When an interrupt occurs, the H8/300L CPU stores the program counter and CCR contents in the location indicated by the stack pointer, then fetches the address of the interrupt handler from the vector table, and begins executing that interrupt handler.

Interrupt Controller Block Diagram



9. Memory Map

The H8/300L CPU supports two special memory areas, the 8-bit memory indirect addressing area at addresses H'0000 to H'00FF and the 8-bit absolute addressing area at locations H'FF00 to H'FFFF.



8-Bit Memory Indirect Addressing Area (Addresses H'0000 to H'00FF)

The H8/300L CPU uses the lowest locations in the ROM area as the interrupt vector table. Since the details of the relationship between the interrupt vector table and the interrupts differ for different products in the H8/300L Series, those details are described in the hardware manual for each product. The H8/300L CPU supports the use of locations H'0000 to H'00FF, which include the interrupt vector table, for indirect addressing with 8-bit addresses that are included in the instruction code. This allows program sizes to be reduced by storing frequently used branch addresses in this region.

8-Bit Memory Direct Addressing Area (Addresses H'FF00 to H'FFFF)

The H8/300L CPU provides a short absolute addressing mode for the MOV instruction. This allows the H8/300L CPU to access locations H'FF00 to H'FFFF rapidly and programs to be implemented compactly using these short instructions. Since RAM is mapped to locations H'FF00 to H'FF7F and I/O registers are mapped to locations H'FF80 to H'FFFF, programs can implement high speed data handling by making effective use of the short absolute addressing mode.

Low Power Modes

The H8/300L Series microcomputers support active (high speed) mode in which programs are executed rapidly, and seven low power modes in which the IC power dissipation is significantly reduced. There are two low power modes in which programs are executed at relatively low speeds, namely, active (medium speed) mode and subactive mode. The five modes in which CPU operation is stopped are sleep (high speed) mode, sleep (medium speed) mode, sub-sleep mode, watch mode, and standby mode. Please refer to section 3, “Product Series and Operating Modes” for operating mode details for individual products, since the low power modes differ between products in the H8/300L Series.

1. Overview of Operating Mode Transitions

Active (High Speed) Mode

In active (high speed) mode the CPU operates at high speed based on a system clock with a 5 MHz operating frequency when the oscillator frequency is 10 MHz.

Active (Medium Speed) Mode

In active (medium speed) mode the CPU operates at a relatively lower speed based on a system clock generated by dividing a 5 MHz clock operating frequency (when the oscillator frequency is 10 MHz). The clock division ratio differs depending on the individual product.

Subactive Mode

In subactive mode the system clock oscillator used in active mode is stopped and the CPU operates at low speed and low power based on a subclock (16384 Hz, 8192 Hz, or 4096 Hz) generated by dividing a 32.768 kHz oscillator frequency.

Sleep (High Speed) Mode

In sleep (high speed) mode the on-chip peripheral modules operate based on a 5 MHz system clock (when the oscillator frequency is 10 MHz).

Sleep (Medium Speed) Mode

In sleep (medium speed) mode the on-chip peripheral modules operate based on a system clock generated by dividing a 5 MHz clock (when the oscillator frequency is 10 MHz). The clock division ratio differs depending on the individual product.

Subsleep Mode

In subsleep mode the on-chip peripheral modules operate based on the subclock. Subsleep mode differs from subactive mode in that the CPU is stopped in subsleep mode.

Watch Mode

In watch mode, a subset of the on-chip peripheral modules operate based on the subclock.

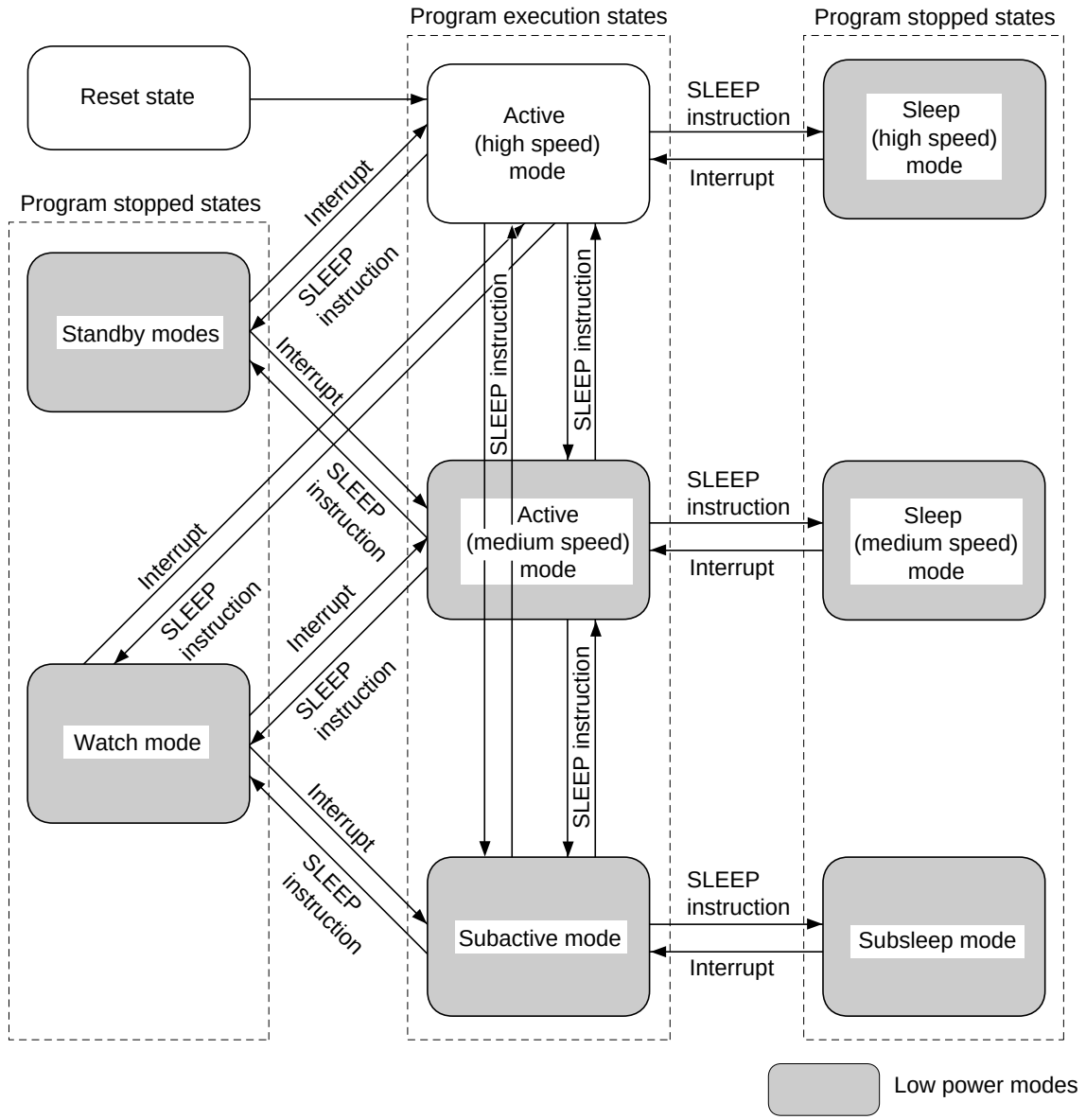
Standby Mode

In standby mode the CPU and all the on-chip peripheral modules are stopped. In this mode the IC's current drain is reduced to its lowest level, only a few µA. The contents of the on-chip RAM can be maintained by applying the specified data retention voltage to the IC.

Low Power Modes

The following figure provides an overview of the H8/300L Series operating modes and the transitions between those operating modes. The transitions between modes are made by interrupts and the execution of the SLEEP instruction.

H8/3927 Series Operating Modes and Transitions



Notes: 1. The IC switches to the reset state when the $\overline{\text{RES}}$ signal goes low, whatever the current state.
2. The particular interrupts that can clear a given low power mode differ for each mode.

2. Operating Modes and Current Drain

The table below shows the relationship between the operating modes and the IC current drain. The H8/300L Series microcomputers allow precise program control (using the SLEEP instruction) of power dissipation to match the power saving conditions required by the application. Thus these microcomputers can be extremely effective when used in portable equipment requiring battery operation.

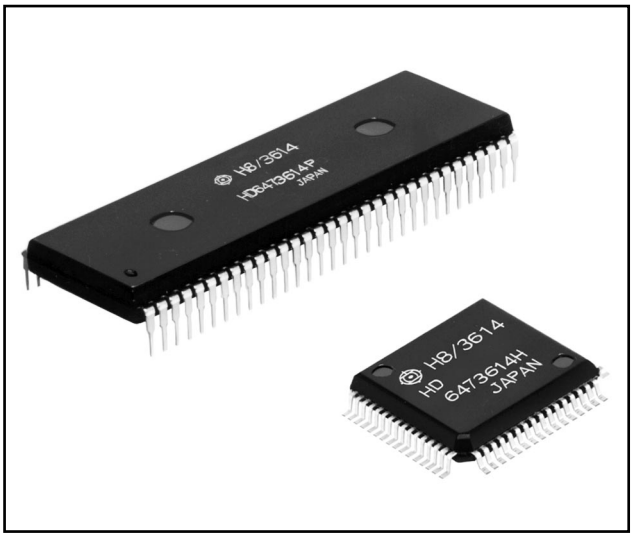
Operating Mode	Standby	Watch	Subactive	Sleep (High Speed)	Active (High Speed)
System clock oscillator	Stopped	Stopped	Stopped	Operating	Operating
CPU	Stopped	Stopped	Operating	Stopped	Operating
On-chip peripheral modules	Stopped	Stopped (except for clock functions)	Operating	Operating	Operating
Current dissipation reference value (typical)	2 µA	3 µA	10 µA	5 mA	15 mA
Power supply voltage (V_{CC})	2.7 V	2.7 V	2.7 V	5 V	5 V

The IC current drain differ between products. Refer to the hardware manual published by Hitachi for the corresponding products for details.

3. Product Series and Supported Operating Modes

The following table lists the correspondence between the products in the H8/300L Series and the operating modes supported. These operating modes differ slightly between products. Refer to the hardware manual published by Hitachi for the corresponding product for details.

Operating Mode / Product No.	Active (High Speed)	Active (Medium Speed)	Sleep (High Speed)	Sleep (Medium Speed)	Subactive ($ø_W$/2)	Subactive ($ø_W$/4)	Subactive ($ø_W$/8)	Sub-Sleep	Watch	Standby
H8/3612	●	—	●	—	—	—	●	—	●	●
H8/3613	●	—	●	—	—	—	●	—	●	●
H8/3614	●	—	●	—	—	—	●	—	●	●
H8/3712	●	—	●	—	—	—	●	—	●	●
H8/3713	●	—	●	—	—	—	●	—	●	●
H8/3714	●	—	●	—	—	—	●	—	●	●
H8/3723	●	—	●	—	—	—	●	—	●	●
H8/3724	●	—	●	—	—	—	●	—	●	●
H8/3725	●	—	●	—	—	—	●	—	●	●
H8/3726	●	—	●	—	—	—	●	—	●	●
H8/3753	●	—	●	—	—	—	●	—	●	●
H8/3754	●	—	●	—	—	—	●	—	●	●
H8/3812	●	●	●	—	●	●	●	●	●	●
H8/3813	●	●	●	—	●	●	●	●	●	●
H8/3814	●	●	●	—	●	●	●	●	●	●
H8/3834	●	●	●	—	●	●	●	●	●	●
H8/3836	●	●	●	—	●	●	●	●	●	●
H8/3837	●	●	●	—	●	●	●	●	●	●
H8/3875	●	●	●	—	●	●	●	●	●	●
H8/3876	●	●	●	—	●	●	●	●	●	●
H8/3877	●	●	●	—	●	●	●	●	●	●
H8/3924	●	●	●	●	●	●	●	●	●	●
H8/3925	●	●	●	●	●	●	●	●	●	●
H8/3926	●	●	●	●	●	●	●	●	●	●
H8/3927	●	●	●	●	●	●	●	●	●	●



The H8/3614 Series microcomputers are general purpose 8-bit microcomputers that include an on-chip A/D converter in a 64-pin package.

The H8/3614 Series microcomputers integrate, around an H8/300L CPU core, a rich set of peripheral functions, including 16, 24, and 32 kbytes of ROM, 512, 1024, and 1024 bytes of RAM, timers, two serial communications interfaces, an A/D converter, and I/O ports in a 64-pin package. They provide an optimal structure for relatively small-scale systems.

Additionally, the H8/3614 Series includes a ZTAT™ (zero turn around time) version of the H8/3614 that allows users to freely write programs to the on-chip PROM.

Features

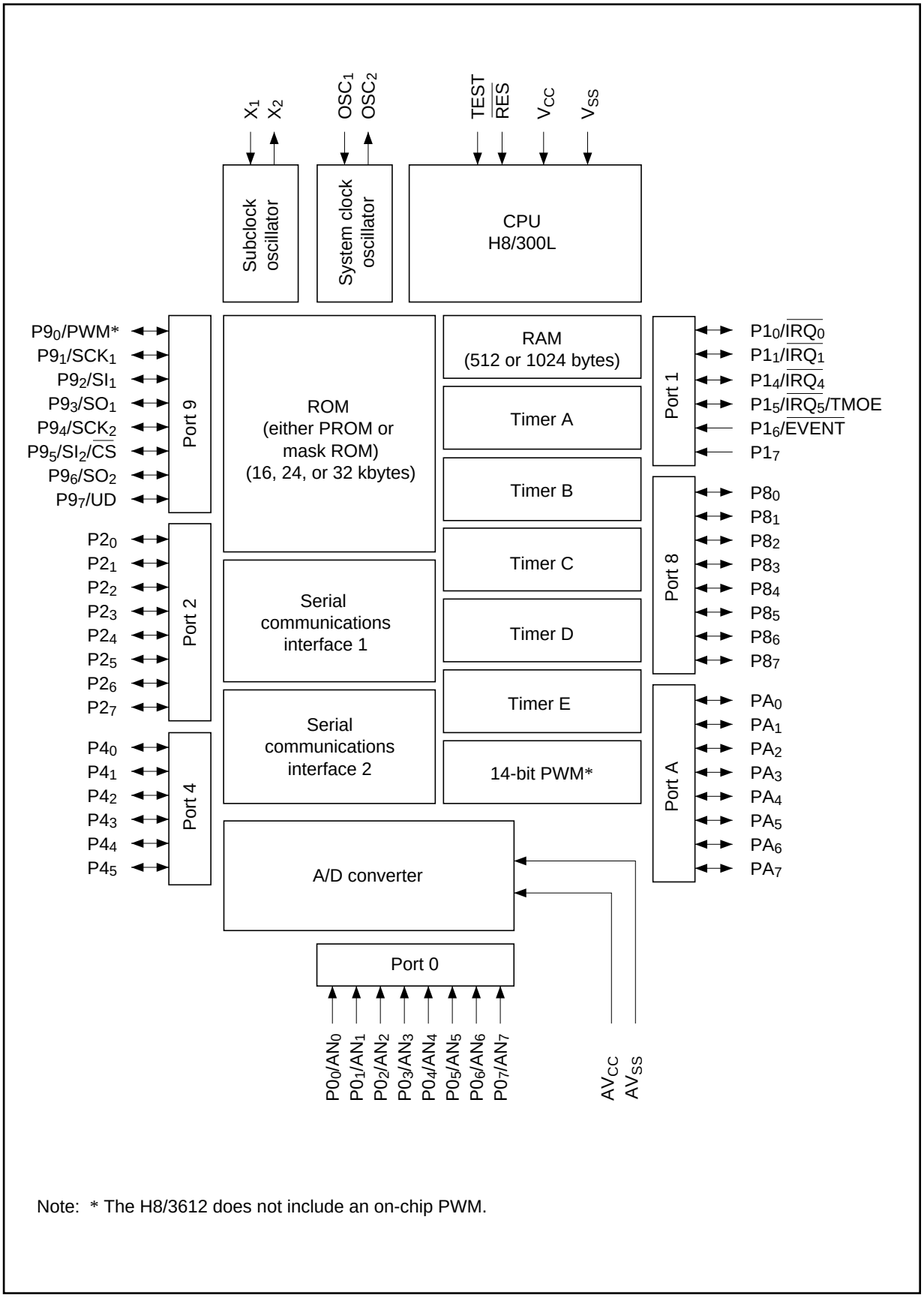
- **16, 24, and 32 kbytes of on-chip ROM**
- **512, 1024, and 1024 bytes of on-chip RAM**
- **Five 8-bit multi-function timer channels**
  - — Timer A: 8-bit interval timer or clock timer
  - — Timer B: 8-bit reload timer or event counter
  - — Timer C: 8-bit reload timer or event counter
  - — Timer D: 8-bit event counter
  - — Timer E: 8-bit reload timer
- **Serial communications interface (two channels)**
  - — SCI1: 8- or 16-bit clock synchronous transfers
  - — SCI2: 8-bit clock synchronous transfers (includes a 32-byte data buffer)
- **14-bit PWM (H8/3613 and H8/3614)**
  - — Pulse divider technique used to reduce ripple
- **A/D converter**
  - — Resolution: 8 bits
  - — Eight analog voltage input channels
  - — Resistor ladder based successive approximations
  - — Sample-and-hold function

- **I/O ports**
  - — I/O pins: 44 pins (of which six are PMOS open drain circuits)
  - — Input pins: 10 pins
- **Interrupts**
  - — External interrupts: Six interrupts ($\overline{IRQ_0}$, $\overline{IRQ_1}$, $\overline{IRQ_2}$, $\overline{IRQ_3}$, $\overline{IRQ_4}$, and $\overline{IRQ_5}$)
  - — Internal interrupts: Nine interrupts
- **Low power states**
  - — Sleep mode
  - — Standby mode
  - — Watch mode (when a 32 kHz subclock is used)
  - — Subactive mode (when a 32 kHz subclock is used)
- **Two independent on-chip clock oscillator systems**
  - — System clock oscillator (oscillator frequency: 2 to 8.38 MHz)
  - — Subclock oscillator (oscillator frequency: 32.768 kHz)

Ordering Information

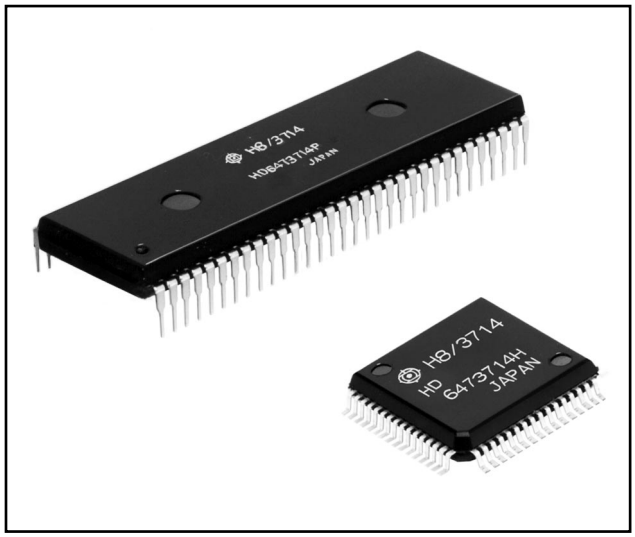
Product No.	Package	ROM
HD6433612P	DP-64S	Mask ROM
HD6433612H	FP-64A	
HD6433613P	DP-64S	Mask ROM
HD6433613H	FP-64A	
HD6433614P	DP-64S	Mask ROM
HD6433614H	FP-64A	
HD6473614P	DP-64S	PROM
HD6473614H	FP-64A	

Block Diagram



Note: * The H8/3612 does not include an on-chip PWM.

H8/3712, H8/3713, H8/3714



The H8/3714 Series microcomputers are 8-bit single chip microcomputers that can directly drive vacuum fluorescent displays (VFD).

The H8/3712, H8/3713, and H8/3714 microcomputers integrate, around an H8/300L CPU core, a rich set of peripheral functions, including 16, 24, and 32 kbytes of ROM, 384, 384, and 512 bytes of RAM, a VFD (vacuum fluorescent display) controller/driver, timers, two serial communications interfaces, a 14-bit PWM, an A/D converter, and I/O ports. Since these microcomputers include high breakdown voltage pins that can directly drive VFD panels, they are particularly suited for use in applications that require VFD.

Additionally, the H8/3714 Series includes a ZTAT™ (zero turn around time) version of the H8/3714 that allows users to freely write programs to the on-chip PROM.

Features

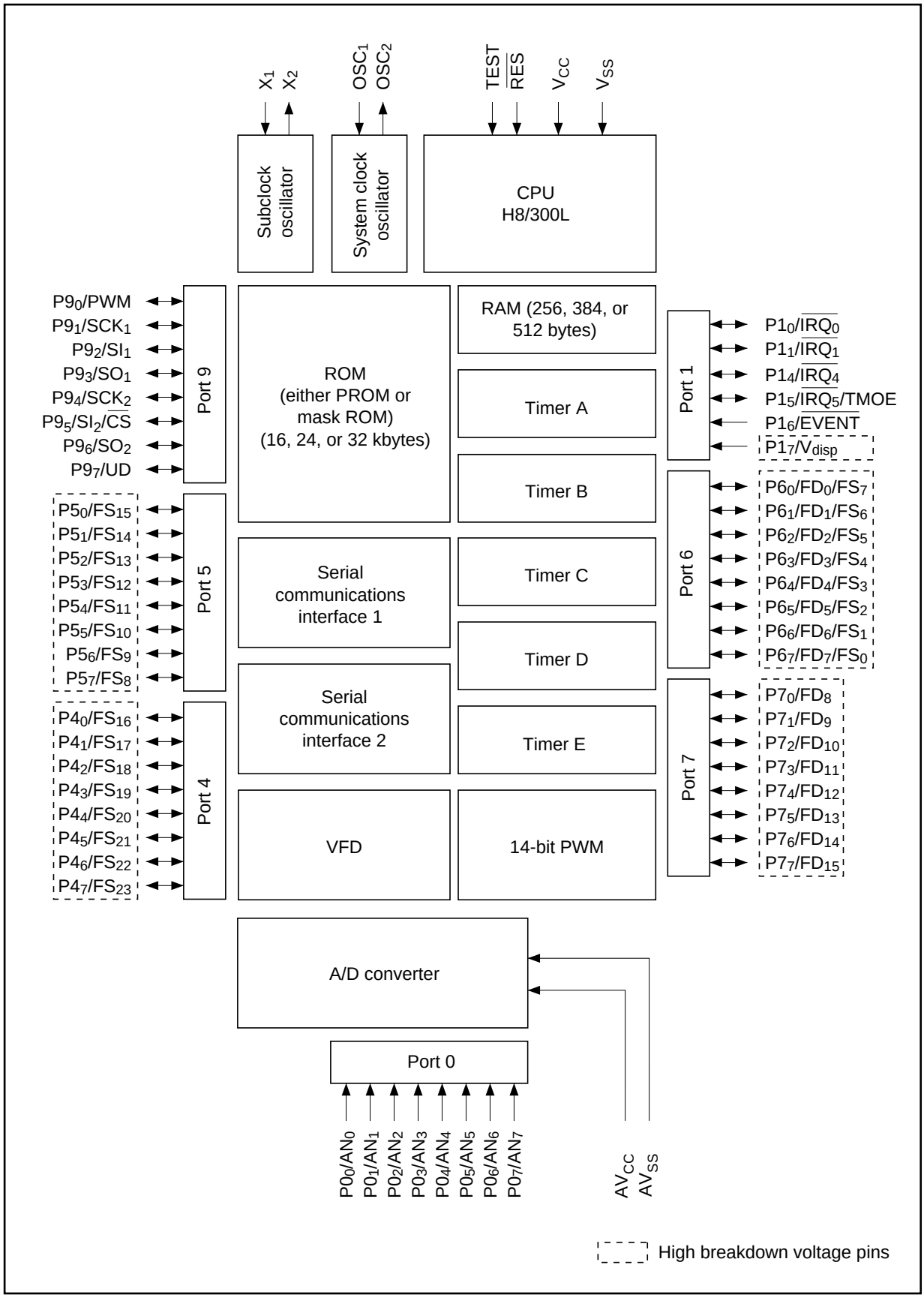
- **16, 24, and 32 kbytes of on-chip ROM**
- **384, 384, and 512 bytes of on-chip RAM**
- **VFD controller/driver**
  - — Digit pins: 1 to 16 pins
  - — Segment pins: 1 to 24 pins (of which 8 also function as digit pins)
  - — Function supporting a variable number of display digits
  - — Eight level dimmer function
- **Five 8-bit multi-function timer channels**
  - — Timer A: 8-bit interval timer or clock timer
  - — Timer B: 8-bit reload timer or event counter
  - — Timer C: 8-bit reload timer or event counter
  - — Timer D: 8-bit event counter
  - — Timer E: 8-bit reload timer
- **Serial communications interface (two channels)**
  - — SCI1: 8- or 16-bit clock synchronous transfers
  - — SCI2: 8-bit clock synchronous transfers (includes a 32-byte data buffer)

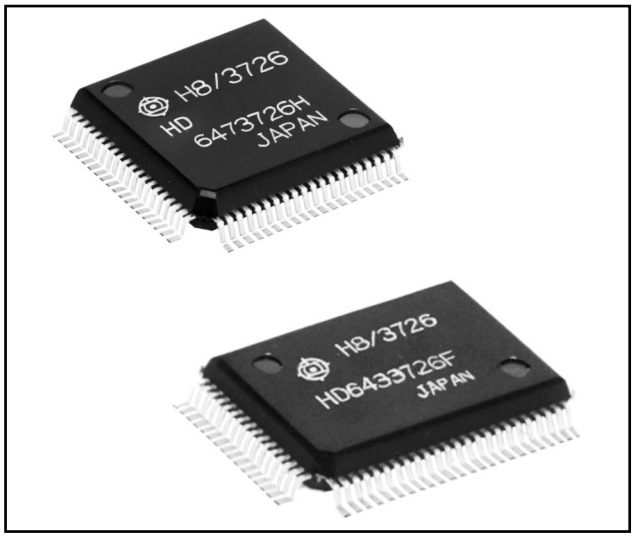
- **14-bit PWM**
  - — Pulse divider technique used to reduce ripple
- **A/D converter**
  - — Resolution: 8 bits
  - — Eight analog voltage input channels
  - — Resistor ladder based successive approximations
  - — Sample-and-hold function
- **I/O ports**
  - — High breakdown voltage I/O pins: 32 pins
  - — High breakdown voltage input pins: 1 pin
  - — Standard breakdown voltage I/O pins: 12 pins
  - — Standard breakdown voltage input pins: 9 pins
- **Interrupts**
  - — External interrupts: Four interrupts ($\overline{IRQ_0}$, $\overline{IRQ_1}$, $\overline{IRQ_4}$, and $\overline{IRQ_5}$)
  - — Internal interrupts: Ten interrupts
- **Low power states**
  - — Sleep mode
  - — Standby mode
  - — Watch mode (when a 32 kHz subclock is used)
  - — Subactive mode (when a 32 kHz subclock is used)
- **Two independent on-chip clock oscillator systems**
  - — System clock oscillator (oscillator frequency: 2 to 8.38 MHz)
  - — Subclock oscillator (oscillator frequency: 32.768 kHz)

Ordering Information

Product No.	Package	ROM
HD6433712P	DP-64S	Mask ROM
HD6433712H	FP-64A	
HD6433713P	DP-64S	Mask ROM
HD6433713H	FP-64A	
HD6433714P	DP-64S	Mask ROM
HD6433714H	FP-64A	
HD6473714P	DP-64S	PROM
HD6473714H	FP-64A	

Block Diagram





The H8/3724 Series microcomputers are 8-bit single chip microcomputers that can directly drive vacuum fluorescent displays (VFD).

The H8/3723, H8/3724, H8/3725, and H8/3726 microcomputers integrate, around an H8/300L CPU core, a rich set of peripheral functions, including 24, 32, 40, and 48 kbytes of ROM, 384, 512, 640, and 1024 bytes of RAM, a VFD (vacuum fluorescent display) controller/driver, timers, two serial communications interfaces, a 14-bit PWM, an A/D converter, and I/O ports. Since these microcomputers include high breakdown voltage pins that can directly drive VFD panels, they are particularly suited for use in applications that require VFD.

Additionally, the H8/3724 Series includes ZTAT™ (zero turn around time) versions of the H8/3724 and H8/3726 that allow users to freely write programs to the on-chip PROM.

Features

- **24, 32, 40, and 48 kbytes of on-chip ROM**
- **384, 512, 640, and 1024 bytes of on-chip RAM**
- **VFD controller/driver**
  - — Digit pins: 1 to 16 pins
  - — Segment pins: 1 to 28 pins (of which 8 also function as digit pins)
  - — Function supporting a variable number of display digits
  - — Eight level dimmer function
- **Five 8-bit multi-function timer channels**
  - — Timer A: 8-bit interval timer or clock timer
  - — Timer B: 8-bit reload timer or event counter
  - — Timer C: 8-bit reload timer or event counter
  - — Timer D: 8-bit event counter
  - — Timer E: 8-bit reload timer
- **Serial communications interface (two channels)**
  - — SCI1: 8- or 16-bit clock synchronous transfers
  - — SCI2: 8-bit clock synchronous transfers (includes a 32-byte data buffer)

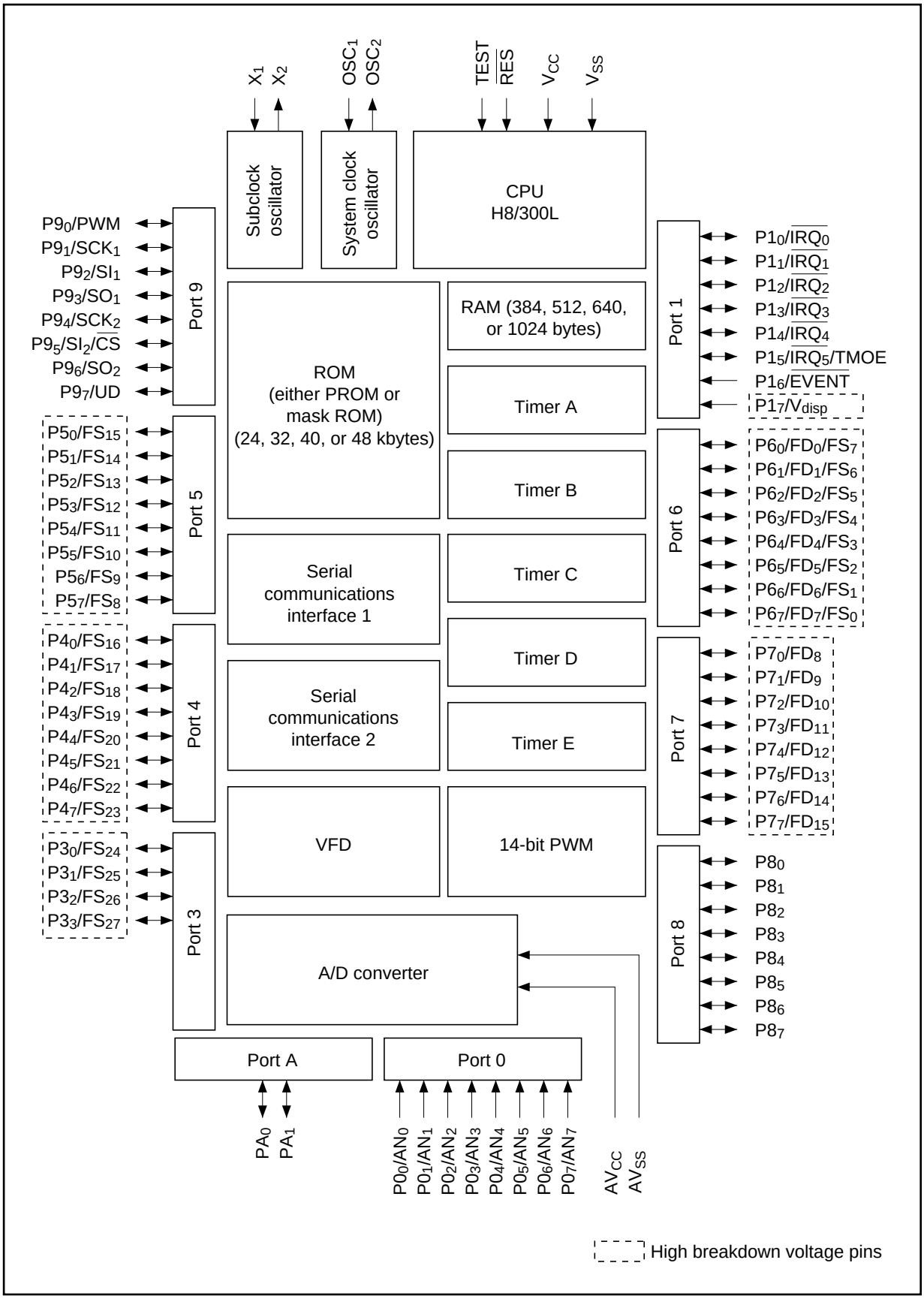
- **14-bit PWM**
  — Pulse divider technique used to reduce ripple
- **A/D converter**
  — Resolution: 8 bits
  — Eight analog voltage input channels
  — Resistor ladder based successive approximations
  — Sample-and-hold function
- **I/O ports**
  — High breakdown voltage I/O pins: 36 pins
  — High breakdown voltage input pins: 1 pin
  — Standard breakdown voltage I/O pins: 24 pins
  — Standard breakdown voltage input pins: 9 pins
- **Interrupts**
  — External interrupts: Six interrupts ($\overline{IRQ_0}$ to $\overline{IRQ_5}$)
  — Internal interrupts: Ten interrupts
- **Low power states**
  — Sleep mode
  — Standby mode
  — Watch mode (when a 32 kHz subclock is used)
  — Subactive mode (when a 32 kHz subclock is used)
- **Two independent on-chip clock oscillator systems**
  — System clock oscillator (oscillator frequency: 2 to 8.38 MHz)
  — Subclock oscillator (oscillator frequency: 32.768 kHz)

Ordering Information

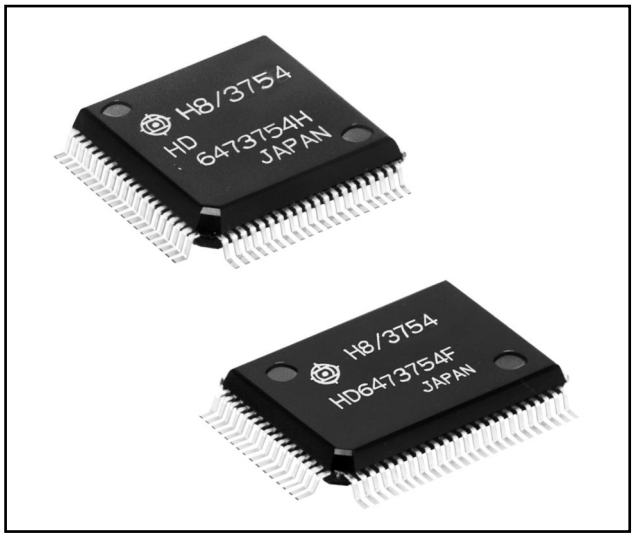
Product No.	Package	ROM
HD6433723H	FP-80A	Mask ROM
HD6433723F	FP-80B	
HD6433724H	FP-80A	Mask ROM
HD6433724F	FP-80B	
HD6433725H	FP-80A	Mask ROM
HD6433725F	FP-80B	

Product No.	Package	ROM
HD6433726H	FP-80A	Mask ROM
HD6433726F	FP-80B	
HD6473724H	FP-80A	PROM
HD6473724F	FP-80B	
HD6473726H	FP-80A	PROM
HD6473726F	FP-80B	

Block Diagram



H8/3753, H8/3754



The H8/3754 Series microcomputers are 8-bit single chip microcomputers that can directly drive vacuum fluorescent displays (VFD).

The H8/3753 and H8/3754 microcomputers integrate, around an H8/300L CPU core, a rich set of peripheral functions, including 24 and 32 kbytes of ROM, 1024 bytes of RAM, a VFD (vacuum fluorescent display) controller/driver, timers, two serial communications interfaces, a 14-bit PWM, an A/D converter, and I/O ports. Since these microcomputers include high breakdown voltage pins that can directly drive VFD panels, they are particularly suited for use in applications that require VFD.

Additionally, the H8/3754 Series includes ZTAT™ (zero turn around time) versions of the H8/3726 that allow users to freely write programs to the on-chip PROM.

Features

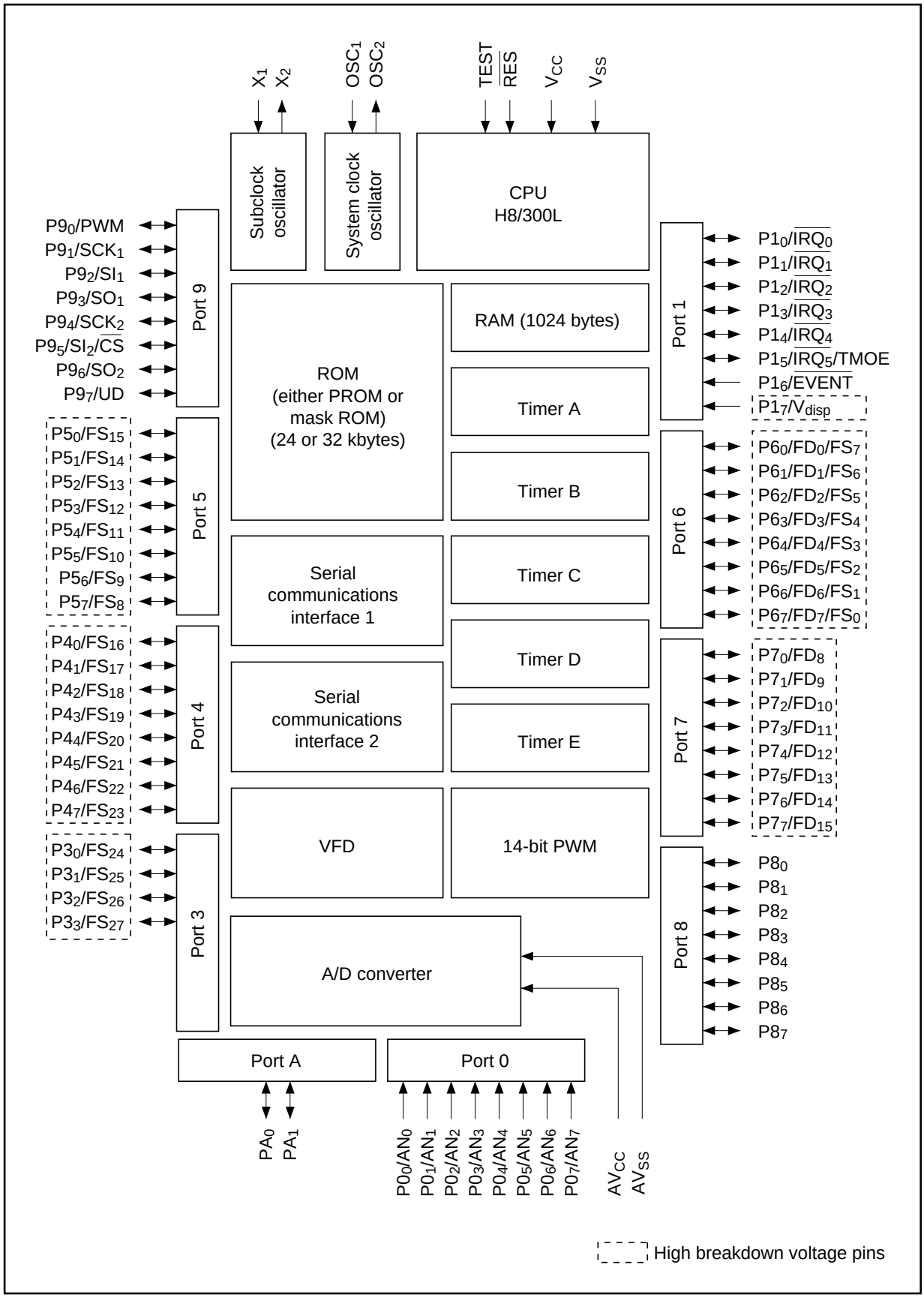
- **24 and 32 kbytes of on-chip ROM**
- **1024 bytes of on-chip RAM**
- **VFD controller/driver**
  - — Digit pins: 1 to 16 pins
  - — Segment pins: 1 to 28 pins (of which 8 also function as digit pins)
  - — Function supporting a variable number of display digits
  - — Eight level dimmer function
- **Five 8-bit multi-function timer channels**
  - — Timer A: 8-bit interval timer or clock timer
  - — Timer B: 8-bit reload timer or event counter
  - — Timer C: 8-bit reload timer or event counter
  - — Timer D: 8-bit event counter
  - — Timer E: 8-bit reload timer
- **Serial communications interface (two channels)**
  - — SCI1: 8- or 16-bit clock synchronous transfers
  - — SCI2: 8-bit clock synchronous transfers (includes a 32-byte data buffer)

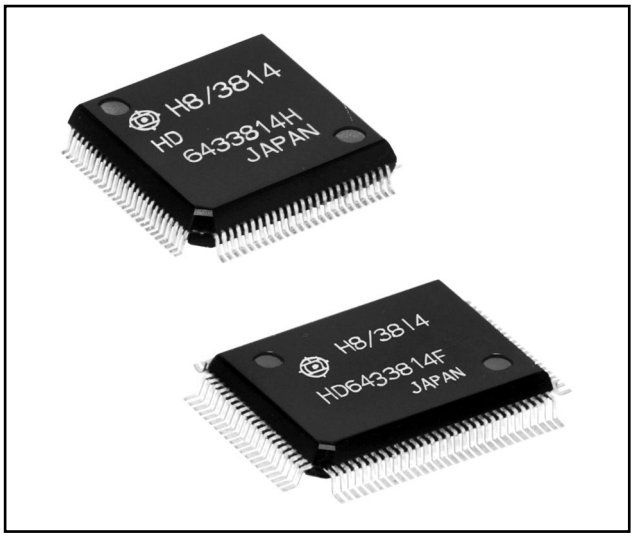
- **14-bit PWM**
  - — Pulse divider technique used to reduce ripple
- **A/D converter**
  - — Resolution: 8 bits
  - — Eight analog voltage input channels
  - — Resistor ladder based successive approximations
  - — Sample-and-hold function
- **I/O ports**
  - — High breakdown voltage I/O pins: 36 pins
  - — High breakdown voltage input pins: 1 pin
  - — Standard breakdown voltage I/O pins: 24 pins
  - — Standard breakdown voltage input pins: 9 pins
- **Interrupts**
  - — External interrupts: Six interrupts ($\overline{IRQ_0}$ to $\overline{IRQ_5}$)
  - — Internal interrupts: Ten interrupts
- **Low power states**
  - — Sleep mode
  - — Standby mode
  - — Watch mode (when a 32 kHz subclock is used)
  - — Subactive mode (when a 32 kHz subclock is used)
- **Two independent on-chip clock oscillator systems**
  - — System clock oscillator (oscillator frequency: 2 to 8.38 MHz)
  - — Subclock oscillator (oscillator frequency: 32.768 kHz)

Ordering Information

Product No.	Package	ROM
HD6433753H	FP-80A	Mask ROM
HD6433753F	FP-80B	
HD6433754H	FP-80A	Mask ROM
HD6433754F	FP-80B	
HD6473726H	FP-80A	PROM
HD6473726F	FP-80B	

Block Diagram





The H8/3814 Series microcomputers are 8-bit single chip microcomputers that can directly drive liquid crystal display (LCD).

The H8/3812, H8/3813, and H8/3814 microcomputers integrate, around an H8/300L CPU core, a rich set of peripheral functions, including 16, 24, and 32 kbytes of ROM, 512 bytes of RAM, an LCD (liquid crystal display) controller/driver, timers, two serial communications interfaces, an A/D converter, and I/O ports. These products are particularly suited for use as the embedded microprocessor in applications that require LCD.

Additionally, the H8/3814 Series includes a ZTAT™ (zero turn around time) version of the H8/3834 that allows users to freely write programs to the on-chip PROM.

Features

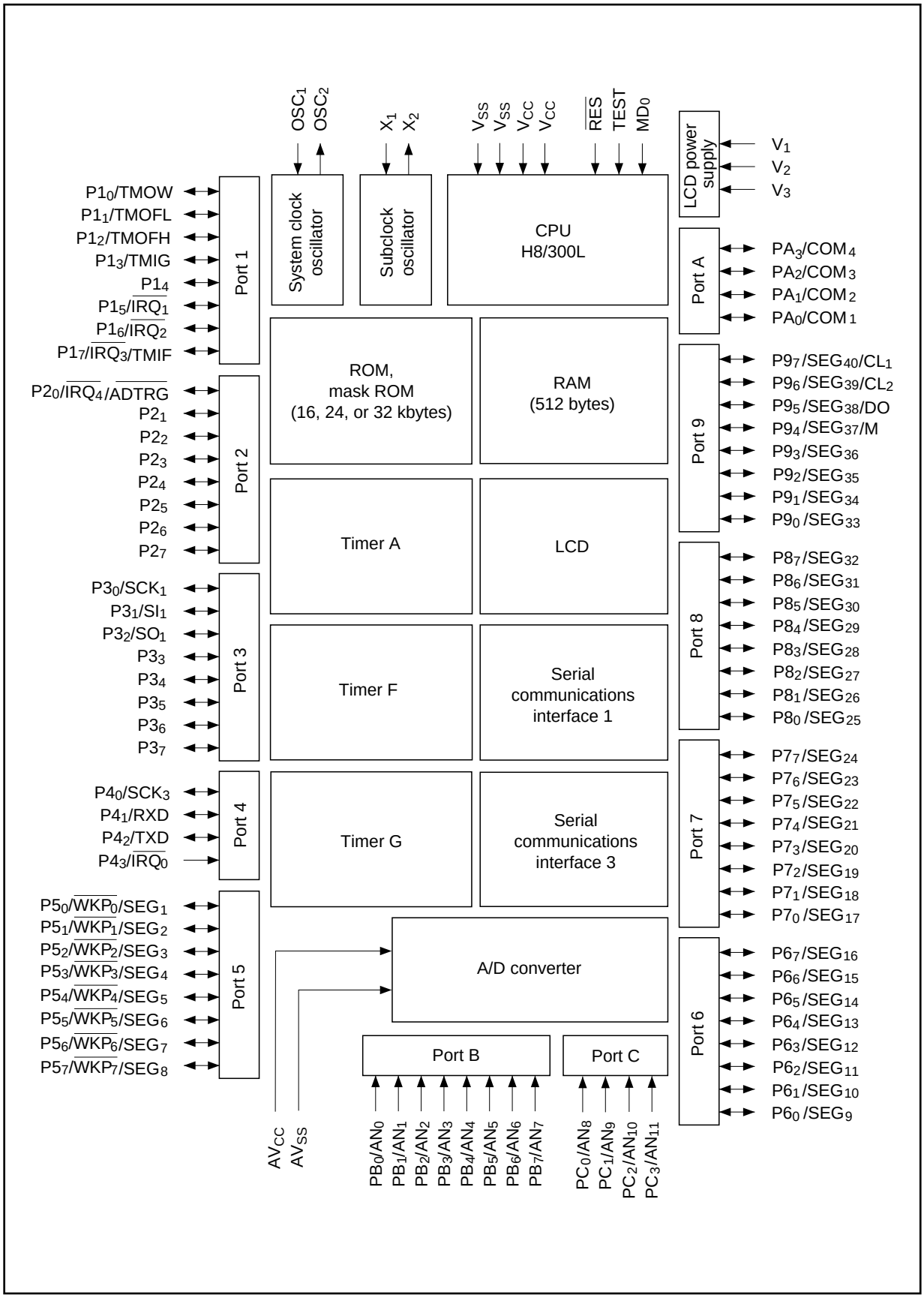
- **16, 24, and 32 kbytes of on-chip ROM**
- **512 bytes of on-chip RAM**
- **LCD controller/driver**
  - — Forty segment pins and four common pins built in
  - — Four duty ratios: Static, 1/2, 1/3 and 1/4
  - — External segment expansion (however, only with static and 1/2 duty)
  - — Segment pins: Can be switched to be used as general purpose port pins in 4-pin units
- **Three 8- and 16-bit multi-function timer channels**
  - — Timer A: 8-bit interval timer or clock timer
  - — Timer F: 16-bit output compare timer or event counter
  - — Timer G: 8-bit interval timer or input capture timer
- **Serial communications interface (two channels)**
  - — SCI1: 8- or 16-bit clock synchronous transfers
  - — SCI3: 8-bit clock synchronous/asynchronous transfers (includes a multi-processor communications function)

- **A/D converter**
  - — Resolution: 8 bits
  - — Twelve analog voltage input channels
  - — Resistor ladder based successive approximations
  - — Sample-and-hold function
- **I/O ports**
  - — I/O pins: 71 pins
  - — Input pins: 13 pins
- **Interrupts**
  - — External interrupts: 13 interrupts ($\overline{IRQ_0}$ to $\overline{IRQ_4}$, and $\overline{WKP_0}$ to $\overline{WKP_7}$)
  - — Internal interrupts: 16 interrupts
- **Low power modes**
  - — Sleep mode
  - — Standby mode
  - — Watch mode
  - — Subsleep mode
  - — Subactive mode
  - — Active (medium speed) mode
- **Two independent on-chip clock oscillator systems**
  - — System clock oscillator (oscillator frequency: 1 to 10 MHz)
  - — Subclock oscillator (oscillator frequency: 32.768 kHz)

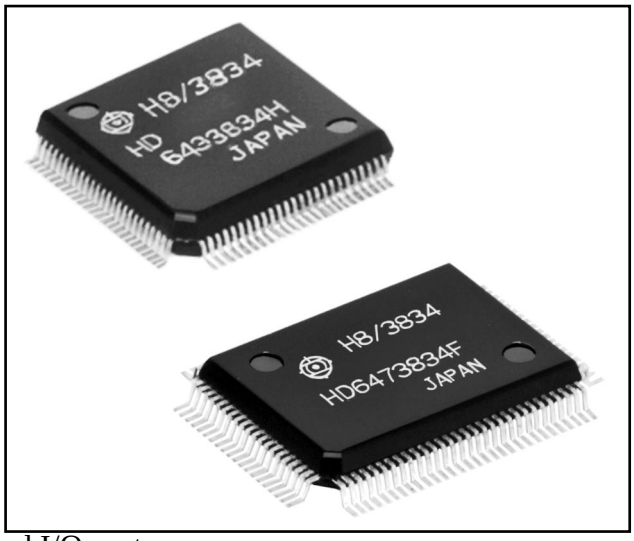
Ordering Information

Product No.	Package	ROM
HD6433812H	FP-100B	Mask ROM
HD6433812F	FP-100A	
HD6433813H	FP-100B	Mask ROM
HD6433813F	FP-100A	
HD6433814H	FP-100B	Mask ROM
HD6433814F	FP-100A	
HD6473834H	FP-100B	PROM
HD6473834F	FP-100A	

Block Diagram



H8/3834, H8/3836, H8/3837



The H8/3834 Series microcomputers are 8-bit single chip microcomputers that can directly drive liquid crystal display (LCD).

The H8/3834, H8/3836, and H8/3837 microcomputers integrate, around an H8/300L CPU core, a rich set of peripheral functions, including 32, 48, and 60 kbytes of ROM, 1, 2, and 2 kbytes of RAM, an LCD (liquid crystal display) controller/ driver, timers, three serial communications interfaces, a 14-bit PWM, an A/D converter, and I/O ports.
These products are particularly suited for use as the embedded microprocessor in applications that require LCD.

Additionally, the H8/3834 Series includes ZTAT™ (zero turn around time) versions of the H8/3834 and H8/3837 that allow users to freely write programs to the on-chip PROM.

Features

- **32, 48, and 60 kbytes of on-chip ROM**
- **1, 2, and 2 kbytes of on-chip RAM**
- **LCD controller/driver**
  - — Forty segment pins and four common pins built in
  - — Four duty ratios: Static, 1/2, 1/3 and 1/4
  - — External segment expansion
  - — Segment pins: Can be switched to be used as general purpose port pins in 4-pin units.
- **Five 8- and 16-bit multi-function timer channels**
  - — Timer A: 8-bit interval timer or clock timer
  - — Timer B: 8-bit reload timer or event counter
  - — Timer C: 8-bit reload timer or event counter
  - — Timer F: 16-bit output compare timer or event counter
  - — Timer G: 8-bit interval timer or input capture timer
- **Serial communications interface (three channels)**
  - — SCI1: 8- or 16-bit clock synchronous transfers
  - — SCI2: 8-bit clock synchronous transfers (includes a 32-byte data buffer)
  - — SCI3: 8-bit clock synchronous/asynchronous transfers (includes a multi-processor communications function)

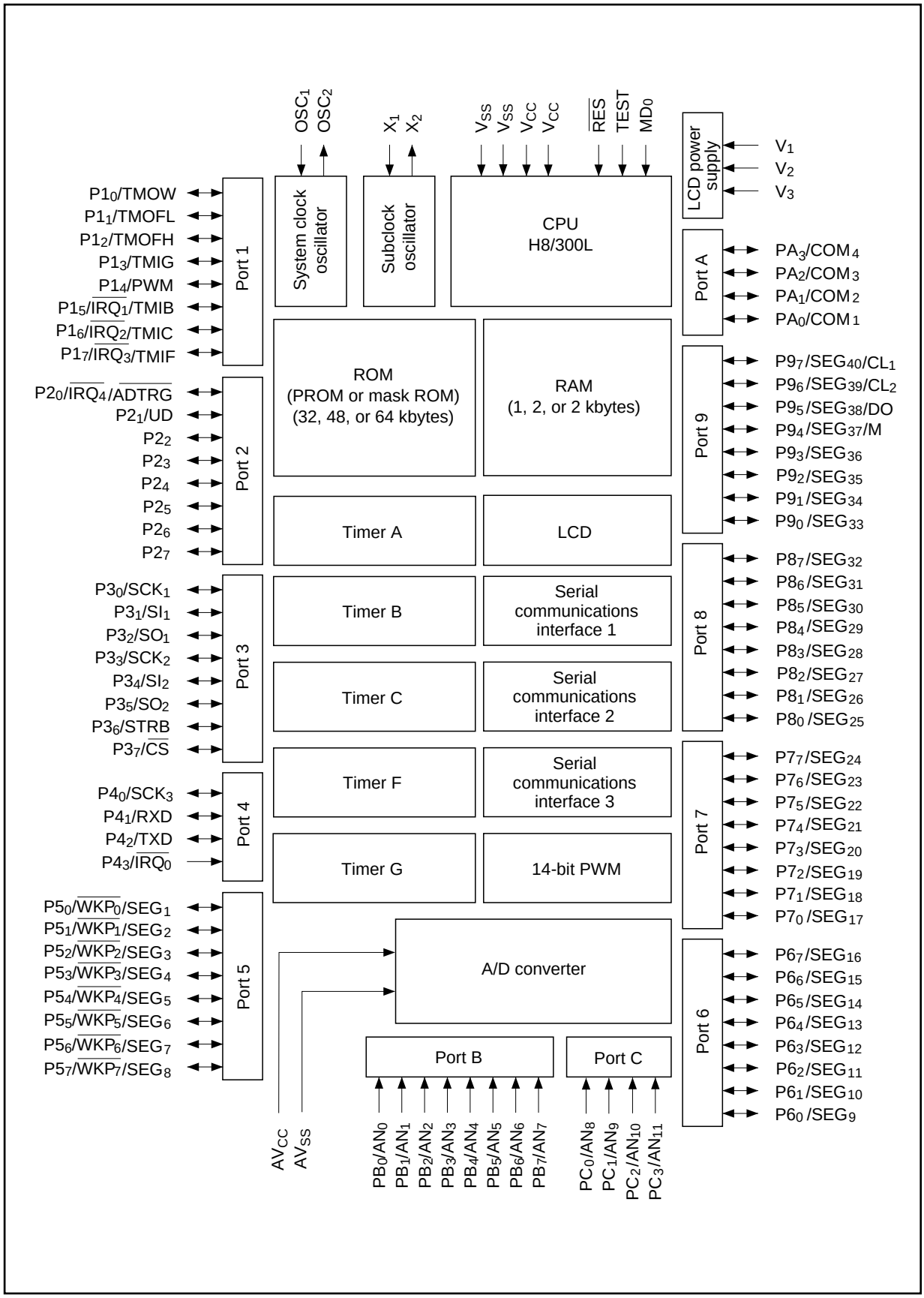
- **14-bit PWM**
  - — Pulse divider technique used to reduce ripple.
- **A/D converter**
  - — Resolution: 8 bits
  - — Twelve analog voltage input channels
  - — Resistor ladder based successive approximations
  - — Sample-and-hold function
- **I/O ports**
  - — I/O pins: 71 pins
  - — Input pins: 13 pins
- **Interrupts**
  - — External interrupts: 13 interrupts ($\overline{IRQ_0}$ to $\overline{IRQ_4}$, and $\overline{WKP_0}$ to $\overline{WKP_7}$)
  - — Internal interrupts: 20 interrupts
- **Low power modes**
  - — Sleep mode
  - — Standby mode
  - — Watch mode
  - — Subsleep mode
  - — Subactive mode
  - — Active (medium speed) mode
- **Two independent on-chip clock oscillator systems**
  - — System clock oscillator (oscillator frequency: 1 to 10 MHz)
  - — Subclock oscillator (oscillator frequency: 32.768 kHz)

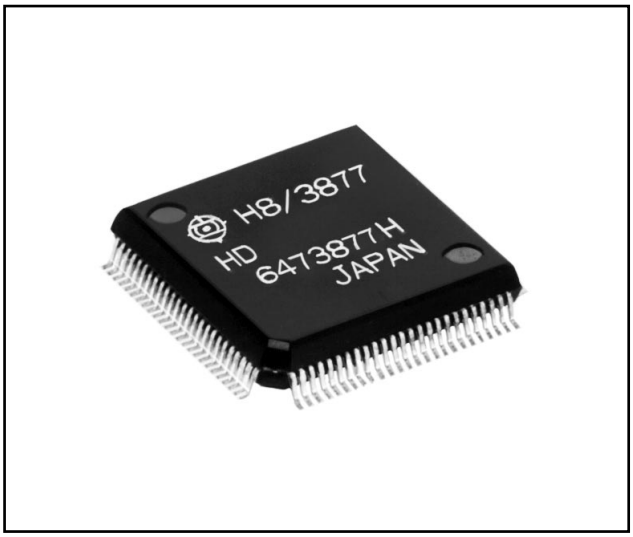
Ordering Information

Product No.	Package	ROM
HD6433834H	FP-100B	Mask ROM
HD6433834F	FP-100A	
HD6433836H	FP-100B	Mask ROM
HD6433836F	FP-100A	
HD6433837H	FP-100B	Mask ROM
HD6433837F	FP-100A	

Product No.	Package	ROM
HD6473834H	FP-100B	PROM
HD6473834F	FP-100A	
HD6473837H	FP-100B	PROM
HD6473837F	FP-100A	

Block Diagram





The H8/3877 Series microcomputers are 8-bit single chip microcomputers that can output tones of arbitrary frequencies.

The H8/3875, H8/3876, and H8/3877 microcomputers integrate, around an H8/300L CPU core, a rich set of peripheral functions, including 40, 48, and 60 kbytes of ROM, 2 kbytes of RAM, a DTMF (dual tone multi-frequency) generator, a multi-tone generator, an LCD (liquid crystal display) controller/driver, timers, two serial communications interfaces, an A/D converter, and I/O ports. These products are particularly suited for use as the embedded microprocessor in applications that require LCD and tone generation.

Additionally, the H8/3877 Series includes a ZTAT™ (zero turn around time) version of the H8/3877 that allows users to freely write programs to the on-chip PROM.

Features

- **40, 48, and 60 kbytes of on-chip ROM**
- **2 kbytes of on-chip RAM**
- **DTMF generator**
  — Tone dialing oscillator clock: 1.2 MHz to 10 MHz in 400 kHz increments
- **Multi-tone generator**

— Arbitrary frequency and arbitrary waveform output (40 Hz to 4 kHz when a 10 MHz clock oscillator is used)

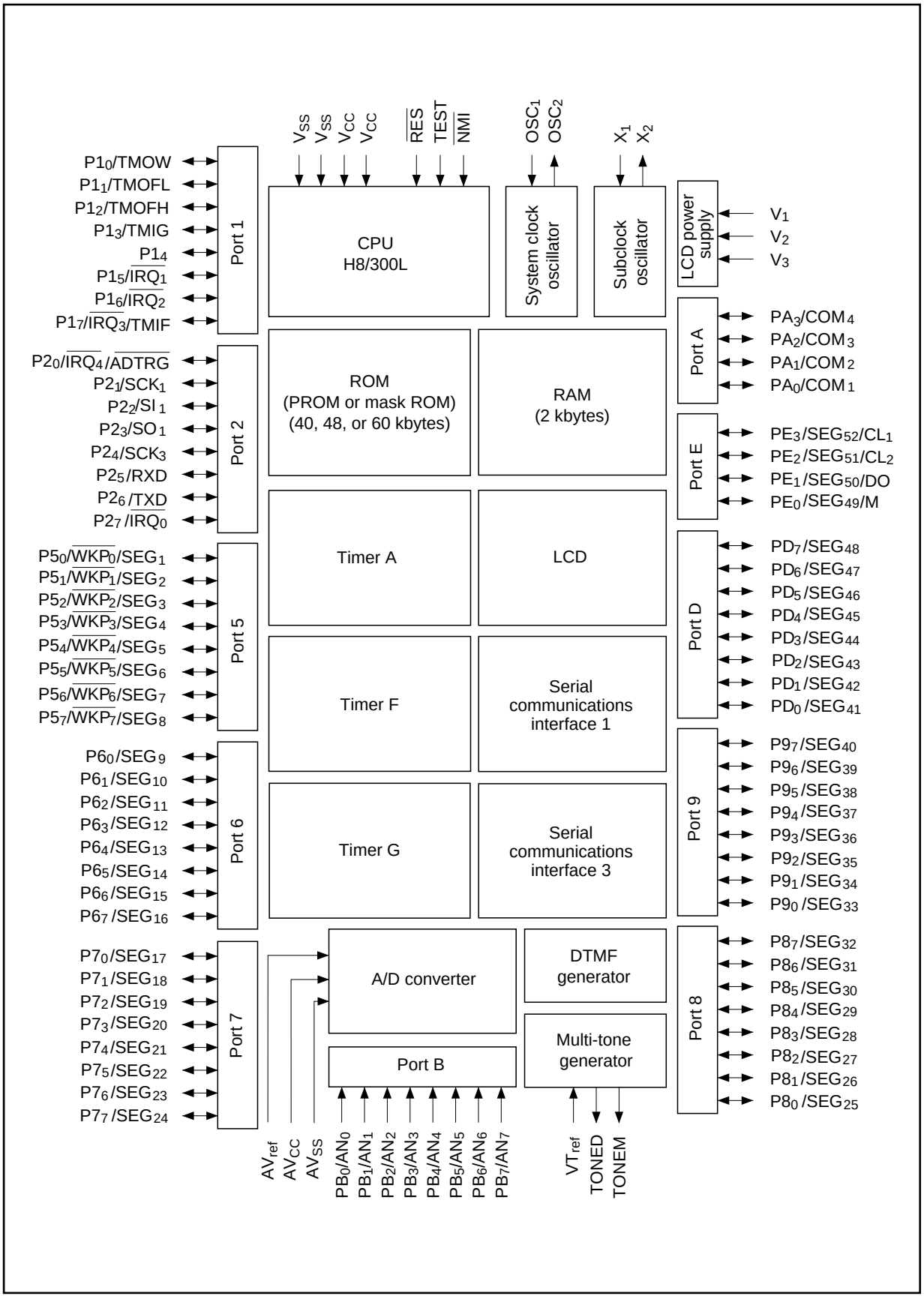
- **LCD controller/driver**
  — Fifty two segment pins and four common pins built in
  — Four duty ratios: Static, 1/2, 1/3 and 1/4
  — External segment expansion (however, only with static and 1/2 duty)
  — Segment pins: Can be switched to be used as general purpose port pins in 4-pin units.
- **Three 8- and 16-bit multi-function timer channels**
  — Timer A: 8-bit interval timer or clock timer
  — Timer F: 16-bit output compare timer or event counter
  — Timer G: 8-bit interval timer or input capture timer

- **Serial communications interface (two channels)**
  - — SCI1: 8- or 16-bit clock synchronous transfers
  - — SCI3: 8-bit clock synchronous/asynchronous transfers (includes a multi-processor communications function)
- **A/D converter**
  - — Resolution: 8 bits
  - — Eight analog voltage input channels
  - — Resistor ladder based successive approximations (AV_{ref} pin is provided)
  - — Sample-and-hold function
- **I/O ports**
  - — I/O pins: 72 pins
  - — Input pins: 8 pins
- **Interrupts**
  - — External interrupts: 14 interrupts ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_4}$, and $\overline{WKP_0}$ to $\overline{WKP_7}$)
  - — Internal interrupts: 17 interrupts
- **Low power modes**
  - — Sleep mode
  - — Standby mode
  - — Watch mode
  - — Subsleep mode
  - — Subactive mode
  - — Active (medium speed) mode
- **Two independent on-chip clock oscillator systems**
  - — System clock oscillator (oscillator frequency: 1 to 10 MHz)
  - — Subclock oscillator (oscillator frequency: 32.768 kHz)

Ordering Information

Product No.	Package	ROM
HD6433875H	FP-100B	Mask ROM
HD6433876H	FP-100B	
HD6433877H	FP-100B	
HD6473877H	FP-100B	PROM

Block Diagram



H8/3924, H8/3925, H8/3926, H8/3927

The H8/3927 Series microcomputers are 8-bit single chip microcomputers that provide an on-chip D/A converter.

The H8/3924, H8/3925, H8/3926, and H8/3927 microcomputers integrate, around an H8/300L CPU core, a rich set of peripheral functions, including 32, 40, 48, and 60 kbytes of ROM, 1 kbyte of RAM, a D/A converter, timers, a 14-bit PWM, two serial communications interfaces, an A/D converter, and I/O ports. These products are particularly suited for use as the embedded microprocessor in applications that require the control of analog signals.

Additionally, the H8/3927 Series includes a ZTAT™ (zero turn around time) version of the H8/3927 that allows users to freely write programs to the on-chip PROM.

Features

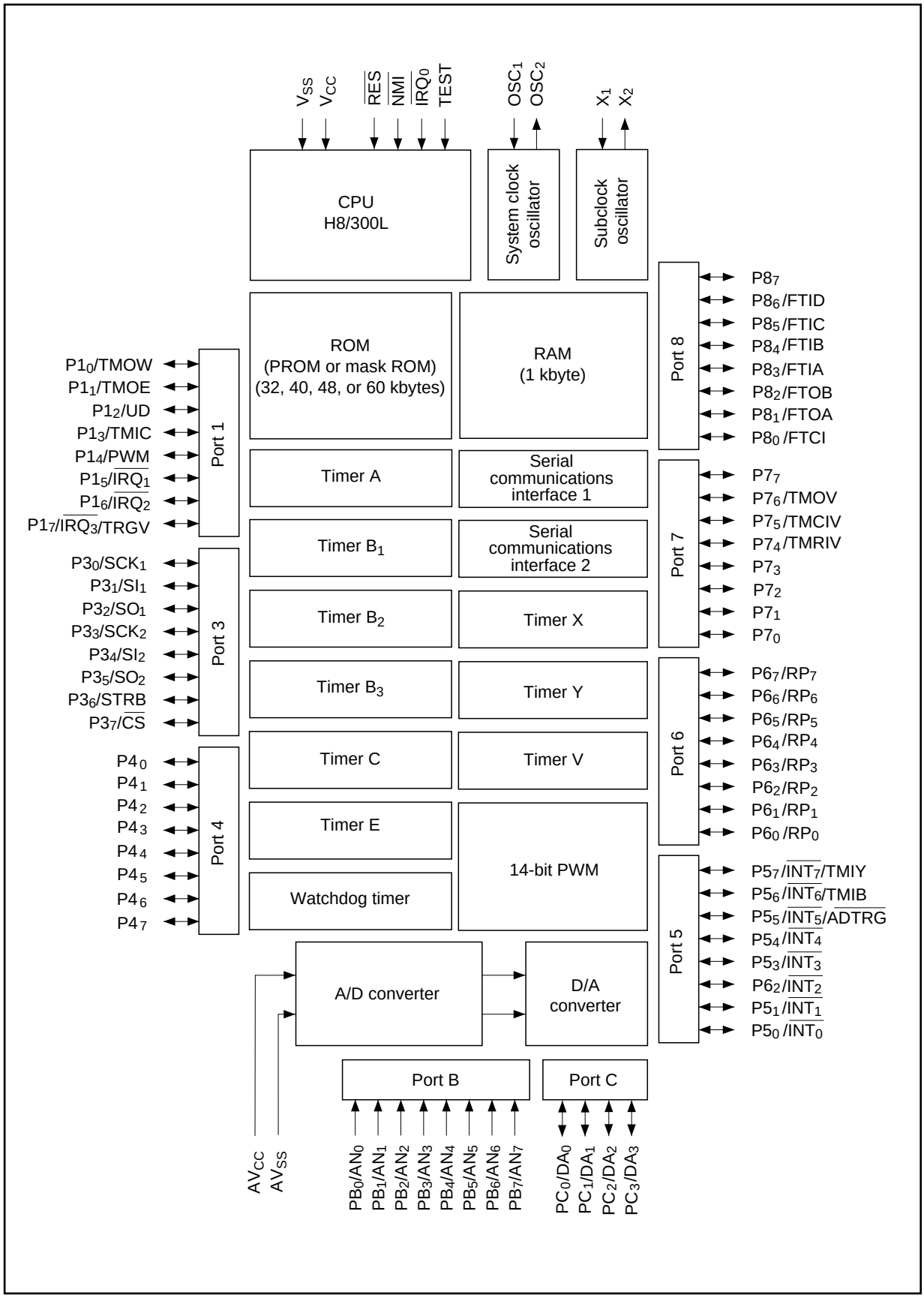
- **32, 40, 48, and 60 kbytes of on-chip ROM**
- **1 kbyte of on-chip RAM**
- **D/A converter**
  - — Resolution: 8 bits
  - — Four analog voltage output channels
  - — 8-bit D/A conversion based on a R-2R technique
- **Ten 8- and 16-bit multi-function timer channels**
  - — Timer A: 8-bit interval timer or clock timer
  - — Timer B_1: 8-bit reload timer or event counter
  - — Timer B_2: 8-bit reload timer
  - — Timer B_3: 8-bit reload timer
  - — Timer C: 8-bit reload timer or event counter
  - — Timer E: 8-bit reload timer
  - — Timer V: 8-bit timer or event counter
  - — Timer X: 16-bit timer or event counter
  - — Timer Y: 16-bit reload timer or event counter
  - — Watchdog timer: Generates a reset signal on the overflow of an 8-bit counter.

- **Serial communications interface (two channels)**
  - — SCI1: 8- or 16-bit clock synchronous transfers
  - — SCI2: 8-bit clock synchronous transfers (includes a 32-byte data buffer)
- **A/D converter**
  - — Resolution: 8 bits
  - — Eight analog voltage input channels
  - — Resistor ladder based successive approximations
  - — Sample-and-hold function
- **I/O ports**
  - — I/O pins: 56 pins (of which 8 are real time output ports)
  - — Input pins: 12 pins
- **Interrupts**
  - — External interrupts: 13 interrupts ($\overline{\text{NMI}}$, $\overline{\text{IRQ}_0}$ to $\overline{\text{IRQ}_3}$, and $\overline{\text{INT}_0}$ to $\overline{\text{INT}_7}$)
  - — Internal interrupts: 23 interrupts
- **Low power modes**
  - — Sleep mode (high speed)
  - — Sleep mode (medium speed)
  - — Standby mode
  - — Watch mode
  - — Subsleep mode
  - — Subactive mode
  - — Active (medium speed) mode
- **Two independent on-chip clock oscillator systems**
  - — System clock oscillator (oscillator frequency: 1 to 10 MHz)
  - — Subclock oscillator (oscillator frequency: 32.768 kHz)

Ordering Information

Product No.	Package	ROM
HD6433924F	FP-80B	Mask ROM
HD6433925F	FP-80B	Mask ROM
HD6433926F	FP-80B	Mask ROM
HD6433927F	FP-80B	Mask ROM
HD6473927F	FP-80B	PROM

Block Diagram



1. Timers

The H8/300L Series microcomputers provide on-chip timers that are optimal for application embedded microcontrollers. A wide variety of functions are supported by the H8/300L Series timers, including reload, event counting, compare match, and capture functions.

Timer Functions

	Clock	16-Bit Reload	8-Bit Reload	16-Bit Event	8-Bit Event	8-Bit Up/Down	16-Bit Compare	8-Bit Compare	16-Bit Capture	8-Bit Capture	Watchdog
Timer A	●										
Timer B			●		●						
Timer C			●		●	●					
Timer D					●						
Timer E			●								
Timer F					●		●	●			
Timer G										●	
Timer V								●			
Timer X							●		●		
Timer Y		●		●							
Watchdog											●

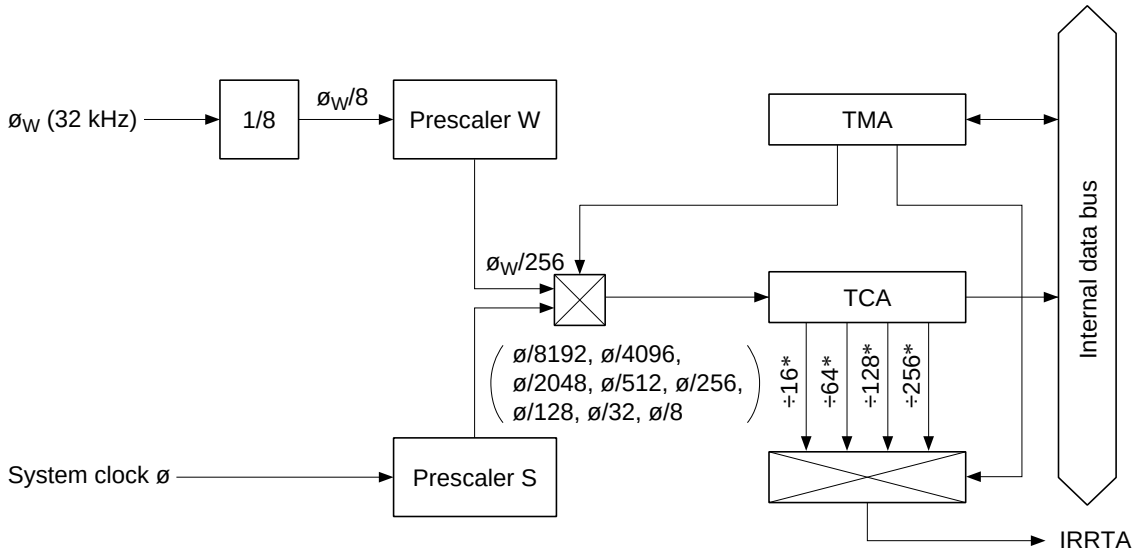
Timer A

This version of timer A is included in the H8/3614 Series, the H8/3714 Series, the H8/3724 Series, and the H8/3754 Series microcomputers.

Function: Timer A is an 8-bit interval timer that can also be used as a clock time base.

Features:
- The timer A clock can be selected from eight internal clock frequencies (ø/8192, ø/4096, ø/2048, ø/512, ø/256, ø/128, ø/32, and ø/8).
- Four overflow periods (2, 1, 0.5, and 0.125 seconds when used at 32.768 kHz) available when used as a clock time base.
- Generates a counter overflow interrupt.

Block Diagram



<Notation>
TMA: Timer mode register A
TCA: Timer counter A
IRRTA: Timer A overflow interrupt request flag

Notes: 1. * These can only be selected when the prescaler W output ($ø_W$/256) is used as the TCA input clock.
2. This figure shows the Timer A circuit used in the H8/3724.

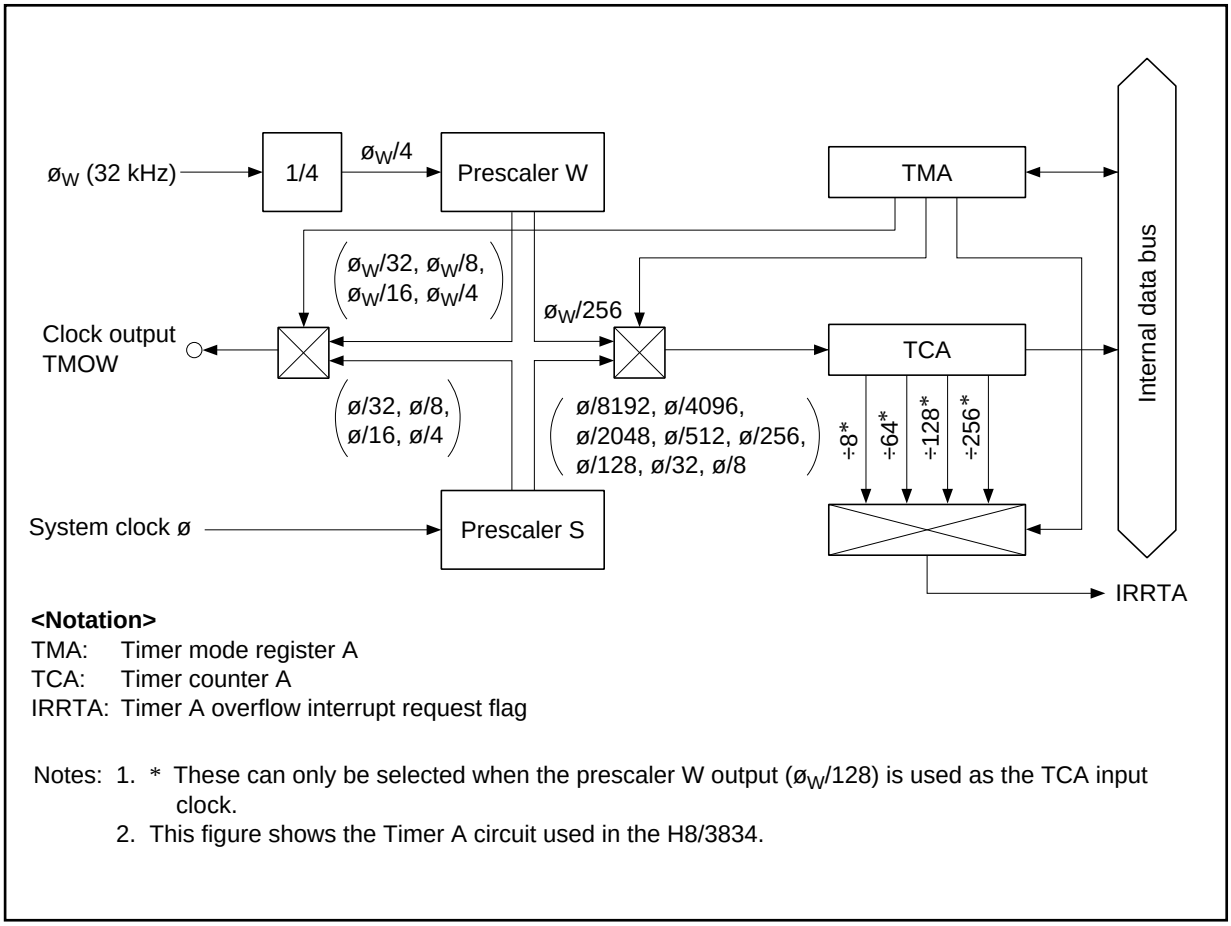
Timer A

This version of timer is included in the H8/3814 Series, the H8/3834 Series, the H8/3877 Series, and the H8/3927 Series microcomputers.

Function: Timer A is an 8-bit interval timer that can also be used as a clock time base.

Features:
- The timer A clock can be selected from eight internal clock frequencies (ø/8192, ø/4096, ø/2048, ø/512, ø/256, ø/128, ø/32, and ø/8).
- Four overflow periods (2, 1, 0.5, and 0.125 seconds when used at 32.768 kHz) available when used as a clock time base.
- Generates a counter overflow interrupt.
- A clock with one of eight periods (ø/32, ø/16, ø/8, ø/4, $ø_W$/32, $ø_W$/16, $ø_W$/8, and $ø_W$/4) can be output from the TMOW pin.

Block Diagram



<Notation>
TMA: Timer mode register A
TCA: Timer counter A
IRRTA: Timer A overflow interrupt request flag

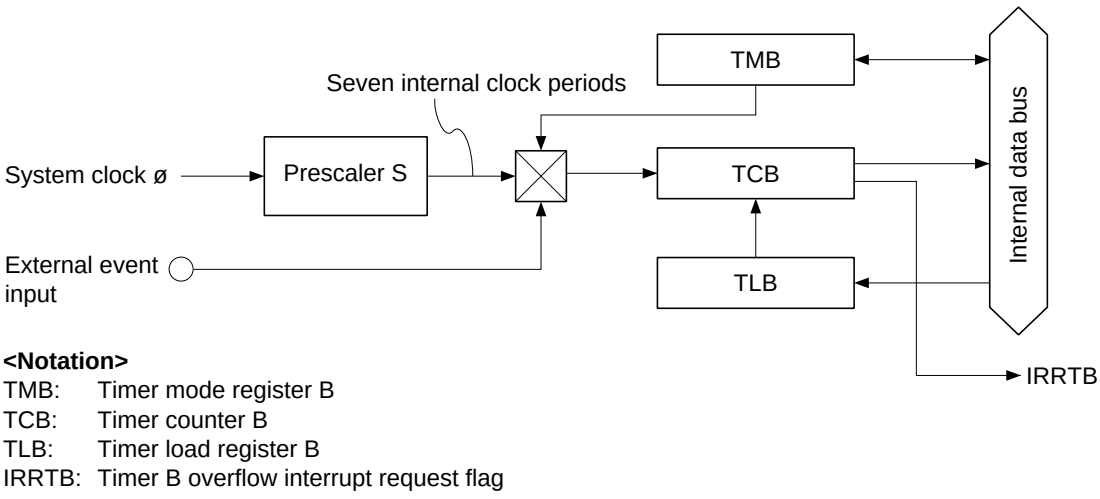
Notes: 1. * These can only be selected when the prescaler W output ($ø_W$/128) is used as the TCA input clock.
2. This figure shows the Timer A circuit used in the H8/3834.

Timer B

Function: Timer B is an 8-bit up/down counter that supports two operating modes, namely free-running mode and auto-reload mode.

Features:
- The timer B clock can be selected from seven internal clock frequencies or an external clock. (It can also be taken from external event input.)
- Generates a counter overflow interrupt.

Block Diagram



<Notation>
TMB: Timer mode register B
TCB: Timer counter B
TLB: Timer load register B
IRRTB: Timer B overflow interrupt request flag

Timer B Internal Clock Periods

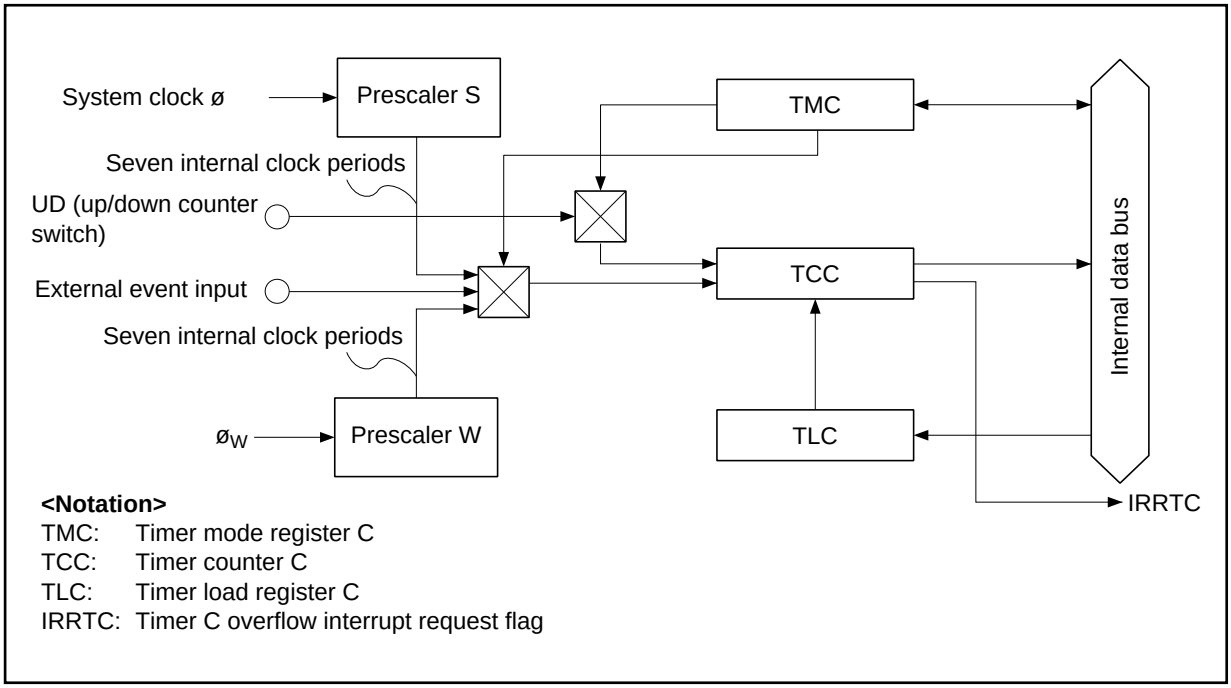
Product Series		ø/8192	ø/4096	ø/2048	ø/1024	ø/512	ø/256	ø/128	ø/64	ø/32	ø/16	ø/8	ø/4	ø/2	External Event Input
H8/3614 Series H8/3714 Series H8/3724 Series H8/3754 Series	B	●		●		●	●	●		●		●			Supported
H8/3814 Series H8/3834 Series H8/3877 Series	B	●		●		●	●		●		●		●		Supported
H8/3927 Series	B_1	●		●		●	●		●		●		●		Supported
	B_2			●		●	●		●		●	●	●		Not supported
	B_3			●		●	●		●		●	●	●		Not supported

Timer C

Function: Timer C is an 8-bit up/down counter that supports two operating modes, namely free-running mode and auto-reload mode.

Features:
- Can be switched between functioning as an up counter and as a down counter.
- The timer C clock can be selected from one of seven internal clocks or an external clock. (It can also function as an external event counter.)
- Generates a counter overflow interrupt.

Block Diagram



Timer C Internal Clock Periods

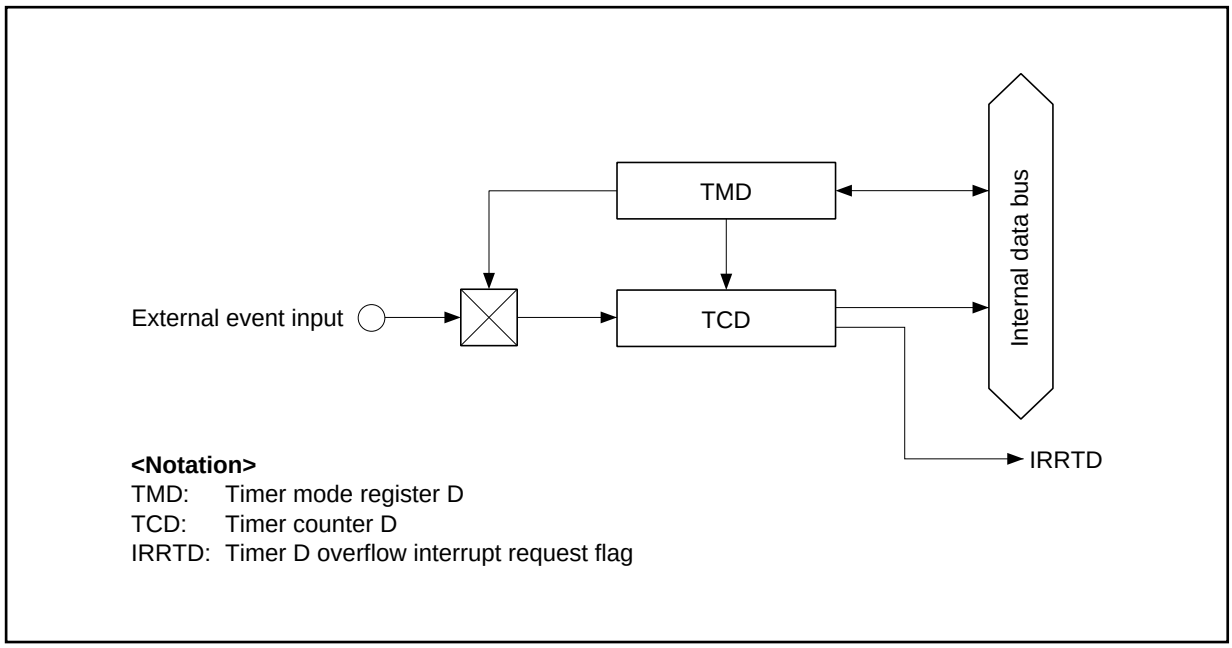
Product Series		ø/8192	ø/4096	ø/2048	ø/1024	ø/512	ø/256	ø/128	ø/64	ø/32	ø/16	ø/8	ø/4	ø/2	øw/4	External Event Input
H8/3614 Series H8/3714 Series H8/3724 Series H8/3754 Series	C	●		●		●	●	●		●		●				Supported
H8/3814 Series H8/3834 Series H8/3877 Series H8/3927 Series	C	●		●		●			●		●		●		●	Supported

Timer D

Function: Timer D is an 8-bit event counter that is incremented by an external event signal.

Features:
- Can be set to count either rising or falling edges of the external signal.
- Generates a counter overflow interrupt.

Block Diagram

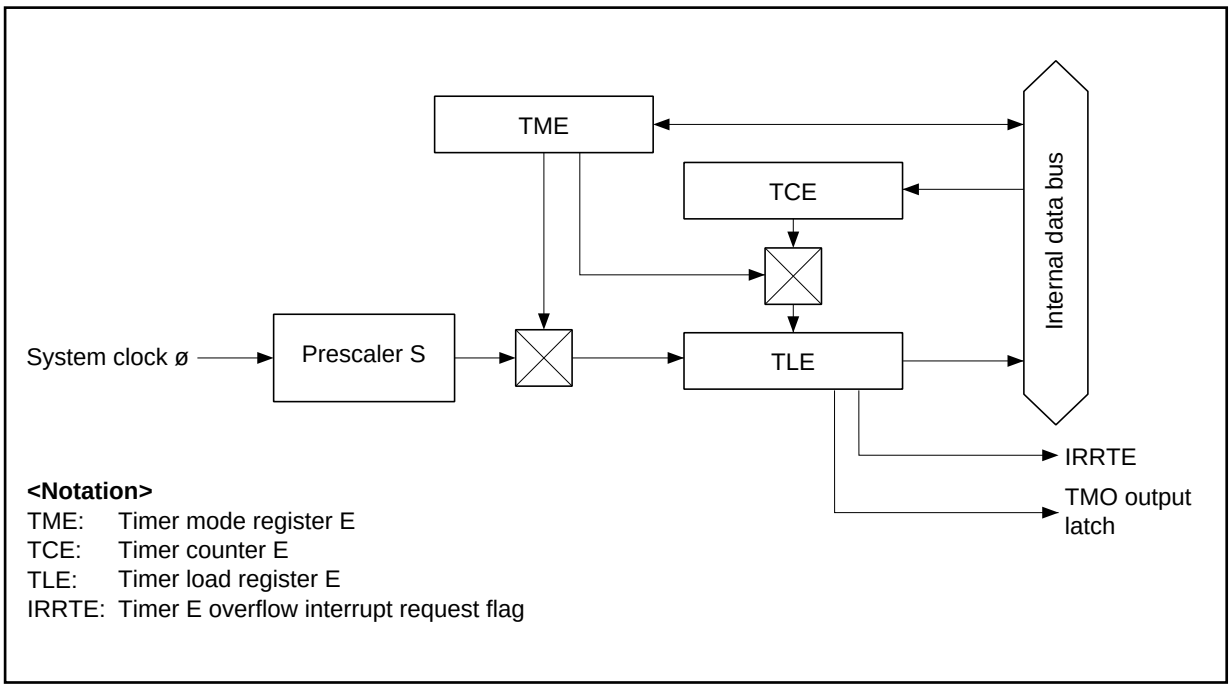


Timer E

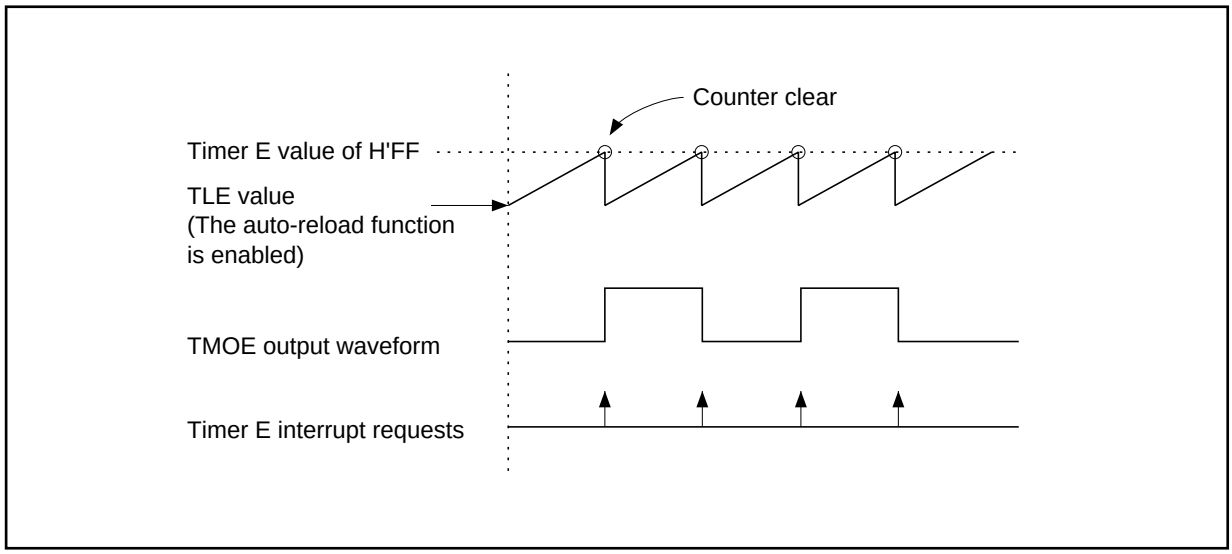
Function: Timer E is an 8-bit timer that is incremented by an input clock and has two operating modes, namely free running mode and auto-reload mode.

Features:
- The timer E clock can be selected from eight internal clock frequencies (ø/8192, ø/4096, ø/2048, ø/512, ø/256, ø/128, ø/32, and ø/8).
- Generates a counter overflow interrupt.
- Supports output of a fixed frequency 50% duty signal using the prescaler divisor.
  When ø is 5 MHz: 2.45 kHz or 4.9 kHz
  When ø is 2 MHz: 0.98 kHz or 1.95 kHz
- Supports output of a 50% duty arbitrary frequency square wave signal using either the overflow signal or the prescaler S signal.

Block Diagram



Timer E Overflow Based Output Waveform

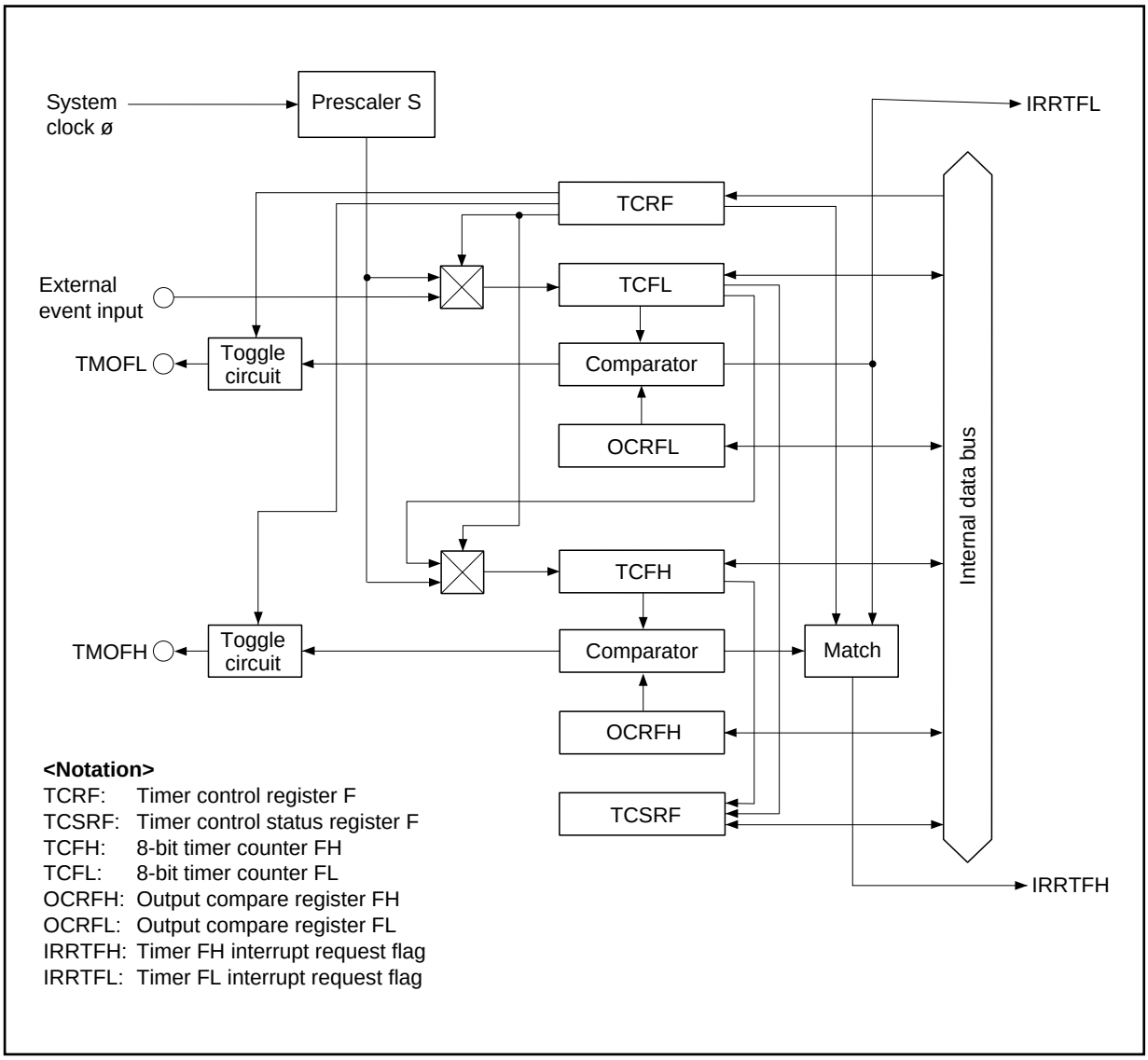


Timer F

Function: Timer F is a 16-bit timer that, in addition to supporting external event counting, also supports functions such as counter reset in response to a compare match signal, interrupt requests, and toggle output. It can also function as two independent 8-bit timers.

Features:
- The timer F clock can be selected from four internal clock frequencies (ø/32, ø/16, ø/4, and ø/2) and an external clock.
- The counter can be reset from a single compare match signal.
- Interrupts: One compare match interrupt and one overflow interrupt.
- Can be used as two independent 8-bit timers, timer FL and timer FH.

Block Diagram

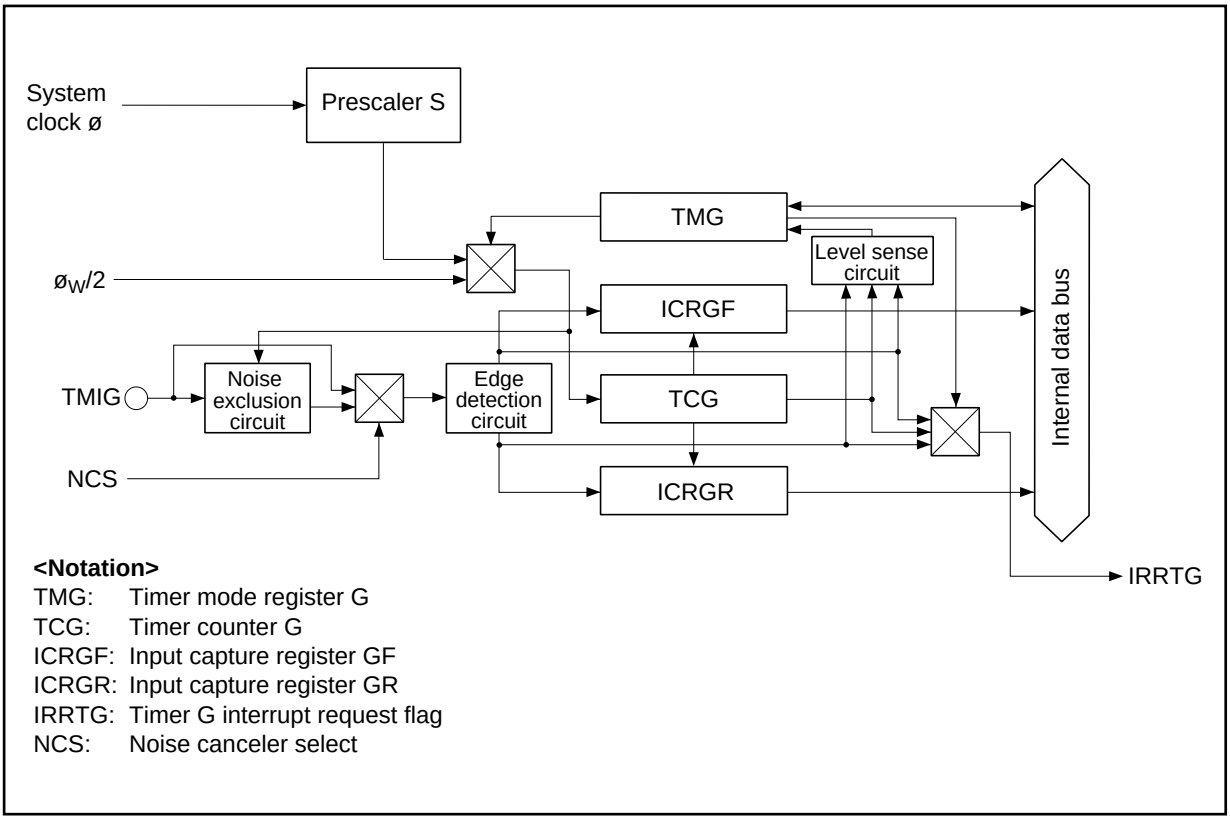


Timer G

Function: Timer G is an 8-bit timer that has dedicated input capture functions for both the rising and falling edges of pulses input to the input capture pin.

Features:
- The timer G clock can be selected from four internal clock frequencies; ø/64, ø/32, ø/2048, ø/2, and $ø_W$/2.
- Provides dedicated input capture functions for both rising and falling edges.
- Two types of counter overflow are detected.
- A counter clear operation can be specified.
- Interrupts: One input capture interrupt and one overflow interrupt.
- Built-in noise exclusion circuit (5 ø, or less)

Block Diagram



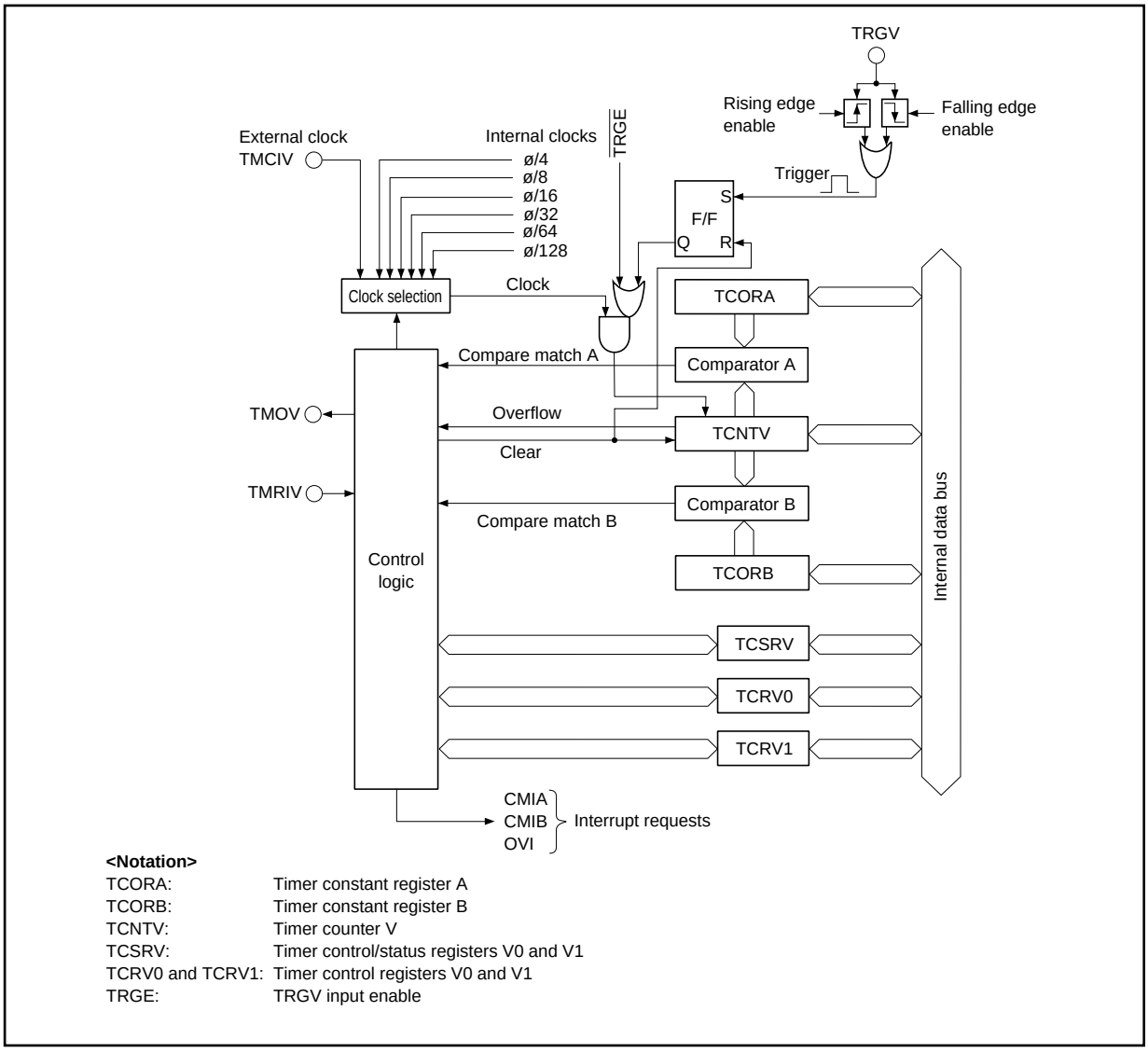
<Notation>
TMG: Timer mode register G
TCG: Timer counter G
ICRGF: Input capture register GF
ICRGR: Input capture register GR
IRRTG: Timer G interrupt request flag
NCS: Noise canceler select

Timer V

Function: Timer V is an 8-bit timer that has, in addition to a timer counter, a timer constant register, and can output an arbitrary duty pulse based on a compare match signal generated when these registers match.

Features:
- The timer V clock can be selected from six internal clock frequencies (ø/128, ø/64, ø/32, ø/16, ø/8, and ø/4) and an external clock. (It can also be taken from external event input.)
- A counter clear operation can be specified.
- Interrupts: two compare match interrupts and one overflow interrupt.
- Counter operation can be started according to an external trigger input.

Block Diagram



<Notation>

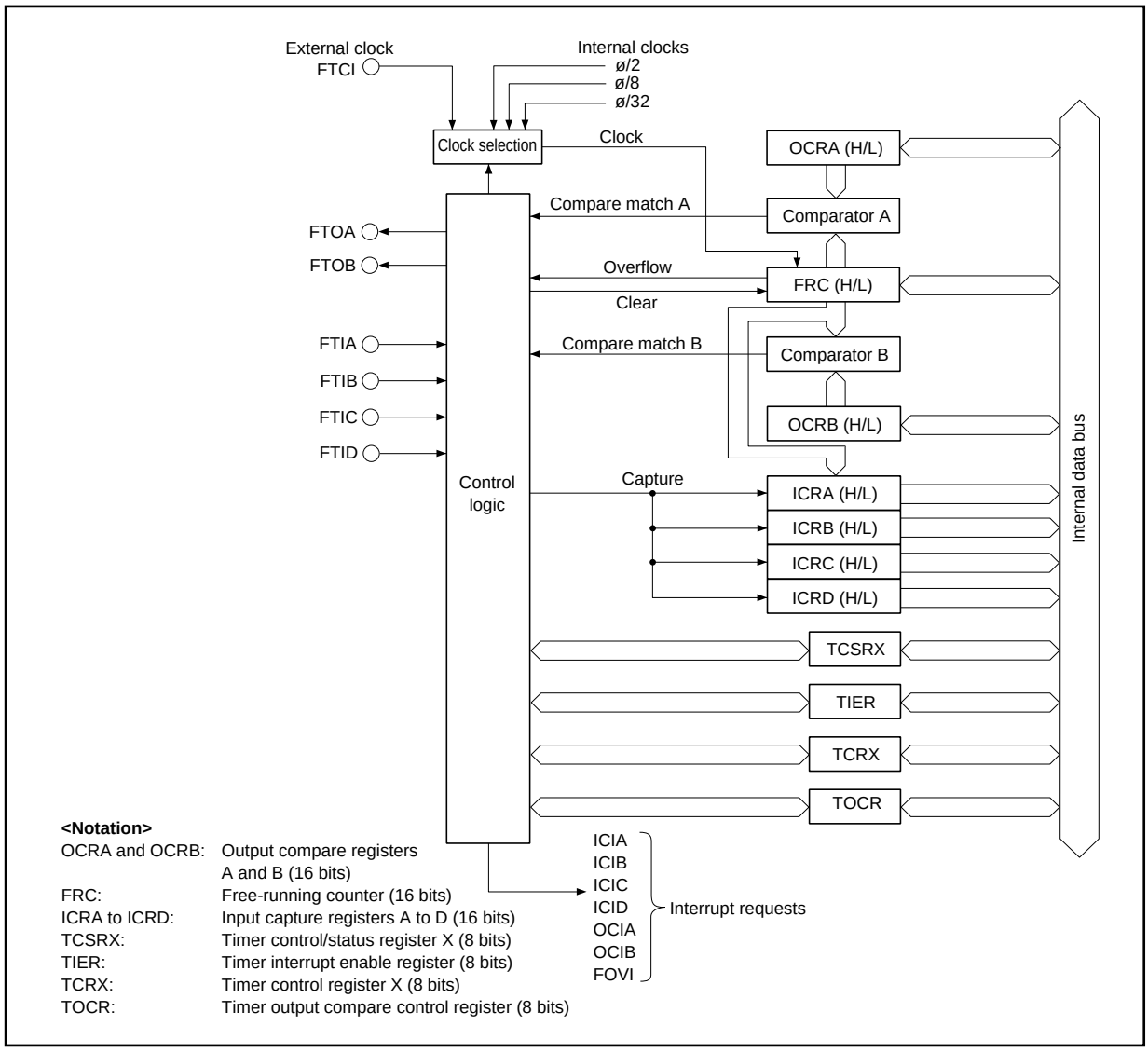
TCORA:	Timer constant register A
TCORB:	Timer constant register B
TCNTV:	Timer counter V
TCSRV:	Timer control/status registers V0 and V1
TCRV0 and TCRV1:	Timer control registers V0 and V1
TRGE:	TRGV input enable

Timer X

Function: Timer X is a 16-bit timer that can output two independent waveforms based on a free-running counter.

Features:
- The timer X clock can be selected from three internal clock frequencies (ø/32, ø/8, and ø/2) and an external clock.
- Timer X can output two waveforms.
- Four independent input capture functions
- A counter clear operation can be specified.
- Interrupts: two compare match interrupts, four input capture interrupts, and one overflow interrupt.

Block Diagram

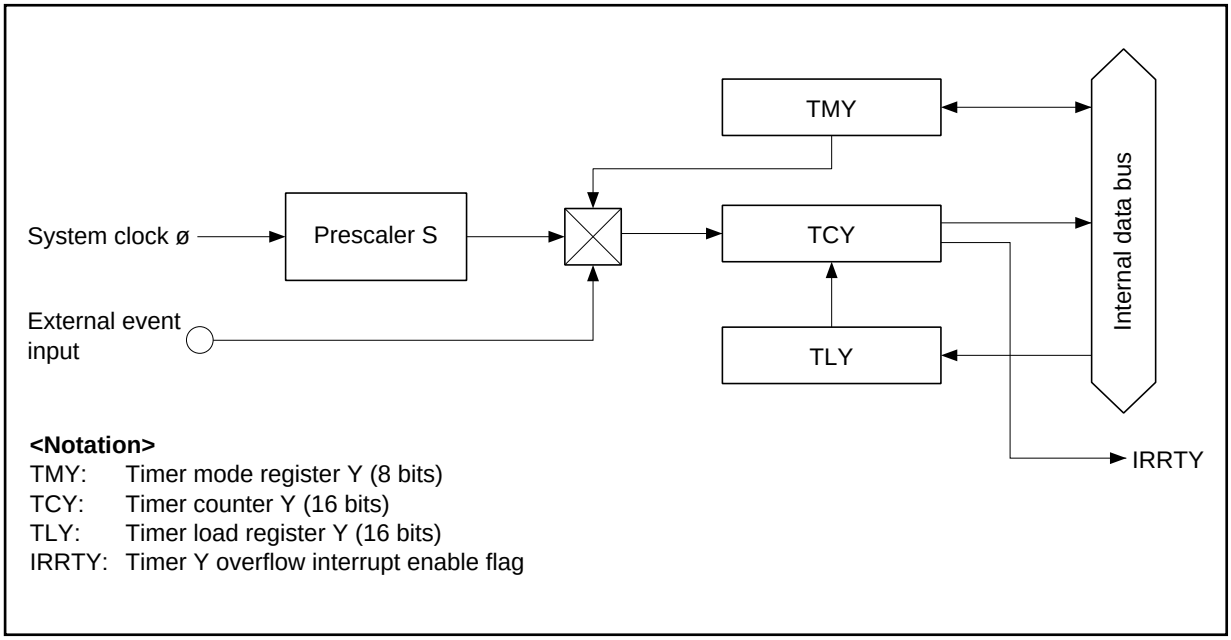


Timer Y

Function: Timer Y is a 16-bit timer that is incremented by the input clock and supports two operating modes, namely interval mode and auto-reload mode.

Features:
- The timer V clock can be selected from seven internal clock frequencies (ø/8192, ø/2048, ø/512, ø/256, ø/64, ø/16, and ø/4) and an external clock. (It can also be taken from external event input.)
- Generates an interrupt on counter overflow.

Block Diagram

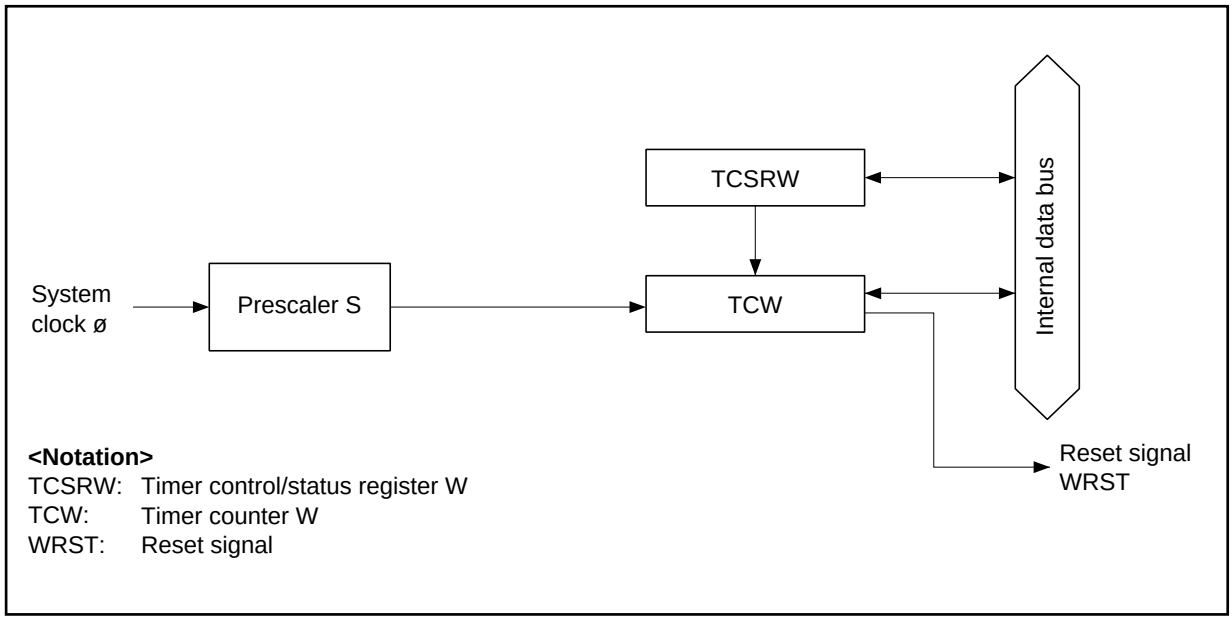


Watchdog Timer

Function: The watchdog timer is an 8-bit counter incremented by the input clock. It provides a monitoring function that resets the IC internally when, due to system runaway or other problem, the counter overflows before the counter value is rewritten.

Features:
- The watchdog timer counter is incremented by an internal clock with a frequency of ø/8192, and generates a reset signal (WRST) when the counter overflows.
- The overflow period can be set to a value between 1 and 256 times 8192/ø.

Block Diagram

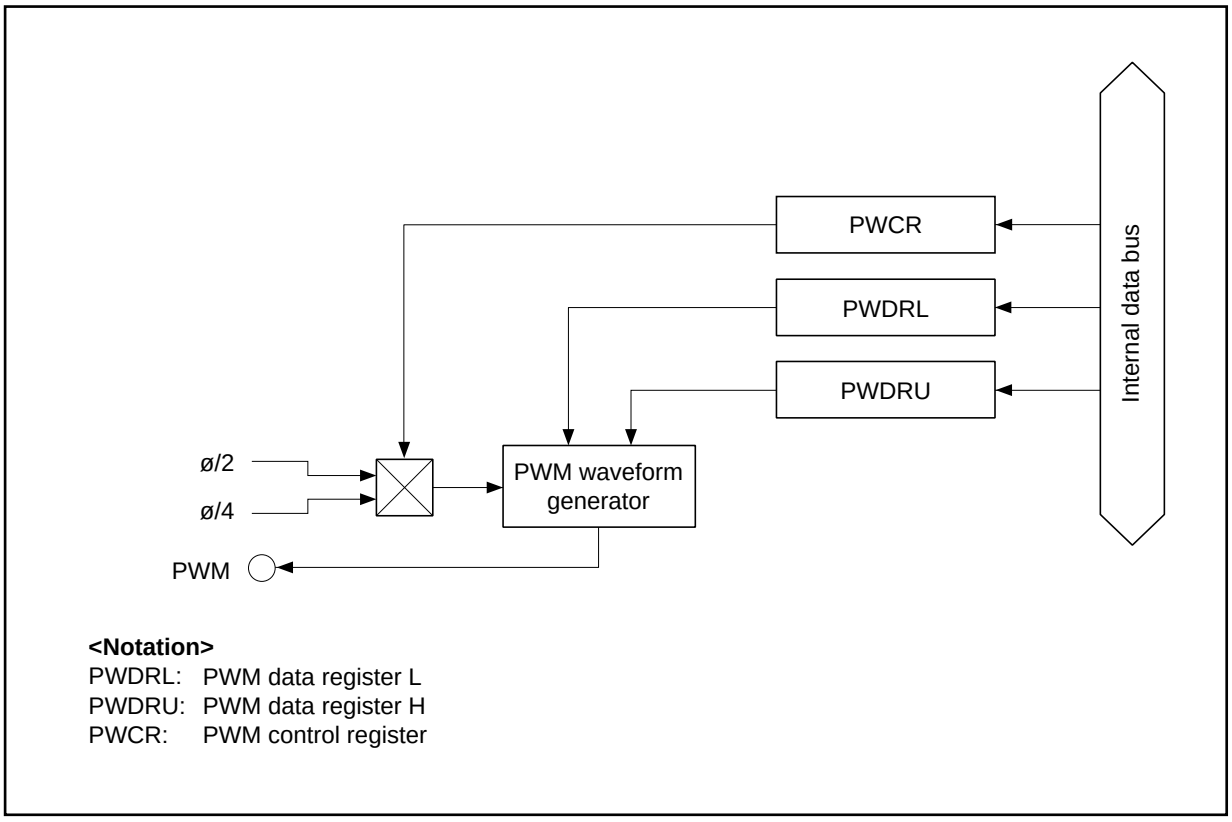


2. 14-Bit PWM

The H8/300L Series microcomputers provide a single channel pulse division type 14-bit PWM (pulse width modulation) on-chip. It can be used as a 14-bit D/A converter when combined with an external low pass filter.

Features:
- Either a conversion period of 32768/ø and a minimum conversion width of 2/ø, or a conversion period of 16384/ø and a minimum conversion width of 1/ø.
- A pulse division circuit is employed to reduce ripple.

Block Diagram



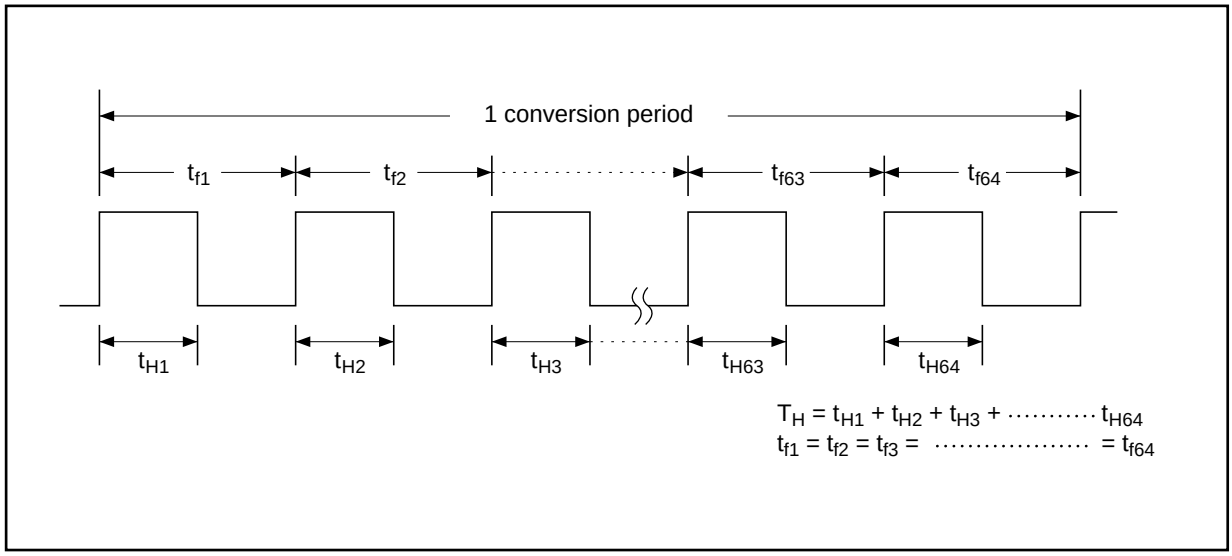
<Notation>
PWDRL: PWM data register L
PWDRU: PWM data register H
PWCR: PWM control register

14-Bit PWM Operation: The total time (T_H) of the 64 pulses generated in a single conversion cycle corresponds to the data loaded into the PWM data registers L and H as described by the formula below.

T_H = (data value + 64) × tø/2

Where: tø = 2/ø when PWCR0 is 0 and
tø = 4/ø when PWCR0 is 1

PWM Output Waveform



The output will be a high level output (100%) when the data value is between H'3FC0 and H'3FFF. The minimum conversion width pulse is output when the data value is H'0000.

3. Serial Communication Interface (SCI)

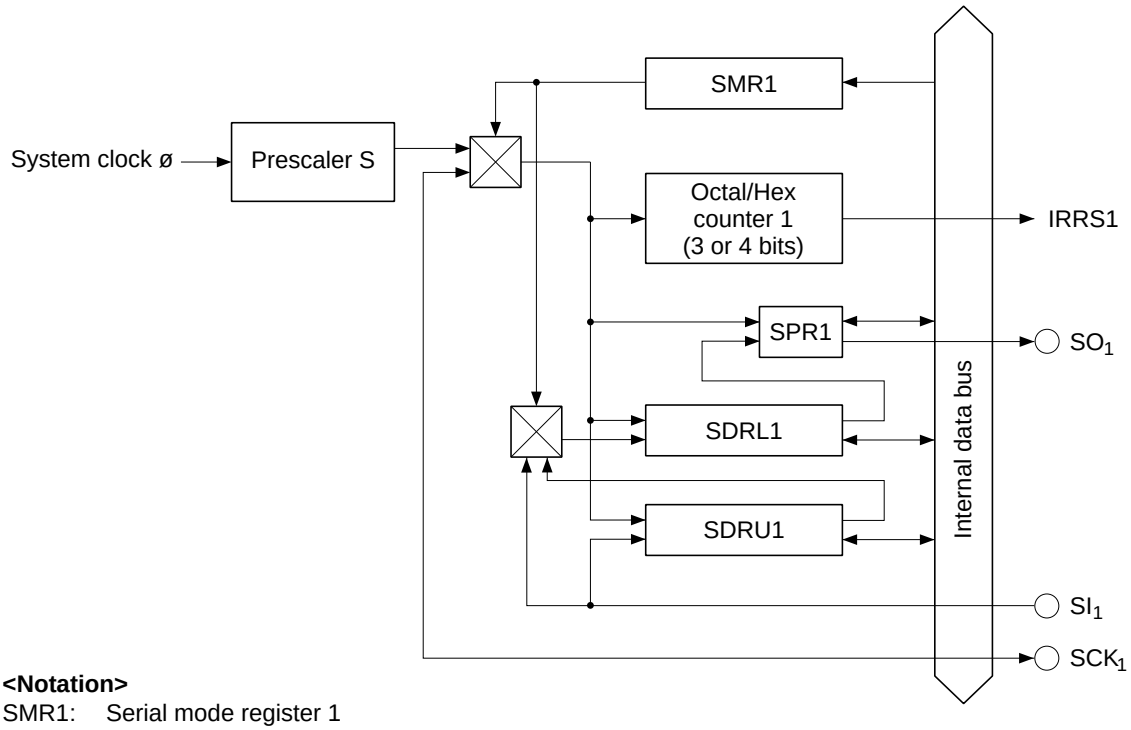
The H8/300L Series microcomputers provide serial communications interfaces that are optimal for application embedded microcontrollers. There are three serial communications interfaces provided by the H8/300L Series, namely 8/16-bit synchronous serial, 8-bit synchronous with 32-byte buffer, and 8-bit synchronous/asynchronous serial interfaces.

SCI1

Function: The SCI1 supports 8- and 16-bit clock synchronous serial data transfers.

Features:
- Data sizes of 8 and 16 bits can be selected.
- One of eight internal clocks (ø/1024, ø/256, ø/64, ø/32, ø/16, ø/8, ø/4, and ø/2) or an external clock can be used as the clock source.
- Interrupts are generated on transfer completion and errors.

Block Diagram



<Notation>
SMR1: Serial mode register 1
SPR1: Serial port register 1
SDRL1: Serial data register L1
SDRU1: Serial data register U1
IRRS1: Serial communications interface 1 interrupt request flag

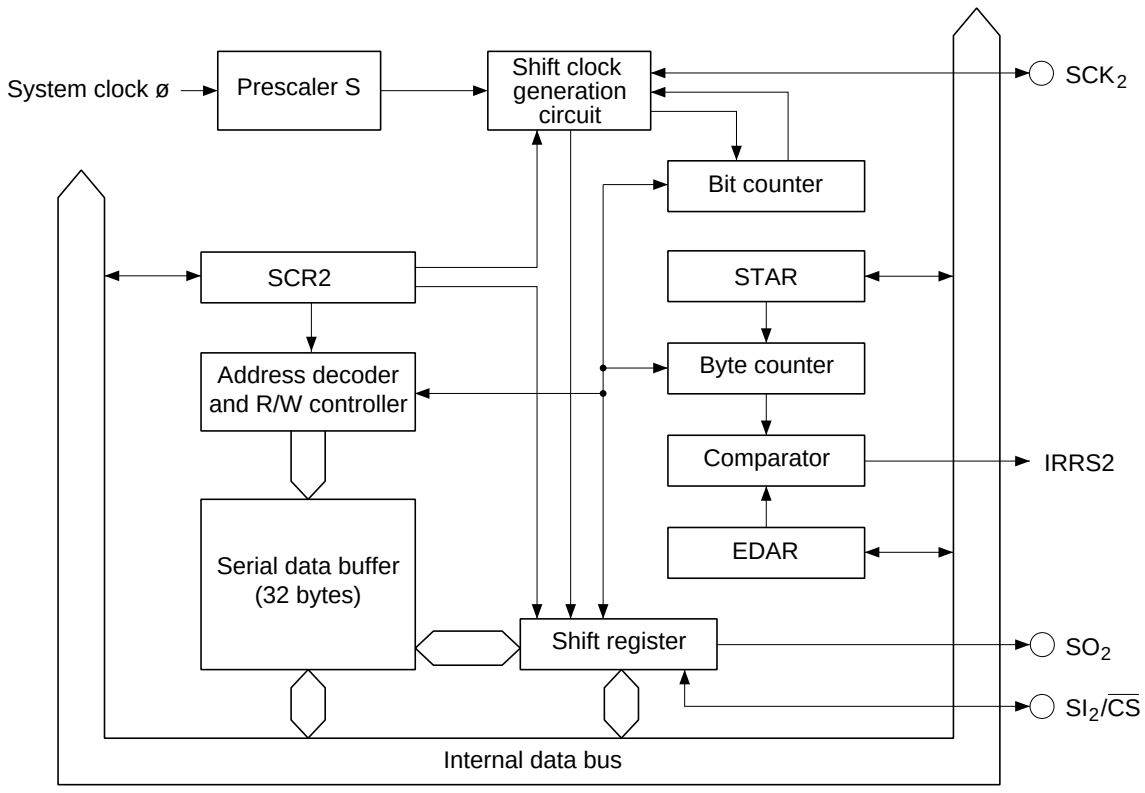
Note: This figure shows the SCI1 used in the H8/3724 series.

SCI2 (H8/3614 Series, H8/3714 Series, H8/3724 Series, and H8/3754 Series)

Function: The SCI2 has a 32-byte internal data buffer, and supports clock synchronous transfers in units of 1 to 32 bytes.

Features:
- Automatic transfers of up to 32 bytes
- Either an internal clock (ø/8, ø/4, or ø/2) or an external clock can be used as the clock source.
- Interrupts are generated on transfer completion and errors.

Block Diagram



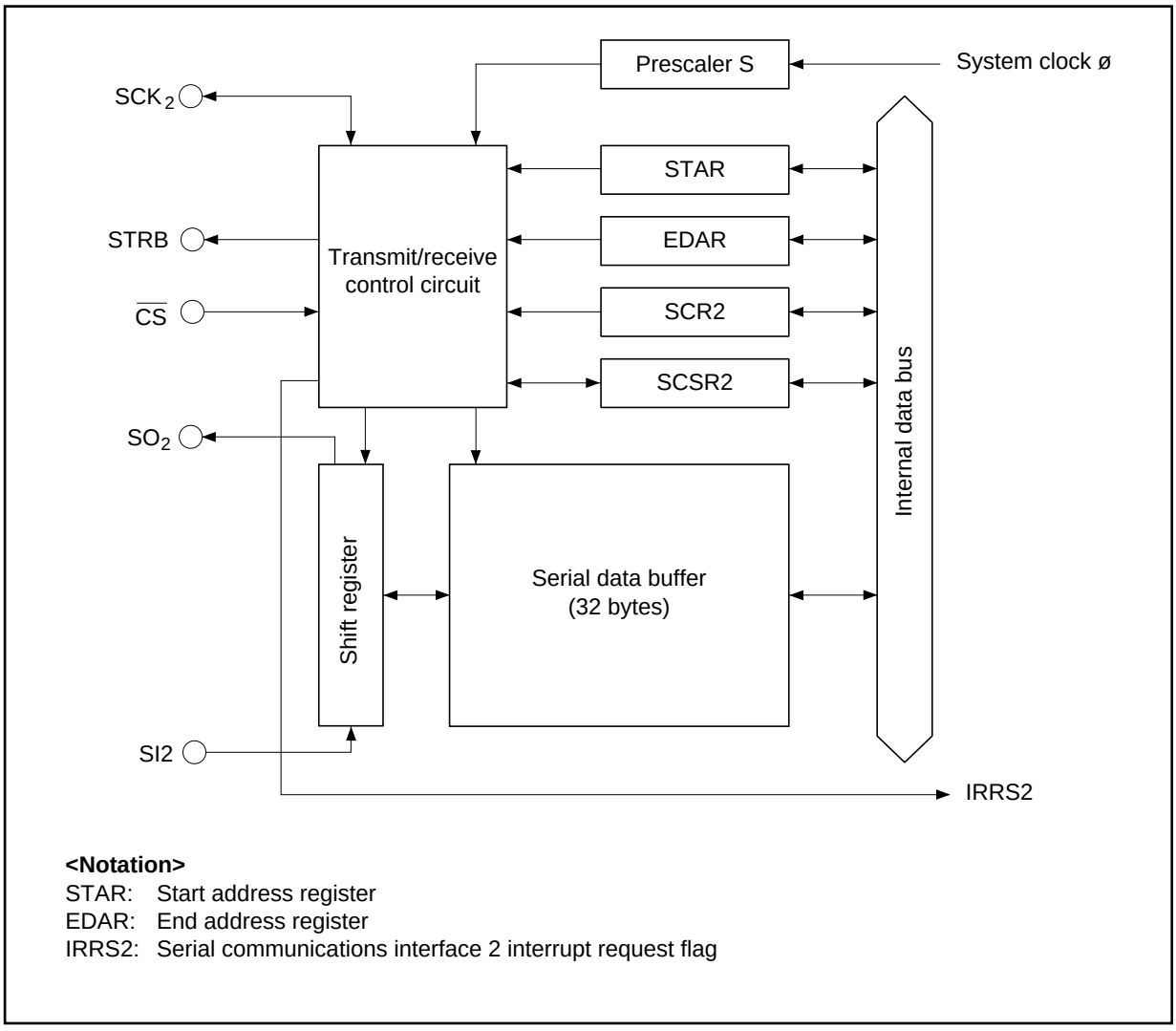
<Notation>
STAR: Start address register
EDAR: End address register
IRRS2: Serial communications interface 2 interrupt request flag

SCI2 (H8/3834 Series and H8/3927 Series)

Function: The SCI2 has a 32-byte internal data buffer, and supports 32-byte clock synchronous data transfers in a single operation.

Features:
- Data blocks of 32 bytes can be automatically transferred.
- One of seven internal clocks (ø/256, ø/64, ø/32, ø/16, ø/8, ø/4, and ø/2) or an external clock can be used as the clock source.
- Interrupts are generated on transfer completion and errors.
- A transfer data interval can be left between each byte. The transfer interval can be 56, 24, or 8 times the internal clock period.
- Transfer starts can be controlled from the chip select input.
- A strobe pulse can be output on each byte transfer.

Block Diagram



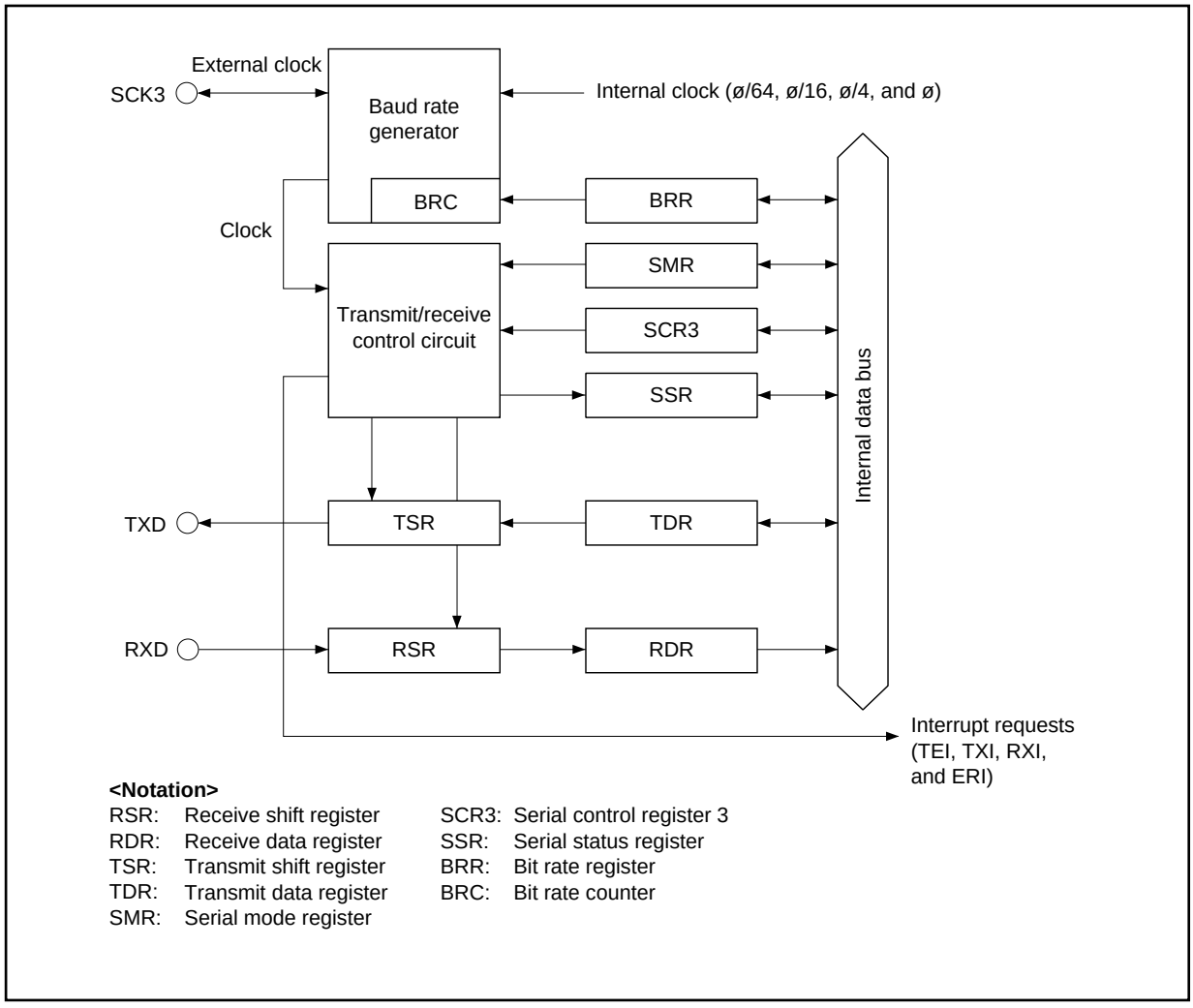
<Notation>
STAR: Start address register
EDAR: End address register
IRRS2: Serial communications interface 2 interrupt request flag

SCI3

Function: The SCI3 supports synchronous and asynchronous serial data transfers. It also has a multi-processor communications function that supports serial communications between multiple processors.

Features:
- Serial data transfers in either synchronous or asynchronous mode
- Full duplex communication
- Double buffered data registers support continuous bidirectional communication.
- Support for arbitrary bit rate selection using the built-in baud rate generator
- Either an internal or an external clock can be used as the transfer clock source.
- Generates six interrupts: transmission complete, transmission data empty, receive data full, overrun error, framing error, and parity error.

Block Diagram

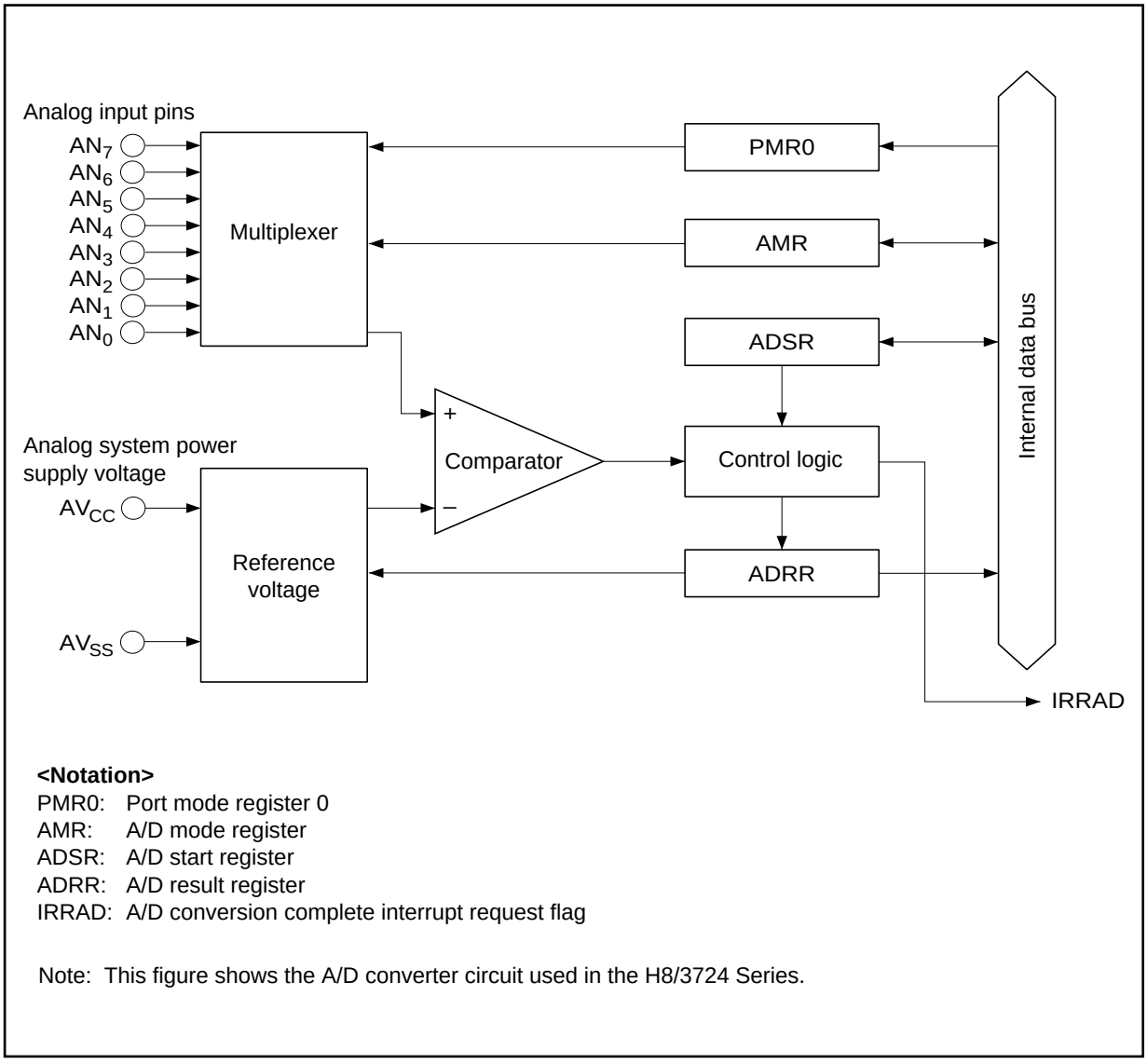


4. A/D Converter

The H8/300L Series A/D converter is an on-chip resistor ladder successive approximations A/D converter that allows the microcomputer to measure multiple analog input channel signals.

Features:
- Eight-bit resolution
- Multiple analog input channel pins
- Conversion time: A minimum of 31/ø per channel (12.4 µs for an fosc of 10 MHz)
- Generates an interrupt at the completion of A/D conversion.
- Built-in sample and hold circuit

Block Diagram..



<Notation>
PMR0: Port mode register 0
AMR: A/D mode register
ADSR: A/D start register
ADRR: A/D result register
IRRAD: A/D conversion complete interrupt request flag

Note: This figure shows the A/D converter circuit used in the H8/3724 Series.

Number of Channels and Conversion Times

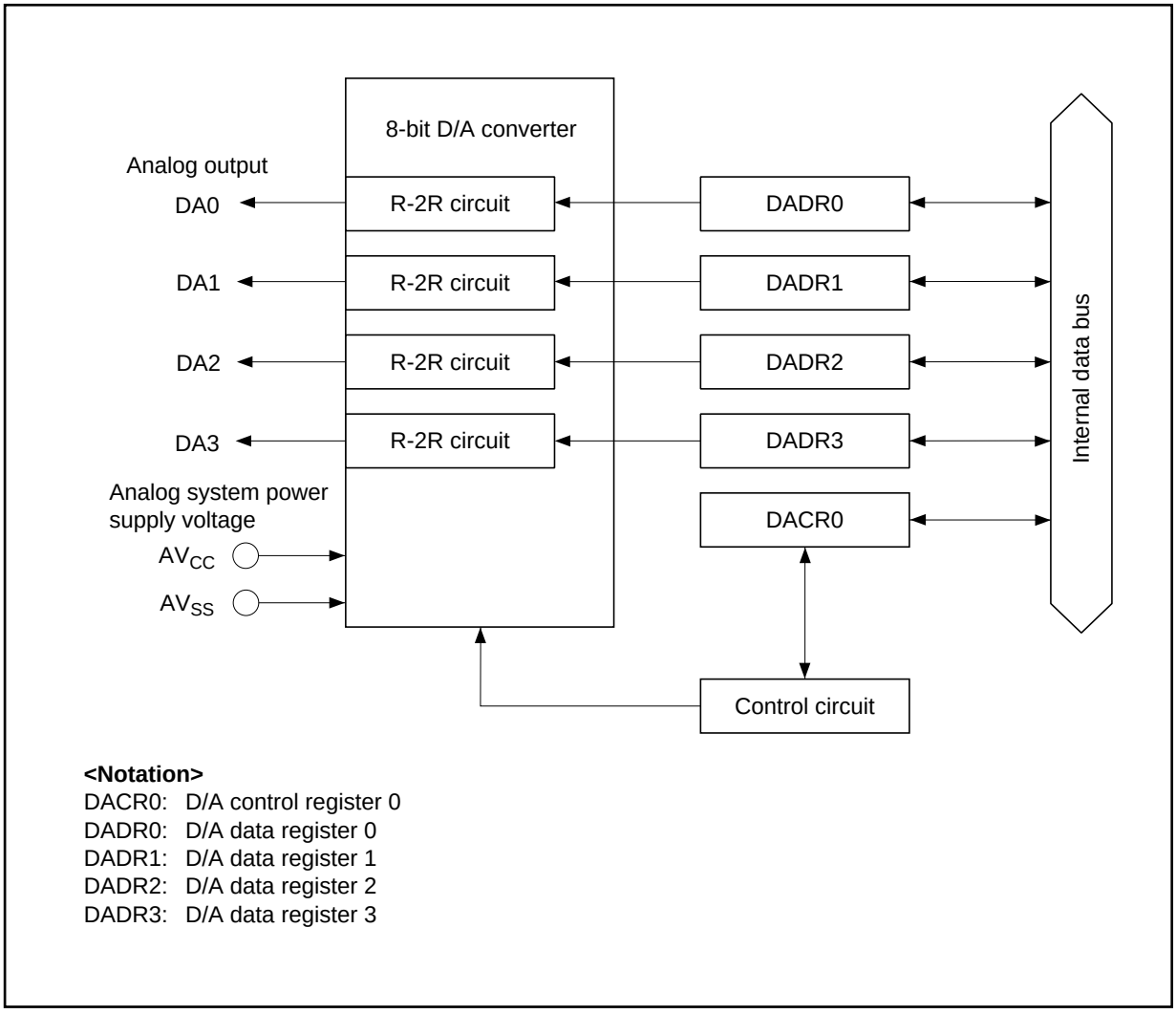
Product Series	Conversion Time		Number of Channels	External Trigger	V_{ref} Pin
H8/3614 Series H8/3714 Series H8/3724 Series H8/3754 Series	31/ø, 62/ø	14.8 µs minimum	8 channels	Not supported	Not provided
H8/3814 Series H8/3834 Series	31/ø, 62/ø	12.4 µs minimum	12 channels	Supported	Not provided
H8/3877 Series	31/ø, 62/ø, 124/ø	12.4 µs minimum	8 channels	Supported	Provided
H8/3927 Series	31/ø, 62/ø	12.4 µs minimum	8 channels	Supported	Not provided

5. D/A Converter

The H8/300L Series on-chip D/A converter uses an R-2R conversion circuit. It can provide up to four analog voltage output channels.

Features:
- Eight-bit resolution
- Four analog voltage output channels
- Conversion time: 3 µs minimum

Block Diagram



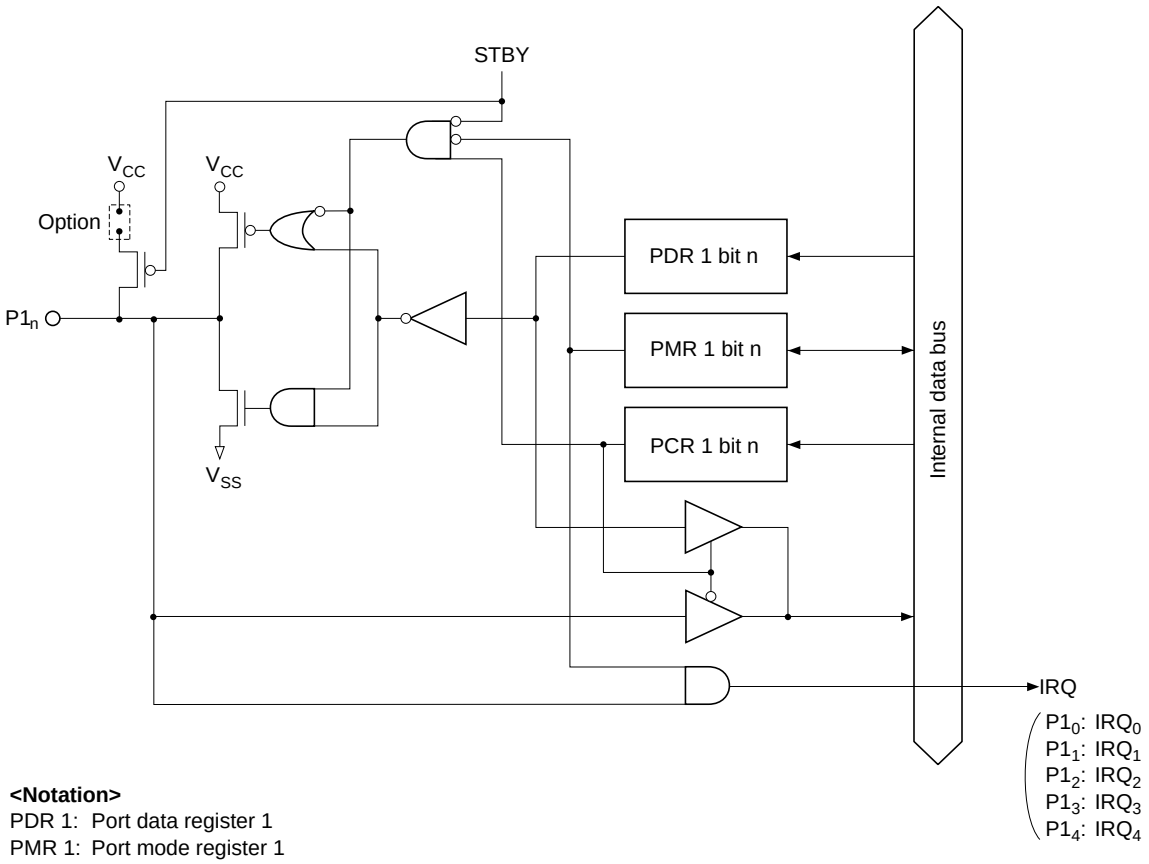
<Notation>
DACR0: D/A control register 0
DADR0: D/A data register 0
DADR1: D/A data register 1
DADR2: D/A data register 2
DADR3: D/A data register 3

6. I/O Ports

The H8/300L Series microcomputers provide I/O ports that are optimal for application embedded microcontrollers. In addition to general purpose bidirectional (input and output) ports, the H8/300L Series microcomputers also provide a set of specialized I/O ports that differ between products and that include real time ports that allow immediate output control in response to external events, high current ports that can drive LEDs, and high breakdown voltage (40 V) ports with built-in pull-down MOS transistors.

Port Functions

General Purpose I/O Ports: General purpose I/O ports include a port data register (PDR) that holds the data value to be output from the port and a port control register that determines the direction of the port. Additionally, ports that are allocated to share functions with peripheral module dedicated I/O signals also have a port mode register that switches the pin function.



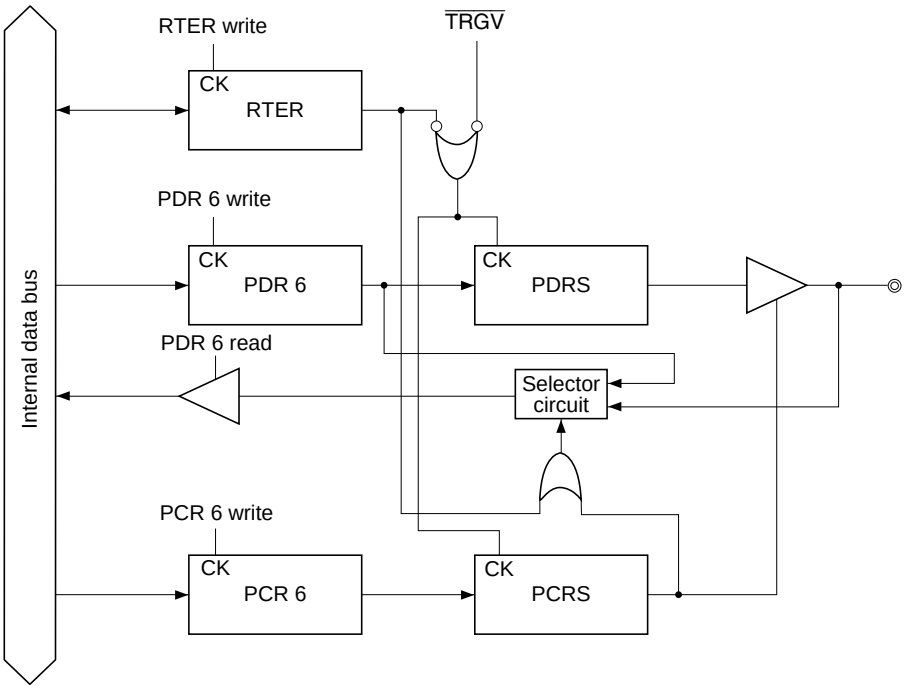
<Notation>
PDR 1: Port data register 1
PMR 1: Port mode register 1
PCR 1: Port control register 1
n = 0 to 4

Note: The figure shows the H8/3724 port 1.

General Purpose I/O Ports with Built-In Pull-Up MOS Transistors: The H8/300L Series general purpose I/O ports are provided with pull-up MOS transistors. In some products, the pull-up MOS transistors can be enabled as a mask option, and in other products, the pull-up MOS transistors can be controlled by application programs.

Mask Option Products	Program Control Products
H8/3614 Series	H8/3814 Series
H8/3714 Series	H8/3834 Series
H8/3724 Series	H8/3877 Series
H8/3754 Series	H8/3927 Series

Real Time Output Ports: The H8/300L Series microcomputers provide I/O ports with a real time output function. This real-time output function allows a pin state to be switched immediately upon the input of an external trigger input to a pin. The pin output state can be specified to be an output data toggle operation or an input/output control switch operation.



<Notation>
PDR 6: Port data register 6
PCR 6: Port control register 6
PDRS: Port data register slave
PCRS: Port control register slave
RTER: Real time enable register

Note: This figure shows the H8/3927 port 6.

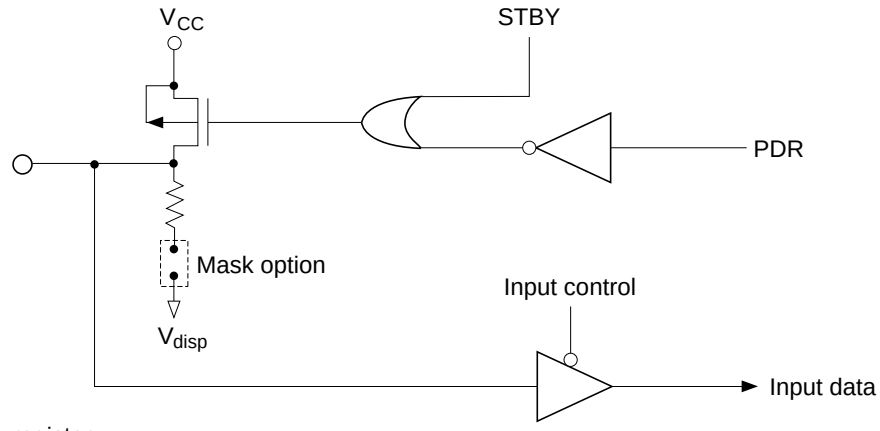
High Current Ports: These are high current ports that can drive external LEDs. The port functions are the same as general purpose I/O ports.

Item	Symbol	Condition	Rating
Output low level voltage	V_{OL}	V_{CC} = 4.0 to 5.5 V I_{OL} = 10 mA	1.5 V

Built-In Pull-Down MOS Transistors High Breakdown Voltage Ports: These ports are provided in the H8/3714 Series and the H8/3724 Series, and are 40 V breakdown voltage ports that can drive vacuum fluorescent displays. The table below lists their current drive capabilities.

Item	Symbol	Condition	Rating
Output high level voltage	V_{OH}	$-I_{OH}$ = 15 mA	V_{CC} – 3.0 V
		$-I_{OH}$ = 10 mA	V_{CC} – 2.0 V
		$-I_{OH}$ = 4 mA	V_{CC} – 1.0 V
Output low level voltage	V_{OL}	150 kΩ pull-down resistor Pull-down voltage Vdisp = V_{CC} – 40 V	V_{CC} – 37 V

The pull-down MOS transistors built into these ports can be enabled or disabled as a mask option.



<Notation>
PDR: Port data register

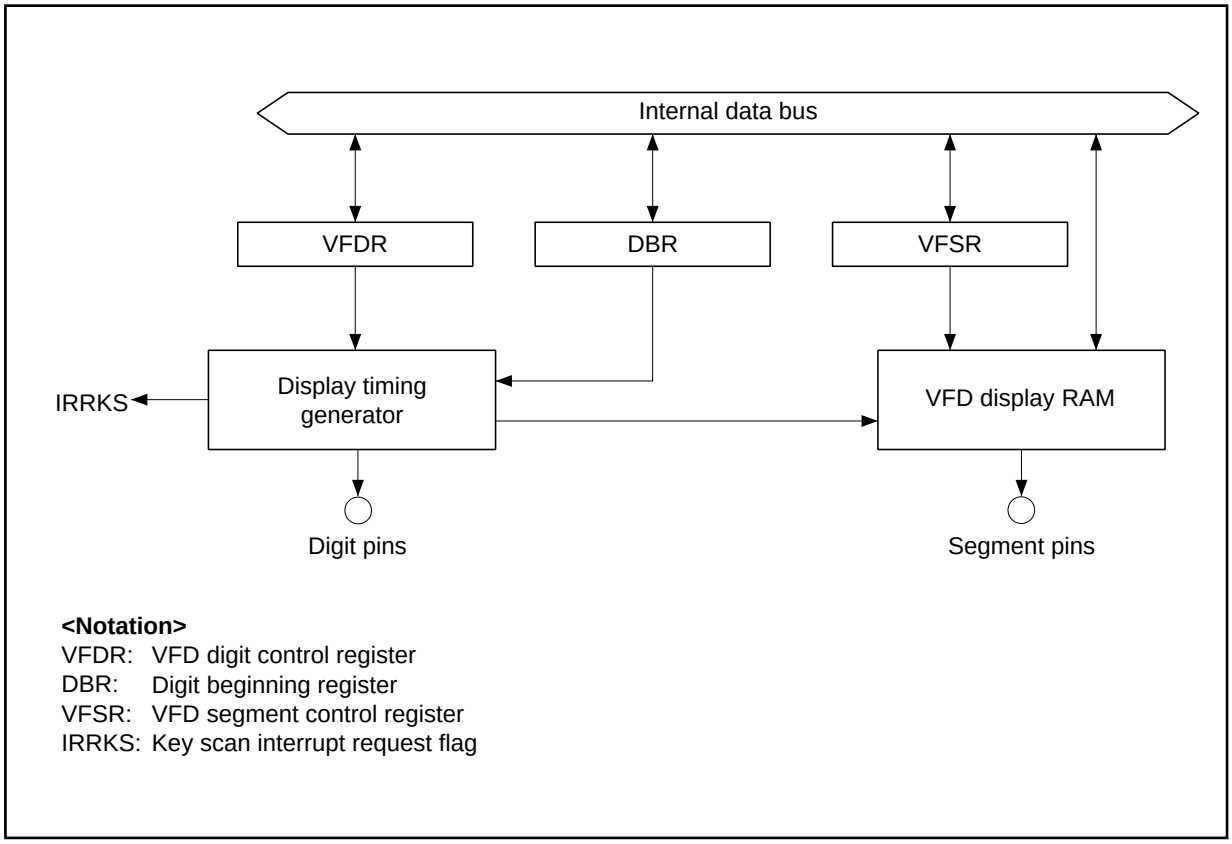
Note: This figure shows the H8/3724 high breakdown voltage port.

7. Vacuum Fluorescent Display (VFD) Controller/Driver

The H8/3714 Series, the H8/3724 Series and H8/3754 Series include a vacuum fluorescent display (VFD) controller/driver and high breakdown voltage high current pins. These allow the H8/3714 Series, the H8/3724 Series and H8/3754 Series to directly drive vacuum fluorescent displays.

Features:
- Up to 28 segment pins and up to 16 digit pins (of which 8 are shared function pins) built in.
- The VFD brightness can be adjusted over eight levels using the dimmer function.
- The display digit can be changed automatically.
- The digit and segment pins can be switched to function as general purpose high breakdown voltage pins.
- A key scan period can be enabled or disabled.
- Generates an interrupt at the start of the key scan period.

Block Diagram



8. Liquid Crystal Display (LCD) Controller/Driver

The H8/300L Series on-chip segment liquid crystal display (LCD) controller, LCD driver, and power supply circuit allow these microcomputers to directly drive an LCD panel.

To support the implementation of LCD control appropriate for the application area, the H8/300L Series provides three types of LCD controller/driver that differ in the particular combination of number of segments and amount of display memory provided.

Liquid Crystal Display (LCD) Controller/Driver 1 (H8/3834 Series)

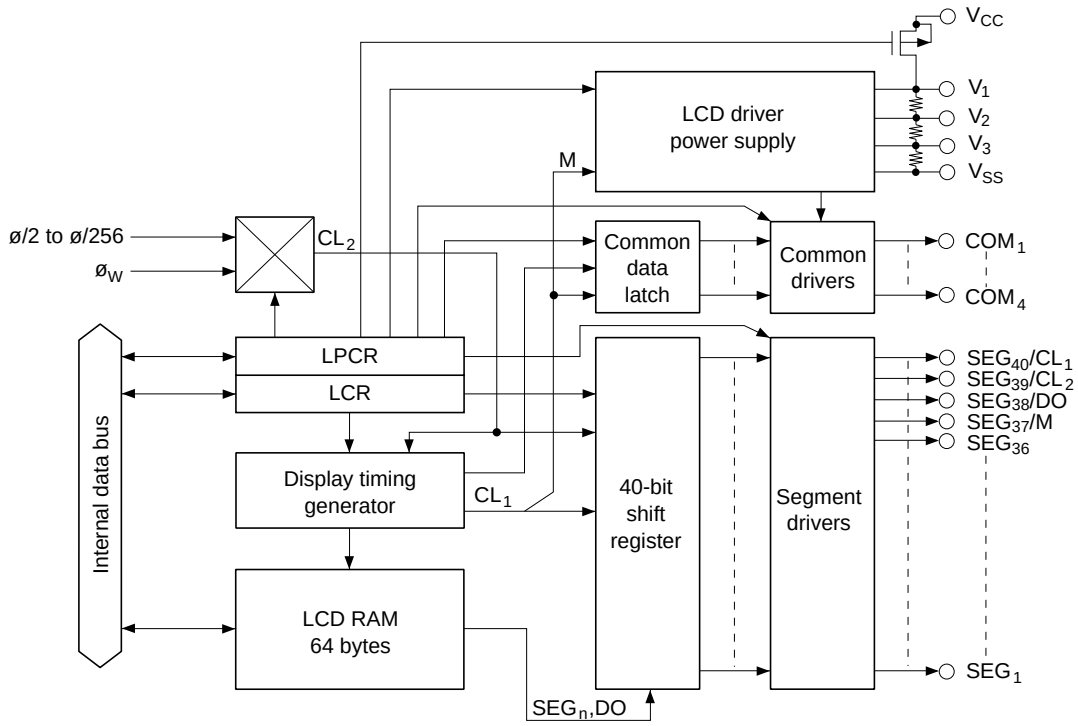
Features: • Display size

	Duty	Internal Drivers	External Expansion Drivers
When only internal drivers are used	Static	40 segments	0
	1/2	40 segments	0
	1/3	40 segments	0
	1/4	40 segments	0
When external expansion drivers are used	Static	36 segments	476 segments
	1/2	36 segments	220 segments
	1/3	36 segments	92 segments
	1/4	36 segments	92 segments

Note: The HD66100 can be used for external expansion.

- LCD RAM capacity: 16 bits × 32 bytes (512 bits)
- The LCD RAM can be accessed in word units.
- The segment output pins can be used as ports in 4-pin units.
- Common output pins that are not used due to the duty chosen can be used as either common buffers or ports as desired.
- Display is possible in all modes other than standby mode.
- Eleven frame frequencies are available.
- Power supply divider resistors are built in and used to provide the LCD drive power.

Block Diagram



<Notation>
LPCR: LCD port control register
LCR: LCD control register

Liquid Crystal Display (LCD) Controller/Driver 2 (H8/3814 Series)

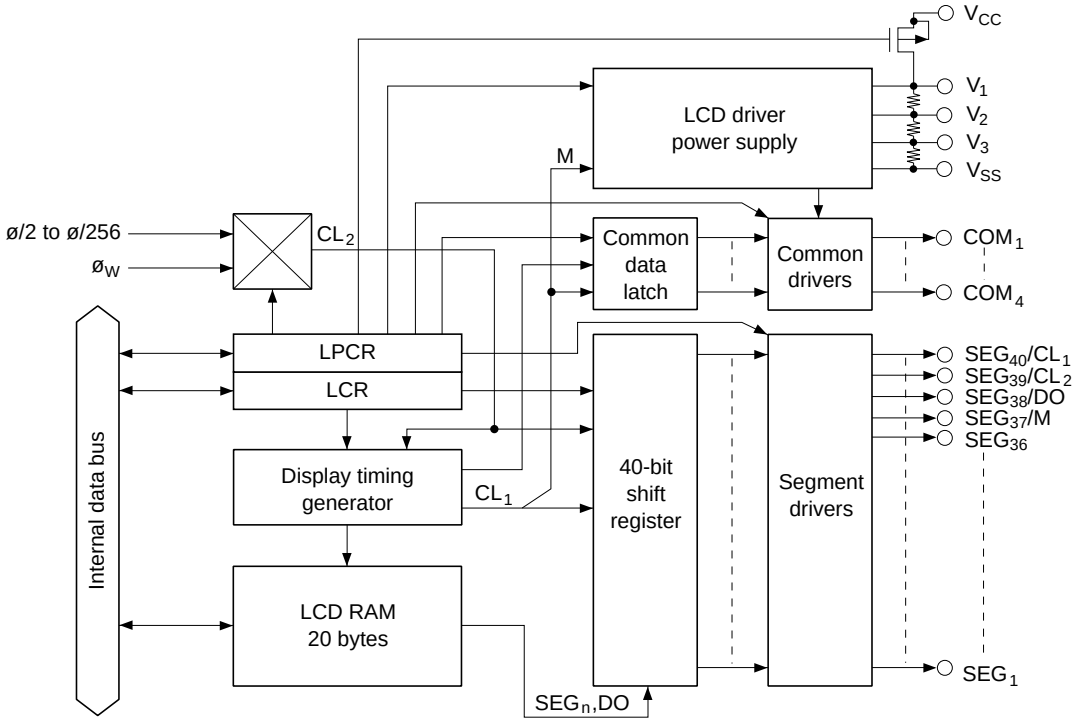
Features: • Display size

	Duty	Internal Drivers	External Expansion Drivers
When only internal drivers are used	Static	40 segments	0
	1/2	40 segments	0
	1/3	40 segments	0
	1/4	40 segments	0
When external expansion drivers are used	Static	36 segments	124 segments
	1/2	36 segments	44 segments
	1/3	36 segments	—
	1/4	36 segments	—

Note: The HD66100 can be used for external expansion.

- LCD RAM capacity: 16 bits × 10 bytes (160 bits)
- The LCD RAM can be accessed in word units.
- The segment output pins can be used as ports in 4-pin units.
- Common output pins that are not used due to the duty chosen can be used as either common buffers or ports as desired.
- Display is possible in all modes other than standby mode.
- Eleven frame frequencies are available.
- Power supply divider resistors are built in and used to provide the LCD drive power.

Block Diagram



<Notation>
LPCR: LCD port control register
LCR: LCD control register

Liquid Crystal Display (LCD) Controller/Driver 3 (H8/3877 Series)

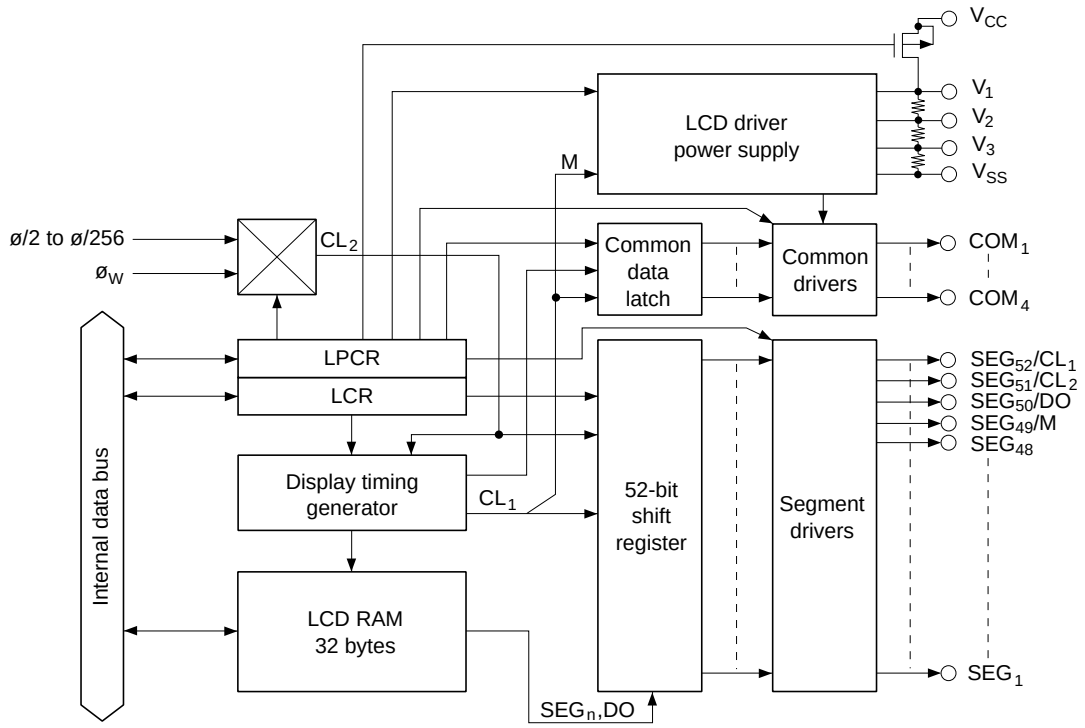
Features: • Display size

	Duty	Internal Drivers	External Expansion Drivers
When only internal drivers are used	Static	52 segments	0
	1/2	52 segments	0
	1/3	52 segments	0
	1/4	52 segments	0
When external expansion drivers are used	Static	48 segments	208 segments
	1/2	48 segments	80 segments
	1/3	48 segments	—
	1/4	48 segments	—

Note: The HD66100 can be used for external expansion.

- LCD RAM capacity: 16 bits × 16 bytes (256 bits)
- The LCD RAM can be accessed in word units.
- The segment output pins can be used as ports in 4-pin units.
- Common output pins that are not used due to the duty chosen can be used as either common buffers or ports as desired.
- Display is possible in all modes other than standby mode.
- Eleven frame frequencies are available.
- Power supply divider resistors are built in and used to supply the LCD drive power.

Block Diagram

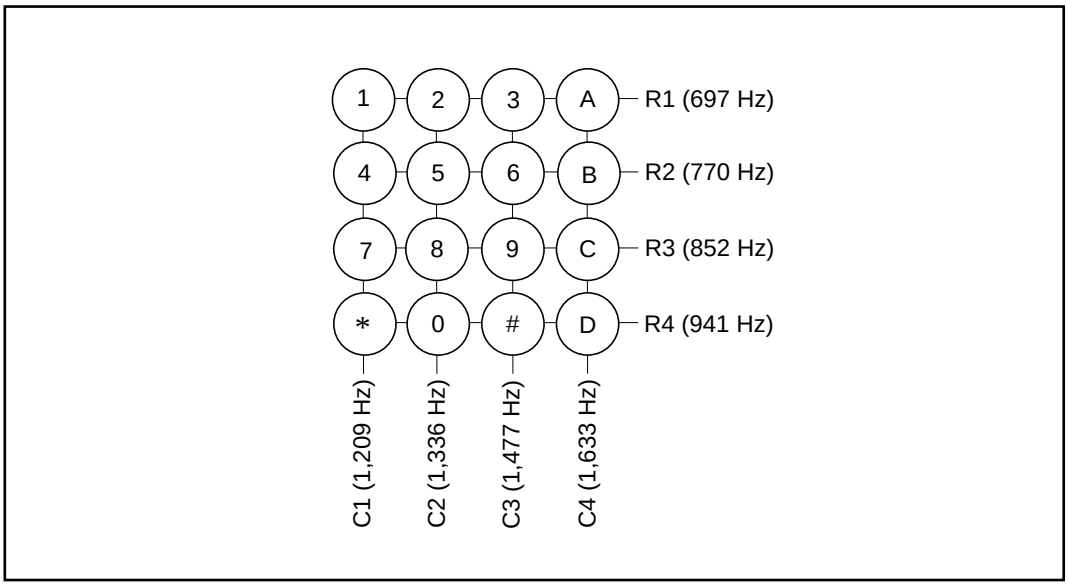


<Notation>
LPCR: LCD port control register
LCR: LCD control register

9. Dual Tone Multi Frequency (DTMF) Generator

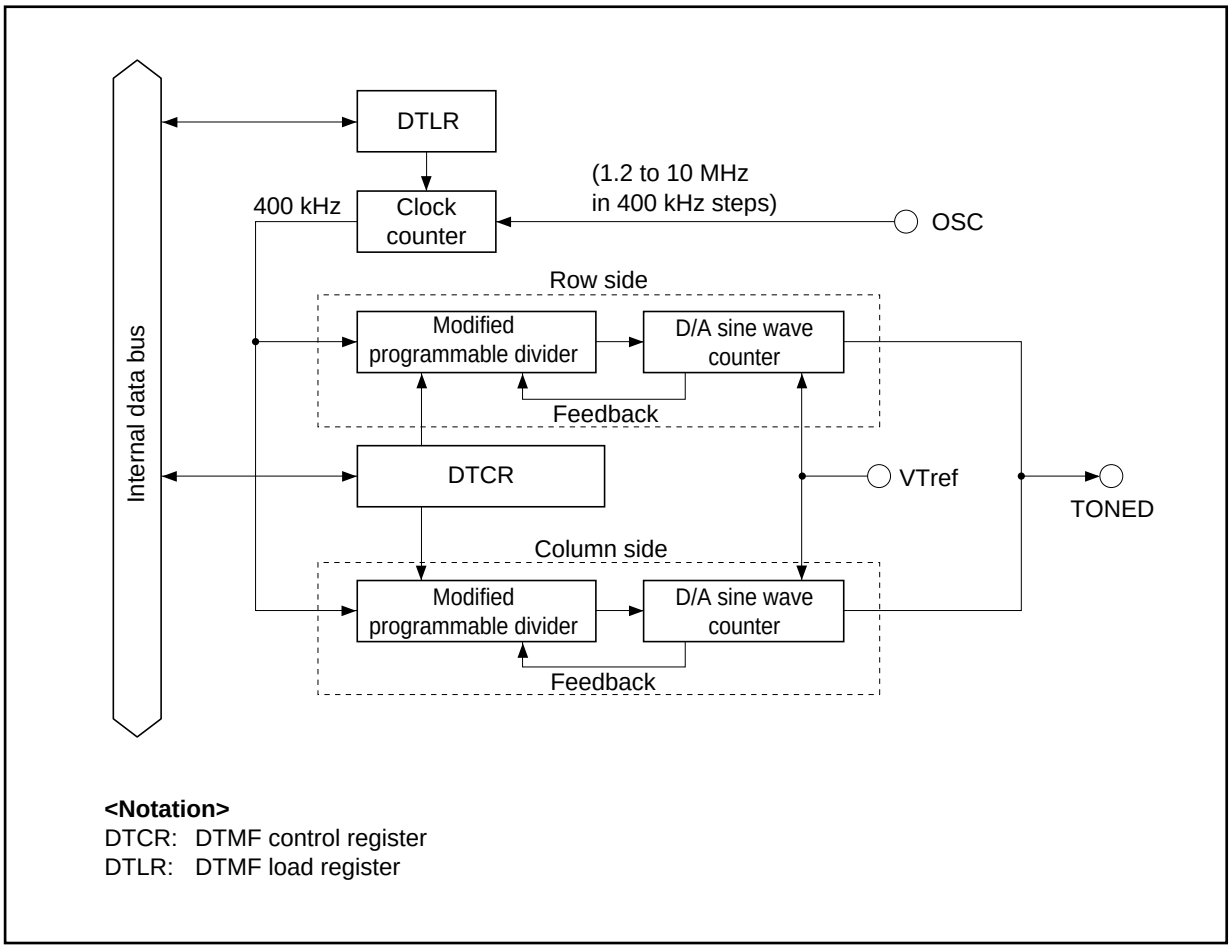
The H8/3877 Series on-chip dual tone multi frequency (DTMF) generator allows applications to output DTMF signals.

Features: DTMF signals are used to access telephone exchange equipment and consist of two sine waves expressed as a frequency matrix. The DTMF generator generates frequency combinations corresponding to the numbers and symbols on a telephone touch-pad.



- The DTMF frequencies are generated by dividing the oscillator clock (1.2 to 10 MHz in 400 kHz steps).
- Sine waves are output by a high-precision resistor ladder D/A converter, allowing low distortion high stability waveforms to be acquired.
- Output of either row group/column group composite signals or independent signals.

Block Diagram



<Notation>
DTCR: DTMF control register
DTLR: DTMF load register

10. Multi-Tone Generator

The H8/3877 Series on-chip multi-tone generator can output arbitrary waveforms at arbitrary frequencies.

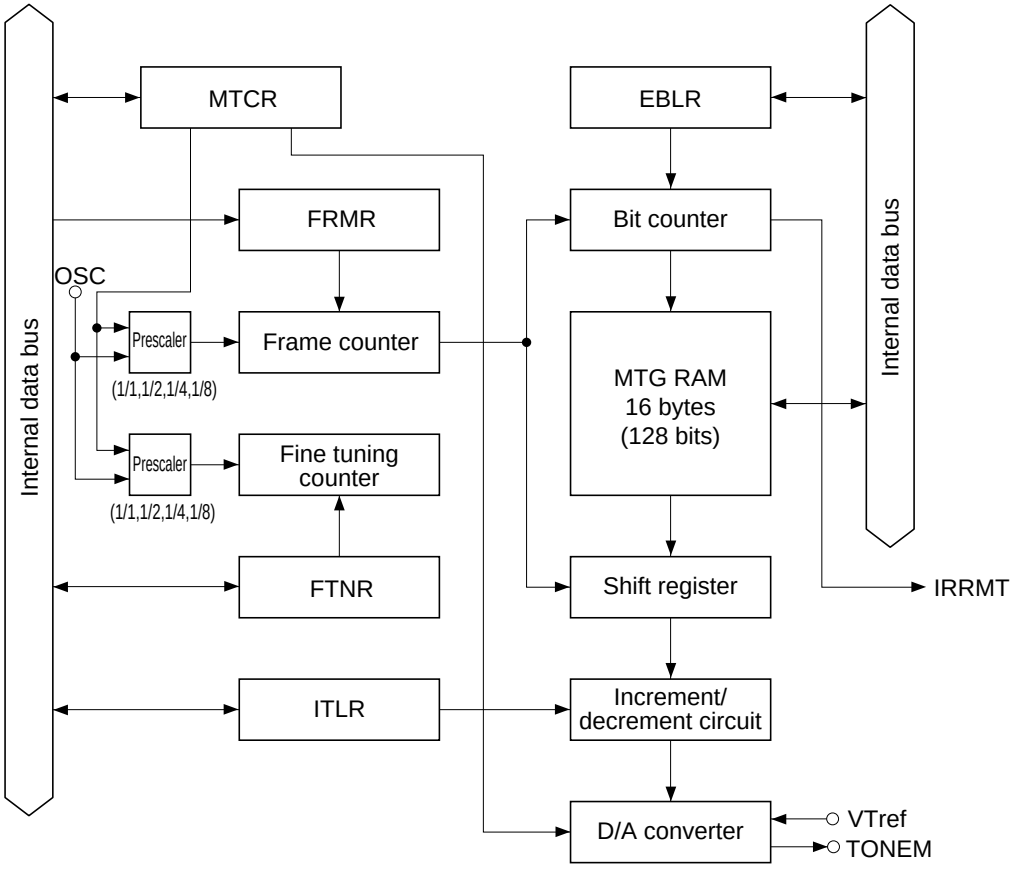
Features:

- Generates a wide range of frequencies, from 40 Hz to 4000 Hz (when OSC = 10 MHz).

Frequency Range	Step Size	Precision
40 Hz to 1000 Hz	1 Hz	±0.05 Hz
1000 Hz to 3000 Hz	1 Hz	±0.5 Hz
3000 Hz to 4000 Hz	2 Hz	±1 Hz

  The output frequency is generated by using a frame counter and a fine tuning counter to divide the oscillator clock (f_{OSC}).
- The output waveform is generated by a 5-bit resolution R-2R type D/A converter at up to 128 divisions per cycle. This allows a stable low-distortion waveform to be acquired.
- An arbitrary waveform pattern can be formed by storing a bit pattern in MTG RAM (up to 128 bits).

Block Diagram



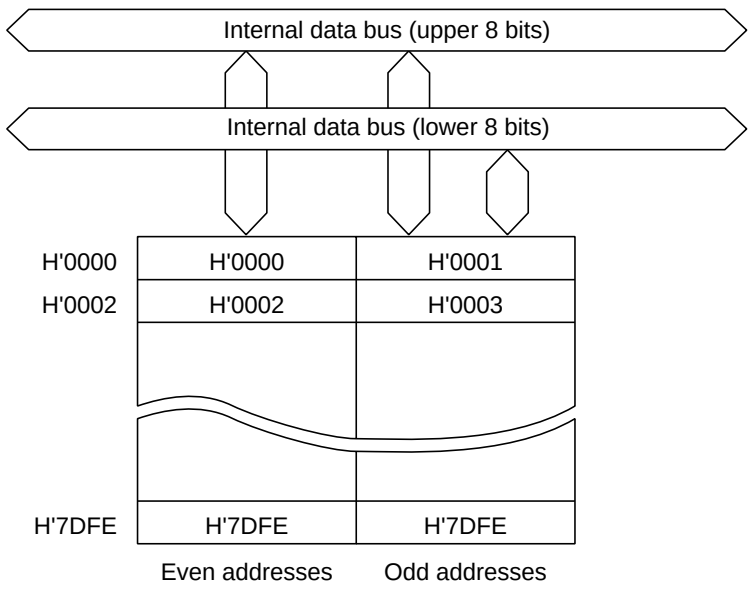
<Notation>

MTCR: Multi-tone control register
EBLR: Effective bit-length register
FRMR: Frame register
FTNR: Fine tuning register
ITLR: Initial level register
IRRMT: Multi-tone half-period interrupt request flag

11. ROM

The H8/300L Series product lineup includes microcomputers with on-chip ROM capacities from 16 kbytes to 60 kbytes. The H8/300L Series ROM is connected to the CPU over a 16-bit data bus, and can be accessed in only 2 states in both byte and word access modes. Due to the speed of this ROM, the H8/300L CPU has a minimum instruction execution time of 0.4 µs when the operating frequency is 5 MHz.

Block Diagram



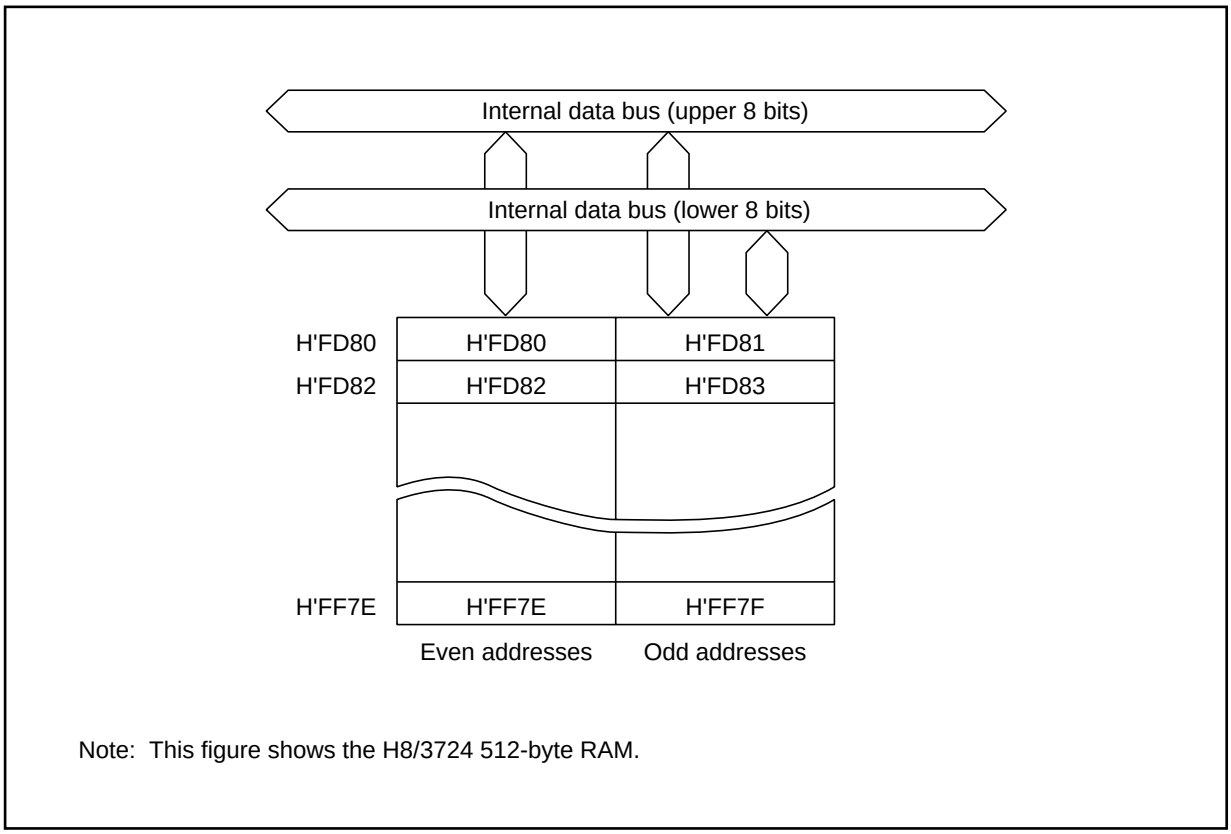
Note: This figure shows the H8/3724 32-kbyte ROM.

The lowest addresses in the H8/300L Series ROM area are used as the interrupt vector region. The relationship between interrupts and the interrupt vector region differs for each product, and is described in the individual product hardware manuals. The area from H'0000 to H'00FF, which includes the interrupt vector area, can be accessed using an indirect addressing mode based on an 8-bit address included in the H8/300L Series CPU instruction code. Application programs can be coded compactly by storing commonly used branch addresses in this area.

12. RAM

The H8/300L Series product lineup includes microcomputers with on-chip RAM capacities from 512 bytes to 2 kbytes. The H8/300L Series RAM is connected to the CPU over a 16-bit data bus, and can be accessed in only 2 states in both byte and word access modes. Due to the speed of this RAM, the H8/300L CPU can execute data handling instructions in only 0.4 µs.

Block Diagram



Note: This figure shows the H8/3724 512-byte RAM.

A short absolute addressing mode is provided by the H8/300L Series CPU MOV instruction for rapid access to locations from H'FF00 to H'FFFF. Furthermore, programs can be coded compactly due to the short instruction length. Since RAM locations H'FF00 to H'FF7F can be accessed by this short absolute addressing mode, programs can use this mode to implement high speed data handling.

H8/300L Series Document

Product No.	Document No.				
	Microcomputer Series Catalogs	Quick Reference Guides	H8 Series Individual Product Catalogs	Series Overview Documents	
H8/3612	ADJ-102-006P			ADJ-802-134 ADE-802-154	
H8/3613					
H8/3614					
H8/3712	ADJ-102-006P		ADJ-102-013F		
H8/3713	ADJ-102-006P	ADJ-301-002F ADE-301-001K	ADJ-102-013F		
H8/3714	ADJ-102-006P	ADJ-301-002F ADE-301-001K	ADJ-102-013F		
H8/3723	ADJ-102-006P	ADJ-301-002F ADE-301-001K	ADJ-102-013F		
H8/3724	ADJ-102-006P	ADJ-301-002F ADE-301-001K	ADJ-102-013F		
H8/3725	ADJ-102-006P	ADJ-301-002F ADE-301-001K	ADJ-102-013F		
H8/3726	ADJ-102-006P	ADJ-301-002F ADE-301-001K	ADJ-102-013F		
H8/3753					
H8/3754					
H8/3812	ADJ-102-006P	ADJ-301-002F ADE-301-001K	ADJ-102-013F		
H8/3813	ADJ-102-006P	ADJ-301-002F ADE-301-001K	ADJ-102-013F		
H8/3814	ADJ-102-006P	ADJ-301-002F ADE-301-001K	ADJ-102-013F		
H8/3834	ADJ-102-006P	ADJ-301-002F ADE-301-001K	ADJ-102-013F		
H8/3836	ADJ-102-006P		ADJ-102-013F		
H8/3837	ADJ-102-006P		ADJ-102-013F		
H8/3875	ADJ-102-006P		ADJ-102-013F		
H8/3876	ADJ-102-006P		ADJ-102-013F		
H8/3877	ADJ-102-006P		ADJ-102-013F		
H8/3924	ADJ-102-006P		ADJ-102-013F		
H8/3925	ADJ-102-006P		ADJ-102-013F		
H8/3926	ADJ-102-006P		ADJ-102-013F		
H8/3927	ADJ-102-006P		ADJ-102-013F		

Notes: Documents in Japanese (e.g., those prefixed with “ADJ”) are listed first.
Documents in English (e.g., those prefixed with “ADE”) are listed below.

	Document No.				
	Databooks	**GAIN**	**System Catalogs**	**User's Manuals**	**Application Notes**
				ADJ-602-087	ADJ-502-026
				ADJ-602-087	ADJ-502-026
				ADJ-602-087	ADJ-502-026
				ADJ-602-070A ADE-602-056	ADJ-502-026
		No. 97 Vol. 12		ADJ-602-070A ADE-602-056	ADJ-502-026
		No. 97 Vol. 12		ADJ-602-070A ADE-602-056	ADJ-502-026
		No. 97 Vol. 12	ADJ-109-017/018	ADJ-602-057A ADE-602-044A	ADJ-502-026
		No. 97 Vol. 11	ADJ-109-017/018	ADJ-602-057A ADE-602-044A	ADJ-502-026
		No. 97	ADJ-109-017	ADJ-602-057A ADE-602-044A	ADJ-502-026
		No. 97	ADJ-109-017	ADJ-602-057A ADE-602-044A	ADJ-502-026
					ADJ-502-026
					ADJ-502-026
		No. 97		ADJ-602-074 ADE-602-059	ADJ-502-026
				ADJ-602-074 ADE-602-059	ADJ-502-026
				ADJ-602-074 ADE-602-059	ADJ-502-026
		No. 97 Vol. 12	ADJ-109-018	ADJ-602-069B ADE602-054A	ADJ-502-026
				ADJ-602-069B ADE-602-054A	ADJ-502-026
				ADJ-602-069B ADE-602-054A	ADJ-502-026
		No. 98		ADJ-602-080A ADE-602-060	ADJ-502-026
		No. 98		ADJ-602-080A ADE-602-060	ADJ-502-026
		No. 98		ADJ-602-080A ADE-602-060	ADJ-502-026
				ADJ-602-079A	ADJ-502-026
				ADJ-602-079A	ADJ-502-026
				ADJ-602-079A	ADJ-502-026
		No. 98 Vol. 12		ADJ-602-079A	ADJ-502-026