HD66732

(Graphics Liquid Crystal Display Controller/Driver Supporting JIS Level-1 and Level-2 Kanji ROM)

HITACHI

ADE-207-314(Z)
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Description

The HD66732 is a dot-matrix liquid crystal display (LCD) controller and driver LSI that displays 11-by-12 dot Japanese characters consisting of kanji and hiragana according to the Japanese Industrial Standard (JIS) Level-1 and Level-2 Kanji Set. The HD66732 incorporates the following five functions on a single chip: (1) display control function for the dot matrix LCD, (2) a display RAM to store character codes, (3) ROM fonts to support level-1 and level-2 kanji, (4) an LCD driver, and (5) a booster to drive the LCD. A 4-line 10-character kanji display can be easily achieved by receiving character codes (2 bytes/character) from the microcomputer. The software processing loads on the microcomputer for kanji-font display development can be greatly reduced, and an external kanji character generator or key scan circuit is not needed. The character font includes font ROMs of 6,353 kanji from the JIS Level-1 and Level-2 Kanji Set, 285 JIS non-kanji characters, and 256 half-size alphanumeric characters and symbols. Full-size fonts such as Japanese kanji and half-size fonts such as alphanumeric characters can be displayed together. In addition, the HD66732 supports a 120-by-52 dot graphics display function that can display not only characters such as kanji but also graphics such as drawings or maps.

The HD66732 has various functions to reduce the power consumption of an LCD system, such as low-voltage operation at 2.4 V, a low-power LCD drive operating amplifier, and a booster to switch the boosting rate. Combining these hardware functions with software functions such as standby and sleep modes allows precise power control. The HD66732 is suitable for any battery-driven product requiring long-term driving capabilities such as cellular phones, pagers, or portable devices.

Features

- Dot-matrix liquid crystal display controller/driver supporting the display of kanji from the JIS Level-1 and Level-2 Kanji Set
- Kanji display and high-speed font development processing enabled by data transfer of two bytes/character
- 4-line 10-character kanji and 120-by-52-dot graphics display
- Mark display using 200 monochrome segments (marks) or 40 grayscale segments
- Control up to a 4 x 8 (32 key) matrix key scan (at a serial interface)

- Large character generator ROM for full-size display: corresponds to 8,128 full-size fonts
  - — Kanji according to JIS Level-1 Kanji (11 x 12 dots): 2,965-character font
  - — Kanji according to JIS Level-2 Kanji (11 x 12 dots): 3,388-character font
  - — JIS non-kanji (11 x 12 dots): 285-character font
- Character generator ROM for half-size display: corresponds to 256 half-size fonts
  - — Alphanumeric characters (6 x 12 dots): 128 fonts x 2 banks (256 fonts)
- 120-by-52-dot bit-map graphics display
- Combined display of 11 x 12 dots for full-size fonts consisting of kanji and kana, 6 x 12 dots for half-size fonts of alphanumeric characters and symbols
- Low-power operation support:
  - — Vcc = 2.4 to 5.5 V (low voltage)
  - — Single, double, triple, or quadruple booster for liquid crystal drive voltage
  - — Operational amplifier for low-power LCD drive supply and bleeder-resistors incorporated
  - — Strong power-save functions such as the standby mode and sleep mode supported
  - — Wake-up function using key scan interrupt
  - — Programmable LCD-drive duty ratios and bias values
- Various display control functions:
  - — Combined display (super-imposed display) of kanji characters and bit map graphics
  - — Vertical smooth scroll (dot unit)
  - — Black-white reversed display of full screen
  - — Display-line-unit black-white reversed/underline/blinking display
  - — Black-white reversed/blinking/black-white reversed blinking character display
- Display data RAM: 80 bytes (stores 40-character code in full size)
- Character generator RAM: 780 bytes (stores 120-by-52-dot bit map areas) (30 full-size user fonts can be displayed)
- Segment RAM: 60 bytes (200 segments can be displayed)
- Three-line clock synchronous serial bus, 4-/8-bit bus interface
- No wait cycle for instruction execution and RAM access
- 120-segment x 54-common LCD driver
- Three general output ports built-in
- External R-C oscillator
- LCD drive voltage: 4.5 V to 13.0 V
- External dimensions: Tape carrier package (TCP) and slim chip with Au-bumps

Table 1 Programmable Display Sizes and Duty Ratios

Duty Ratio	Optimum Drive Bias	Number of Full-size Kanji Display Characters	Graphics Display Area	Segment Display	Scanned Keys	General Ports
1/2	1/2	Unavailable	Unavailable	200	32 (4 x 8)	3
1/15	1/5	1 line x 10 characters	120 x 13 dots	(Grayscale		
1/28	1/6	2 lines x 10 characters	120 x 26 dots	segments:		
1/41	1/7	3 lines x 10 characters	120 x 39 dots	40)		
1/54	1/8	4 lines x 10 characters	120 x 52 dots			

Type Name

Type Name	External Dimensions	Display Lines (Graphics Display)	Built-in Full-size Font	Built-in Half-size Font
HD66732A04TB0L	Bending TCP	4-line x 10-character (120 x 52 dots)	JIS Level-1 and Level-2 Kanji Set + non-kanji characters	Alphanumeric characters
HD66732A04BP	Au-bumped chip (slim chip)	4-line x 10-character (120 x 52 dots)	JIS Level-1 and Level-2 Kanji Set + non-kanji characters	Alphanumeric characters

Example of Liquid Crystal Display

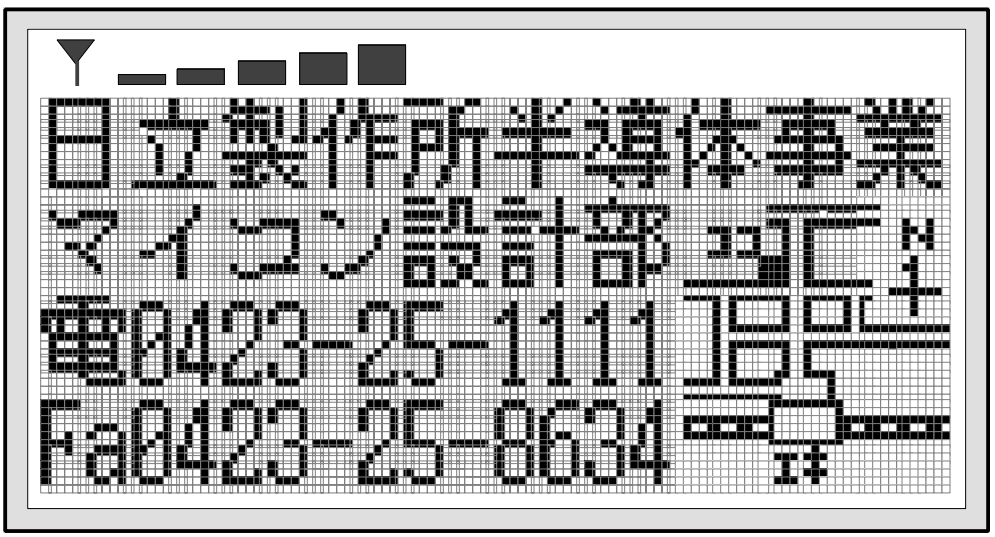


Figure 1 Combined Display of 4-line x 10-character Kanji and Graphics

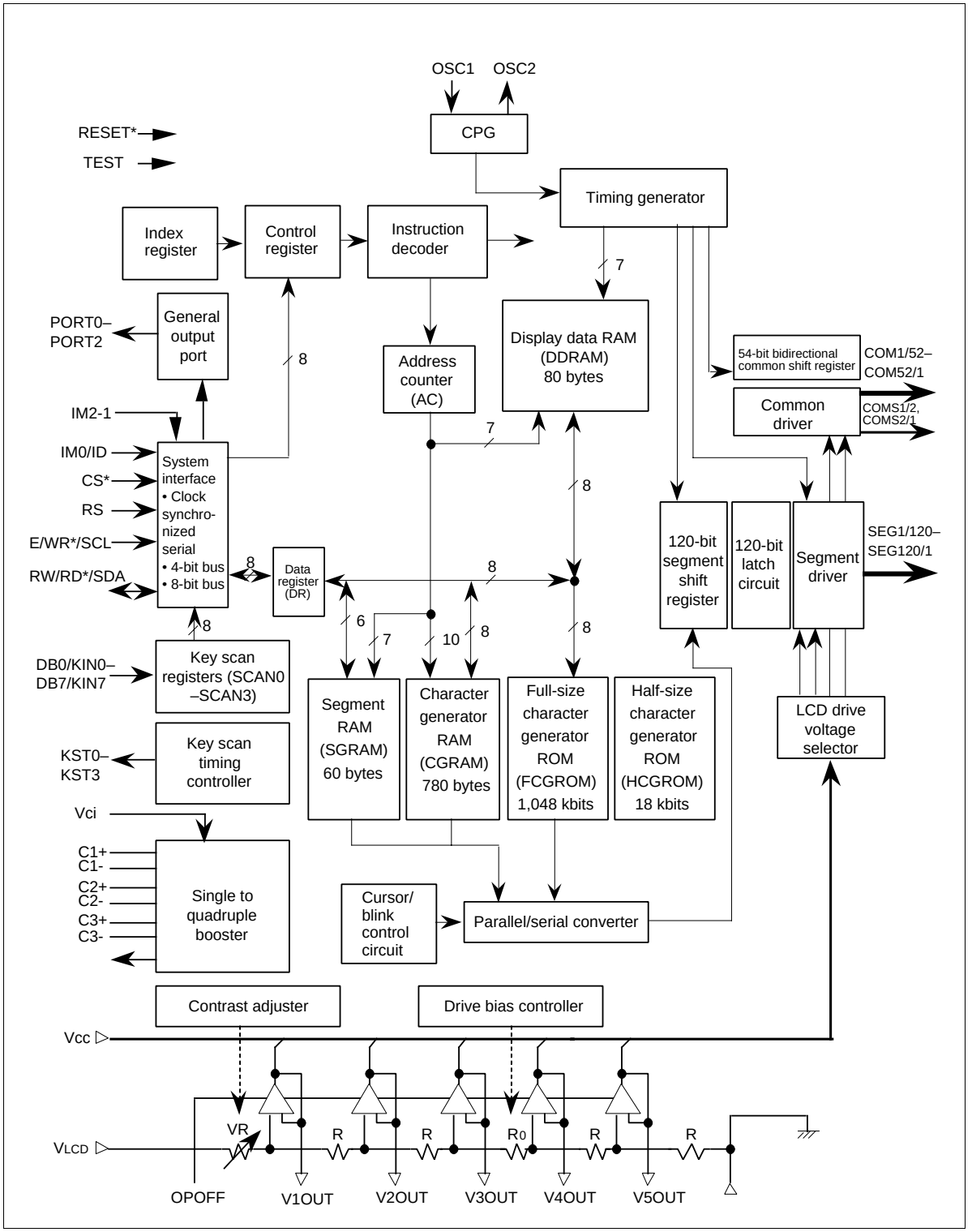
LCD Specification Comparison for Kanji Display

	External Kanji ROM Type		
Items	**HD66724**	**HD66725**	**HD66726**
Kanji display area	72 x 24 dots	96 x 24 dots	96 x 40 dots
Kanji character display	—	—	—
Half-size alphanumeric character display	12 characters x 3 lines	16 characters x 3 lines	16 characters x 5 lines
Graphics display sizes	72 x 26 dots	96 x 26 dots	96 x 42 dots
Multiplexing icons	144	192	192
Key scan control	8 x 4	8 x 4	8 x 4
General output port	3	3	3
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	3 V to 6 V	3 V to 6 V	4.5 V to 11 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits
Expansion driver control	Impossible	Impossible	Impossible
Liquid crystal drive duty ratios	1/2, 10, 18, 26	1/2, 10, 18, 26	1/2, 10, 18, 26, 34, 42
Liquid crystal drive biases	1/4 to 1/6.5	1/4 to 1/6.5	1/2 to 1/8
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Single, double or triple	Single, double, or triple	Single, double, triple, or quadruple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	3-dot unit	3-dot unit	Impossible
Vertical smooth scroll	Raster-row unit	Raster-row unit	Raster-row unit
Double-height display	Yes	Yes	Yes
DDRAM	80 x 8	80 x 8	80 x 8
CGROM	21 k	21 k	21 k
Incorporated font	Alphanumeric character + kana	Alphanumeric character + kana	Alphanumeric character + kana
CGRAM	384 x 8	384 x 8	480 x 8
SEGRAM	72 x 8	96 x 8	96 x 8
Number of CGROM fonts	432	432	432
Number of CGRAM fonts	64	64	64
Font sizes	6 x 8	6 x 8	6 x 8
R-C oscillation resistor/ oscillation frequency	External resistor, incorporated (32 kHz)	External resistor, incorporated (32 kHz)	External resistor (50 kHz)
Reset function	External	External	External
Low power control	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
QFP package	—	—	—
TCP package	TCP	TCP	TCP
Bare chip (without bumps)	—	—	—
Bumped chip	Yes	Yes	Yes
Number of pins	146	170	185
Chip sizes	10.34 x 2.51	10.97 x 2.51	13.13 x 2.51
Pad (bump) intervals	80 µm	80 µm	100 µm

LCD Specification Comparison for Kanji Display (cont)

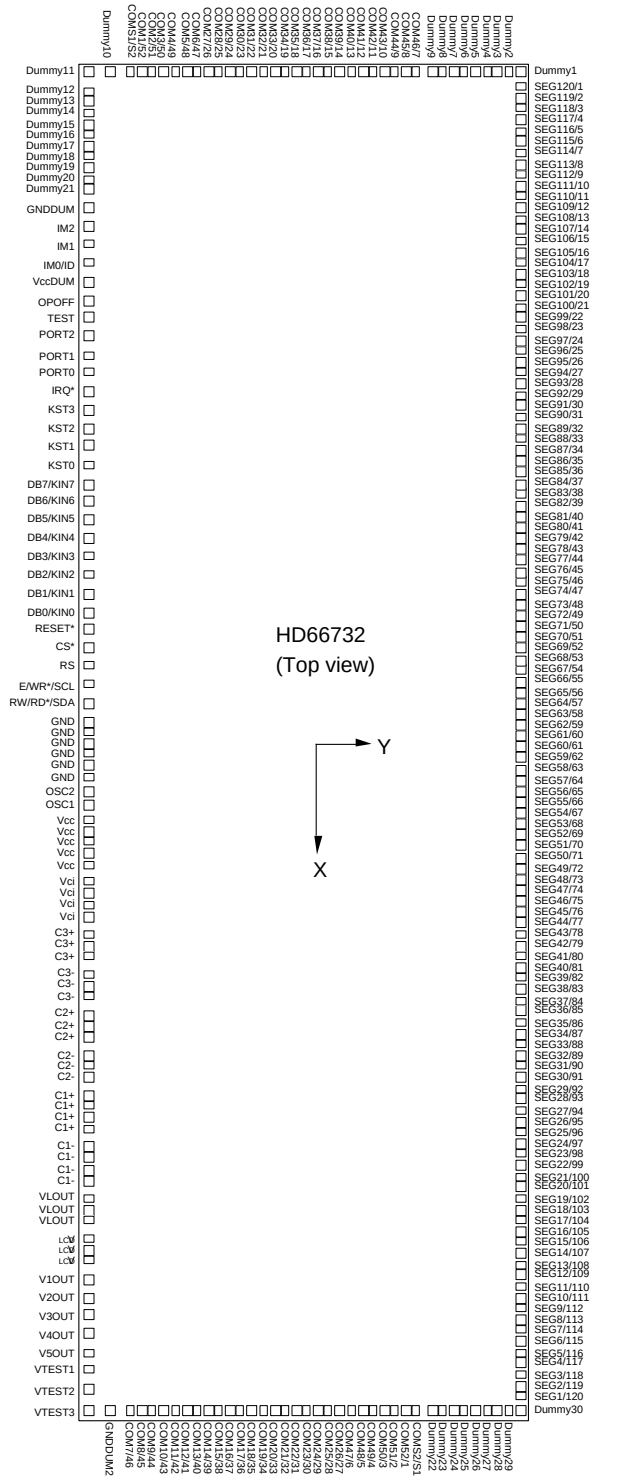
	Internal Kanji ROM Type		
Items	**HD66730**	**HD66731**	**HD66732**
Kanji display area	71 x 25 dots	119 x 51 dots	120 x 52 dots
Kanji character display	6 characters x 2 lines	10 characters x 4 lines	10 characters x 4 lines
Half-size alphanumeric character display	12 characters x 2 lines	20 characters x 4 lines	20 characters x 4 lines
Graphics display sizes	(48 x 26 dots)	(48 x 26 dots)	120 x 52 dots
Multiplexing icons	71	120	200
Key scan control	—	—	8 x 4
General output port	—	—	3
Operating power voltages	2.4 V to 5.5 V	2.4 V to 5.5 V	2.4 V to 5.5 V
Liquid crystal drive voltages	3 V to 15 V	3 V to 15 V	4.5 V to 13 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	8 bits	8 bits	4 bits, 8 bits
Expansion driver control	Possible	Impossible	Impossible
Liquid crystal drive duty ratios	1/14, 27, 40, 53	1/14, 27, 40, 53	1/2, 15, 28, 41, 54
Liquid crystal drive biases	1/4 to 1/8.3	1/4 to 1/8.3	1/2 to 1/8
Liquid crystal drive waveforms	B	B	B + C
Liquid crystal voltage booster	Double or triple	Double or triple	Single, double, triple, or quadruple
Bleeder-resistor for liquid crystal drive	External	External	External
Liquid crystal drive operational amplifier	—	—	Incorporated
Contrast adjuster	—	—	Incorporated
Horizontal smooth scroll	Display unit	Display unit	Impossible
Vertical smooth scroll	Raster-row unit	Raster-row unit	Raster-row unit
Double-height display	—	—	—
DDRAM	80 x 8	80 x 8	80 x 8
CGROM	507 k + 9 k	507 k + 9 k	1,048 k + 18 k
Incorporated font	JIS Level-1 Kanji Set, Hungle	JIS Level-1 Kanji Set, Hungle	JIS Level-1 and Level-2 Kanji Set
CGRAM	208 x 8	208 x 8	780 x 8
SEGRAM	16 x 8	16 x 8	60 x 8
Number of CGROM fonts	3840 + 128 (half size)	3840 + 128 (half size)	8128 + 256 (half size)
Number of CGRAM fonts	8	8	30
Font sizes	11 x 12	11 x 12	11 x 12
R-C oscillation resistor/ oscillation frequency	External resistor (150 kHz)	External resistor (150 kHz)	External resistor (45 to 76 kHz)
Reset function	External	External	External
Low power control	Booster off Internal division function	Booster off Internal division function	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	—	—	SEG, COM
QFP package	QFP-1420	—	—
TCP package	—	TCP	TCP
Bare chip (without bumps)	Yes	—	—
Bumped chip	—	Yes	Yes
Number of pins	128	206	221
Chip sizes	7.48 x 6.46	7.48 x 6.46	12.68 x 4.31
Pad (bump) intervals	180 µm	80 µm	100 µm

HD66732 Block Diagram



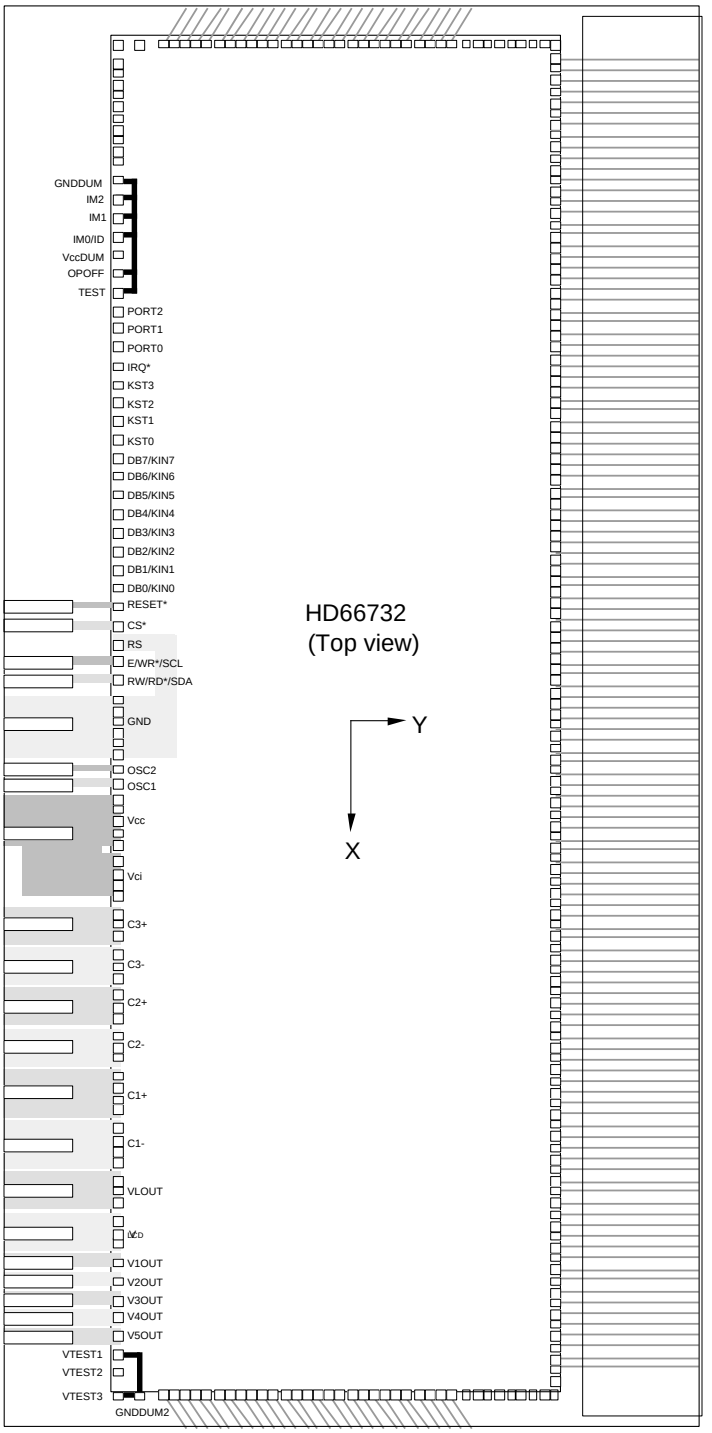
HD66732 Pad Arrangement

- Chip size: 12.68 mm x 4.31 mm
- Pad coordinates: Pad center
- Coordinate origin: Chip center
- Au bump size: 70 µm x 70 µm
- Au bump pitch: 100 µm (min.)



COG Routing Example

- Clock-synchronized serial bus
- Unused key scan
- Unused port output
- Quadruple booster
- Internal operational amplifier

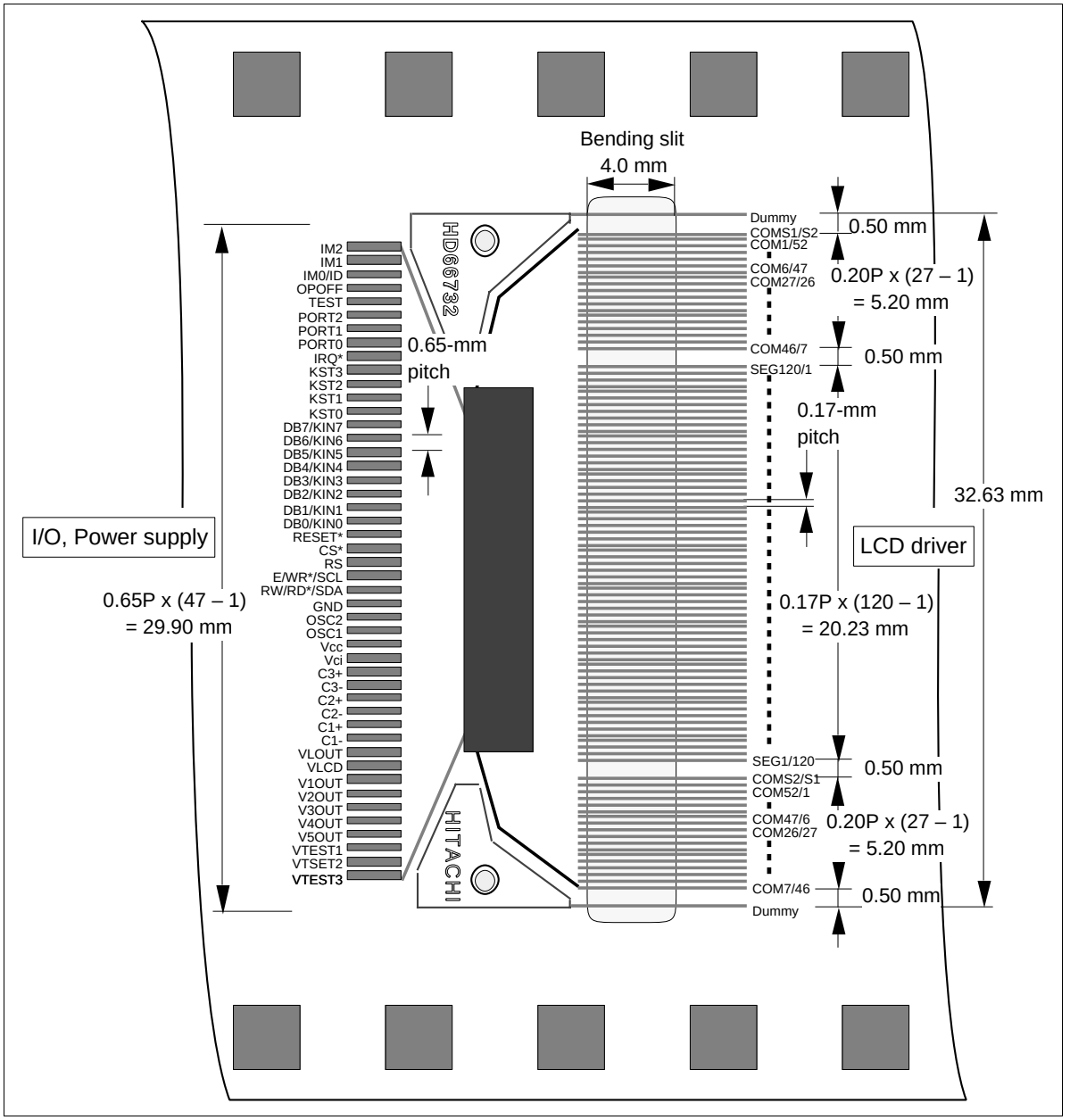


HD66732 Pad Coordinates

Pin No.	Pad Name	Coordinate X	Coordinate Y
—	Dummy1	–6165	1929
—	Dummy2	–6165	1829
—	Dummy3	–6165	1729
—	Dummy4	–6165	1629
—	Dummy5	–6165	1529
—	Dummy6	–6165	1428
—	Dummy7	–6165	1328
—	Dummy8	–6165	1228
—	Dummy9	–6165	1128
228	COM46/7	–6114	972
229	COM45/8	–6114	872
230	COM44/9	–6114	772
231	COM43/10	–6114	671
232	COM42/11	–6114	571
233	COM41/12	–6114	471
234	COM40/13	–6114	371
235	COM39/14	–6114	271
236	COM38/15	–6114	171
237	COM37/16	–6114	71
238	COM36/17	–6114	–29
239	COM35/18	–6114	–129
240	COM34/19	–6114	–229
241	COM33/20	–6114	–329
242	COM32/21	–6114	–429
243	COM31/22	–6114	–529
244	COM30/23	–6114	–630
245	COM29/24	–6114	–730
246	COM28/25	–6114	–830
247	COM27/26	–6114	–930
248	COM6/47	–6114	–1030
249	COM5/48	–6114	–1130
250	COM4/49	–6114	–1230
251	COM3/50	–6114	–1330
252	COM2/51	–6114	–1430
253	COM1/52	–6114	–1530
254	COMS1/S2	–6114	–1630
—	Dummy10	–6114	–1810
—	Dummy11	–6114	–1989
—	Dummy12	–5914	–1989
—	Dummy13	–5814	–1989
—	Dummy14	–5714	–1989
—	Dummy15	–5613	–1989
—	Dummy16	–5513	–1989
—	Dummy17	–5413	–1989
—	Dummy18	–5313	–1989
—	Dummy19	–5213	–1989
—	Dummy20	–5113	–1989
—	Dummy21	–5013	–1989
1	GNDDUM1	–4863	–1989
2	IM2	–4762	–1989
3	IM1	–4578	–1989
4	IM0/ID	–4403	–1989
5	V_{CC}DUM	–4303	–1989
6	OPOFF	–4202	–1989
7	TEST	–4027	–1989
8	PORT2	–3843	–1989
9	PORT1	–3659	–1989
10	PORT0	–3475	–1989
11	IRQ*	–3291	–1989
12	KST3	–3107	–1989
13	KST2	–2923	–1989
14	KST1	–2739	–1989
15	KST0	–2555	–1989
16	DB7/KIN7	–2371	–1989
17	DB6/KIN6	–2187	–1989
18	DB5/KIN5	–2003	–1989
19	DB4/KIN4	–1819	–1989
20	DB3/KIN3	–1635	–1989
21	DB2/KIN2	–1451	–1989
22	DB1/KIN1	–1267	–1989
23	DB0/KIN0	–1083	–1989
24	RESET*	–899	–1989
25	CS*	–715	–1989
26	RS	–531	–1989
27	E/WR*/SCL	–368	–1989
28	RW/RD*/SDA	–238	–1989
29	GND	–53	–1989
30	GND	77	–1989
31	GND	208	–1989
32	GND	338	–1989
33	GND	468	–1989
34	GND	598	–1989
35	OSC2	784	–1989
36	OSC1	968	–1989
37	V_{CC}	1148	–1932
38	V_{CC}	1278	–1932
39	V_{CC}	1408	–1932
40	V_{CC}	1538	–1932
41	V_{CC}	1668	–1932
42	Vci	1965	–1929
43	Vci	1865	–1929
44	Vci	2065	–1929
45	Vci	2165	–1929
46	C3+	2296	–1929
47	C3+	2396	–1929
48	C3+	2496	–1929
49	C3–	2626	–1929
50	C3–	2726	–1929
51	C3–	2826	–1929
52	C2+	2956	–1929
53	C2+	3056	–1929
54	C2+	3156	–1929
55	C2–	3256	–1929
56	C2–	3387	–1929
57	C2–	3487	–1929
58	C1+	3617	–1929
59	C1+	3717	–1929
60	C1+	3817	–1929
61	C1+	3917	–1929
62	C1–	4047	–1929
63	C1–	4147	–1929
64	C1–	4247	–1929
65	C1–	4347	–1929
66	VLOUT	4478	–1929
67	VLOUT	4578	–1929
68	VLOUT	4678	–1929
69	VLCD	4808	–1929
70	VLCD	4908	–1929
71	VLCD	5008	–1929
72	V1OUT	5188	–1940
73	V2OUT	5318	–1940
74	V3OUT	5448	–1940
75	V4OUT	5578	–1940
76	V5OUT	5709	–1940
77	VTEST1	5839	–1940
78	VTEST2	5969	–1940
79	VTEST3	6114	–1940
80	GNDDUM2	6114	–1765
81	COM7/46	6114	–1630
82	COM8/45	6114	–1530
83	COM9/44	6114	–1430
84	COM10/43	6114	–1330
85	COM11/42	6114	–1230
86	COM12/41	6114	–1130
87	COM13/40	6114	–1030
88	COM14/39	6114	–930
89	COM15/38	6114	–830
90	COM16/37	6114	–730
91	COM17/36	6114	–630
92	COM18/35	6114	–529
93	COM19/34	6114	–429
94	COM20/33	6114	–329
95	COM21/32	6114	–229
96	COM22/31	6114	–129
97	COM23/30	6114	–29
98	COM24/29	6114	71
99	COM25/28	6114	171
100	COM26/27	6114	271
101	COM47/6	6114	371
102	COM48/5	6114	471
103	COM49/4	6114	571
104	COM50/3	6114	671
105	COM51/2	6114	772
106	COM52/1	6114	872
107	COMS2/S1	6114	972
—	Dummy22	6165	1128
—	Dummy23	6165	1228
—	Dummy24	6165	1328
—	Dummy25	6165	1428
—	Dummy26	6165	1529
—	Dummy27	6165	1629
—	Dummy28	6165	1729

Pin No.	Pad Name	Coordinate X	Coordinate Y
—	Dummy29	6165	1829
—	Dummy30	6165	1929
108	SEG1/120	5955	1929
109	SEG2/119	5855	1929
110	SEG3/118	5755	1929
111	SEG4/117	5655	1929
112	SEG5/116	5554	1929
113	SEG6/115	5454	1929
114	SEG7/114	5354	1929
115	SEG8/113	5254	1929
116	SEG9/112	5154	1929
117	SEG10/111	5054	1929
118	SEG11/110	4954	1929
119	SEG12/109	4854	1929
120	SEG13/108	4754	1929
121	SEG14/107	4654	1929
122	SEG15/106	4554	1929
123	SEG16/105	4454	1929
124	SEG17/104	4353	1929
125	SEG18/103	4253	1929
126	SEG19/102	4153	1929
127	SEG20/101	4053	1929
128	SEG21/100	3953	1929
129	SEG22/99	3853	1929
130	SEG23/98	3753	1929
131	SEG24/97	3653	1929
132	SEG25/96	3553	1929
133	SEG26/95	3453	1929
134	SEG27/94	3353	1929
135	SEG28/93	3253	1929
136	SEG29/92	3153	1929
137	SEG30/91	3052	1929
138	SEG31/90	2952	1929
139	SEG32/89	2852	1929
140	SEG33/88	2752	1929
141	SEG34/87	2652	1929
142	SEG35/86	2552	1929
143	SEG36/85	2452	1929
144	SEG37/84	2352	1929
145	SEG38/83	2252	1929
146	SEG39/82	2152	1929
147	SEG40/81	2052	1929
148	SEG41/80	1952	1929
149	SEG42/79	1851	1929
150	SEG43/78	1751	1929
151	SEG44/77	1651	1929
152	SEG45/76	1551	1929
153	SEG46/75	1451	1929
154	SEG47/74	1351	1929
155	SEG48/73	1251	1929
156	SEG49/72	1151	1929
157	SEG50/71	1051	1929
158	SEG51/70	951	1929
159	SEG52/69	851	1929
160	SEG53/68	751	1929
161	SEG54/67	651	1929
162	SEG55/66	550	1929
163	SEG56/65	450	1929
164	SEG57/64	350	1929
165	SEG58/63	250	1929
166	SEG59/62	150	1929
167	SEG60/61	50	1929
168	SEG61/60	–50	1929
169	SEG62/59	–150	1929
170	SEG63/58	–250	1929
171	SEG64/57	–350	1929
172	SEG65/56	–450	1929
173	SEG66/55	–550	1929
174	SEG67/54	–651	1929
175	SEG68/53	–751	1929
176	SEG69/52	–851	1929
177	SEG70/51	–951	1929
178	SEG71/50	–1051	1929
179	SEG72/49	–1151	1929
180	SEG73/48	–1251	1929
181	SEG74/47	–1351	1929
182	SEG75/46	–1451	1929
193	SEG76/45	–1551	1929
184	SEG77/44	–1651	1929
185	SEG78/43	–1751	1929
186	SEG79/42	–1851	1929
187	SEG80/41	–1952	1929
188	SEG81/40	–2052	1929
189	SEG82/39	–2152	1929
190	SEG83/38	–2252	1929
191	SEG84/37	–2352	1929
192	SEG85/36	–2452	1929
193	SEG86/35	–2552	1929
194	SEG87/34	–2652	1929
195	SEG88/33	–2752	1929
196	SEG89/32	–2852	1929
197	SEG90/31	–2952	1929
198	SEG91/30	–3052	1929
199	SEG92/29	–3153	1929
200	SEG93/28	–3253	1929
201	SEG94/27	–3353	1929
202	SEG95/26	–3453	1929
203	SEG96/25	–3553	1929
204	SEG97/24	–3653	1929
205	SEG98/23	–3753	1929
206	SEG99/22	–3853	1929
207	SEG100/21	–3953	1929
208	SEG101/20	–4053	1929
209	SEG102/19	–4153	1929
210	SEG103/18	–4253	1929
211	SEG104/17	–4353	1929
212	SEG105/16	–4454	1929
213	SEG106/15	–4554	1929
214	SEG107/14	–4654	1929
215	SEG108/13	–4754	1929
216	SEG109/12	–4854	1929
217	SEG110/11	–4954	1929
218	SEG111/10	–5054	1929
219	SEG112/9	–5154	1929
220	SEG113/8	–5254	1929
221	SEG114/7	–5354	1929
222	SEG115/6	–5454	1929
223	SEG116/5	–5554	1929
224	SEG117/4	–5655	1929
225	SEG118/3	–5755	1929
226	SEG119/2	–5855	1929
227	SEG120/1	–5955	1929

TCP Dimensions (HD66732xxxTB0)



Pin Functions

Table 2 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM2, IM1	2	I	V_{CC} or GND	Selects the MPU interface mode: IM2 / IM1 / MPU interface mode "GND" / "GND" / Clock-synchronized serial interface "GND" / "Vcc" / 68-system parallel bus interface "Vcc" / "GND" / Setting inhibited "Vcc" / "Vcc" / 80-system parallel bus interface
IM0/ID	1	I	V_{CC} or GND	Inputs the ID of the device ID code for a serial bus interface. Selects the transfer bus length for a parallel bus interface. GND: 8-bit bus, Vcc: 4-bit bus
CS*	1	I	MPU	Selects the HD66732: Low: HD66732 is selected and can be accessed High: HD66732 is not selected and cannot be accessed Must be fixed at GND level when not in use.
RS	1	I	MPU	Selects the register for a parallel bus interface. Low: Instruction High: RAM access Selects the key scan interrupt method in the standby period for a serial interface. Monitors a total of eight keys connected to KST0 at the GND level and monitors all keys at the Vcc level to generate an interrupt. Must be fixed at the GND or Vcc level.
E/WR*/SCL	1	I	MPU	Inputs the serial transfer clock for a serial interface. Fetches data at the rising edge of a clock. For a 68-system parallel bus interface, serves as an enable signal to activate data read/write operation. For an 80-system parallel bus interface, serves as a write strobe signal and writes data at the low level.
RW/RD*/ SDA	1	I or I/O	MPU	Serves as the bidirectional serial transfer data for a serial interface. Sends/Receives data. For a 68-system parallel bus interface, serves as a signal to select data read/write operation. For an 80-system parallel bus interface, serves as a write strobe signal and reads data at the low level.
IRQ*	1	O	MPU	Generates the key scan interrupt signal.
KST0– KST3	4	O	Key matrix	Generates strobe signals for latching scanned data from the key matrix at specific time intervals. Available for a serial interface only.
DB0/KIN0– DB7/KIN7	8	I or I/O	Key matrix or MPU	Samples key state from key matrix synchronously with strobe signals for a serial interface. Serves as a bidirectional data bus for a parallel bus interface. For a 4-bit bus, data transfer uses KIN7/DB7-KIN4/DB4; leave KIN3/DB3-KIN0/DB0 disconnected.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
PORT0–PORT2	3	O	General output	General output ports. These ports cannot drive current such as for LEDs or backlighting control. Boost the current using an external transistor.
COMS1/2, COMS2/1	2	O	LCD	Common output signals for segment-icon display.
COM1/52–COM52/1	52	O	LCD	Common output signals for character/graphics display: COM1 to COM13 for the first line, COM14 to COM26 for the second line, COM27 to COM39 for the third line, and COM40 to COM52 for the fourth line. All the unused pins output unselected waveforms. In the sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1/52 is COM1. If CMS = 1, COM1/52 is COM52.
SEG1/120–SEG120/1	120	O	LCD	Segment output signals for segment-icon display and character/graphics display. In the sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, SEG1/120 is SEG1. If SGS = 1, SEG1/120 is SEG120.
V1OUT–V5OUT	10	I or O	Open or external bleeder-resistor	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = V_{CC}), V1 to V5 voltages can be supplied to these pins externally.
V_{LCD}	3	—	Power supply	Power supply for LCD drive. V_{LCD} – GND = 13 V max.
V_{CC}, GND	7	—	Power supply	V_{CC}: +2.4 V to +5.5 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Oscillation-resistor or clock	For R-C oscillation using an external resistor, connect an external resistor. For external clock supply, input clock pulses to OSC1.
Vci	3	I	Power supply	Inputs a reference voltage and supplies power to the booster; generates the liquid crystal display drive voltage from the operating voltage. Must be left disconnected when the booster is not used.
VLOUT	3	O	V_{LCD} pin/booster capacitance	Potential difference between Vci and GND is single- to quadruple-boosted and then output. Magnitude of boost is selected by instruction.
C1+, C1–	8	—	Booster capacitance	External capacitance should be connected here when using the double, triple, or quadruple booster.
C2+, C2–	8	—	Booster capacitance	External capacitance should be connected here when using the triple or quadruple booster.
C3+, C3–	8	—	Booster capacitance	External capacitance should be connected here when using the quadruple booster.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must be reset after power-on.
OPOFF	1	I	V_{CC} or GND	Turns the internal operational amplifier off when OPOFF = V_{CC}, and turns it on when OPOFF = GND. If the amplifier is turned off (OPOFF = V_{CC}), V1 to V5 must be supplied to the V1OUT to V5OUT pins.
VccDUM	1	O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM	1	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST1	1	I	Vcc or GND	Adjust the driving ability of the internal LCD operational amplifier. Normal drive mode in the GND side, and high-power drive mode in the Vcc side. Use the high-power drive mode when the display quality is insufficient although current consumption increases.
VTEST2	1	—	—	Test pin. Must be open.
VTEST3	1	I	Vcc or GND	Adjust the driving ability of the internal LCD operational amplifier. Normal drive mode or high-power drive mode in the GND side, and low-power drive mode in the Vcc side.

Block Function Description

System Interface

The HD66732 has five types of system interfaces, and a clock-synchronized serial interface, a 68-system 4-bit/8-bit bus, and a 80-system 4-bit/8-bit bus. The interface mode is selected by the IM2-0 pins. The key scan of the HD66732 is not available for the 4-bit/8-bit bus interface. Instead, use the clock-synchronized serial interface.

The HD66732 has five 8-bit registers: an index register (IR), a status register (SR), control registers, a RAM address register, and a RAM data register.

The IR specifies the index address of the register to be accessed. The SR reads the key scan data in the serial interface mode, and the internal states in the bus interface mode. Control registers (CNRs) set instructions such as clear display or display control. The RAM address register and RAM data register store the addresses or data of the display data RAM (DDRAM), character generator RAM (CGRAM), or segment RAM (SEGRAM).

Data written into the RAM data register from the MPU is automatically written into the DDRAM, CGRAM, or SEGRAM by internal operation. Data is read and temporarily latched in the RAM data register when reading from the RAM, and the first read data is invalid and the second data is normal. After reading, data in the DDRAM, CGRAM, or SEGRAM at the next address is sent to the RAM data register for the next reading from the MPU.

Execution time for instructions, excluding clear display, is 0 clock cycles and instructions can be written in succession.

Table 3 Register Selection by RS and R/W Bits

R/W Bits	RS Bits	Operations
0	0	Writes to the index register (IR)
1	0	Reads the status register (SR)
0	1	Writes to the control register, RAM address register, and RAM data register
1	1	Reads the RAM data register

Key Scan Registers (SCAN0 to SCAN3)

The key matrix scanner senses and holds the key states at each rising edge of the key strobe signals that are output by the HD66732. The key strobe signals are output as time-multiplexed signals from KST0 to KST3. After passing through the key matrix, these strobe signals are used to sample the key status on eight inputs from KIN0 to KIN7, enabling up to 32 keys to be scanned.

The states of inputs KIN0 to KIN7 are sampled by key strobe signal KST0 and latched into register SCAN0. Similarly, the data sampled by strobe signals KST1 to KST3 is latched into registers SCAN1 to SCAN3, respectively.

General Output Ports (PORT0 to PORT 2)

The HD66732 has three general output ports. These ports control drive current such as that for LEDs or backlighting by using the current boosted by an external transistor.

Address Counter (AC)

The address counter (AC) assigns addresses to the DDRAM, CGRAM, or SEGRAM. When an address is written into the RAM address register, the address information is sent to the AC. Selection of the DDRAM, CGRAM, and SEGRAM is also determined concurrently by the RAM select bit (RM1/0).

After writing data into DDRAM, CGRAM, or SEGRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading the data, the AC is automatically updated or not updated by the RDM bit. The cursor display position is determined by the address counter value.

Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes in the character display mode. Its capacity is 80 x 8 bits, or 80 characters, which is equivalent to an area of 10 characters x 4 lines. Any number of display lines (LCD drive duty ratio) from 1 to 4 can be selected by software. Here, assignment of DDRAM addresses is the same for all display modes. The line to be displayed at the top of the display (display-start line) can also be selected by register settings. The graphics display mode does not use data in the DDRAM.

Full-size Character Generator ROM (FCGROM)

Full-size character generator ROM (FCGROM) generates 11 x 12-dot character patterns from 13-bit character codes. It is equipped with 8,128 full-size font patterns such as the JIS Level-1 and Level-2 Kanji Set or non-Kanji Set. For the relationships between JIS codes and character codes to be set in the DDRAM, see the Combined Display of Full-size and Half-size Characters section.

Half-size Character Generator ROM (HCGROM)

Half-size character generator ROM (HCGROM) generates 6 x 12-dot character patterns from 7-bit character codes. It is equipped with two banks of 128 half-size font patterns, and 256 half-size fonts in total. For details, see the Combined Display of Full-size and Half-size Characters section and the Display Attribute Designation section.

Character Generator RAM (CGRAM)

Character generator RAM (CGRAM) allows the user to redefine the character patterns in the character display mode. Up to 40 character patterns of 12 x 13-dot characters can be simultaneously displayed. DRAM-specified character code can be selected to display one of these user font patterns.

The CGRAM serves as a RAM to store 120 x 52-dot bit pattern data in the graphics display mode. Here, display patterns are directly written into CGRAM. Character codes set in the DDRAM are not used. For details, see the Character Display Functions and Graphics Display Functions section.

Segment RAM (SEGRAM)

The segment RAM (SEGRAM) is used to enable control of segments such as icons and marks through the user program. Segments and characters are driven by a multiplexing drive method.

The SEGRAM has a capacity of 120 x 4 bits, and can control a display of up to 200 icon segments. Since 40 segments can be controlled by grayscale. While COMS1 and COMS2 outputs are being selected, 120 segments are driven. The 40 grayscale-controlled segments output the same display data in both the COMS1 drive and COMS2 drive modes.

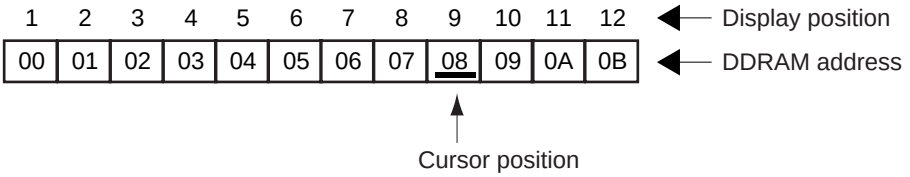
Bits in the SEGRAM corresponding to segments to be displayed are set directly by the MPU, regardless of the contents of the DDRAM and CGRAM.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as DDRAM, CGROM, CGRAM, and SEGRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another. This prevents flickering in areas other than the display area when writing data to DDRAM, for example.

Cursor/Blink Controller

The cursor/blink (or black-white reversed) control is used to create a cursor or a flashing area on the display in a position corresponding to the location stored in the address counter (AC).



Note: The cursor/blink or black-white reversed control is also active when the address counter indicates the CGRAM or SEGRAM. However, it has no effect on the display.

Figure 2 Cursor Position and DDRAM Address

Oscillation Circuit (OSC)

The HD66732 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 54 common signal drivers (COM1 to COM52, COMS1, and COMS2) and 120 segment signal drivers (SEG1 to SEG120). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output unselected waveforms.

Character pattern data is sent serially through a 120-bit shift register and latched when all needed data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs.

The shift direction of 120-bit data can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Booster (DC-DC Converter)

The booster doubles, triples, or quadruples a voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Boost output level from single to quadruple boost can be selected by software. For details, see the Power Supply for Liquid Crystal Display Drive section.

V-pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/2 bias to 1/8 bias, according to the liquid crystal display drive duty value. The voltage followers can be turned off while multiplexing drive is not being used. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 32 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

DDRAM Address Map

Table 4 DDRAM Addresses and Display Positions

Display Line	Display Character (Half Size)																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1st	**"00"**	**"01"**	**"02"**	**"03"**	**"04"**	**"05"**	**"06"**	**"07"**	**"08"**	**"09"**	**"0A"**	**"0B"**	**"0C"**	**"0D"**	**"0E"**	**"0F"**	**"10"**	**"11"**	**"12"**	**"13"**
2nd	**"20"**	**"21"**	**"22"**	**"23"**	**"24"**	**"25"**	**"26"**	**"27"**	**"28"**	**"29"**	**"2A"**	**"2B"**	**"2C"**	**"2D"**	**"2E"**	**"2F"**	**"30"**	**"31"**	**"32"**	**"33"**
3rd	**"40"**	**"41"**	**"42"**	**"43"**	**"44"**	**"45"**	**"46"**	**"47"**	**"48"**	**"49"**	**"4A"**	**"4B"**	**"4C"**	**"4D"**	**"4E"**	**"4F"**	**"50"**	**"51"**	**"52"**	**"53"**
4th	**"60"**	**"61"**	**"62"**	**"63"**	**"64"**	**"65"**	**"66"**	**"67"**	**"68"**	**"69"**	**"6A"**	**"6B"**	**"6C"**	**"6D"**	**"6E"**	**"6F"**	**"70"**	**"71"**	**"72"**	**"73"**

Note: When SGS = 0, SEG1/120 to SEG6/115 appear at the first character at the extreme left of the screen.
When SGS = 1, SEG120/1 to SEG115/6 appear at the first character at the extreme left of the screen.

Table 5 Display-line Modes, Display-start Line, and DDRAM Addresses

			Display-start Lines			
Display-line Mode	**Duty Ratio**	**Common Pins**	**1st Line (SN = 00)**	**2nd Line (SN = 01)**	**3rd Line (SN = 10)**	**4th Line (SN = 11)**
1-line (NL = 001)	1/15	COM1–COM13	00H–13H	20H–33H	40H–53H	60H–73H
2-line (NL = 010)	1/28	COM1–COM13	00H–13H	20H–33H	40H–53H	60H–73H
		COM14–COM26	20H–33H	40H–53H	60H–73H	00H–13H
3-line (NL = 011)	1/41	COM1–COM13	00H–13H	20H–33H	40H–53H	60H–73H
		COM14–COM26	20H–33H	40H–53H	60H–73H	00H–13H
		COM27–COM39	40H–53H	60H–73H	00H–13H	20H–33H
4-line (NL = 100)	1/54	COM1–COM13	00H–13H	20H–33H	40H–53H	60H–73H
		COM14–COM26	20H–33H	40H–53H	60H–73H	00H–13H
		COM27–COM39	40H–53H	60H–73H	00H–13H	20H–33H
		COM40–COM52	60H–73H	00H–13H	20H–33H	40H–53H

CGRAM Address Map

Table 6 Relationship between Character Code in Character Display Mode (GR = SPR = 0) and CGRAM Address

Character Code		"0000"	"0001"	"0002"	"0003"	"0004"	"0005"	"0006"	"0007"	"0008"	"0009"
CGRAM Address	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	000–00B	00C–017	018–023	024–02F	030–03B	03C–047	048–053	054–05F	060–06B	06C–077
	DB0 DB1 DB2 DB3 DB4	100–10B	10C–117	118–123	124–12F	130–13B	13C–147	148–153	154–15F	160–16B	16C–177

Character Code		"0010"	"0011"	"0012"	"0013"	"0014"	"0015"	"0016"	"0017"	"0018"	"0019"
CGRAM Address	DB5 DB6 DB7	100–10B	10C–117	118–123	124–12F	130–13B	13C–147	148–153	154–15F	160–16B	16C–177
	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	200–20B	20C–217	218–223	224–22F	230–23B	23C–247	248–253	254–25F	260–26B	26C–277
	DB0 DB1	300–30B	30C–317	318–323	324–32F	330–33B	33C–347	348–353	354–35F	360–36B	36C–377

Character Code		"1000"	"1001"	"1002"	"1003"	"1004"	"1005"	"1006"	"1007"	"1008"	"1009"
CGRAM Address	DB2 DB3 DB4 DB5 DB6 DB7	300–30B	30C–317	318–323	324–32F	330–33B	33C–347	348–353	354–35F	360–36B	36C–377
	DB0 DB1 DB2 DB3 DB4 DB5 DB6	400–40B	40C–417	418–423	424–42F	430–43B	43C–447	448–453	454–45F	460–46B	46C–477

Character Code		"1010"	"1011"	"1012"	"1013"	"1014"	"1015"	"1016"	"1017"	"1018"	"1019"
	DB7	400–40B	40C–417	418–423	424–42F	430–43B	43C–447	448–453	454–45F	460–46B	46C–477
CGRAM Address	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	500–50B	50C–517	518–523	524–52F	530–53B	53C–547	548–553	554–55F	560–56B	56C–577
	DB0 DB1 DB2 DB3	600–60B	60C–617	618–623	624–62F	630–63B	63C–647	648–653	654–65F	660–66B	66C–677

Notes: 1. In the character display mode (GR = SPR = 0), RM1/0 = 10 is set and CGRAM is used.
2. In the character display mode (GR = SPR = 0), the CGRAM font pattern is displayed using character codes set to the DDRAM as per the above table. In the graphics display mode (GR = 1 and SPR = 0) or super-imposed mode (SPR = 1), the CGRAM data is displayed irrespective of the DDRAM set data (character code).
3. The least significant bit (LSB) of the write data is displayed on the first line.
4. The 13th raster-row is the cursor position and its display is formed by a logical OR with the cursor.
5. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

Table 7 Relationship between Display Position and CGRAM Address in Graphics Display Mode (GR = 1, SPR = 0) and Super-imposed Display Mode (SPR = 1)

Segment Driver		SEG1/120	SEG2/119	SEG3/118	SEG4/117	SEG5/116	SEG6/115	SEG7/114	SEG8/113	SEG9/112	SEG10/111	SEG11/110	SEG12/109	SEG13/108	SEG14/107	SEG15/106	SEG16/105	SEG17/104	...	SEG116/5	SEG117/4	SEG118/3	SEG119/2	SEG120/1	Segment / Common
Address	SGS=0	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	...	073	074	075	076	077	(HEX)
	SGS=1	077	076	075	074	073	072	071	070	06F	06E	06D	06C	06B	06A	069	068	067	...	004	003	002	001	000	
	DB0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	...	0	0	1	0	0	COM1
	DB1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	...	0	1	1	0	0	COM2
	DB2	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	...	0	0	1	0	0	COM3
	DB3	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	0	1	0	0	COM4
	DB4	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	1	0	0	COM5
	DB5	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	1	0	0	COM6
	DB6	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	1	1	1	0	COM7
	DB7	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	0	0	0	COM8
Address	SGS=0	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	...	173	174	175	176	177	(HEX)
	SGS=1	177	176	175	174	173	172	171	170	16F	16E	16D	16C	16B	16A	169	168	167	...	104	103	102	101	100	
	DB0–DB7																								COM9–COM16
Address	SGS=0	200	201	202	203	204	205	206	207	208	209	20A	20B	20C	20D	20E	20F	210	...	273	274	275	276	277	(HEX)
	SGS=1	277	276	275	274	273	272	271	270	26F	26E	26D	26C	26B	26A	269	268	267	...	204	203	202	201	200	
	DB0–DB7																								COM17–COM24
Address	SGS=0	300	301	302	303	304	305	306	307	308	309	30A	30B	30C	30D	30E	30F	310	...	373	374	375	376	377	(HEX)
	SGS=1	377	376	375	374	373	372	371	370	36F	36E	36D	36C	36B	36A	369	368	367	...	304	303	302	301	300	
	DB0–DB7																								COM25–COM32
Address	SGS=0	400	401	402	403	404	405	406	407	408	409	40A	40B	40C	40D	40E	40F	410	...	473	474	475	476	477	(HEX)
	SGS=1	477	476	475	474	473	472	471	470	46F	46E	46D	46C	46B	46A	469	468	467	...	404	403	402	401	400	
	DB0–DB7																								COM33–COM40
Address	SGS=0	500	501	502	503	504	505	506	507	508	509	50A	50B	50C	50D	50E	50F	510	...	573	574	575	576	577	(HEX)
	SGS=1	577	576	575	574	573	572	571	570	56F	56E	56D	56C	56B	56A	569	568	567	...	504	503	502	501	500	
	DB0–DB7																								COM41–COM48
Address	SGS=0	600	601	602	603	604	605	606	607	608	609	60A	60B	60C	60D	60E	60F	610	...	673	674	675	676	677	(HEX)
	SGS=1	677	676	675	674	673	672	671	670	66F	66E	66D	66C	66B	66A	669	668	667	...	604	603	602	601	600	
	DB0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	COM49
	DB1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	COM50
	DB2	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	COM51
	DB3	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	COM52

Notes: 1. When the RM1/0 bit is set to "10", the CGRAM can be selected.
2. In the graphics display mode (GR = 1 and SPR = 0) and super-imposed display mode (SPR = 1), the CGRAM data is displayed irrespective of the DDRAM set data.
3. Writing to the upper four bits (DB4–DB7) in CGRAM addresses 600H–677H is invalid.
4. A set bit in CGRAM 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

SEGRAM Address Map

Table 8 Relationship between SEGRAM Address and Screen Display Position

Segment Driver		SEG1/120	SEG2/119	SEG3/118	SEG4/117	SEG5/116	SEG6/115	SEG7/114	SEG8/113	SEG9/112	SEG10/111	SEG11/110	SEG12/109	SEG13/108	SEG14/107	SEG15/106	SEG16/105	SEG17/104	---	SEG116/5	SEG117/4	SEG118/3	SEG119/2	SEG120/1	Segment / Common
Address	SGS=0	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	---	073	074	075	076	077	(HEX)
	SGS=1	077	076	075	074	073	072	071	070	06F	06E	06D	06C	06B	06A	069	068	067	---	004	003	002	001	000	
	DB0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	---	*	*	*	*	*	
	DB1	*	*	*	*	*	*	*	*	(Invalid area)					*	*	*	*	---	*	*	*	*	*	
	DB2	*	*	*	*	*	*	*	*						*	*	*	*	---	*	*	*	*	*	
	DB3	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	---	*	*	*	*	*	
	DB4	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	---	0/1	0/1	0/1	0/1	0/1	COMS1
	DB5	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	---	0/1	0/1	0/1	0/1	0/1	
	DB6	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	---	0/1	0/1	0/1	0/1	0/1	COMS2
	DB7	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	---	0/1	0/1	0/1	0/1	0/1	

Notes: 1. When the RM1/0 bit is set to "11", the SEGRAM can be selected.
2. Writing to the lower four bits (DB0–DB3) in the SEGRAM is invalid.
3. The segment output that can be controlled by grayscale is enabled for only the 40 segments (table 9). These grayscale-controlled segments are driven by the same grayscale data at COMS1 and COMS2 selection.
4. Other outputs than the grayscale-controlled segment outputs can control segment on/off and blinking. The COMS1 and COMS2 outputs are independently controlled.

Table 9 Relationship between Segment Driver Output Pin and Segment Display Function

When SGS = 0	When SGS = 1	Remarks
SEG1/120, SEG4/117, SEG7/114, SEG10/111, SEG13/108, SEG16/105, SEG19/102, SEG22/99, SEG25/96, SEG28/93, SEG31/90, SEG34/87, SEG37/84, SEG40/81, SEG43/78, SEG46/75, SEG49/72, SEG52/69, SEG55/66, SEG58/63, SEG61/60, SEG64/57, SEG67/54, SEG70/51, SEG73/48, SEG76/45, SEG79/42, SEG82/39, SEG85/36, SEG88/33, SEG91/30, SEG94/27, SEG97/24, SEG100/21, SEG103/18, SEG106/15, SEG109/12, SEG112/9, SEG115/6, SEG118/3	SEG120/1, SEG117/4, SEG114/7, SEG111/10, SEG108/13, SEG105/16, SEG102/19, SEG99/22, SEG96/25, SEG93/28, SEG90/31, SEG87/34, SEG84/37, SEG81/40, SEG78/43, SEG75/46, SEG72/49, SEG69/52, SEG66/55, SEG63/58, SEG60/61, SEG57/64, SEG54/67, SEG51/70, SEG48/73, SEG45/76, SEG42/79, SEG39/82, SEG36/85, SEG33/88, SEG30/91, SEG27/94, SEG24/97, SEG21/100, SEG18/103, SEG15/106, SEG12/109, SEG9/112, SEG6/115, SEG3/118	The COMS1 and COMS2 outputs are controlled by the same grayscale. Total: 40 segments
Output pins other than above	Output pins other than above	The COMS1 and COMS2 outputs are independently controlled. Total: 80 x 2 = 160 segments

Table 10 Relationship between SEGRAM Data and Grayscale-Controlled Segment Display

SEGRAM Data				
DB7	**DB6**	**DB5**	**DB4**	**Effective Applied Voltage for COMS1 and COMS2 Output**
0	0	0	0	0 (Always unlit)
0	0	0	1	1 (Always lit)
0	0	1	0	0.34 (Grayscale display)
0	0	1	1	0.38 (Grayscale display)
0	1	0	0	0.41 (Grayscale display)
0	1	0	1	0.44 (Grayscale display)
0	1	1	0	0.47 (Grayscale display)
0	1	1	1	0.50 (Grayscale display)
1	0	0	0	(Blink display)*
1	0	0	1	0.53 (Grayscale display)
1	0	1	0	0.56 (Grayscale display)
1	0	1	1	0.59 (Grayscale display)
1	1	0	0	0.63 (Grayscale display)
1	1	0	1	0.66 (Grayscale display)
1	1	1	0	0.69 (Grayscale display)
1	1	1	1	0.72 (Grayscale display)

Notes: 1. For details, see the Reflective Color Mark/Blink Mark Display section.
2. Blinking is provided by repeatedly turning on the segment for 32 frames and turning it off for the next 32 frames.

Table 11 Relationship between SEGRAM Data and Blinking Segment Display (1)

SEGRAM Data		
DB5	**DB4**	**LCD Display Control for COMS1 Segment**
0	0	Always unlit
0	1	Always lit
1	0	Blinking display (32-frame unit)
1	1	Double-speed blinking display (16-frame unit)

Table 12 Relationship between SEGRAM Data and Blinking Segment Display (2)

SEGRAM Data		
DB7	**DB6**	**LCD Display Control for COMS2 Segment**
0	0	Always unlit
0	1	Always lit
1	0	Blinking display (32-frame unit)
1	1	Double-speed blinking display (16-frame unit)

Table 13 HD66732 Full-size Character Codes and JIS Codes (Level-1, Non-kanji)

Character Code	JIS Code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	[300]	For CGRAM (0000–0009)										Shares for CGRAM					
001	[301]	For CGRAM (0010–0019)															
002	302		亜	唖	娃	阿	哀	愛	挨	姶	逢	葵	茜	穐	悪	握	渥
003	303	旭	葦	芦	鯵	梓	圧	斡	扱	宛	姐	虻	飴	絢	綾	鮎	或
004	304	粟	袷	安	庵	按	暗	案	闇	鞍	杏	以	伊	位	依	偉	囲
005	305	夷	委	威	尉	惟	意	慰	易	椅	為	畏	異	移	維	緯	胃
006	306	萎	衣	謂	違	遺	医	井	亥	域	育	郁	磯	一	壱	溢	逸
007	307	稲	茨	芋	鰯	允	印	咽	員	因	姻	引	飲	淫	胤	蔭	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
008	[310]																
009	[311]																
00A	312		院	陰	隠	韻	吋	右	宇	烏	羽	迂	雨	卯	鶯	窺	丑
00B	313	碓	臼	渦	嘘	唄	欝	蔚	鰻	姥	厩	浦	瓜	閏	噂	云	運
00C	314	雲	荏	餌	叡	営	嬰	影	映	曳	栄	永	泳	洩	瑛	盈	穎
00D	315	頴	英	衛	詠	鋭	液	疫	益	駅	悦	謁	越	閲	榎	厭	円
00E	316	園	堰	奄	宴	延	怨	掩	援	沿	演	炎	焔	煙	燕	猿	縁
00F	317	艶	苑	薗	遠	鉛	鴛	塩	於	汚	甥	凹	央	奥	往	応	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
010	[320]																
011	[321]																
012	322		押	旺	横	欧	殴	王	翁	襖	鴬	鴎	黄	岡	沖	荻	億
013	323	屋	憶	臆	桶	牡	乙	俺	卸	恩	温	穏	音	下	化	仮	何
014	324	伽	価	佳	加	可	嘉	夏	嫁	家	寡	科	暇	果	架	歌	河
015	325	火	珂	禍	禾	稼	箇	花	苛	茄	荷	華	菓	蝦	課	嘩	貨
016	326	迦	過	霞	蚊	俄	峨	我	牙	画	臥	芽	蛾	賀	雅	餓	駕
017	327	介	会	解	回	塊	壊	廻	快	怪	悔	恢	懐	戒	拐	改	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
018	[330]																
019	[331]																
01A	332		魁	晦	械	海	灰	界	皆	絵	芥	蟹	開	階	貝	凱	劾
01B	333	外	咳	害	崖	慨	概	涯	碍	蓋	街	該	鎧	骸	浬	馨	蛙
01C	334	垣	柿	蛎	鈎	劃	嚇	各	廓	拡	撹	格	核	殻	獲	確	穫
01D	335	覚	角	赫	較	郭	閣	隔	革	学	岳	楽	額	顎	掛	笠	樫
01E	336	橿	梶	鰍	潟	割	喝	恰	括	活	渇	滑	葛	褐	轄	且	鰹
01F	337	叶	椛	樺	鞄	株	兜	竈	蒲	釜	鎌	噛	鴨	栢	茅	萱	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
020	[340]																
021	[341]																
022	342		粥	刈	苅	瓦	乾	侃	冠	寒	刊	勘	勧	巻	喚	堪	姦
023	343	完	官	寛	干	幹	患	感	慣	憾	換	敢	柑	桓	棺	款	歓
024	344	汗	漢	澗	潅	環	甘	監	看	竿	管	簡	緩	缶	翰	肝	艦
025	345	莞	観	諌	貫	還	鑑	間	閑	関	陥	韓	館	舘	丸	含	岸
026	346	巌	玩	癌	眼	岩	翫	贋	雁	頑	顔	願	企	伎	危	喜	器
027	347	基	奇	嬉	寄	岐	希	幾	忌	揮	机	旗	既	期	棋	棄	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
028	[350]																
029	[351]																
02A	352		機	帰	毅	気	汽	畿	祈	季	稀	紀	徽	規	記	貴	起
02B	353	軌	輝	飢	騎	鬼	亀	偽	儀	妓	宜	戯	技	擬	欺	犠	疑
02C	354	祇	義	蟻	誼	議	掬	菊	鞠	吉	吃	喫	桔	橘	詰	砧	杵
02D	355	黍	却	客	脚	虐	逆	丘	久	仇	休	及	吸	宮	弓	急	救
02E	356	朽	求	汲	泣	灸	球	究	窮	笈	級	糾	給	旧	牛	去	居
02F	357	巨	拒	拠	挙	渠	虚	許	距	鋸	漁	禦	魚	亨	享	京	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
030	[360]																
031	[361]																
032	362		供	侠	僑	兇	競	共	凶	協	匡	卿	叫	喬	境	峡	強
033	363	彊	怯	恐	恭	挟	教	橋	況	狂	狭	矯	胸	脅	興	蕎	郷
034	364	鏡	響	饗	驚	仰	凝	尭	暁	業	局	曲	極	玉	桐	粁	僅
035	365	勤	均	巾	錦	斤	欣	欽	琴	禁	禽	筋	緊	芹	菌	衿	襟
036	366	謹	近	金	吟	銀	九	倶	句	区	狗	玖	矩	苦	躯	駆	駈
037	367	駒	具	愚	虞	喰	空	偶	寓	遇	隅	串	櫛	釧	屑	屈	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
038	[370]																
039	[371]																
03A	372		掘	窟	沓	靴	轡	窪	熊	隈	粂	栗	繰	桑	鍬	勲	君
03B	373	薫	訓	群	軍	郡	卦	袈	祁	係	傾	刑	兄	啓	圭	珪	型
03C	374	契	形	径	恵	慶	慧	憩	掲	携	敬	景	桂	渓	畦	稽	系
03D	375	経	継	繋	罫	茎	荊	蛍	計	詣	警	軽	頚	鶏	芸	迎	鯨
03E	376	劇	戟	撃	激	隙	桁	傑	欠	決	潔	穴	結	血	訣	月	件
03F	377	倹	倦	健	兼	券	剣	喧	圏	堅	嫌	建	憲	懸	拳	捲	

No CGROMs
(Cannot be used as CGROMs.)

- XXX : Not allocated to JIS codes.
  (Do not correspond to JIS codes.)
  Can be used as CGROMs.
- The following JIS codes cannot be used:
  (They overlap with the character codes for non-kanji JIS codes 2120–287F.)

Unavailable JIS codes (non-kanji: 2920–2F7F):
- 2920–297F
- 2A20–2A7F
- 2B20–2B7F
- 2C20–2C7F
- 2D20–2D7F
- 2E20–2E7F
- 2F20–2F7F

Character Code	JIS Code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
040	282		─	│	┌	┐	┘	└	├	┬	┤	┴	┼	━	┃	┏	┓
041	283	┛	┗	┣	┳	┫	┻	╋	┠	┯	┨	┷	┿	┝	┰	┥	┸
042	382		検	権	牽	犬	献	研	硯	絹	県	肩	見	謙	賢	軒	遣
043	383	鍵	険	顕	験	鹸	元	原	厳	幻	弦	減	源	玄	現	絃	舷
044	384	言	諺	限	乎	個	古	呼	固	姑	孤	己	庫	弧	戸	故	枯
045	385	湖	狐	糊	袴	股	胡	菰	虎	誇	跨	鈷	雇	顧	鼓	五	互
046	386	伍	午	呉	吾	娯	後	御	悟	梧	檎	瑚	碁	語	誤	護	醐
047	387	乞	鯉	交	佼	侯	候	倖	光	公	功	効	勾	厚	口	向	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
048	212			、	。	，	．	・	：	；	？	！	゛	゜	´	｀	¨
049	213	＾	￣	＿	ヽ	ヾ	ゝ	ゞ	〃	仝	々	〆	〇	ー	―	‐	／
04A	392		后	喉	坑	垢	好	孔	孝	宏	工	巧	巷	幸	広	庚	康
04B	393	弘	恒	慌	抗	拘	控	攻	昂	晃	更	杭	校	梗	構	江	洪
04C	394	浩	港	溝	甲	皇	硬	稿	糠	紅	紘	絞	綱	耕	考	肯	肱
04D	395	腔	膏	航	荒	行	衡	講	貢	購	郊	酵	鉱	砿	鋼	閤	降
04E	396	項	香	高	鴻	剛	劫	号	合	壕	拷	濠	豪	轟	麹	克	刻
04F	397	告	国	穀	酷	鵠	黒	獄	漉	腰	甑	忽	惚	骨	狛	込	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
050	222		◆	□	■	△	▲	▽	▼	※	〒	→	←	↑	↓	〓	
051	223											∈	∋	⊆	⊇	⊂	⊃
052	3A2		此	頃	今	困	坤	墾	婚	恨	懇	昏	昆	根	梱	混	痕
053	3A3	紺	艮	魂	些	佐	叉	唆	嵯	左	差	査	沙	瑳	砂	詐	鎖
054	3A4	裟	坐	座	挫	債	催	再	最	哉	塞	妻	宰	彩	才	採	栽
055	3A5	歳	済	災	采	犀	砕	砦	祭	斎	細	菜	裁	載	際	剤	在
056	3A6	材	罪	財	冴	坂	阪	堺	榊	肴	咲	崎	埼	碕	鷺	作	削
057	3A7	咋	搾	昨	朔	柵	窄	策	索	錯	桜	鮭	笹	匙	冊	刷	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
058	232																
059	233	０	１	２	３	４	５	６	７	８	９						
05A	3B2		察	拶	撮	擦	札	殺	薩	雑	皐	鯖	捌	錆	鮫	皿	晒
05B	3B3	三	傘	参	山	惨	撒	散	桟	燦	珊	産	算	纂	蚕	讃	賛
05C	3B4	酸	餐	斬	暫	残	仕	仔	伺	使	刺	司	史	嗣	四	士	始
05D	3B5	姉	姿	子	屍	市	師	志	思	指	支	孜	斯	施	旨	枝	止
05E	3B6	死	氏	獅	祉	私	糸	紙	紫	肢	脂	至	視	詞	詩	試	誌
05F	3B7	諮	資	賜	雌	飼	歯	事	似	侍	児	字	寺	慈	持	時	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
060	242		ぁ	あ	ぃ	い	ぅ	う	ぇ	え	ぉ	お	か	が	き	ぎ	く
061	243	ぐ	け	げ	こ	ご	さ	ざ	し	じ	す	ず	せ	ぜ	そ	ぞ	た
062	3C2		次	滋	治	爾	璽	痔	磁	示	而	耳	自	蒔	辞	汐	鹿
063	3C3	式	識	鴫	竺	軸	宍	雫	七	叱	執	失	嫉	室	悉	湿	漆
064	3C4	疾	質	実	蔀	篠	偲	柴	芝	屡	蕊	縞	舎	写	射	捨	赦
065	3C5	斜	煮	社	紗	者	謝	車	遮	蛇	邪	借	勺	尺	杓	灼	爵
066	3C6	酌	釈	錫	若	寂	弱	惹	主	取	守	手	朱	殊	狩	珠	種
067	3C7	腫	趣	酒	首	儒	受	呪	寿	授	樹	綬	需	囚	収	周	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
068	252		ァ	ア	ィ	イ	ゥ	ウ	ェ	エ	ォ	オ	カ	ガ	キ	ギ	ク
069	253	グ	ケ	ゲ	コ	ゴ	サ	ザ	シ	ジ	ス	ズ	セ	ゼ	ソ	ゾ	タ
06A	3D2		宗	就	州	修	愁	拾	洲	秀	秋	終	繍	習	臭	舟	蒐
06B	3D3	衆	襲	讐	蹴	輯	週	酋	酬	集	醜	什	住	充	十	従	戎
06C	3D4	柔	汁	渋	獣	縦	重	銃	叔	夙	宿	淑	祝	縮	粛	塾	熟
06D	3D5	出	術	述	俊	峻	春	瞬	竣	舜	駿	准	循	旬	楯	殉	淳
06E	3D6	準	潤	盾	純	巡	遵	醇	順	処	初	所	暑	曙	渚	庶	緒
06F	3D7	署	書	薯	藷	諸	助	叙	女	序	徐	恕	鋤	除	傷	償	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
070	262		Α	Β	Γ	Δ	Ε	Ζ	Η	Θ	Ι	Κ	Λ	Μ	Ν	Ξ	Ο
071	263	Π	Ρ	Σ	Τ	Υ	Φ	Χ	Ψ	Ω							
072	3E2		勝	匠	升	召	哨	商	唱	嘗	奨	妾	娼	宵	将	小	少
073	3E3	尚	庄	床	廠	彰	承	抄	招	掌	捷	昇	昌	昭	晶	松	梢
074	3E4	樟	樵	沼	消	渉	湘	焼	焦	照	症	省	硝	礁	祥	称	章
075	3E5	笑	粧	紹	肖	菖	蒋	蕉	衝	裳	訟	証	詔	詳	象	賞	醤
076	3E6	鉦	鍾	鐘	障	鞘	上	丈	丞	乗	冗	剰	城	場	壌	嬢	常
077	3E7	情	擾	条	杖	浄	状	畳	穣	蒸	譲	醸	錠	嘱	埴	飾	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
078	272		А	Б	В	Г	Д	Е	Ё	Ж	З	И	Й	К	Л	М	Н
079	273	О	П	Р	С	Т	У	Ф	Х	Ц	Ч	Ш	Щ	Ъ	Ы	Ь	Э
07A	3F2		拭	植	殖	燭	織	職	色	触	食	蝕	辱	尻	伸	信	侵
07B	3F3	唇	娠	寝	審	心	慎	振	新	晋	森	榛	浸	深	申	疹	真
07C	3F4	神	秦	紳	臣	芯	薪	親	診	身	辛	進	針	震	人	仁	刃
07D	3F5	塵	壬	尋	甚	尽	腎	訊	迅	陣	靭	笥	諏	須	酢	図	厨
07E	3F6	逗	吹	垂	帥	推	水	炊	睡	粋	翠	衰	遂	酔	錐	錘	随
07F	3F7	瑞	髄	崇	嵩	数	枢	趨	雛	据	杉	椙	菅	頗	雀	裾	

Character Code	JIS Code	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
080	284	╂															
081	285																
082	402		澄	摺	寸	世	瀬	畝	是	凄	制	勢	姓	征	性	成	政
083	403	整	星	晴	棲	栖	正	清	牲	生	盛	精	聖	声	製	西	誠
084	404	誓	請	逝	醒	青	静	斉	税	脆	隻	席	惜	戚	斥	昔	析
085	405	石	積	籍	績	脊	責	赤	跡	蹟	碩	切	拙	接	摂	折	設
086	406	窃	節	説	雪	絶	舌	蝉	仙	先	千	占	宣	専	尖	川	戦
087	407	扇	撰	栓	栴	泉	浅	洗	染	潜	煎	煽	旋	穿	箭	線	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
088	214	＼	～	∥	｜	…	‥	‘	’	“	”	（	）	〔	〕	［	］
089	215	｛	｝	〈	〉	《	》	「	」	『	』	【	】	＋	－	±	×
08A	412		繊	羨	腺	舛	船	薦	詮	賎	践	選	遷	銭	銑	閃	鮮
08B	413	前	善	漸	然	全	禅	繕	膳	糎	噌	塑	岨	措	曾	曽	楚
08C	414	狙	疏	疎	礎	祖	租	粗	素	組	蘇	訴	阻	遡	鼠	僧	創
08D	415	双	叢	倉	喪	壮	奏	爽	宋	層	匝	惣	想	捜	掃	挿	掻
08E	416	操	早	曹	巣	槍	槽	漕	燥	争	痩	相	窓	糟	総	綜	聡
08F	417	草	荘	葬	蒼	藻	装	走	送	遭	鎗	霜	騒	像	増	憎	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
090	224	∪	∩									∧	∨	¬	⇒	⇔	∀
091	225	∃												∠	⊥		∂
092	422		臓	蔵	贈	造	促	側	則	即	息	捉	束	測	足	速	俗
093	423	属	賊	族	続	卒	袖	其	揃	存	孫	尊	損	村	遜	他	多
094	424	太	汰	詑	唾	堕	妥	惰	打	柁	舵	楕	陀	駄	騨	体	堆
095	425	対	耐	岱	帯	待	怠	態	戴	替	泰	滞	胎	腿	苔	袋	貸
096	426	退	逮	隊	黛	鯛	代	台	大	第	醍	題	鷹	滝	瀧	卓	啄
097	427	宅	托	択	拓	沢	濯	琢	託	鐸	濁	諾	茸	凧	蛸	只	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
098	234		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
099	235	P	Q	R	S	T	U	V	W	X	Y	Z					
09A	432		叩	但	達	辰	奪	脱	巽	竪	辿	棚	谷	狸	鱈	樽	誰
09B	433	丹	単	嘆	坦	担	探	旦	歎	淡	湛	炭	短	端	箪	綻	耽
09C	434	胆	蛋	誕	鍛	団	壇	弾	断	暖	檀	段	男	談	値	知	地
09D	435	弛	恥	智	池	痴	稚	置	致	蜘	遅	馳	築	畜	竹	筑	蓄
09E	436	逐	秩	窒	茶	嫡	着	中	仲	宙	忠	抽	昼	柱	注	虫	衷
09F	437	註	酎	鋳	駐	樗	瀦	猪	苧	著	貯	丁	兆	凋	喋	寵	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0A0	244	だ	ち	ぢ	っ	つ	づ	て	で	と	ど	な	に	ぬ	ね	の	は
0A1	245	ば	ぱ	ひ	び	ぴ	ふ	ぶ	ぷ	へ	べ	ぺ	ほ	ぼ	ぽ	ま	み
0A2	442		帖	帳	庁	弔	張	彫	徴	懲	挑	暢	朝	潮	牒	町	眺
0A3	443	聴	脹	腸	蝶	調	諜	超	跳	銚	長	頂	鳥	勅	捗	直	朕
0A4	444	沈	珍	賃	鎮	陳	津	墜	椎	槌	追	鎚	痛	通	塚	栂	掴
0A5	445	槻	佃	漬	柘	辻	蔦	綴	鍔	椿	潰	坪	壷	嬬	紬	爪	吊
0A6	446	釣	鶴	亭	低	停	偵	剃	貞	呈	堤	定	帝	底	庭	廷	弟
0A7	447	悌	抵	挺	提	梯	汀	碇	禎	程	締	艇	訂	諦	蹄	逓	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0A8	254	ダ	チ	ヂ	ッ	ツ	ヅ	テ	デ	ト	ド	ナ	ニ	ヌ	ネ	ノ	ハ
0A9	255	バ	パ	ヒ	ビ	ピ	フ	ブ	プ	ヘ	ベ	ペ	ホ	ボ	ポ	マ	ミ
0AA	452		邸	鄭	釘	鼎	泥	摘	擢	敵	滴	的	笛	適	鏑	溺	哲
0AB	453	徹	撤	轍	迭	鉄	典	填	天	展	店	添	纏	甜	貼	転	顛
0AC	454	点	伝	殿	澱	田	電	兎	吐	堵	塗	妬	屠	徒	斗	杜	渡
0AD	455	登	菟	賭	途	都	鍍	砥	砺	努	度	土	奴	怒	倒	党	冬
0AE	456	凍	刀	唐	塔	塘	套	宕	島	嶋	悼	投	搭	東	桃	梼	棟
0AF	457	盗	淘	湯	涛	灯	燈	当	痘	祷	等	答	筒	糖	統	到	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0B0	264		α	β	γ	δ	ε	ζ	η	θ	ι	κ	λ	μ	ν	ξ	ο
0B1	265	π	ρ	σ	τ	υ	φ	χ	ψ	ω							
0B2	462		董	蕩	藤	討	謄	豆	踏	逃	透	鐙	陶	頭	騰	闘	働
0B3	463	動	同	堂	導	憧	撞	洞	瞳	童	胴	萄	道	銅	峠	鴇	匿
0B4	464	得	徳	涜	特	督	禿	篤	毒	独	読	栃	橡	凸	突	椴	届
0B5	465	鳶	苫	寅	酉	瀞	噸	屯	惇	敦	沌	豚	遁	頓	呑	曇	鈍
0B6	466	奈	那	内	乍	凪	薙	謎	灘	捺	鍋	楢	馴	縄	畷	南	楠
0B7	467	軟	難	汝	二	尼	弐	迩	匂	賑	肉	虹	廿	日	乳	入	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0B8	274	Ю	Я														
0B9	275		а	б	в	г	д	е	ё	ж	з	и	й	к	л	м	н
0BA	472		如	尿	韮	任	妊	忍	認	濡	禰	祢	寧	葱	猫	熱	年
0BB	473	念	捻	撚	燃	粘	乃	廼	之	埜	嚢	悩	濃	納	能	脳	膿
0BC	474	農	覗	蚤	巴	把	播	覇	杷	波	派	琶	破	婆	罵	芭	馬
0BD	475	俳	廃	拝	排	敗	杯	盃	牌	背	肺	輩	配	倍	培	媒	梅
0BE	476	楳	煤	狽	買	売	賠	陪	這	蝿	秤	矧	萩	伯	剥	博	拍
0BF	477	柏	泊	白	箔	粕	舶	薄	迫	曝	漠	爆	縛	莫	駁	麦	

Character Code	JIS Code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0C0	**286**																
0C1	**287**																
0C2	482		函	箱	硲	箸	肇	筈	櫨	幡	肌	畑	畠	八	鉢	溌	発
0C3	483	醗	髪	伐	罰	抜	筏	閥	鳩	噺	塙	蛤	隼	伴	判	半	反
0C4	484	叛	帆	搬	斑	板	氾	汎	版	犯	班	畔	繁	般	藩	販	範
0C5	485	釆	煩	頒	飯	挽	晩	番	盤	磐	蕃	蛮	匪	卑	否	妃	庇
0C6	486	彼	悲	扉	批	披	斐	比	泌	疲	皮	碑	秘	緋	罷	肥	被
0C7	487	誹	費	避	非	飛	樋	簸	備	尾	微	枇	毘	琵	眉	美	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0C8	**216**	÷	=	≠	<	>	≦	≧	∞	∴	♂	♀	°	′	″	℃	¥
0C9	**217**	$	¢	£	%	#	&	*	@	§	☆	★	○	●	◎	◇	
0CA	492		鼻	柊	稗	匹	疋	髭	彦	膝	菱	肘	弼	必	畢	筆	逼
0CB	493	桧	姫	媛	紐	百	謬	俵	彪	標	氷	漂	瓢	票	表	評	豹
0CC	494	廟	描	病	秒	苗	錨	鋲	蒜	蛭	鰭	品	彬	斌	浜	瀕	貧
0CD	495	賓	頻	敏	瓶	不	付	埠	夫	婦	富	冨	布	府	怖	扶	敷
0CE	496	斧	普	浮	父	符	腐	膚	芙	譜	負	賦	赴	阜	附	侮	撫
0CF	497	武	舞	葡	蕪	部	封	楓	風	葺	蕗	伏	副	復	幅	服	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0D0	**226**	∇	≡	≒	≪	≫	√	∽	∝	∵	∫	∬					
0D1	**227**			Å	‰	♯	♭	♪	†	‡	¶					◯	
0D2	4A2		福	腹	複	覆	淵	弗	払	沸	仏	物	鮒	分	吻	噴	墳
0D3	4A3	憤	扮	焚	奮	粉	糞	紛	雰	文	聞	丙	併	兵	塀	幣	平
0D4	4A4	弊	柄	並	蔽	閉	陛	米	頁	僻	壁	癖	碧	別	瞥	蔑	箆
0D5	4A5	偏	変	片	篇	編	辺	返	遍	便	勉	娩	弁	鞭	保	舗	鋪
0D6	4A6	圃	捕	歩	甫	補	輔	穂	募	墓	慕	戊	暮	母	簿	菩	倣
0D7	4A7	俸	包	呆	報	奉	宝	峰	峯	崩	庖	抱	捧	放	方	朋	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0D8	**236**		a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
0D9	**237**	p	q	r	s	t	u	v	w	x	y	z					
0DA	4B2		法	泡	烹	砲	縫	胞	芳	萌	蓬	蜂	褒	訪	豊	邦	鋒
0DB	4B3	飽	鳳	鵬	乏	亡	傍	剖	坊	妨	帽	忘	忙	房	暴	望	某
0DC	4B4	棒	冒	紡	肪	膨	謀	貌	貿	鉾	防	吠	頬	北	僕	卜	墨
0DD	4B5	撲	朴	牧	睦	穆	釦	勃	没	殆	堀	幌	奔	本	翻	凡	盆
0DE	4B6	摩	磨	魔	麻	埋	妹	昧	枚	毎	哩	槙	幕	膜	枕	鮪	柾
0DF	4B7	鱒	桝	亦	俣	又	抹	末	沫	迄	侭	繭	麿	万	慢	満	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0E0	**246**	む	め	も	ゃ	や	ゅ	ゆ	ょ	よ	ら	り	る	れ	ろ	ゎ	わ
0E1	**247**	ゐ	ゑ	を	ん												
0E2	4C2		漫	蔓	味	未	魅	巳	箕	岬	密	蜜	湊	蓑	稔	脈	妙
0E3	4C3	粍	民	眠	務	夢	無	牟	矛	霧	鵡	椋	婿	娘	冥	名	命
0E4	4C4	明	盟	迷	銘	鳴	姪	牝	滅	免	棉	綿	緬	面	麺	摸	模
0E5	4C5	茂	妄	孟	毛	猛	盲	網	耗	蒙	儲	木	黙	目	杢	勿	餅
0E6	4C6	尤	戻	籾	貰	問	悶	紋	門	匁	也	冶	夜	爺	耶	野	弥
0E7	4C7	矢	厄	役	約	薬	訳	躍	靖	柳	薮	鑓	愉	愈	油	癒	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0E8	**256**	ム	メ	モ	ャ	ヤ	ュ	ユ	ョ	ヨ	ラ	リ	ル	レ	ロ	ヮ	ワ
0E9	**257**	ヰ	ヱ	ヲ	ン	ヴ	ヵ	ヶ									
0EA	4D2		諭	輸	唯	佑	優	勇	友	宥	幽	悠	憂	揖	有	柚	湧
0EB	4D3	涌	猶	猷	由	祐	裕	誘	遊	邑	郵	雄	融	夕	予	余	与
0EC	4D4	誉	輿	預	傭	幼	妖	容	庸	揚	揺	擁	曜	楊	様	洋	溶
0ED	4D5	熔	用	窯	羊	耀	葉	蓉	要	謡	踊	遥	陽	養	慾	抑	欲
0EE	4D6	沃	浴	翌	翼	淀	羅	螺	裸	来	莱	頼	雷	洛	絡	落	酪
0EF	4D7	乱	卵	嵐	欄	濫	藍	蘭	覧	利	吏	履	李	梨	理	璃	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0F0	**266**																
0F1	**267**																
0F2	4E2		痢	裏	裡	里	離	陸	律	率	立	葎	掠	略	劉	流	溜
0F3	4E3	琉	留	硫	粒	隆	竜	龍	侶	慮	旅	虜	了	亮	僚	両	凌
0F4	4E4	寮	料	梁	涼	猟	療	瞭	稜	糧	良	諒	遼	量	陵	領	力
0F5	4E5	緑	倫	厘	林	淋	燐	琳	臨	輪	隣	鱗	麟	瑠	塁	涙	累
0F6	4E6	類	令	伶	例	冷	励	嶺	怜	玲	礼	苓	鈴	隷	零	霊	麗
0F7	4E7	齢	暦	歴	列	劣	烈	裂	廉	恋	憐	漣	煉	簾	練	聯	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0F8	**276**	о	п	р	с	т	у	ф	х	ц	ч	ш	щ	ъ	ы	ь	э
0F9	**277**	ю	я														
0FA	4F2		蓮	連	錬	呂	魯	櫓	炉	賂	路	露	労	婁	廊	弄	朗
0FB	4F3	楼	榔	浪	漏	牢	狼	篭	老	聾	蝋	郎	六	麓	禄	肋	録
0FC	4F4	論	倭	和	話	歪	賄	脇	惑	枠	鷲	亙	亘	鰐	詫	藁	蕨
0FD	4F5	椀	湾	碗	腕												
0FE	4F6																
0FF	4F7																

Table 14 HD66732 Full-size Character Codes and JIS Codes (Level-2)

Character Code	JIS Code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
100	[500]	For CGRAM (1000–1009)										Spares for CGRAM					
101	[501]	For CGRAM (1010–1019)															
102	502		弌	丐	丕	个	丱	丶	丼	丿	乂	乖	乘	亂	亅	豫	亊
103	503	舒	弍	于	亞	亟	亠	亢	亰	亳	亶	从	仍	仄	仆	仂	仗
104	504	仞	仭	仟	价	伉	佚	估	佛	佝	佗	佇	佶	侈	侏	侘	佻
105	505	佩	佰	侑	佯	來	侖	儘	俔	俟	俎	俘	俛	俑	俚	俐	俤
106	506	俥	倚	倨	倔	倪	倥	倅	伜	俶	倡	倩	倬	俾	俯	們	倆
107	507	偃	假	會	偕	偐	偈	做	偖	偬	偸	傀	傚	傅	傴	傲	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
108	[510]																
109	[511]																
10A	512		僉	僊	傳	僂	僖	僞	僥	僭	僣	僮	價	僵	儉	儁	儂
10B	513	儖	儕	儔	儚	儡	儺	儷	儼	儻	儿	兀	兒	兌	兔	兢	竸
10C	514	兩	兪	兮	冀	冂	囘	册	冉	冏	冑	冓	冕	冖	冤	冦	冢
10D	515	冩	冪	冫	决	冱	冲	冰	况	冽	凅	凉	凛	几	處	凩	凭
10E	516	凰	凵	凾	刄	刋	刔	刎	刧	刪	刮	刳	刹	剏	剄	剋	剌
10F	517	剞	剔	剪	剴	剩	剳	剿	剽	劍	劔	劒	剱	劈	劑	辨	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
110	[520]																
111	[521]																
112	522		辧	劬	劭	劼	劵	勁	勍	勗	勞	勣	勦	飭	勠	勳	勵
113	523	勸	勹	匆	匈	甸	匍	匐	匏	匕	匚	匣	匯	匱	匳	匸	區
114	524	卆	卅	丗	卉	卍	凖	卞	卩	卮	夘	卻	卷	厂	厖	厠	厦
115	525	厥	厮	厰	厶	參	簒	雙	叟	曼	燮	叮	叨	叭	叺	吁	吽
116	526	呀	听	吭	吼	吮	吶	吩	吝	呎	咏	呵	咎	呟	呱	呷	呰
117	527	咒	呻	咀	呶	咄	咐	咆	哇	咢	咸	咥	咬	哄	哈	咨	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
118	[530]																
119	[531]																
11A	532		咫	哂	咤	咾	咼	哘	哥	哦	唏	唔	哽	哮	哭	哺	哢
11B	533	唹	啀	啣	啌	售	啜	啅	啖	啗	唸	唳	啝	喙	喀	咯	喊
11C	534	喟	啻	啾	喘	喞	單	啼	喃	喩	喇	喨	嗚	嗅	嗟	嗄	嗜
11D	535	嗤	嗔	嘔	嗷	嘖	嗾	嗽	嘛	嗹	噎	噐	營	嘴	嘶	嘲	嘸
11E	536	噫	噤	嘯	噬	噪	嚆	嚀	嚊	嚠	嚔	嚏	嚥	嚮	嚶	嚴	囂
11F	537	嚼	囁	囃	囀	囈	囎	囑	囓	囗	囮	囹	圀	囿	圄	圉	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
120	[540]																
121	[541]																
122	542		圈	國	圍	圓	團	圖	嗇	圜	圦	圷	圸	坎	圻	址	坏
123	543	坩	埀	垈	坡	坿	垉	垓	垠	垳	垤	垪	垰	埃	埆	埔	埒
124	544	埓	堊	埖	埣	堋	堙	堝	塲	堡	塢	塋	塰	毀	塒	堽	塹
125	545	墅	墹	墟	墫	墺	壞	墻	墸	墮	壅	壓	壑	壗	壙	壘	壥
126	546	壜	壤	壟	壯	壺	壹	壻	壼	壽	夂	夊	夐	夛	梦	夥	夬
127	547	夭	夲	夸	夾	竒	奕	奐	奎	奚	奘	奢	奠	奧	奬	奩	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
128	[550]																
129	[551]																
12A	552		奸	妁	妝	佞	侫	妣	妲	姆	姨	姜	妍	姙	姚	娥	娟
12B	553	娑	娜	娉	娚	婀	婬	婉	娵	娶	婢	婪	媚	媼	媾	嫋	嫂
12C	554	媽	嫣	嫗	嫦	嫩	嫖	嫺	嫻	嬌	嬋	嬖	嬲	嫐	嬪	嬶	嬾
12D	555	孃	孅	孀	孑	孕	孚	孛	孥	孩	孰	孳	孵	學	斈	孺	宀
12E	556	它	宦	宸	寃	寇	寉	寔	寐	寤	實	寢	寞	寥	寫	寰	寶
12F	557	寳	尅	將	專	對	尓	尠	尢	尨	尸	尹	屁	屆	屎	屓	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
130	[560]																
131	[561]																
132	562		屐	屏	孱	屬	屮	乢	屶	屹	岌	岑	岔	妛	岫	岻	岶
133	563	岼	岷	峅	岾	峇	峙	峩	峽	峺	峭	嶌	峪	崋	崕	崗	嵜
134	564	崟	崛	崑	崔	崢	崚	崙	崘	嵌	嵒	嵎	嵋	嵬	嵳	嵶	嶇
135	565	嶄	嶂	嶢	嶝	嶬	嶮	嶽	嶐	嶷	嶼	巉	巍	巓	巒	巖	巛
136	566	巫	已	巵	帋	帚	帙	帑	帛	帶	帷	幄	幃	幀	幎	幗	幔
137	567	幟	幢	幤	幇	幵	并	幺	麼	广	庠	廁	廂	廈	廐	廏	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
138	[570]																
139	[571]																
13A	572		廖	廣	廝	廚	廛	廢	廡	廨	廩	廬	廱	廳	廰	廴	廸
13B	573	廾	弃	弉	彝	彜	弋	弑	弖	弩	弭	弸	彁	彈	彌	彎	弯
13C	574	彑	彖	彗	彙	彡	彭	彳	彷	徃	徂	彿	徊	很	徑	徇	從
13D	575	徙	徘	徠	徨	徭	徼	忖	忻	忤	忸	忱	忝	悳	忿	怡	恠
13E	576	怙	怐	怩	怎	怱	怛	怕	怫	怦	怏	怺	恚	恁	恪	恷	恟
13F	577	恊	恆	恍	恣	恃	恤	恂	恬	恫	恙	悁	悍	惧	悃	悚	

No CGROMs

• [XXX] : Not allocated to JIS codes. (Do not correspond to JIS codes.) Can be used as CGROMs.

Character Code	JIS Code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
140	**702**		陝	陟	陦	陲	陬	隍	隘	隕	隗	險	隧	隱	隲	隰	隴
141	**703**	隶	隸	隹	雎	雋	雉	雍	襍	雜	霍	雕	雹	霄	霆	霈	霓
142	582		悄	悛	悖	悗	悒	悧	悋	惡	悸	惠	惓	悴	忰	悽	惆
143	583	悵	惘	慍	愕	愆	惶	惷	愀	惴	惺	愃	愡	惻	惱	愍	愎
144	584	慇	愾	愨	愧	慊	愿	愼	愬	愴	愽	慂	慄	慳	慷	慘	慙
145	585	慚	慫	慴	慯	慥	慱	慟	慝	慓	慵	憙	憖	憇	憬	憔	憚
146	586	憊	憑	憫	憮	懌	懊	應	懷	懈	懃	懆	憺	懋	罹	懍	懦
147	587	懣	懶	懺	懴	懿	懽	懼	懾	戀	戈	戉	戍	戌	戔	戛	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
148	**712**		顱	顴	顳	颪	颯	颱	颶	飄	飃	飆	飩	飫	餃	餉	餒
149	**713**	餔	餘	餡	餝	餞	餤	餠	餬	餮	餽	餾	饂	饉	饅	饐	饋
14A	592		戞	戡	截	戮	戰	戲	戳	扁	扎	扞	扣	扛	扠	扨	扼
14B	593	抂	抉	找	抒	抓	抖	拔	抃	抔	拗	拑	抻	拏	拿	拆	擔
14C	594	拈	拜	拌	拊	拂	拇	抛	拉	挌	拮	拱	挧	挂	挈	拯	拵
14D	595	捐	挾	捍	搜	捏	掖	掎	掀	掫	捶	掣	掏	掉	掟	掵	捫
14E	596	捩	掾	揩	揀	揆	揣	揉	插	揶	揄	搖	搴	搆	搓	搦	搶
14F	597	攝	搗	搨	搏	摧	摯	摶	摎	攪	撕	撓	撥	撩	撈	撼	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
150	**722**		髻	鬆	鬘	鬚	鬟	鬢	鬣	鬥	鬧	鬨	鬩	鬪	鬮	鬯	鬲
151	**723**	魄	魃	魏	魍	魎	魑	魘	魴	鮓	鮃	鮑	鮖	鮗	鮟	鮠	鮨
152	5A2		據	擒	擅	擇	撻	擘	擂	擱	擧	舉	擠	擡	抬	擣	擯
153	5A3	攬	擶	擴	擲	擺	攀	擽	攘	攜	攅	攤	攣	攫	攴	攵	攷
154	5A4	收	攸	畋	效	敖	敕	敍	敘	敞	敝	敲	數	斂	斃	變	斛
155	5A5	斟	斫	斷	旃	旆	旁	旄	旌	旒	旛	旙	无	旡	旱	杲	昊
156	5A6	昃	旻	杳	昵	昶	昴	昜	晏	晄	晉	晁	晞	晝	晤	晧	晨
157	5A7	晟	晢	晰	暃	暈	暎	暉	暄	暘	暝	曁	暹	曉	暾	暼	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
158	**732**		鵝	鵞	鵤	鵑	鵐	鵙	鵲	鶉	鶇	鶫	鵯	鵺	鶚	鶤	鶩
159	**733**	鶲	鷄	鷁	鶻	鶸	鶺	鷆	鷏	鷂	鷙	鷓	鷸	鷦	鷭	鷯	鷽
15A	5B2		曄	暸	曖	曚	曠	昿	曦	曩	曰	曵	曷	朏	朖	朞	朦
15B	5B3	朧	霸	朮	朿	朶	杁	朸	朷	杆	杞	杠	杙	杣	杤	枉	杰
15C	5B4	枩	杼	杪	枌	枋	枦	枡	枅	枷	柯	枴	柬	枳	柩	枸	柤
15D	5B5	柞	柝	柢	柮	枹	柎	柆	柧	檜	栞	框	栩	桀	桍	栲	桎
15E	5B6	梳	栫	桙	档	桷	桿	梟	梏	梭	梔	條	梛	梃	檮	梹	桴
15F	5B7	梵	梠	梺	椏	梍	桾	椁	棊	椈	棘	椢	椦	棡	椌	棍	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
160	**742**		堯	槇	遙	瑤	凜	熙									
161	[743]																
162	5C2		棔	棧	棕	椶	椒	椄	棗	棣	椥	棹	棠	棯	椨	椪	椚
163	5C3	椣	椡	棆	楹	楷	楜	楸	楫	楔	楾	楮	椹	楴	椽	楙	椰
164	5C4	楡	楞	楝	榁	楪	榲	榮	槐	榿	槁	槓	榾	槎	寨	槊	槝
165	5C5	榻	槃	榧	樮	榑	榠	榜	榕	榴	槞	槨	樂	樛	槿	權	槹
166	5C6	槲	槧	樅	榱	樞	槭	樔	槫	樊	樒	櫁	樣	樓	橄	樌	橲
167	5C7	樶	橸	橇	橢	橙	橦	橈	樸	樢	檐	檍	檠	檄	檢	檣	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
168	[5D0]																
169	[5D1]																
16A	5D2		檗	蘗	檻	櫃	櫂	檸	檳	檬	櫞	櫑	櫟	檪	櫚	櫪	櫻
16B	5D3	欅	蘖	櫺	欒	欖	鬱	欟	欸	欷	盜	欹	飮	歇	歃	歉	歐
16C	5D4	歙	歔	歛	歟	歡	歸	歹	歿	殀	殄	殃	殍	殘	殕	殞	殤
16D	5D5	殪	殫	殯	殲	殱	殳	殷	殼	毆	毋	毓	毟	毬	毫	毳	毯
16E	5D6	麾	氈	氓	气	氛	氤	氣	汞	汕	汢	汪	沂	沍	沚	沁	沛
16F	5D7	汾	汨	汳	沒	沐	泄	泱	泓	沽	泗	泅	泝	沮	沱	沾	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
170	[5E0]																
171	[5E1]																
172	5E2		沺	泛	泯	泙	泪	洟	衍	洶	洫	洽	洸	洙	洵	洳	洒
173	5E3	洌	浣	涓	浤	浚	浹	浙	涎	涕	濤	涅	淹	渕	渊	涵	淇
174	5E4	淦	涸	淆	淬	淞	淌	淨	淒	淅	淺	淙	淤	淕	淪	淮	渭
175	5E5	湮	渮	渙	湲	湟	渾	渣	湫	渫	湶	湍	渟	湃	渺	湎	渤
176	5E6	滿	渝	游	溂	溪	溘	滉	溷	滓	溽	溯	滄	溲	滔	滕	溏
177	5E7	溥	滂	溟	潁	漑	灌	滬	滸	滾	漿	滲	漱	滯	漲	滌	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
178	[5F0]																
179	[5F1]																
17A	5F2		漾	漓	滷	澆	潺	潸	澁	澀	潯	潛	濳	潭	澂	潼	潘
17B	5F3	澎	澑	濂	潦	澳	澣	澡	澤	澹	濆	澪	濟	濕	濬	濔	濘
17C	5F4	濱	濮	濛	瀉	瀋	濺	瀑	瀁	瀏	濾	瀛	瀚	潴	瀝	瀘	瀟
17D	5F5	瀰	瀾	瀲	灑	灣	炙	炒	炯	烱	炬	炸	炳	炮	烟	烋	烝
17E	5F6	烙	焉	烽	焜	焙	煥	煕	熈	煦	煢	煌	煖	煬	熏	燻	熄
17F	5F7	熕	熨	熬	燗	熹	熾	燒	燉	燔	燎	燠	燬	燧	燵	燼	

Character Code	JIS Code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
180	**704**	霎	霑	霏	霖	霙	霤	霪	霰	霹	霽	霾	靄	靆	靈	靂	靉
181	**705**	靜	靠	靤	靦	靨	勒	靫	靱	靹	鞅	靼	鞁	靺	鞆	鞋	鞏
182	602		燹	燿	爍	爐	爛	爨	爭	爬	爰	爲	爻	爼	爿	牀	牆
183	603	牋	牘	牴	牾	犂	犁	犇	犒	犖	犢	犧	犹	犲	狃	狆	狄
184	604	狎	狒	狢	狠	狡	狹	狷	倏	猗	猊	猜	猖	猝	猴	猯	猩
185	605	猥	猾	獎	獏	默	獗	獪	獨	獰	獸	獵	獻	獺	珈	玳	珎
186	606	玻	珀	珥	珮	珞	璢	琅	瑯	琥	珸	琲	琺	瑕	琿	瑟	瑙
187	607	瑁	瑜	瑩	瑰	瑣	瑪	瑶	瑾	璋	璞	璧	瓊	瓏	瓔	珱	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
188	**714**	饑	饒	饌	饕	馗	馘	馥	馭	馮	馼	駟	駛	駝	駘	駑	駭
189	**715**	駮	駱	駲	駻	駸	騁	騏	騅	駢	騙	騫	騷	驅	驂	驀	驃
18A	612		瓠	瓣	瓧	瓩	瓮	瓲	瓰	瓱	瓸	瓷	甄	甃	甅	甌	甎
18B	613	甍	甕	甓	甞	甦	甬	甼	畄	畍	畊	畉	畛	畆	畚	畩	畤
18C	614	畧	畫	畭	畸	當	疆	疇	畴	疊	疉	疂	疔	疚	疝	疥	疣
18D	615	痂	疳	痃	疵	疽	疸	疼	疱	痍	痊	痒	痙	痣	痞	痾	痿
18E	616	痼	瘁	痰	痺	痲	痳	瘋	瘍	瘉	瘟	瘧	瘠	瘡	瘢	瘤	瘴
18F	617	瘰	瘻	癇	癈	癆	癜	癘	癡	癢	癨	癩	癪	癧	癬	癰	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
190	**724**	鮴	鯀	鯊	鮹	鯆	鯏	鯑	鯒	鯣	鯢	鯤	鯔	鯡	鰺	鯲	鯱
191	**725**	鯰	鰕	鰔	鰉	鰓	鰌	鰆	鰈	鰒	鰊	鰄	鰮	鰛	鰥	鰤	鰡
192	622		癲	癶	癸	發	皀	皃	皈	皋	皎	皖	皓	皙	皚	皰	皴
193	623	皸	皹	皺	盂	盍	盖	盒	盞	盡	盥	盧	盪	蘯	盻	眈	眇
194	624	眄	眩	眤	眞	眥	眦	眛	眷	眸	睇	睚	睨	睫	睛	睥	睿
195	625	睾	睹	瞎	瞋	瞑	瞠	瞞	瞰	瞶	瞹	瞿	瞼	瞽	瞻	矇	矍
196	626	矗	矚	矜	矣	矮	矼	砌	砒	礦	砠	礪	硅	碎	硴	碆	硼
197	627	碚	碌	碣	碵	碪	碯	磑	磆	磋	磔	碾	碼	磅	磊	磬	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
198	**734**	鸚	鸛	鸞	鹵	鹹	鹽	麁	麈	麋	麌	麒	麕	麑	麝	麥	麩
199	**735**	麸	麪	麭	靡	黌	黎	黏	黐	黔	黜	點	黝	黠	黥	黨	黯
19A	632		磧	磚	磽	磴	礇	礒	礑	礙	礬	礫	祀	祠	祗	祟	祚
19B	633	祕	祓	祺	祿	禊	禝	禧	齋	禪	禮	禳	禹	禺	秉	秕	秧
19C	634	秬	秡	秣	稈	稍	稘	稙	稠	稟	禀	稱	稻	稾	稷	穃	穗
19D	635	穉	穡	穢	穩	龝	穰	穹	穽	窈	窗	窕	窘	窖	窩	竈	窰
19E	636	窶	竅	竄	窿	邃	竇	竊	竍	竏	竕	竓	站	竚	竝	竡	竢
19F	637	竦	竭	竰	笂	笏	笊	笆	笳	笘	笙	笞	笵	笨	笶	筐	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1A0	[744]																
1A1	[745]																
1A2	642		筺	笄	筍	笋	筌	筅	筵	筥	筴	筧	筰	筱	筬	筮	箝
1A3	643	箘	箟	箍	箜	箚	箋	箒	箏	筝	箙	篋	篁	篌	篏	箴	篆
1A4	644	篝	篩	簑	簔	篦	篥	籠	簀	簇	簓	篳	篷	簗	簍	篶	簣
1A5	645	簧	簪	簟	簷	簫	簽	籌	籃	籔	籏	籀	籐	籘	籟	籤	籖
1A6	646	籥	籬	籵	粃	粐	粤	粭	粢	粫	粡	粨	粳	粲	粱	粮	粹
1A7	647	粽	糀	糅	糂	糘	糒	糜	糢	鬻	糯	糲	糴	糶	糺	紆	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1A8	[650]																
1A9	[651]																
1AA	652		紂	紜	紕	紊	絅	絋	紮	紲	紿	紵	絆	絳	絖	絎	絲
1AB	653	絨	絮	絏	絣	經	綉	絛	綏	絽	綛	綺	綮	綣	綵	緇	綽
1AC	654	綫	總	綢	綯	緜	綸	綟	綰	緘	緝	緤	緞	緻	緲	緡	縅
1AD	655	縊	縣	縡	縒	縱	縟	縉	縋	縢	繆	繦	縻	縵	縹	繃	縷
1AE	656	縲	縺	繧	繝	繖	繞	繙	繚	繹	繪	繩	繼	繻	纃	緕	繽
1AF	657	辮	繿	纈	纉	續	纒	纐	纓	纔	纖	纎	纛	纜	缸	缺	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1B0	[660]																
1B1	[661]																
1B2	662		罅	罌	罍	罎	罐	网	罕	罔	罘	罟	罠	罨	罩	罧	罸
1B3	663	羂	羆	羃	羈	羇	羌	羔	羞	羝	羚	羣	羯	羲	羹	羮	羶
1B4	664	羸	譱	翅	翆	翊	翕	翔	翡	翦	翩	翳	翹	飜	耆	耄	耋
1B5	665	耒	耘	耙	耜	耡	耨	耿	耻	聊	聆	聒	聘	聚	聟	聢	聨
1B6	666	聳	聲	聰	聶	聹	聽	聿	肄	肆	肅	肛	肓	肚	肭	冐	肬
1B7	667	胛	胥	胙	胝	胄	胚	胖	脉	胯	胱	脛	脩	脣	脯	腋	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1B8	[670]																
1B9	[671]																
1BA	672		隋	腆	脾	腓	腑	胼	腱	腮	腥	腦	腴	膃	膈	膊	膀
1BB	673	膂	膠	膕	膤	膣	腟	膓	膩	膰	膵	膾	膸	膽	臀	臂	膺
1BC	674	臉	臍	臑	臙	臘	臈	臚	臟	臠	臧	臺	臻	臾	舁	舂	舅
1BD	675	與	舊	舍	舐	舖	舩	舫	舸	舳	艀	艙	艘	艝	艚	艟	艤
1BE	676	艢	艨	艪	艫	舮	艱	艷	艸	艾	芍	芒	芫	芟	芻	芬	苡
1BF	677	苣	苟	苒	苴	苳	苺	莓	范	苻	苹	苞	茆	苜	茉	苙	

Character Code	JIS Code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1C0	**706**	鞜	鞨	鞦	鞣	鞳	鞴	韃	韆	韈	韋	韜	韭	齏	韲	竟	韶
1C1	**707**	韵	頏	頌	頸	頤	頡	頷	頽	顆	顏	顋	顫	顯	顰	顱	
1C2	682		茵	茴	茖	茲	茱	荀	茹	荐	荅	茯	茫	茗	茘	莅	莚
1C3	683	莪	莟	莢	莖	茣	莎	莇	莊	荼	莵	荳	荵	莠	莉	莨	菴
1C4	684	萓	菫	菎	菽	萃	菘	萋	菁	菷	萇	菠	菲	萍	萢	萠	莽
1C5	685	萸	蔆	菻	葭	萪	萼	蕚	蒄	葷	葫	蒭	葮	蒂	葩	葆	萬
1C6	686	葯	葹	萵	蓊	葢	蒹	蒿	蒟	蓙	蓍	蒻	蓚	蓐	蓁	蓆	蓖
1C7	687	蒡	蔡	蓿	蓴	蔗	蔘	蔬	蔟	蔕	蔔	蓼	蕀	蕣	蕘	蕈	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1C8	**716**	騾	驕	驍	驛	驗	驟	驢	驥	驤	驩	驫	驪	骭	骰	骼	髀
1C9	**717**	髏	髑	髓	體	髞	髟	髢	髣	髦	髯	髫	髮	髴	髱	髷	
1CA	692		蕁	蘂	蕋	蕕	薀	薤	薈	薑	薊	薨	蕭	薔	薛	藪	薇
1CB	693	薜	蕷	蕾	薐	藉	薺	藏	薹	藐	藕	藝	藥	藜	藹	蘊	蘓
1CC	694	蘋	藾	藺	蘆	蘢	蘚	蘰	蘿	虍	乕	虔	號	虧	虱	蚓	蚣
1CD	695	蚩	蚪	蚋	蚌	蚶	蚯	蛄	蛆	蚰	蛉	蠣	蚫	蛔	蛞	蛩	蛬
1CE	696	蛟	蛛	蛯	蜒	蜆	蜈	蜀	蜃	蛻	蜑	蜉	蜍	蛹	蜊	蜴	蜿
1CF	697	蜷	蜻	蜥	蜩	蜚	蝠	蝟	蝸	蝌	蝎	蝴	蝗	蝨	蝮	蝙	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1D0	**726**	鰰	鱇	鰲	鱆	鰾	鱚	鱠	鱧	鱶	鱸	鳧	鳬	鳰	鴉	鴈	鳫
1D1	**727**	鴃	鴆	鴪	鴦	鶯	鴣	鴟	鵄	鴕	鴒	鵁	鴿	鴾	鵆	鵈	
1D2	6A2		蝓	蝣	蝪	蠅	螢	螟	螂	螯	蟋	螽	蟀	蟐	雖	螫	蟄
1D3	6A3	螳	蟇	蟆	螻	蟯	蟲	蟠	蠏	蠍	蟾	蟶	蟷	蠎	蟒	蠑	蠖
1D4	6A4	蠕	蠢	蠡	蠱	蠶	蠹	蠧	蠻	衄	衂	衒	衙	衞	衢	衫	袁
1D5	6A5	衾	袞	衵	衽	袵	衲	袂	袗	袒	袮	袙	袢	袍	袤	袰	袿
1D6	6A6	袱	裃	裄	裔	裘	裙	裝	裹	褂	裼	裴	裨	裲	褄	褌	褊
1D7	6A7	褓	襃	褞	褥	褪	褫	襁	襄	褻	褶	褸	襌	褝	襠	襞	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1D8	**736**	黴	黶	黷	黹	黻	黼	黽	鼇	鼈	皷	鼕	鼡	鼬	鼾	齊	齒
1D9	**737**	齔	齣	齟	齠	齡	齦	齧	齬	齪	齷	齲	齶	龕	龜	龠	
1DA	6B2		襦	襤	襭	襪	襯	襴	襷	襾	覃	覈	覊	覓	覘	覡	覩
1DB	6B3	覦	覬	覯	覲	覺	覽	覿	觀	觚	觜	觝	觧	觴	觸	訃	訖
1DC	6B4	訐	訌	訛	訝	訥	訶	詁	詛	詒	詆	詈	詼	詭	詬	詢	誅
1DD	6B5	誂	誄	誨	誡	誑	誥	誦	誚	誣	諄	諍	諂	諚	諫	諳	諧
1DE	6B6	諤	諱	謔	諠	諢	諷	諞	諛	謌	謇	謚	諡	謖	謐	謗	謠
1DF	6B7	謳	鞫	謦	謫	謾	謨	譁	譌	譏	譎	證	譖	譛	譚	譫	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1E0	[746]																
1E1	[747]																
1E2	6C2		譟	譬	譯	譴	譽	讀	讌	讎	讒	讓	讖	讙	讚	谺	豁
1E3	6C3	谿	豈	豌	豎	豐	豕	豢	豬	豸	豺	貂	貉	貅	貊	貍	貎
1E4	6C4	貔	豼	貘	戝	貭	貪	貽	貲	貳	貮	貶	賈	賁	賤	賣	賚
1E5	6C5	賽	賺	賻	贄	贅	贊	贇	贏	贍	贐	齎	贓	賍	贔	贖	赧
1E6	6C6	赭	赱	赳	趁	趙	跂	趾	趺	跏	跚	跖	跌	跛	跋	跪	跫
1E7	6C7	跟	跣	跼	踈	踉	跿	踝	踞	踐	踟	蹂	踵	踰	踴	蹊	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1E8	[6D0]																
1E9	[6D1]																
1EA	6D2		蹇	蹉	蹌	蹐	蹈	蹙	蹤	蹠	踪	蹣	蹕	蹶	蹲	蹼	躁
1EB	6D3	躇	躅	躄	躋	躊	躓	躑	躔	躙	躪	躡	躬	躰	軆	躱	躾
1EC	6D4	軅	軈	軋	軛	軣	軼	軻	軫	軾	輊	輅	輕	輒	輙	輓	輜
1ED	6D5	輟	輛	輌	輦	輳	輻	輹	轅	轂	輾	轌	轉	轆	轎	轗	轜
1EE	6D6	轢	轣	轤	辜	辟	辣	辭	辯	辷	迚	迥	迢	迪	迯	邇	迴
1EF	6D7	逅	迹	迺	逑	逕	逡	逍	逞	逖	逋	逧	逶	逵	逹	迸	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1F0	[6E0]																
1F1	[6E1]																
1F2	6E2		遏	遐	遑	遒	逎	遉	逾	遖	遘	遞	遨	遯	遶	隨	遲
1F3	6E3	邂	遽	邁	邀	邊	邉	邏	邨	邯	邱	邵	郢	郤	扈	郛	鄂
1F4	6E4	鄒	鄙	鄲	鄰	酊	酖	酘	酣	酥	酩	酳	酲	醋	醉	醂	醢
1F5	6E5	醫	醯	醪	醵	醴	醺	釀	釁	釉	釋	釐	釖	釟	釡	釛	釼
1F6	6E6	釵	釶	鈞	釿	鈔	鈬	鈕	鈑	鉞	鉗	鉅	鉉	鉤	鉈	銕	鈿
1F7	6E7	鉋	鉐	銜	銖	銓	銛	鉚	鋏	銹	銷	鋩	錏	鋺	鍄	錮	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1F8	[6F0]																
1F9	[6F1]																
1FA	6F2		錙	錢	錚	錣	錺	錵	錻	鍜	鍠	鍼	鍮	鍖	鎰	鎬	鎭
1FB	6F3	鎔	鎹	鏖	鏗	鏨	鏥	鏘	鏃	鏝	鏐	鏈	鏤	鐚	鐔	鐓	鐃
1FC	6F4	鐇	鐐	鐶	鐫	鐵	鐡	鐺	鑁	鑒	鑄	鑛	鑠	鑢	鑞	鑪	鈩
1FD	6F5	鑰	鑵	鑷	鑽	鑚	鑼	鑾	钁	鑿	閂	閇	閊	閔	閖	閘	閙
1FE	6F6	閠	閨	閧	閭	閼	閻	閹	閾	闊	濶	闃	闍	闌	闕	闔	闖
1FF	6F7	關	闡	闥	闢	阡	阨	阮	阯	陂	陌	陏	陋	陷	陜	陞	

Table 15 A00 Standard Half-size Font Pattern (ROM Bank 0 (ROM = 0)

ROM	Lower / Upper	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	1	2	3	4	5	6	7	8	9	、	。	：	；	（	）
0	1	ゃ	ゅ	ょ	ャ	ュ	ョ	ア	ィ	ウ	ェ	ォ	「	」	*	#	／
0	2	space	あ	い	う	え	お	か	き	く	け	こ	さ	し	す	せ	そ
0	3	っ	た	ち	つ	て	と	な	に	ぬ	ね	の	は	ひ	ふ	へ	ほ
0	4	ま	み	む	め	も	や	ゆ	よ	ら	り	る	れ	ろ	わ	を	ん
0	5	ー	ア	イ	ウ	エ	オ	カ	キ	ク	ケ	コ	サ	シ	ス	セ	ソ
0	6	ッ	タ	チ	ツ	テ	ト	ナ	ニ	ヌ	ネ	ノ	ハ	ヒ	フ	ヘ	ホ
0	7	マ	ミ	ム	メ	モ	ヤ	ユ	ヨ	ラ	リ	ル	レ	ロ	ワ	ヲ	ン

Table 16 A00 Standard Half-size Font Pattern (ROM Bank 1 (ROM = 1)

ROM	Lower / Upper	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	1	2	3	4	5	6	7	8	9	^	_	：	；	,	.
0	1	ー	ア	イ	ウ	エ	オ	カ	キ	ク	ケ	コ	サ	シ	ス	セ	ソ
0	2	space	タ	チ	ツ	テ	ト	ナ	ニ	ヌ	ネ	ノ	ハ	ヒ	フ	ヘ	ホ
0	3	マ	ミ	ム	メ	モ	ヤ	ユ	ヨ	ラ	リ	ル	レ	ロ	ワ	ヲ	ン
0	4	*	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
0	5	P	Q	R	S	T	U	V	W	X	Y	Z	ッ	ャ	ュ	ョ	■
0	6	#	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
0	7	p	q	r	s	t	u	v	w	x	y	z	゛	°	@	!	?

HD66732 CGROM Character Pattern Write

1. When Using Two 1-M EPROMs (for Full Size) + One 32-k EPROM (for Half Size)

1.1 Full-size Character (Level-1 Kanji Set, Non-Kanji) (FCGROM-1)

- 11 x 12 dots, up to 4064 types (not including 32 types of CGRAM (character code: 0000 to 001F))
- EPROM: HN27C101G/AG x one
- Divide the character pattern into six left-half dots (A16 = 0) and five right-half dots (A16 = 1)
- EPROM addresses A16 to A 0 designate the "left/right distinction bit + full-size character code (C11 to C0) + line position" (Not using C12 of a full-size character code)
- Write "0" into I/0s 7 and 6 of the left-half character pattern (A16 = 0)
- Write "0" into I/0s 7, 6 and 5 of the right-half character pattern (A16 = 1)
- When A3, A2, A1, or A0 = $C to $F (1100 to 1111), write "0" into I/Os 7 to 0
- Write "0" into $0 to $1FF and $10000 to $101FF (corresponding to the CGRAM character codes 0000 to 001F) (The data of $0 to $1FF, and $10000 to $101FF are ignored)

Table 17 FCGROM-1 Write (1)

FCGROM-1 EPROM Address																A16 = 0 (left) Data						A16 = 1 (right) Data					
		A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	
		C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	漢
								↓						0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	
								↓						0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	
								↓						0	0	1	1	1	0	0	0	1	1	1	1	1	1	1	
								↓						0	1	0	0	0	1	0	0	1	0	0	1	0	0	1	
								↓						0	1	0	1	0	0	0	0	1	1	1	1	1	1	1	
								↓						0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	
								↓						0	1	1	1	0	0	1	0	1	1	1	1	1	1	1	
								↓						1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	
								↓						1	0	0	1	0	1	0	0	1	1	1	1	1	1	1	
								↓						1	0	1	0	0	1	0	0	0	0	1	0	1	0	0	
								↓						1	0	1	1	1	0	0	0	1	1	0	0	0	1	1	
								↓						1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
								↓						1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	
								↓						1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
								↓						1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	

Character code (C11 to C0) | Line position | Character pattern

Note: For character codes (C12 to C0), 0000 to 001F are used as CGRAM codes, and EPROM addresses $0 to $1FF and the data of $10000 to $101FF are ignored.

1.2 Full-size Character (Level-2 Kanji Set) (FCGROM-2)

[the same as a Full-size Character (Level-1 Kanji Set, Non-Kanji) (FCGROM-1)]

- 11 x 12 dots, up to 4064 types (not including 32 types of CGRAM (character code: 1000 to 101F))
- EPROM: HN27C101G/AG x one
- Divide the character pattern into six left-half dots (A16 = 0) and five right-half dots (A16 = 1)
- EPROM addresses A16 to A 0 designate the "left/right distinction bit + full-size character code (C11 to C0) + line position" (Not using C12 of a full-size character code)
- Write "0" into I/0s 7 and 6 of the left-half character pattern (A16 = 0)
- Write "0" into I/0s 7, 6 and 5 of the right-half character pattern (A16 = 1)
- When A3, A2, A1, or A0 = $C to $F (1100 to 1111), write "0" into I/Os 7 to 0
- Write "0" into $0 to $1FF and $10000 to $101FF (corresponding to the CGRAM character codes 1000 to 101F) (The data of $0 to $1FF, and $10000 to $101FF are ignored)

Table 18 FCGROM-2 Write (1)

FCGROM-1 EPROM Address																A16 = 0 (left) Data						A16 = 1 (right) Data					
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	
C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	弋
						↓						0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	
						↓						0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	
						↓						0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	
						↓						0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	
						↓						0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	
						↓						0	1	1	0	0	1	1	1	1	0	0	1	0	0	0	
						↓						0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	
						↓						1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	
						↓						1	0	0	1	0	0	0	1	1	1	0	0	1	0	0	
						↓						1	0	1	0	1	1	1	0	0	0	0	0	1	0	1	
						↓						1	0	1	1	0	0	0	0	0	0	0	0	0	1	1	
						↓						1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
						↓						1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	
						↓						1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
						↓						1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	

Character code (C11 to C0) | Line position | Character pattern

Note: For character codes (C12 to C0), 1000 to 101F are used as CGRAM codes, and EPROM addresses $0 to $1FF and the data of $10000 to $101FF are ignored.

1.3 Half-size Character (HCGROM)

- 6 x 12 dots, up to 256 types (128 types x 2 banks)
- EPROM: an EPROM with 512 bytes or more capacity, such as the HN27C256AG
- EPROM addresses A11 to A0 designate the "half-size CGROM bank bit (bk) + half-size character code (C6 to C0) + line position"
- Write "0" into the rightmost bit as a character space (I/O 0 = 0)
- Write "0" into I/Os 7 and 6
- When A3, A2, A1, or A0 = $C to $F (1100 to 1111), write "0" into I/Os 7 to 0

Table 19 HCGROM Write

HCGROM EPROM Address												A16 = 0 Data						
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	
bk	C6	C5	C4	C3	C2	C1	C0	0	0	0	0	0	1	1	1	1	0	J
				↓				0	0	0	1	0	0	0	1	0	0	
				↓				0	0	1	0	0	0	0	1	0	0	
				↓				0	0	1	1	0	0	0	1	0	0	
				↓				0	1	0	0	0	0	0	1	0	0	
				↓				0	1	0	1	0	0	0	1	0	0	
				↓				0	1	1	0	0	0	0	1	0	0	
				↓				0	1	1	1	0	0	0	1	0	0	
				↓				1	0	0	0	0	0	0	1	0	0	
				↓				1	0	0	1	1	0	0	1	0	0	
				↓				1	0	1	0	1	0	0	1	0	0	
				↓				1	0	1	1	0	1	1	0	0	0	
				↓				1	1	0	0	0	0	0	0	0	0	
				↓				1	1	0	1	0	0	0	0	0	0	
				↓				1	1	1	0	0	0	0	0	0	0	
				↓				1	1	1	1	0	0	0	0	0	0	

Half-size CGROM bank bit — Character code (C6 to C0) — Line position — Character pattern "0" Space

*** Relationship between HD66732 Full-size Character Codes and JIS Codes**

Table 20 Full-size Character Codes and JIS Codes

• Full-size Character Codes

0 A1 A2	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	b7	b6	b5	
	0	a7	a6	b3	b2	b1	0	0	a5	a4	a3	a2	a1	0	1	0	
	0	b7	b4	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1	0	1	1	
	0	b7	b4	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1	1	0	0	
	1	b6	b4	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1	1	0	1	
	1	b6	b4	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1	1	1	0	
	1	a7	a6	b3	b2	b1	0	0	a5	a4	a3	a2	a1	1	1	1	
	u6	0	0	0	0	0	0	0	u5	u4	u3	u2	u1	–	–	–	User font (CGRAM)

• JIS Codes

b7 b6 b5 b4 b3 b2 b1 — JIS first byte

a7 a6 a5 a4 a3 a2 a1 — JIS second byte

• Character Codes for CGRAM (40 characters)
  - 0000 to 0009
  - 0010 to 0019
  - 1000 to 1009
  - 1010 to 1019

  (Codes for 24 remaining characters are reserved.)

2. When Using One 4-M EPROM

2.1 Full-size Character (Level-1 Kanji Set, Non-Kanji) (FCGROM-1)

- 11 x 12 dots, up to 4064 types (not including 32 types of CGRAM (character code: 0000 to 001F))
- EPROM: HN27C4001G x one (address: $0 to $1FFFF)
- Divide character pattern into six left-half dots (A16 = 0) and five right-half dots (A16 = 1)
- EPROM addresses A18 to A 0 designate the "0 + full-size character code (C12) + left/right distinction bit + full-size character code (C11 to C0) + line position" (C12 of the full-size character code is used as an EPROM address A17)
- Write "0" into I/0s 7 and 6 of the left-half character pattern (A16 = 0)
- Write "0" into I/0s 7, 6 and 5 of the right-half character pattern (A16 = 1)
- When A3, A2, A1, or A0 = $C to $F (1100 to 1111), write "0" into I/Os 7 to 0
- Write "0" into $0 to $1FF, and $10000 to $101FF (corresponding to the CGRAM character codes 0000 to 001F) (The data of $0 to $1FF, and $10000 to $101FF are ignored)

Table 21 FCGROM-1 Write (2)

FCGROM-1 EPROM Address																				(*) A16 = 0 (left) Data						(*) A16 = 1 (right) Data					
A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	
0	C12	(*)	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	0	0	0	0		0	1	0	0	0	0	1	0	1	0	0	漢
									↓						0	0	0	1		0	0	1	0	1	1	1	1	1	1	1	
									↓						0	0	1	0		0	0	0	0	0	0	1	0	1	0	0	
									↓						0	0	1	1		1	0	0	0	1	1	1	1	1	1	1	
									↓						0	1	0	0		0	1	0	0	1	0	0	1	0	0	1	
									↓						0	1	0	1		0	0	0	0	1	1	1	1	1	1	1	
									↓						0	1	1	0		0	0	0	0	0	0	0	1	0	0	0	
									↓						0	1	1	1		0	0	1	0	1	1	1	1	1	1	1	
									↓						1	0	0	0		0	0	1	0	0	0	0	1	0	0	0	
									↓						1	0	0	1		0	1	0	0	1	1	1	1	1	1	1	
									↓						1	0	1	0		0	1	0	0	0	0	1	0	1	0	0	
									↓						1	0	1	1		1	0	0	0	1	1	0	0	0	1	1	
									↓						1	1	0	0		0	0	0	0	0	0	0	0	0	0	0	
									↓						1	1	0	1		0	0	0	0	0	0	0	0	0	0	0	
									↓						1	1	1	0		0	0	0	0	0	0	0	0	0	0	0	
									↓						1	1	1	1		0	0	0	0	0	0	0	0	0	0	0	
			Character code (C11 to C0)												Line position					Character pattern											

Note: For character codes (C12 to C0), 0000 to 001F are used as CGRAM codes, and EPROM addresses $0 to $1FF and the data of $10000 to $101FF are ignored.

2.2 Full-size Character (Level-2 Kanji Set) (FCGROM-2)

- 11 x 12 dots, up to 4064 types (not including 32 types of CGRAM (character code: 1000 to 101F))
- EPROM: HN27C4001G x one (address: $20000 to $3FFFF)
- Divide character pattern into six left-half dots (A16 = 0) and five right-half dots (A16 = 1)
- EPROM addresses A18 to A 0 designate the "0 + full-size character code (C12) + left/right distinction bit + full-size character code (C11 to C0) + line position" (C12 of the full-size character code is used as EPROM address A17)
- Write "0" into I/0s 7 and 6 of the left-half character pattern (A16 = 0)
- Write "0" into I/0s 7, 6 and 5 of the right-half character pattern (A16 = 1)
- When A3, A2, A1, or A0 = $C to $F (1100 to 1111), write "0" into I/Os 7 to 0
- Write "0" into $0 to $1FF, and $10000 to $101FF (corresponding to the CGRAM character codes 1000 to 101F) (The data of $0 to $1FF, and $10000 to $101FF are ignored)

Table 22 FCGROM-2 Write (2)

FCGROM-2 EPROM Address																		(*) A16 = 0 (left) Data						(*) A16 = 1 (right) Data					
A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
0	C12	(*)	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0
									↓						0	0	0	1	0	0	0	0	0	1	0	0	0	1	0
									↓						0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
									↓						0	0	1	1	1	1	1	1	1	1	1	1	1	1	0
									↓						0	1	0	0	0	0	0	0	0	0	1	0	0	0	0
									↓						0	1	0	1	0	0	0	0	0	0	0	1	0	0	0
									↓						0	1	1	0	0	1	1	1	1	0	0	1	0	0	0
									↓						0	1	1	1	0	0	0	0	0	0	0	1	0	0	0
									↓						1	0	0	0	0	0	0	0	0	0	0	0	1	0	0
									↓						1	0	0	1	0	0	0	1	1	1	0	0	1	0	0
									↓						1	0	1	0	1	1	1	0	0	0	0	0	1	0	1
									↓						1	0	1	1	0	0	0	0	0	0	0	0	0	1	1
									↓						1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
									↓						1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
									↓						1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
									↓						1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Character code (C12) | Character code (C11 to C0) | Line position | Character pattern

Note: For character codes (C12 to C0), 1000 to 101F are used as CGRAM codes, and EPROM addresses $20000 to $201FF and the data of $30000 to $301FF are ignored.

2.3 Half-size Character (HCGROM)

- 6 x 12 dots, up to 256 types (128 types x 2 banks)
- EPROM: HN27C4001G x one (address: $40000 to $40FFF)
- EPROM addresses A18 to A0 designate the "$40 + half-size CGROM bank bit (bk) + half-size character code (C6 to C0) + line position"
- Write "0" into the rightmost bit as a character space (I/O 0 = 0)
- Write "0" into I/Os 7 and 6
- When A3, A2, A1, or A0 = $C to $F (1100 to 1111), write "0" into I/Os 7 to 0

Table 23 HCGROM Write (2)

HCGROM EPROM Address																		A16 = 0 Data						
A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	
1	0	0	0	0	0	0	bk	C6	C5	C4	C3	C2	C1	C0	0	0	0	0	0	1	1	1	1	0	J
											↓				0	0	0	1	0	0	0	1	0	0	
											↓				0	0	1	0	0	0	0	1	0	0	
											↓				0	0	1	1	0	0	0	1	0	0	
											↓				0	1	0	0	0	0	0	1	0	0	
											↓				0	1	0	1	0	0	0	1	0	0	
											↓				0	1	1	0	0	0	0	1	0	0	
											↓				0	1	1	1	0	0	0	1	0	0	
											↓				1	0	0	0	0	0	0	1	0	0	
											↓				1	0	0	1	1	0	0	1	0	0	
											↓				1	0	1	0	1	0	0	1	0	0	
											↓				1	0	1	1	0	1	1	0	0	0	
											↓				1	1	0	0	0	0	0	0	0	0	
											↓				1	1	0	1	0	0	0	0	0	0	
											↓				1	1	1	0	0	0	0	0	0	0	
											↓				1	1	1	1	0	0	0	0	0	0	

Half-size CGROM bank bit | Character code (C6 to C0) | Line position | Character pattern "0" Space

Table 24 4-M EPROM Address

		4-M EPROM Address																				
		A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	hex.
Level 1 Kanji Set + non-Kanji	(left)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
	(right)	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10000
		0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFF
Level 2 Kanji Set	(left)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	20000
		0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2FFFF
	(right)	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	30000
		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFFF
Half-size Font	bk = 0 (bank 0)	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	40000
		1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	407FF
	bk = 1 (bank 1)	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	40800
		1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	40FFF

Instruction Registers

Outline

The HD66732 consists of the following five types of register:

- Index register (IR): Selects control registers, RAM addresses, or data registers
- Status register (SR): Reads the internal state or key scan data
- Control registers (R0–RC): Set the display control or key scan control
- RAM address registers (RD and RE): Select RAMs and set RAM addresses
- RAM data register (RF): Receives the write and read data for the RAM

Normally, instructions that transfer display data are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66732 RAM addresses after each data write can reduce the MPU program load.

Because instructions other than the clear-display instruction are executed in 0 cycles, instructions can be written in succession.

While the clear-display instruction is being executed for internal operation, or during reset, no instruction other than the SR read instruction can be executed.

Instruction Descriptions

Index Register (IR)

The index register designates control registers (R0 to RC), RAM address registers (RD and RE), and RAM data register (RF). The register index value must be set between addresses 0000 to 1110.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IR:	1	0	**0**	**0**	**0**	**0**	**ID3**	**ID2**	**ID1**	**ID0**

Figure 3 Index Register Instruction

Status Register (SR)

The status register reads the busy flag (BF), LCD-driven display lines (NF1/0), and display raster-rows (LF3 to LF0).

In a serial interface, the SR reads the key scan data in key scan registers SCAN0 to SCAN3. After the start byte has been transferred, the SR starts reading from SCAN0, then SCAN1, SCAN2, and SCAN3. After SCAN3 has been read, SCAN0 is read again. For details, see the Key Scan Control section.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
SR:	1	0	**BF**	**NF1**	**NF0**	**0**	**LF3**	**LF2**	**LF1**	**LF0**	(Bus interface)
SR:	1	0	**SD7**	**SD6**	**SD5**	**SD4**	**SD3**	**SD2**	**SD1**	**SD0**	(Serial interface)

Figure 4 Status Register Instruction

Table 25 Display Line Position

NF1	NF0	Display Line Position
0	0	Displaying the 1st line
0	1	Displaying the 2nd line
1	0	Displaying the 3rd line
1	1	Displaying the 4th line

Table 26 Display Raster-row Position

LF3	LF2	LF1	LF0	Display Raster-row Position
0	0	0	0	Displaying the 1st raster-row
0	0	0	1	Displaying the 2nd raster-row
0	0	1	0	Displaying the 3ed raster-row
0	0	1	1	Displaying the 4th raster-row
0	1	0	0	Displaying the 5th raster-row
0	1	0	1	Displaying the 6th raster-row
	•			•
	•			•
	•			•
1	0	1	1	Displaying the 12th raster-row
1	1	0	0	Displaying the 13th raster-row

Clear Display (R0)

The clear display instruction writes half-size space code A0H (half-size HCROM for character code A0H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter (AC). It also sets I/D to 1 (increment mode) in the entry mode set instruction. Since the execution time of this instruction needs 85 clock cycles, do not transfer the next instruction during this time.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R0:	0	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Figure 5 Clear Display Instruction

Start Oscillation (R1)

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R1:	0	1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Figure 6 Start Oscillation Instruction

Driver Output Control (R2)

NL2-0: Specify the display lines. Display lines change the liquid crystal display drive duty ratio. DDRAM address mapping does not depend on the number of display lines.

CEN: Switches the COM1 output start position. When CEN = 1, it shifts COM1 by one line (13 raster-rows) and outputs COM1 from the center of the screen (the second line). For details, see the Partial-display-on Function section.

CMS: Selects the output shift direction of a common driver. When CMS = "0", COM1/52 shifts to COM1, and COM52/1 to COM52. When CMS = "1", COM1/52 shifts to COM52, and COM52/1 to COM1. Output position of a common driver shifts depending on the CEN bit setting. For details, see the Display On/Off Control section.

SGS: Selects the output shift direction of a segment driver. When SGS = "0", SEG1/120 shifts to SEG1, and SEG120/1 to SEG120. When SGS = "1", SEG1/120 shifts SEG120, and SEG120/1 to SEG1.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R2:	0	1	**0**	**NL2**	**NL1**	**NL0**	**0**	**CEN**	**CMS**	**SGS**

Figure 7 Driver Output Control Instruction

Table 27 NL Bits and Display Lines

NL2	NL1	NL0	Display Lines	Liquid Crystal Display Drive Duty Ratio	Common Driver Used
0	0	0	Segment display	1/2 Duty	COMS1, COMS2
0	0	1	One character line + segment display	1/15 Duty	COM1–13, COMS1, COMS2
0	1	0	Two character lines + segment display	1/28 Duty	COM1–26, COMS1, COMS2
0	1	1	Three character lines + segment display	1/41 Duty	COM1–39, COMS1, COMS2
1	0	0	Four character lines + segment display	1/54 Duty	COM1–52, COMS1, COMS2

LCD Driving Wave (R3)

B/C: Specifies the LCD alternating method. When B/C = "0", a B-pattern waveform is generated and alternates in every frame. When B/C = "1", a C-pattern waveform is generated and alternates (n-raster-row reversed AC drive) in each raster-row specified by NW4–NW0. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set and EOR = "1", the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and n raster-row.

NW4–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting. NW4–NW0 alternate in every n + 1 raster-row, and the first to the 32nd raster-row can be selected.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R3:	0	1	**B/C**	**EOR**	**0**	**NW4**	**NW3**	**NW2**	**NW1**	**NW0**

Figure 8 LCD Driving Wave Instruction

LCD Driving Control (R4)

BS2–0: Set the LCD drive bias values in the range of 1/2 to 1/8 bias. The LCD drive bias value can be selected according to the LCD drive duty and LCD drive voltage. For details, see the LCD Drive Bias Selector section.

CT4–CT0: Control the LCD drive voltage (potential difference between V1 and GND) to adjust contrast. A 32-step adjustment is possible. For details, see the Contrast Adjuster section.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R4:	0	1	**BS2**	**BS1**	**BS0**	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**

Figure 9 LCD Driving Control Instruction

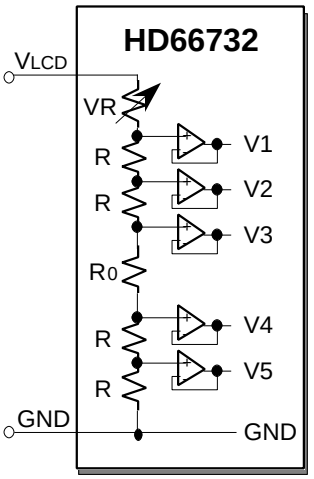


Figure 10 Contrast Adjuster

Table 28 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	Liquid Crystal Display Drive Bias Value
0	0	0	1/8 bias drive
0	0	1	1/7 bias drive
0	1	0	1/6 bias drive
0	1	1	1/5.5 bias drive
1	0	0	1/5 bias drive
1	0	1	1/4.5 bias drive
1	1	0	1/4 bias drive
1	1	1	1/2 bias drive

Table 29 CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value					Variable	CT Set Value					Variable
CT4	CT3	CT2	CT1	CT0	Resistor (VR)	CT4	CT3	CT2	CT1	CT0	Resistor (VR)
0	0	0	0	0	3.2 x R	1	0	0	0	0	1.6 x R
0	0	0	0	1	3.1 x R	1	0	0	0	1	1.5 x R
0	0	0	1	0	3.0 x R	1	0	0	1	0	1.4 x R
0	0	0	1	1	2.9 x R	1	0	0	1	1	1.3 x R
0	0	1	0	0	2.8 x R	1	0	1	0	0	1.2 x R
0	0	1	0	1	2.7 x R	1	0	1	0	1	1.1 x R
0	0	1	1	0	2.6 x R	1	0	1	1	0	1.0 x R
0	0	1	1	1	2.5 x R	1	0	1	1	1	0.9 x R
0	1	0	0	0	2.4 x R	1	1	0	0	0	0.8 x R
0	1	0	0	1	2.3 x R	1	1	0	0	1	0.7 x R
0	1	0	1	0	2.2 x R	1	1	0	1	0	0.6 x R
0	1	0	1	1	2.1 x R	1	1	0	1	1	0.5 x R
0	1	1	0	0	2.0 x R	1	1	1	0	0	0.4 x R
0	1	1	0	1	1.9 x R	1	1	1	0	1	0.3 x R
0	1	1	1	0	1.8 x R	1	1	1	1	0	0.2 x R
0	1	1	1	1	1.7 x R	1	1	1	1	1	0.1 x R

Power Control (R5)

AMP: When AMP = 1, each voltage follower for V1 to V5 pins and the booster are turned on. When AMP = 0, current consumption can be reduced while the display is not being used.

BT1-0: Switch the output of V5OUT between single, double, triple, and quadruple boost. The LCD drive voltage level can be selected according to its drive duty ratio and bias. A lower amplification of the booster consumes less current. When BT1/0 = "00", a single boost is output. When BT1/0 = "01", a double boost is output. When BT1/0 = "10", a triple boost is output. When BT1/0 = "11", a quadruple boost is output.

SLP: When SLP = 1, the HD66732 enters the sleep mode, where the internal operations are halted except for the key scan function and the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

a. Key scan data read
b. Key scan control (IRE, KF1/0 bit)
c. Power control (AMP, SLP, and STB bits)
d. Port control (PT2-0 bits)

During the sleep mode, the other RAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66732 enters the standby mode, where display operation and key scan completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. This setting can be used as the system wake-up, because an interrupt is generated when a specific key is pressed. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Voltage follower circuit on/off (AMP = 1/0)
c. Start oscillation
d. Key scan interrupt generation enabled/disabled (IRE = 1/0)
e. Port control (PT2-0 bits)

During the standby mode, the other RAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R5:	0	1	**AMP**	**0**	**BT1**	**BT0**	**0**	**0**	**SLP**	**STB**

Figure 11 Power Control Instruction

Key Scan Control (R6)

PT2-0: Control the output level of a port output pin (PORT2-PORT0). When PT0 = 0, the PORT0 pin outputs the GND level, and when PT0 = 1, it outputs the VCC level. Similarly, PT1 and PT2 bits control PORT1 and PORT2 output levels respectively.

KSB: When KSB = "1", the mode enters key standby and the key scan is stopped. In this case, key scan interrupts can be generated as well as in the standby mode. When KSB = "0", the keys are scanned normally.

IRE: When IRE = 1, it permits interrupts when a key is pressed. This causes interrupts to occur in the standby period when the oscillator clock is halted, as well as key scan interrupts during normal operation, allowing system wake-up.

KF1-0: Set the key scan cycle. The following table shows the key scan pulse width and key scan cycle used when the oscillation frequency (fosc) is 60 kHz, which depend on the oscillation frequency. For details, see the Key Scan Control section.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R6:	0	1	**0**	**PT2**	**PT1**	**PT0**	**KSB**	**IRE**	**KF1**	**KF0**

Figure 12 Key Scan Control Instruction

Table 30 KF Bits and Key Scan Cycle

KF1	KF0	Key Scan Pulse Width	Key Scan Cycle
0	0	0.25 ms	1.1 ms (64 clock cycles)
0	1	0.5 ms	2.1 ms (128 clock cycles)
1	0	1.1 ms	4.3 ms (256 clock cycles)
1	1	2.1 ms	8.5 ms (512 clock cycles)

Note: The data is a value obtained when the oscillation frequency (fosc) is 60 kHz. The value depends on the oscillation frequency.

Entry Mode (R7)

REV: When REV = "1", the REV displays all character and graphics display sections except for the segment display section with black-white reversal. For details, see the Reversed Display Function section.

SPR: When SPR = "1", the SPR displays combined character and graphics display screens (the super-imposed display mode). In this case, user fonts using the CGRAM in the character display mode cannot be displayed. For details, see the Super-imposed Display Function section.

GR: Activates the character mode when GR = “0”. Displays the font pattern on the CGROM or CGRAM according to the character code written in the DDRAM. Activates the graphics mode when GR = 1. Displays a given pattern according to the bit map data written in the CGRAM. In this case, data in the DDRAM is not used for display. Segment pattern display set to the SEGRAM is enabled both in the character mode and graphics mode. For details, see the Character Display Functions and Graphics Display Functions section.

RDM: When RDM = "0", the RDM increments or decrements the address counter value according to the I/D bit setting after reading the data from the DDRAM/CGRAM/SEGRAM. When RDM = "1", the address counter is not updated after the data has been read from the RAM. The address counter is used when the RAM data is read, modified, and written. Since the first read data is invalid, the read must be done twice. After writing to the RAM, the address counter value must be incremented or decremented.

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from DDRAM. The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to the writing and reading of CGRAM and SEGRAM.

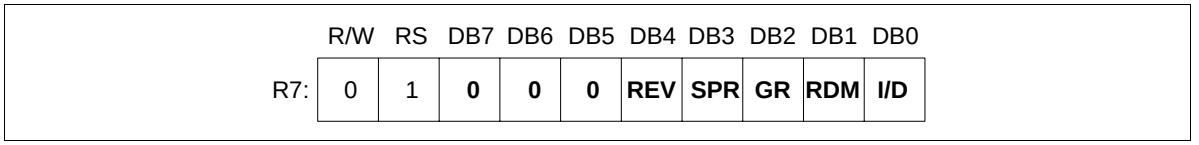


Figure 13 Entry Mode Set Instruction

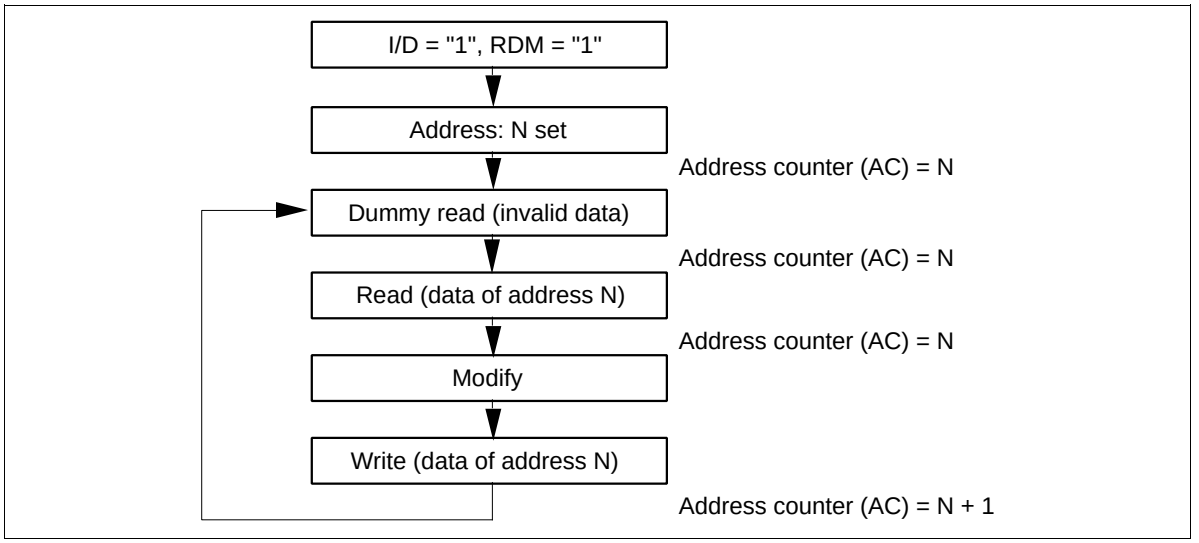


Figure 14 Read, Modify, and Write Sequences in Bus Interface Mode

Cursor Control (R8)

CH: Executes the cursor home instruction and sets DDRAM address 0 into the address counter (AC). The DDRAM contents do not change. The cursor or blinking goes to the top left of the display.

LC: When LC = 1, a cursor attribute is assigned to the line that contains the address counter (AC) value. Cursor mode can be selected with the B/W, C, and B bits. For details, see the Line-cursor Display section.

B/W: When B/W = 1 and LC = 1, the character at the cursor position is cyclically (every 32 frames) blink-displayed with black-white reversal.

When B/W = 1 and LC = 1, all characters including the cursor on the display line appear with black-white reversal. The characters do not blink. For details, see the Line-cursor Display section.

C: The cursor is displayed on the 13th raster-row when C = 1. The 13-dot cursor is ORed with the character pattern and displayed on the 13th raster-row.

B: The character indicated by the cursor blinks when B = 1. The blinking is displayed as switching between all black dots and displayed characters every 32 frames. The cursor and blinking can be set to display simultaneously. When LC =1, setting B = 1 alternately displays all white dots and character pattern in a line unit.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R8:	0	1	**0**	**0**	**0**	**CH**	**LC**	**B/W**	**C**	**B**

Figure 15 Cursor Control Instruction

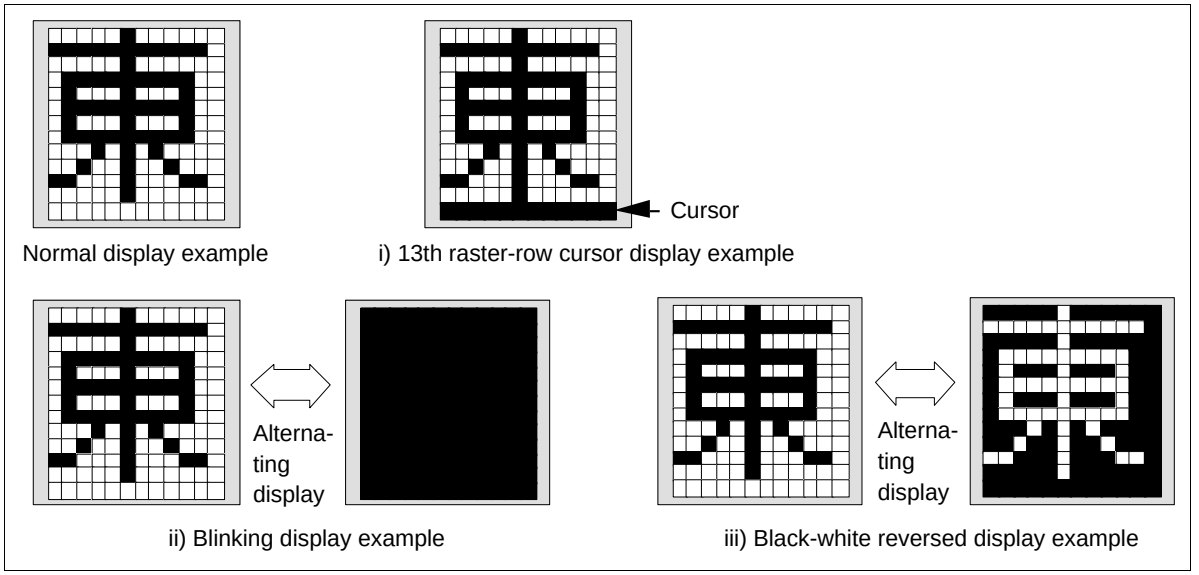


Figure 16 Cursor Control Examples

Display Control (R9)

DC: Character/graphics display is on when DC = 1 and off when DC = 0. When off, the display data remains in the DDRAM and CGRAM, and can be displayed instantly by setting D = 1.

DS: Icon mark segments are on when DS = 1 and off when DS = 0. When off, the display data remains in the SEGRAM, and can be displayed again instantly by setting DS = 1. When DC = DS = 0 and all displays are off, all LCD driver outputs are set to the GND level and the display is off. Because of this, the HD66732 can control charging current for the LCD with AC driving.

NC1–0: Sets the number of display characters per line.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R9:	0	1	**0**	**0**	**DC**	**DS**	**0**	**0**	**NC1**	**NC0**

Figure 17 Display Control Instruction

Table 31 NC Bits and Display Characters

NC1	NC0	Number of Display Characters	Segment Driver Used
0	0	6	SEG1–SEG72
0	1	8	SEG1–SEG96
1	0	10	SEG1–SEG120
1	1	Inhibited	—

Scroll Control (RA)

SN1-0: Specify the display start line output from COM1. The data is displayed sequentially from the first line to the fourth line then repeated from the first line.

SL3–0: Select the top raster-row to be displayed (display-start raster-row) in the display-start lines specified by SN1 to SN0. Any raster-row from the first to fourth can be selected. This function is used to achieve raster-row-unit vertical smooth scrolling together with SN1 to SN0. For details, see the Vertical Smooth Scroll section.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RA:	0	1	**0**	**0**	**SN1**	**SN0**	**SL3**	**SL2**	**SL1**	**SL0**

Figure 18 Scroll Control Instruction

Table 32 SN Bits and Display-start Lines

SN1	SN0	Display-start Line
0	0	1st line
0	1	2nd line
1	0	3rd line
1	1	4th line

Table 33 SL Bits and Display-start Raster-row

SL3	SL2	SL1	SL0	Display-start Raster-row
0	0	0	0	1st raster-row
0	0	0	1	2nd raster-row
0	0	1	0	3rd raster-row
0	0	1	1	4th raster-row
0	1	0	0	5th raster-row
	•			•
	•			•
	•			•
1	1	0	0	13th raster-row

Half-size ROM (HCGROM) Select (RB)

RL4–1: Switch the memory bank of the half-size HCGROM for the specified display line. Bank 0 and bank 2 of the HCGROM each incorporate 128 fonts, and display 256 fonts in total. The RL1–RL4 bits select HCGROM bank 0/1 for the display-line unit. When RL1 = "0", the first line selects bank 0. When RL1 = "1", the first line selects bank 1. The RL2, RL3, and RL4 bits select the second- to fourth-line memory banks, respectively.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RB:	0	1	**0**	**0**	**0**	**0**	**RL4**	**RL3**	**RL2**	**RL1**

Figure 19 HCGROM Select Instruction

Half-size ROM (HCGROM) Display Attribute (RC)

A11/10: Designate the display attributes of all half-size HCGROM fonts displayed in the first line.

A21/20: Designate the display attributes of all half-size HCGROM fonts displayed in the second line.

A31/30: Designate the display attributes of all half-size HCGROM fonts displayed in the third line.

A41/40: Designate the display attributes of all half-size HCGROM fonts displayed in the fourth line.

For details, see the Display Attribute Designation section. The full-size fonts are specified with the two-bit attribute codes in each character code.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RC:	0	1	**A41**	**A40**	**A31**	**A30**	**A21**	**A20**	**A11**	**A10**

Figure 20 HCGROM Display Attribute Instruction

Table 34 Attributes and Half-size Display State

A41	A40	A31	A30	A21	A20	A11	A10	Half-size Display State
0	0	0	0	0	0	0	0	Normal display
0	1	0	1	0	1	0	1	Black-white reversed display
1	0	1	0	1	0	1	0	Blinking display
1	1	1	1	1	1	1	1	Black-white reversed blinking display

RAM Address (RD/RE)

RM1-0: Select DDRAM, CGRAM, and SEGRAM. The selected RAM is accessed with this setting.

AD10-0: Initially set RAM addresses to the address counter (AC). Once the RAM data is written, the AC is automatically updated according to the I/D bit. This allows consecutive writing without resetting addresses. Once the RAM data is read, the AC is automatically updated when RDM = "0", but is not updated when RDM = "1". When the read, modify, and write are executed for every one-byte data, set RDM = "1". RAM address setting is not allowed in the sleep mode or standby mode.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RD:	0	1	**RM1**	**RM0**	**0**	**0**	**0**	**AD10**	**AD9**	**AD8**
RE:	0	1	**AD7**	**AD6**	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**

Figure 21 RAM Address Instruction

Table 35 RM Bits and RAM Selection

RM1	RM0	RAM Selection
0	0	DDRAM
0	1	Inhibited
1	0	CGRAM
1	1	SEGRAM

Table 36 AD Bits and DDRAM Setting

RM1/0	AD1–AD0	DDRAM Setting
00	"000"H–"013"H	Character code on the 1st line
00	"020"H–"033"H	Character code on the 2nd line
00	"040"H–"053"H	Character code on the 3rd line
00	"060"H–"073"H	Character code on the 4th line

Table 37 AD Bits and CGRAM Setting (GR = 0)

RM1/0	AD9–AD0	CGRAM (1) Setting in the Character Mode (GR = 0)
10	"000"H–"077"H	Upper font pattern of CGRAM characters (1) to (10)
10	"100"H–"177"H	Lower font pattern of CGRAM characters (1) to (10)
10	"200"H–"277"H	Upper font pattern of CGRAM characters (11) to (20)
10	"300"H–"377"H	Lower font pattern of CGRAM characters (11) to (20)
10	"400"H–"477"H	Upper font pattern of CGRAM characters (21) to (30)
10	"500"H–"577"H	Lower font pattern of CGRAM characters (21) to (30)

Table 38 AD Bits and CGRAM Setting (GR = 1)

RM1/0	AD10–AD0	CGRAM Setting in the Graphics Mode (GR = 1)
10	"000"H–"077"H	Bit map data for COM1 to COM8
10	"100"H–"177"H	Bit map data for COM9 to COM16
10	"200"H–"277"H	Bit map data for COM17 to COM24
10	"300"H–"377"H	Bit map data for COM25 to COM32
10	"400"H–"477"H	Bit map data for COM33 to COM40
10	"500"H–"577"H	Bit map data for COM41 to COM48
10	"600"H–"677"H	Bit map data for COM49 to COM52

Table 39 AD Bits and SEGRAM Setting

RM1/0	AD10–AD0	SEGRAM Setting
11	"000"H–"077"H	SEGRAM display data

RAM Data (RF)

WD7-0 : Write 8-bit data to the DDRAM and CGRAM, and lower 2-bit data to the SEGRAM. The DDRAM/CGRAM/SEGRAM is selected by the previous specification of the RM 1/0 bit. After a write, the address is automatically incremented or decremented by 1 according to the I/D bit setting in the entry mode set instruction. During the sleep and standby modes, the DDRAM, CGRAM, or SEGRAM cannot be accessed.

RD7-0 : Read 8-bit data from the DDRAM, CGRAM or SEGRAM. The DDRAM, CGRAM, or SEGRAM is selected by the previous specification of the RM 1/0 bit. In the parallel bus interface mode, the first-byte data read will be invalid immediately after the RAM address set, and the consecutive second-byte data will be read normally. In the serial interface mode, two bytes will be invalid immediately after the start byte, and the consecutive third-byte data will be read normally. For details, see the Serial Data Transfer section.

After a RAM read, the address is automatically incremented or decremented by 1 according to the entry mode set instruction. When RDM = "1", the address is not updated.

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RF:	0	1	**WD7**	**WD6**	**WD5**	**WD4**	**WD3**	**WD2**	**WD1**	**WD0**
RF:	1	1	**RD7**	**RD6**	**RD5**	**RD4**	**RD3**	**RD2**	**RD1**	**RD0**

Figure 22 RAM Data Instruction

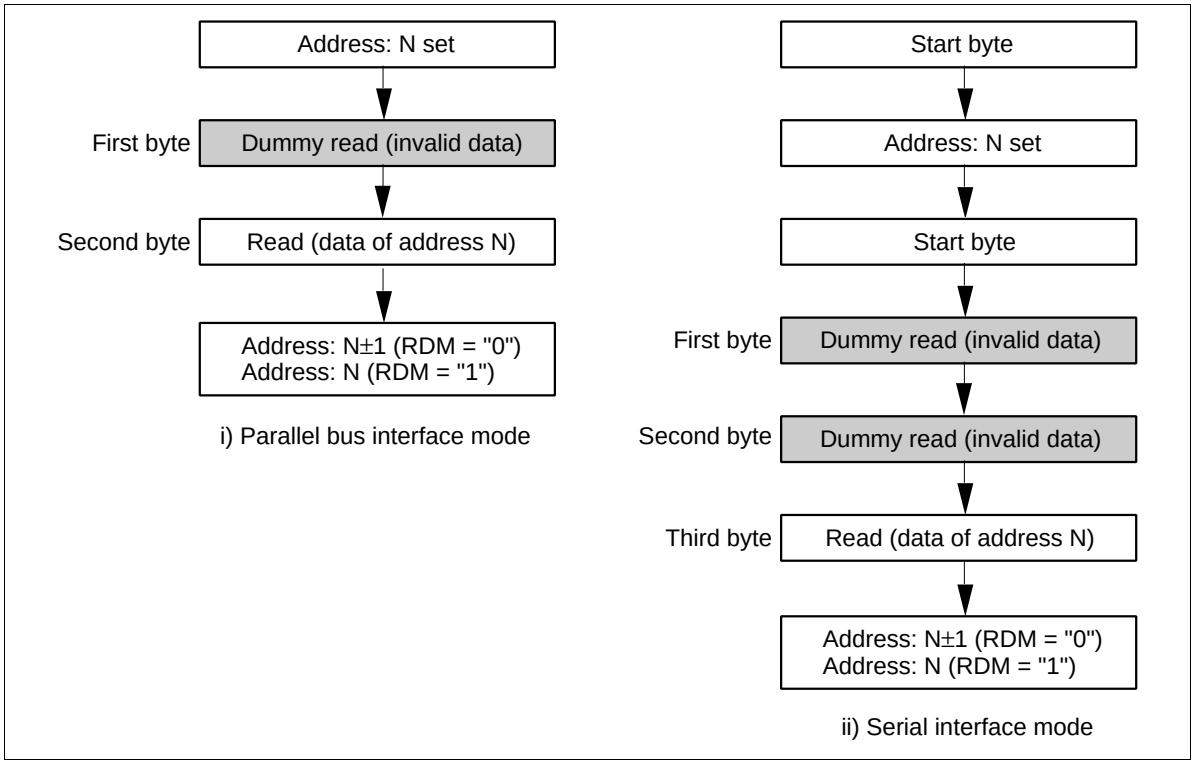


Figure 23 RAM Read Sequence

Table 40 Instruction Register List

No.	Index (Hex)	Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
IR	—	Index	0	0	—	—	—	—	ID3	ID2	ID1	ID0	Sets the register number of the instruction register to be accessed. ID = 0000: R0– 1111: RF	0
SR	—	Status	1	0	BF	NF1	NF0	—	LF3	LF2	LF1	LF0	Reads the busy flag (BF), display line position (NF1/0), and display raster-row position (NL3–NL0) in the bus interface mode.	0
			1	0					KSD				Reads the key scan data (KSD) in the serial interface mode.	0
R0	0	Clear display	0	1	0	0	0	0	0	0	0	1	Clears display and sets address 0 into the address counter.	85*
R1	1	Start oscillation	0	1	0	0	0	0	0	0	0	1	Starts oscillation during the standby mode.	—
R2	2	Driver output control	0	1	0	NL2	NL1	NL0	0	CEN	CMS	SGS	Sets the number of display lines (NL2–0), centering (CEN), common driver shift direction (CMS), and segment driver shift direction (SGS).	0
R3	3	LCD drive waveform	0	1	B/C	EOR	0	NW4	NW3	NW2	NW1	NW0	Selects the LCD drive waveform (B/C), specifies the EOR output (EOR), and the number of n raster-rows (NW4–0).	0
R4	4	LCD drive control	0	1	BS2	BS1	BS0	CT4	CT3	CT2	CT1	CT0	Sets the LCD drive bias (BS2–0) and contrast adjustment (CT4–0).	0
R5	5	Power control	0	1	AMP	0	BT1	BT0	0	0	SLP	STB	Turns on the LCD power supply (AMP), and sets the boosting output ratio (BT1/0), sleep mode (SLP), and standby mode (STB).	0

Table 40 Instruction Register List (cont)

No.	Index (Hex)	Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
R6	6	Key scan control	0	1	0	PT2	PT1	PT0	KSB	IRE	KF1	KF0	Sets the port output control (PT2–0), key standby mode (KSB), key scan interrupt (IRE), and key scan cycle (KF1/0).	0
R7	7	Entry mode	0	1	0	0	0	REV	SPR	GR	RDM	I/D	Sets the black-white reversal (REV), super-imposed display (SPR), graphics mode (GR), read/modify/write (RDM), and address counter update direction after RAM access (I/D).	0
R8	8	Cursor control	0	1	0	0	0	CH	LC	B/W	C	B	Sets cursor home (CH), raster-row cursor (LC), black-white reversed cursor (B/W), 13th raster-row cursor (C), and blinking cursor (B).	0
R9	9	Display control	0	1	0	0	DC	DS	0	0	NC1	NC0	Sets display on (DC), segment display on (DS), and the number of display characters (NC1/0).	0
RA	A	Scroll control	0	1	0	0	SN1	SN0	SL3	SL2	SL1	SL0	Sets the display start line (SN1/0) and start raster-row (SL3–0).	0
RB	B	Half-size ROM select	0	1	0	0	0	0	RL4	RL3	RL2	RL1	Sets the half-size CGROM bank switch (RL1–4) every display line.	0
RC	C	Half-size display attribute	0	1	A41	A40	A31	A30	A21	A20	A11	A10	Sets the half-size display attributes every display line.	0
RD	D	RAM address set (upper)	0	1	RM1	RM0	0	0	0	AD10–8 (upper)			Initially sets the RAM select (RM1/0) and upper three bits of the RAM address (AD10–8).	0

Table 40 Instruction Register List (cont)

No.	Index (Hex)	Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
RE	E	RAM address set (lower)	0	1	AD7–0 (lower)								Initially sets the lower eight bits of the RAM address (AD7–0).	0
RF	F	RAM data	0	1	Write data								Writes or reads the data to or from the DDRAM, CGRAM, or SEGRAM.	0
			1	1	Read data									

Note: The execution time depends on the supplied clock frequency or the internal oscillation frequency.

Bit definition:

BF = 1: Internal processing

NF1/0: Display read line positions

LF3–0: Display read raster-row positions

NL2–0: Display line setting (000: Segment only, 001: One line, 010: Two lines, 011: Three lines, 100: Four lines)

CEN = 1: Display position shift to the center of the screen

CMS = 0: COM1/52 => COM1

SGS = 0: SEG1/120 => SEG1

B/C = 0: B-pattern waveform drive

B/C = 1: C-pattern waveform drive

EOR = 1: EOR alternating drive at C-pattern waveform

NW4–0: Reversed number of n raster-rows at C-pattern waveform drive (alternating with the set value + one raster-row)

BS2–0: LCD drive bias select

CT4–0: Contrast adjustment

AMP = 1: Operating amplifier/booster on

BT1/0: Boost output ratio (00: Single, 01: Double, 10: Triple, 11: Quadruple)

SLP = 1: Sleep mode

STB = 1: Standby mode

PT2–0: Port output control (PT2 = 1: PORT2 = Vcc, PT1 = 1: PORT1 = Vcc, PT0 = 1: PORT0 = Vcc)

KSB = 1: Key standby mode (key scan stop)

IRE = 1: Key scan interrupt generation enabled

KF1/0: Key scan cycle set

REV = 1: Black-white reversed display, but excluding the segment display

SPR = 1: Super-imposed display of the character and graphics

GR = 0: Character display mode

GR = 1: Graphics display mode

RDM = 0: Automatically update the address counter after reading

RDM = 1: Do not automatically update the address counter after reading

I/D = 1: Address counter increment

I/D = 0: Address counter decrement

CH = 1: Cursor home

LC = 1: Raster-row cursor

B/W = 1: Black-white reversed cursor

C = 1: 13th raster-row cursor

B = 1: Blinking cursor

DC = 1: Character/graphics display on

DS = 1: Segment display on

NC1/0: Number of display characters (00: six, 01: eight, 10: 10)

SN1/0: Display-start line specifications (00: 1st line, 01: 2nd line, 10: 3rd line, 11: 4th line)

SL3–0: Scroll-start raster-row specifications (0000: 1st raster-row, 0100: 5th raster-row, 1000: 9th raster-row, 1100: 13th raster row)

RL1–4: Half-size CGROM memory bank selection (RL1: 1st line, RL2: 2nd line, RL3: 3rd line, RL4: 4th line)

A11/10: 1st-line half-size display attribute (00: normal, 01: black-white reversal, 10: blinking, 11: black-white reversed blinking)

A21/20: 2nd-line half-size display attribute
A31/30: 3rd-line half-size display attribute
A41/40: 4th-line half-size display attribute
RM1/0: RAM selection (00/01: DDRAM, 10: CGRAM, 11: SEGRAM)
AD10–0: RAM address

Reset Function

The HD66732 is internally initialized by RESET input. During initialization, the system executes a clear display instruction after reset is canceled. The system executes the other instructions during the reset period. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period and the clear display instruction is executed following reset cancellation, no instruction or RAM data access from the MPU is accepted. The reset input must be held for at least 1 ms. Any initializing instruction must wait for 200 clock cycles after the reset is canceled so that execution of the clear display instruction can be completed.

Instruction Set Initialization:

1. Clear display executed (writes half-size space code A0H to DDRAM)
2. Start oscillation executed
3. Driver output control (NL2–0 = 100: 1/54 duty drive, CEN = 0, SGS = 0, CMS = 0, CEN = 0)
4. LCD waveform control (B/C = 0: B-pattern waveform, EOR = 0, NW4–0 = 0000)
5. LCD drive control (BS2–0 = 000: 1/8 bias drive, CT4–0 = 00000: Weak contrast)
6. Power control (AMP = 0: LCD power off, BT1/0 = 00: Single boost, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
7. Key scan control (KSB = 0: Key scan, IRE = 0: Key scan interrupt (IRQ) generation disabled, KF1/0 = 00: Key scan set to 64 cycles)
8. Port control (PT2/1/0 = 000: PORT2/1/0 output = GND level)
9. Entry mode set (REV = 0, SPR = 0, GR = 0: Character display mode, RDM = 0, I/D = 1: Increment by 1)
10. Cursor control (CH = 0: Cursor home, LC = 0, B/W = 0, C = 0, B = 0)
11. Display control (DC/DS = 00: Display off, NC1/0 = 00: six-character display)
12. Scroll control (SN1/0 = 00, SL3/2/1/0 = 0000: First raster-row displayed at the top of the first line)
13. Half-size ROM control (RL4/3/2/1 = 0000: Bank 0 selection)
14. Half-size display attribute (A41/40 = 00, A31/30 = 00, A21/20 = 00, A11/10 = 00: Normal half-size display)
15. RAM address (RM1/0 = 00: DDRAM selection, AD10–0 = 000H)

RAM Data Initialization:

1. DDRAM

   All addresses are initialized to A0H by the clear-display instruction after the reset is canceled.
2. CGRAM/SEGRAM

   This is not automatically initialized by the reset input but must be initialized by software while the display is off (D = 0).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Outputs GND level
2. Booster output pins (VLOUT): Outputs V_{CC} level
3. Oscillator output pin (OSC2): Outputs oscillation signal
4. Key strobe pins (KST0 to KST3): Output strobe signals at specified time intervals
5. Key scan interrupt pin (IRQ*): Outputs V_{CC} level
6. General output ports (PORT0–PORT2): Output GND level

Serial Data Transfer

Setting the IM1 and IM2 pins (interface mode pins) to the GND level allows standard clock-synchronized serial data transfer, using the chip select line (CS*), serial data line (SDA), and serial transfer clock line (SCL). For a serial interface, the IM0/ID pin function uses an ID pin.

The HD66732 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66732 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66732. The HD66732, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66732 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, an instruction can be issued or key scan data can be read, and when RS = 1, data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit) as shown in table 41.

After receiving the start byte, the HD66732 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. To transfer data consecutively, note that only the clear-display instruction requires 85 clock cycles. Wait after issuing the clear-display instruction.

Two bytes of RAM read data after the start byte are invalid. The HD66732 starts to read correct RAM data from the third byte.

Table 41 Start Byte Format

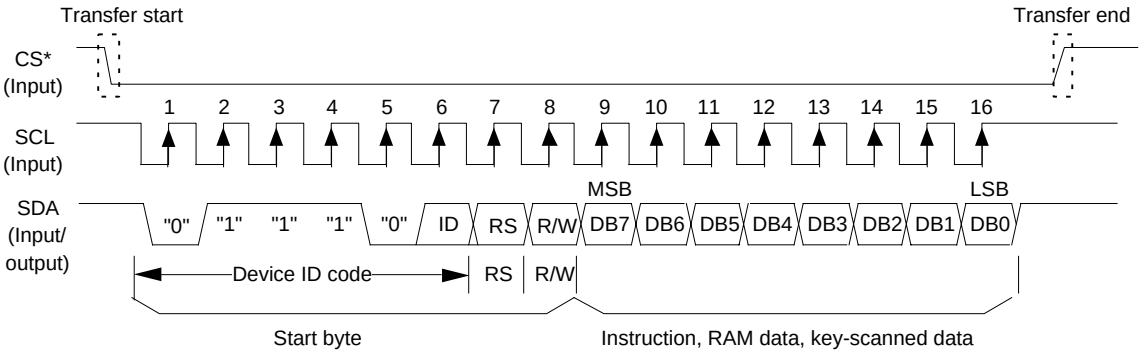
Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

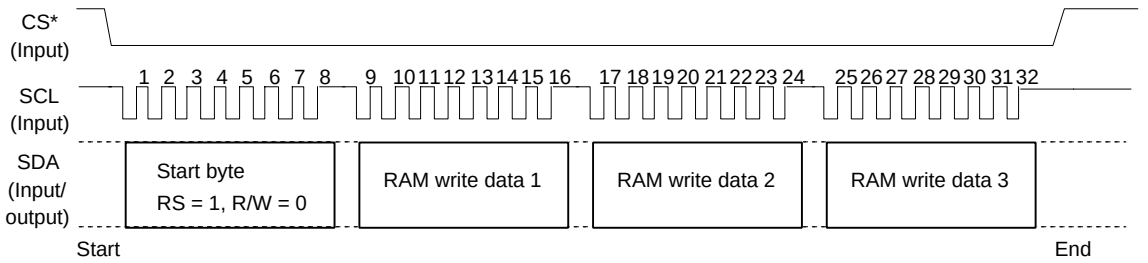
Table 42 RS and R/W Bit Function

RS	R/W	Function
0	0	Sets index address
0	1	Reads status register
1	0	Writes control register, RAM address, or RAM data
1	1	Reads RAM data

a) Basic Data-transfer Timing through Clock-synchronized Serial Bus Interface

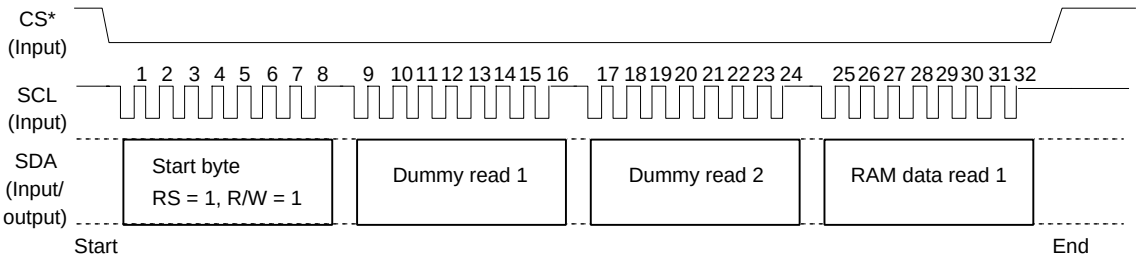


b) Consecutive RAM Data-transfer Timing



Note: The RAM address setting registers (RC and RD) select the write RAM or set the write-start RAM address.

c) RAM Data Read-transfer Timing



Note: Two bytes of the RAM read data after the start byte are invalid. The HD66732 starts to read the correct RAM data from the third byte.

Figure 24 Clock-synchronized Serial Interface Timing Sequence

Key Scan Control

The key matrix scanner senses and holds the key states at each rising edge of key strobe signals (KST) that are output by the HD66732. The key strobe signals are output as time-multiplexed signals from KST0 to KST3. After passing through the key matrix, these strobe signals are used to sample the key state of eight inputs KIN0 to KIN7, enabling up to 32 keys to be scanned.

The states of inputs KIN0 to KIN7 are sampled by key strobe signal KST0 and latched into the SCAN0 register. Similarly, the data sampled by strobe signals KST1 to KST3 is latched into the SCAN1 to SCAN3 registers, respectively. Key pressing is stored as 1 in these registers.

The generation cycle and pulse width of the key strobe signals depend on the operating frequency (oscillation frequency) of the HD66732 and the key scan cycle determined by the KF0 and KF1 bits. For example, when the operating frequency is 60 kHz and KF0 and KF1 are both 10, the generation cycle is 4.3 ms and the pulse width is 1.1 ms. When the operating frequency (oscillation frequency) is changed, the above generation cycle and the pulse width are changed in inverse proportion.

In order to compensate for the mechanical features of the keys, such as chattering and noise and for the key-strobe generation cycle and the pulse width of the HD66732, software should read the scanned data two to three times in succession to obtain valid data. Multiple keypress combinations should also be processed in the software.

Up to three keys can be pressed simultaneously. Note, however, that if the third key is pressed on the intersection between the rows and columns of the first two keys pressed, incorrect data will be sampled. For three-key input, the third key must be on a separate column or row.

Additionally, the HD66732 supports the key standby mode in which only the key scan circuit enters the standby state. When 1 is set to the key standby mode setting bit (KSB), only key scanning is stopped. In this case, as well as in the normal standby mode, the key scan interrupt function can be used. For example, this function is used when only key scanning is stopped to improve the sensitivity of the wave received by a radio system during calling.

The input pins KIN0 to KIN7 are pulled up to V_{CC} with internal MOS transistors (see the Electrical Characteristics section). External resistors may also be required to further pull the voltages up when the internal pull-ups are insufficient for the desired noise margins or for a large key matrix.

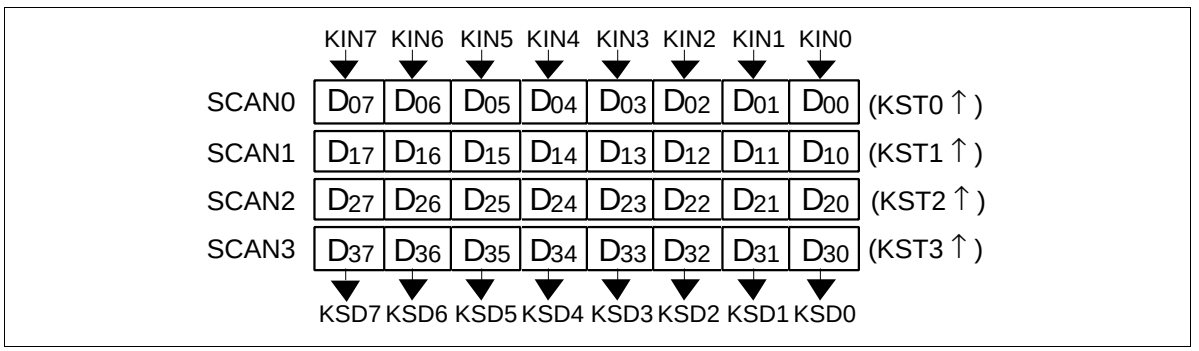


Figure 25 Key Scan Register Configuration

Table 43 Key Scan Cycles for Each Operating Frequency

KF1	KF0	Key Scan Pulse Width	Key Scan Cycle
0	0	0.26 ms	1.1 ms (64 clock cycles)
0	1	0.5 ms	2.1 ms (128 clock cycles)
1	0	1.1 ms	4.3 ms (256 clock cycles)
1	1	2.1 ms	8.5 ms (512 clock cycles)

Note: The data is a value obtained when the oscillation frequency (fosc) is 60 kHz. The value depends on the oscillation frequency.

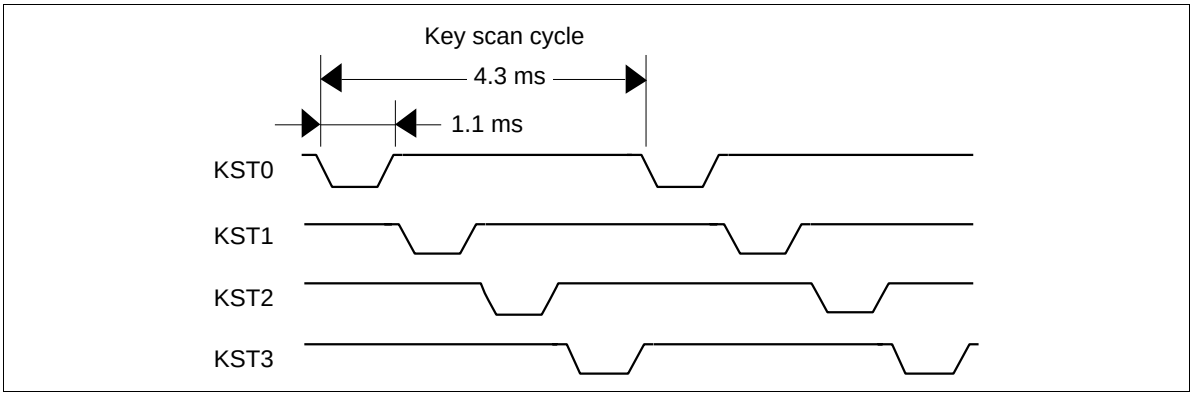


Figure 26 Key Strobe Output Timing (KF1/0 = 10, fcp/fosc = 60 kHz)

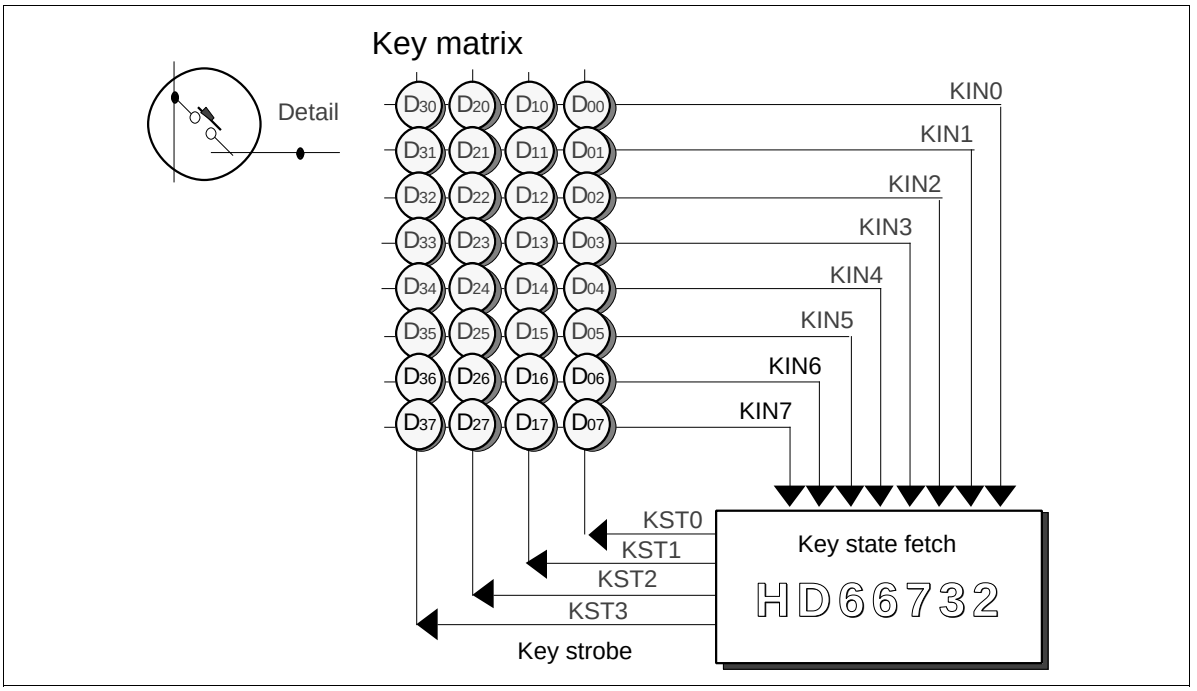


Figure 27 Key Scan Configuration

The key-scanned data can be read by an MPU via a serial interface. First, a start byte should be transferred. After the HD66732 has received the start byte, the MPU reads scan data KSD7 to KSD0 from the SCAN0 register starting from the MSB. Similarly, the MPU reads data from SCAN1, SCAN2 and SCAN3 in that order. After reading SCAN3, the MPU starts at SCAN0 again.

The HD66732 may be read out while it is latching scan data and is thus unstable. Consequently, it should also be reconfirmed with software if required.

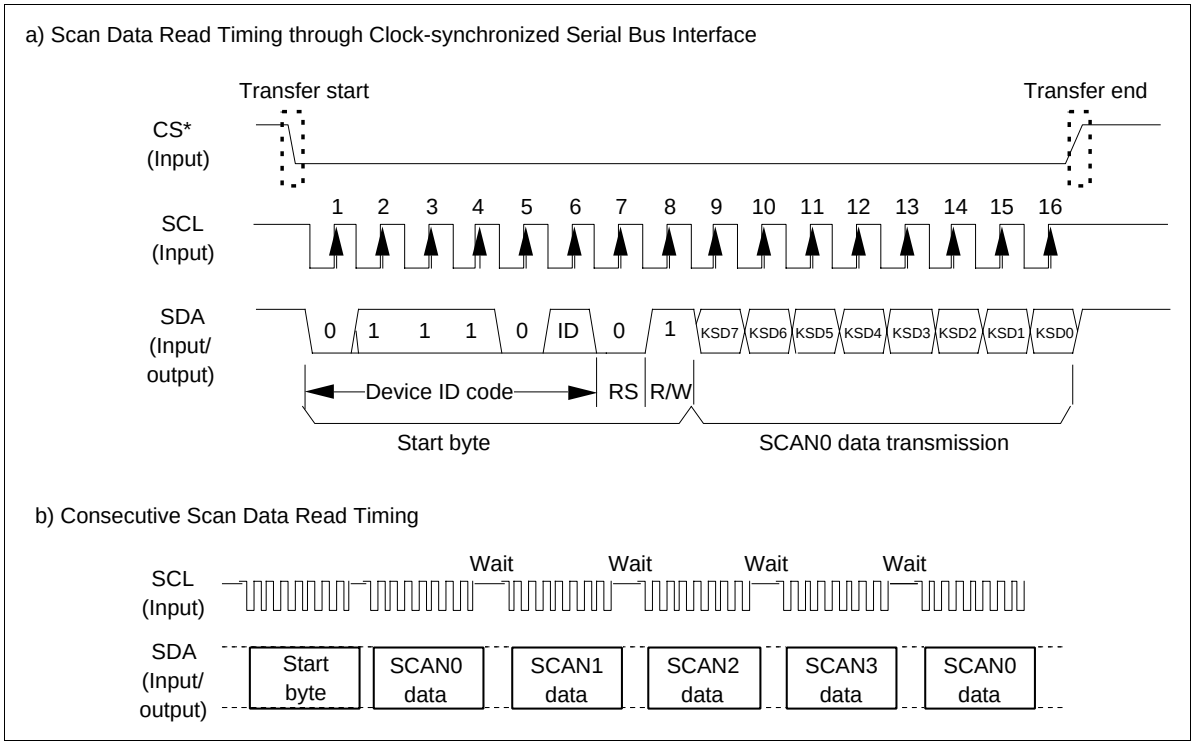


Figure 28 Scan Data Serial Transfer Timing

Key Scan Interrupt (Wake-up Function)

If the interrupt enable bit (IRE) is set to 1, the HD66732 sends an interrupt signal to the MPU on detecting that a key has been pressed in the key scan circuit by setting the IRQ* output pin to a low level. An interrupt signal can be generated by pressing any key in a 32-key matrix. The interrupt level continues to be output during the key scan cycle while the key is being pressed.

Normal key scanning is performed and interrupts can occur in the HD66732 sleep mode (SLP = 1). Accordingly, power consumption can be minimized in the sleep mode, by triggering the MPU to read key states via the interrupt which is generated only when the HD66732 detects a key input. For details, see the Sleep Mode section.

On the other hand, normal key scanning stops in the standby mode (STB = 1) or in the key standby mode (KSB = 1). During this period, the KST0 output is kept low, so the HD66732 can always monitor eight key inputs (KIN0-KIN7) connected to KST0 when RS = GND. Therefore, if any of the eight keys is pressed, an interrupt occurs. When RS = Vcc, all outputs KST0 to KST3 are kept low, so the HD66732 can always monitor 32 key inputs. If any of the 32 keys is pressed, an interrupt occurs. Accordingly, power consumption or noise generation can be further minimized in the standby mode, where the whole system is inactive, by triggering the MPU via the interrupt which is generated only when the HD66732 detects a key input from the above keys. For details, see the Standby Mode section.

The IRQ* output pin is pulled up to the V_{CC} with an internal MOS resistor of approximately 50 kΩ. Additional external resistors may be required to obtain stronger pull-ups. Interrupts may occur if noise occurs in KIN0-KIN7 input during key scanning. Interrupts must be inhibited if not needed by setting the interrupt enable bit (IRE) to 0.

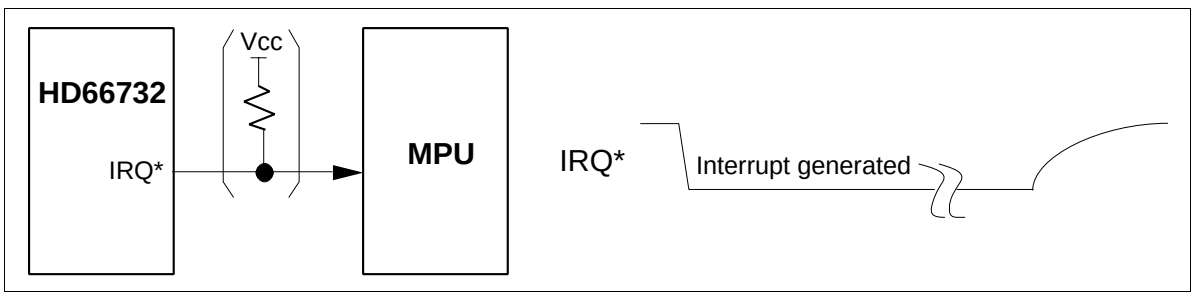


Figure 29 Interrupt Generator

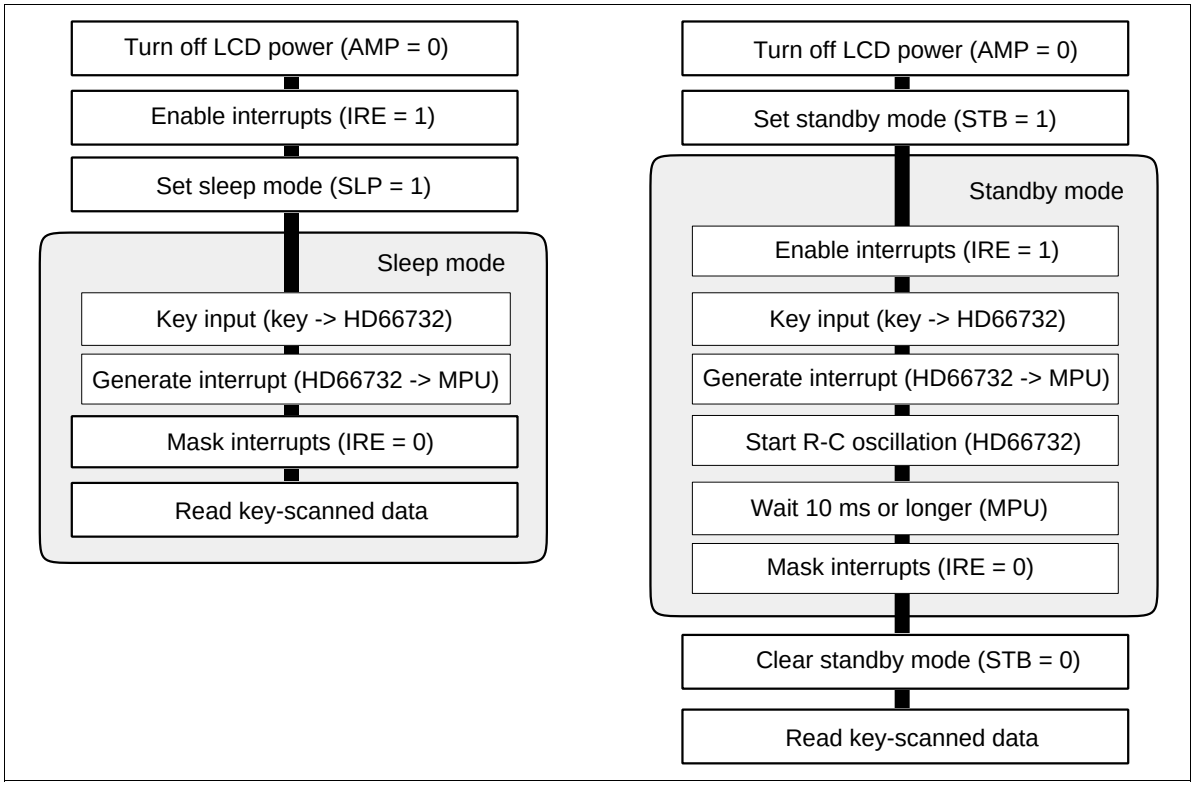


Figure 30 Key Scan Interrupt Processing Flow in Sleep and Standby Modes

Parallel Data Transfer

8-bit Interface

Setting the IM2/1/0 (interface mode) to the GND/Vcc/GND level allows E-clock-synchronized 8-bit parallel data transfer. Setting the IM2/1/0 (interface mode) to the Vcc/Vcc/GND level allows 80-system 8-bit parallel data transfer. When the number of buses or the mounting area is limited, use a 4-bit bus interface or serial data transfer.

Using a parallel bus interface disables the key scan function. To prevent this, use a clock-synchronized serial interface.

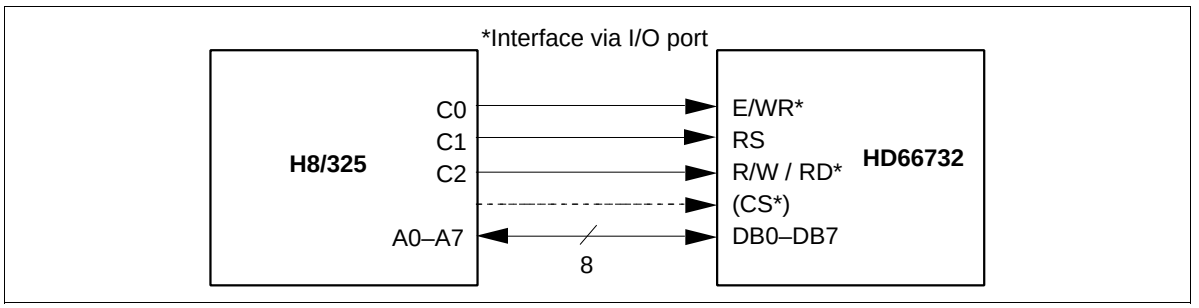


Figure 31 Interface to 8-bit Microcomputer

4-bit Interface

Setting the IM2/1/0 (interface mode) to the GND/Vcc/Vcc level allows E-clock-synchronized 4-bit parallel data transfer using pins DB7/KIN7-DB4/KIN4. Setting the IM2/1/0 (interface mode) to the Vcc/Vcc/Vcc level allows 80-system 4-bit parallel data transfer. 8-bit instructions and RAM data are divided into four upper/lower bits and the transfer starts from the upper four bits.

Using a parallel bus interface disables the key scan function. To prevent this, use a clock-synchronized serial interface.

Note: Transfer synchronization function for a 4-bit bus interface
The HD66732 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 4-bit data transfer in the 4-bit bus interface. Noise causing transfer mismatch between the four upper and lower bits can be corrected by a reset triggered by consecutively writing a 0000 instruction four times. The next transfer starts from the upper four bits. Executing synchronization function periodically can recover any runaway in the display system.

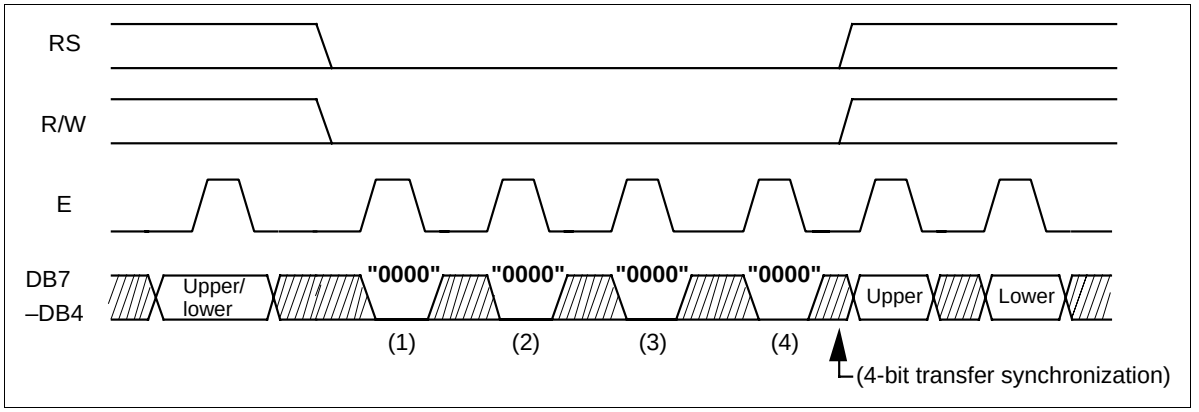


Figure 32 4-bit Transfer Synchronization

Oscillation Circuit

The HD66732 can either be supplied with operating pulses externally (external clock mode), oscillate using an internal R-C oscillator with an external oscillator-resistor. External oscillator-resistors (Rf) can adjust the oscillating frequency. When the power-supply voltage is minimized, the frequency is lowered. See the Electrical Characteristics Notes section for the relationships between the Rf resistance value and oscillating frequency.

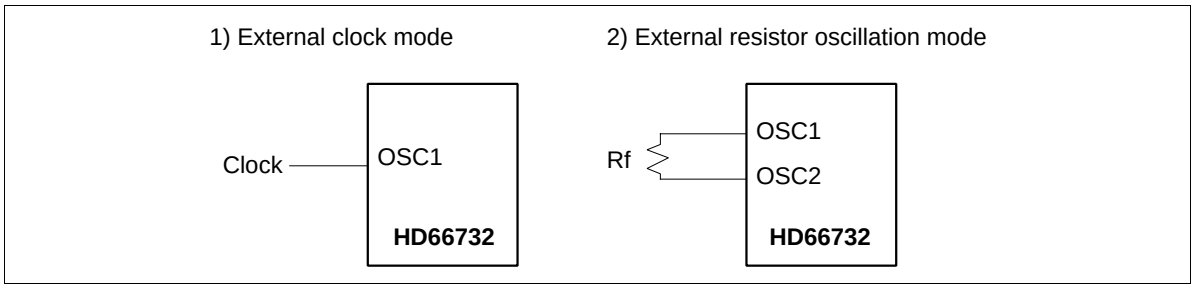


Figure 33 Oscillation Circuits

Table 44 Relationship between Drive Duty Ratio and Frame Frequency

	Number of Display Characters		
	6-character display (NC = 00)	8-character display (NC = 01)	10-character display (NC = 10)
	Recommended R-C Oscillating Frequency		
Frame Frequency	**45 kHz**	**60 kHz**	**76 kHz**
Segment display (NL = 001)	70 Hz	70 Hz	70 Hz
1-line display (NL = 001)	73 Hz	71 Hz	70 Hz
2-line display (NL = 010)	73 Hz	71 Hz	71 Hz
3-line display (NL = 011)	69 Hz	73 Hz	71 Hz
4-line display (NL = 100)	70 Hz	70 Hz	70 Hz

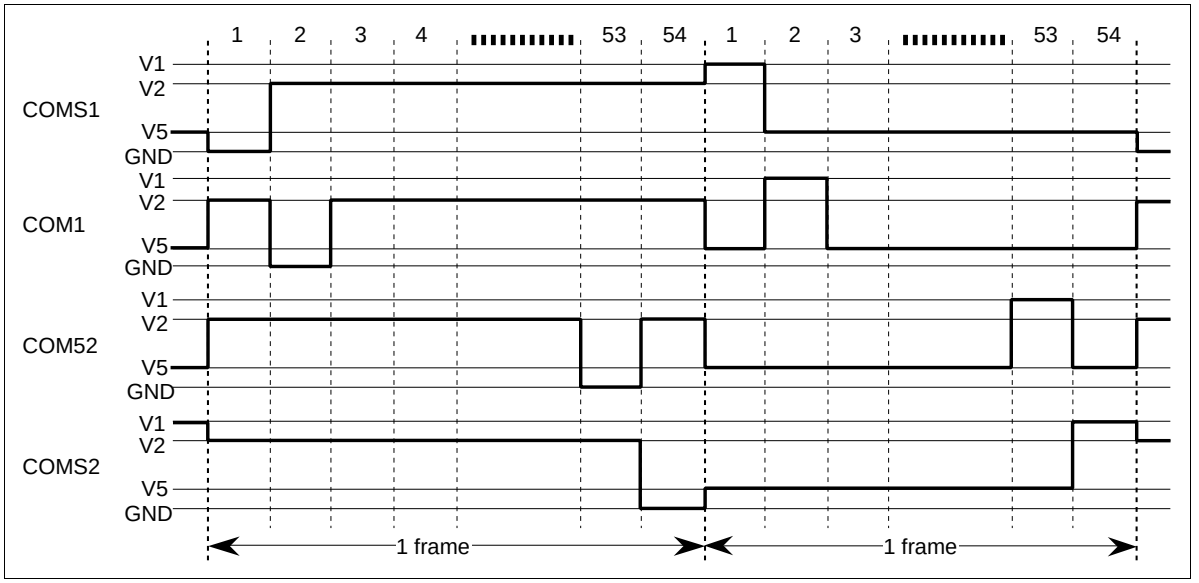


Figure 34 LCD Drive Output Waveform (4-line Display with 1/54 Multiplexing Duty Ratio)

n-raster-row Reversed AC Drive

The HD66732 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 32 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than three lines (1/42 duty), the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality. Determine the number of raster-rows n for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.

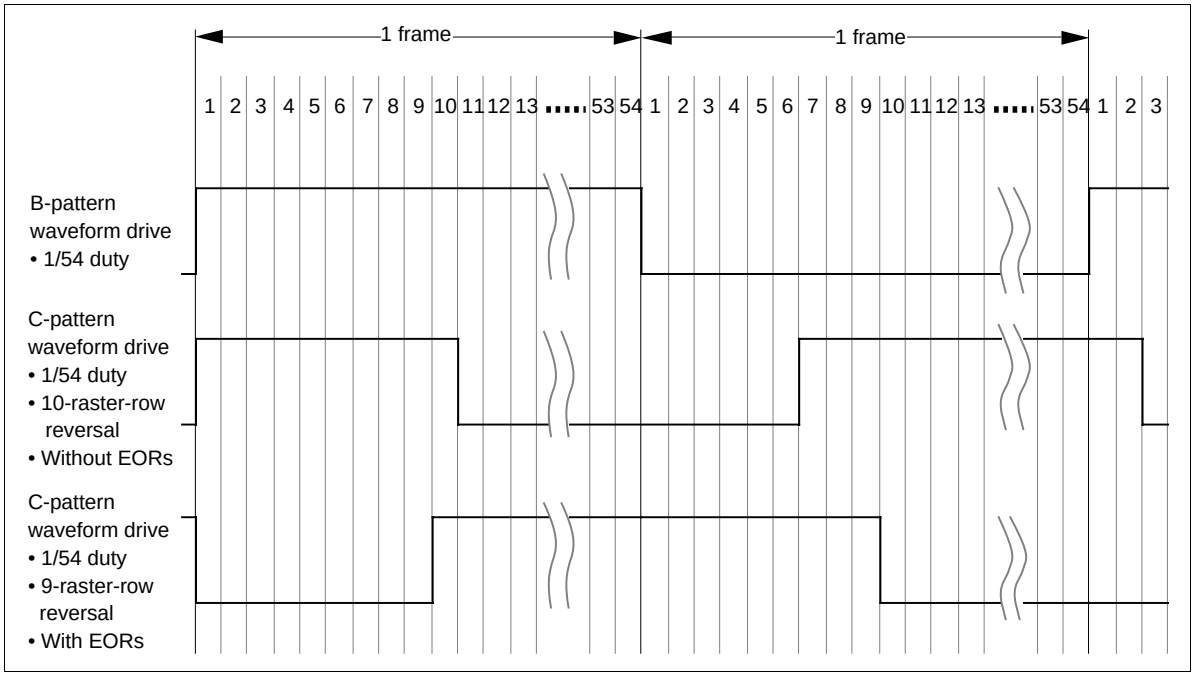


Figure 35 Example of an AC Signal under n-raster-row Reversed AC Drive

Liquid Crystal Display Voltage Generator

When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal booster, circuits should be connected as shown in figure 36. Here, contrast can be adjusted by software through the CT bits of the contrast adjustment register.

The HD66732 incorporates a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, the potential difference between V_{LCD} and V1 must be 0.1 V or higher, and ones between V4 and GND between V2 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.5 µF between each internal operational amplifier V1OUT to V5OUT output and GND and stabilize the output level of the operational amplifier.

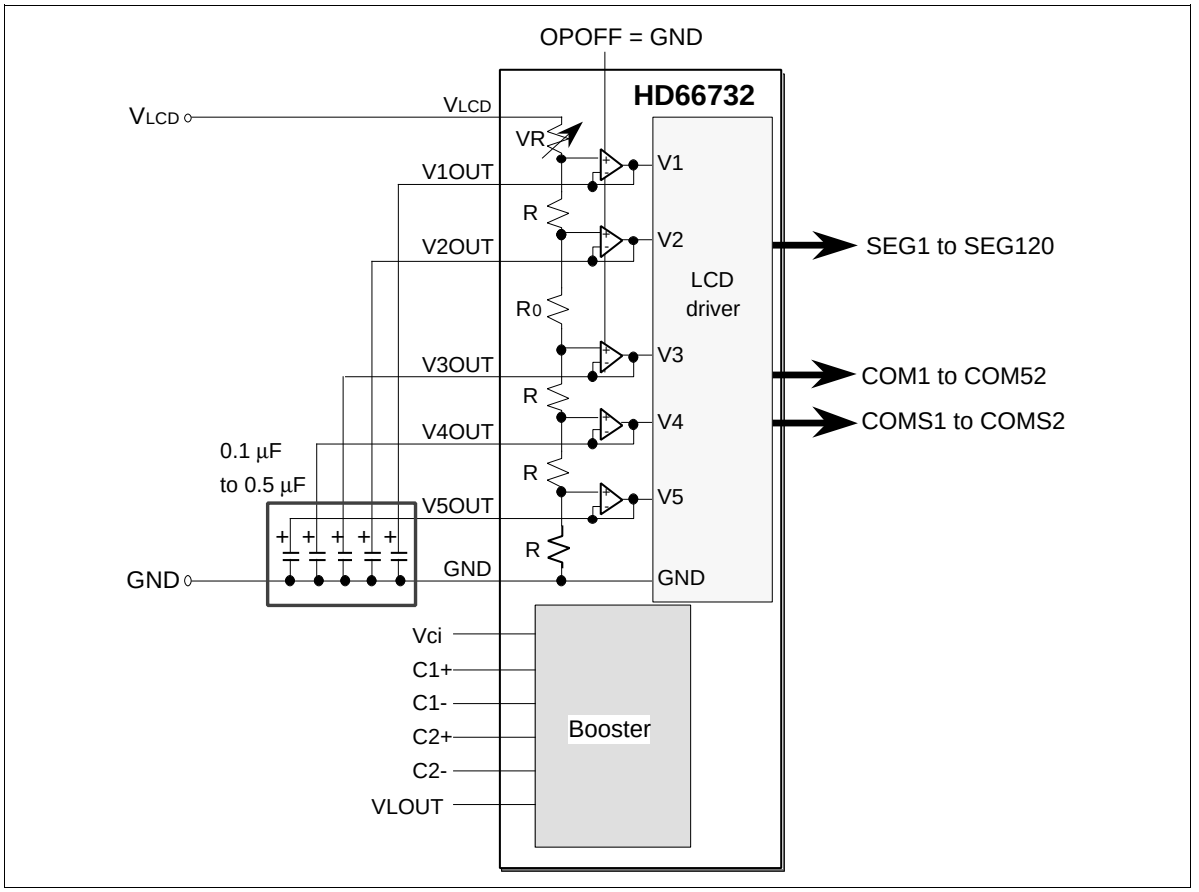


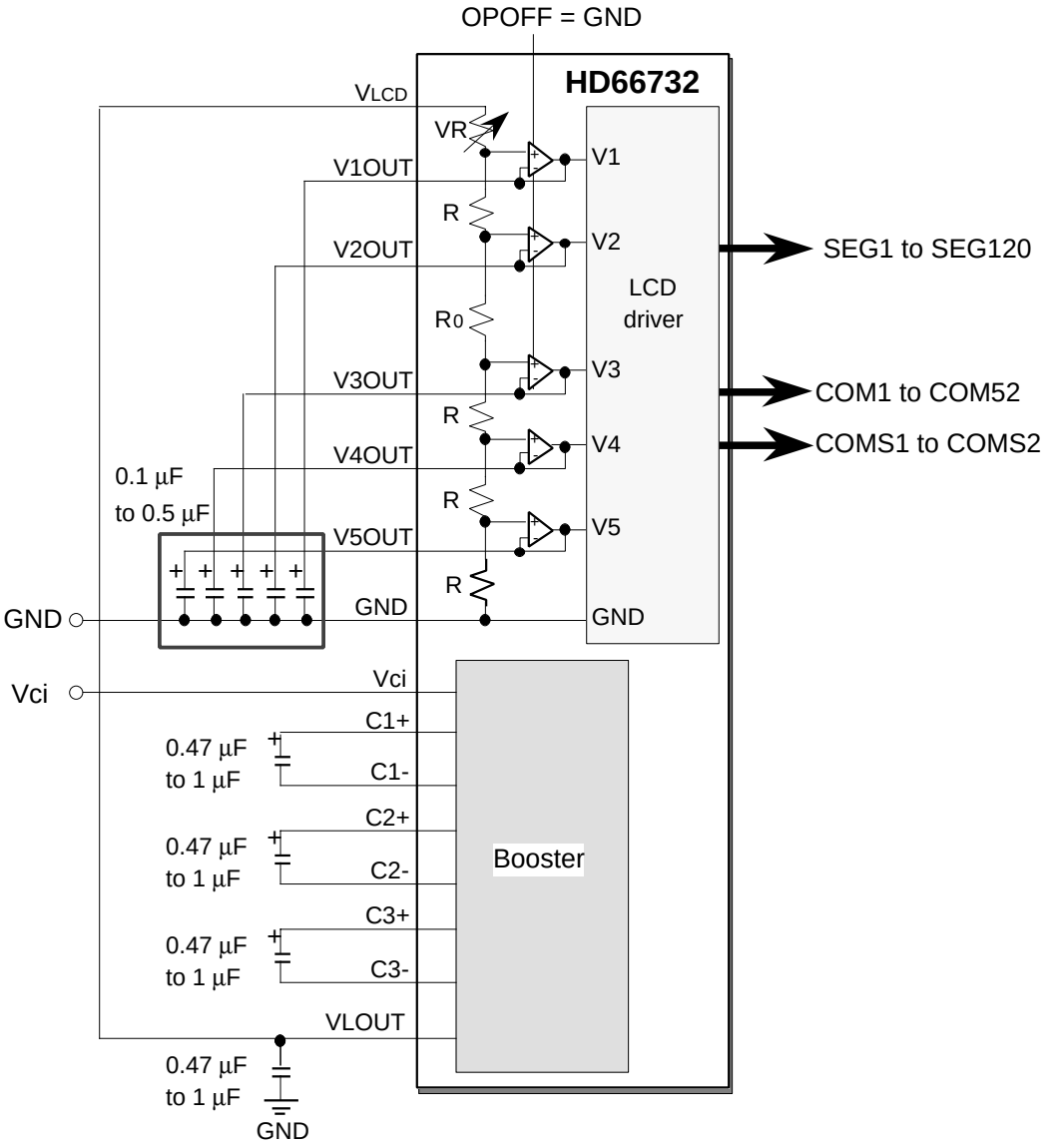
Figure 36 External Power Supply Circuit for LCD Drive Voltage Generation

When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal booster, circuits should be connected as shown in figure 37. Here, contrast can be adjusted through the CT bits of the contrast control instruction. Temperature can be compensated either through the CT bits or by controlling the reference voltage for the booster (Vci pin) using a thermistor.

Note that Vci is both a reference voltage and power supply for the booster. The reference voltage must therefore be adjusted using an emitter-follower or a similar element so that sufficient current can be supplied. In this case, Vci must be equal to or smaller than the V_{CC} level.

The HD66732 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, the potential difference between V_{LCD} and V1 must be 0.1 V or higher, and ones between V4 and GND and between V2 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.5 µF between each internal operational amplifier V1OUT to V5OUT output and GND and stabilize the output level of the operational amplifier.



Notes:
1. The reference voltage input (Vci) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating for the liquid-crystal power supply voltage (13 V). Particularly, Vci must be 3.3 V or less for quadruple boosting.
2. Vci is both a reference voltage and power supply for the booster; connect it to Vcc directly or combine it with a transistor so that sufficient current can be obtained.
3. Vci must be smaller than Vcc.
4. Polarized capacitors must be connected correctly.
5. Circuits for temperature compensation should be based on the sample circuit in figure 38.

Figure 37 Internal Booster for LCD Drive Voltage Generation

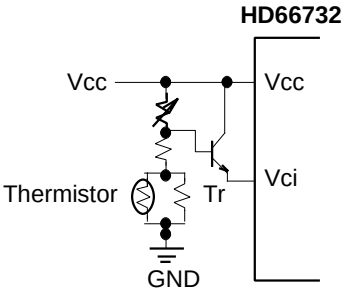


Figure 38 Temperature Compensation Circuit

Instruction bits (BT1/0) can optionally select the boosting multiplying factor of the internal booster. According to the display status, power consumption can be reduced by changing the LCD drive duty and the LCD drive bias, and by controlling the boosting multiplying factor for the minimum requirements. For details, see the Partial-display-on Function section.

Due to the maximum boosting multiplying factor, the following external capacitor needs to be connected. For example, when the maximum boosting is tripled, the capacitors between C3+ and C3– for quadruple boosting are not needed, so these pins must be open.

Table 45 VLOUT Output Status

BT1	BT0	VLOUT Output Status
0	0	Single output (The potential difference between Vci and GND is output to the VLOUT.)
0	1	Double boosting output
1	0	Triple boosting output
1	1	Quadruple boosting output

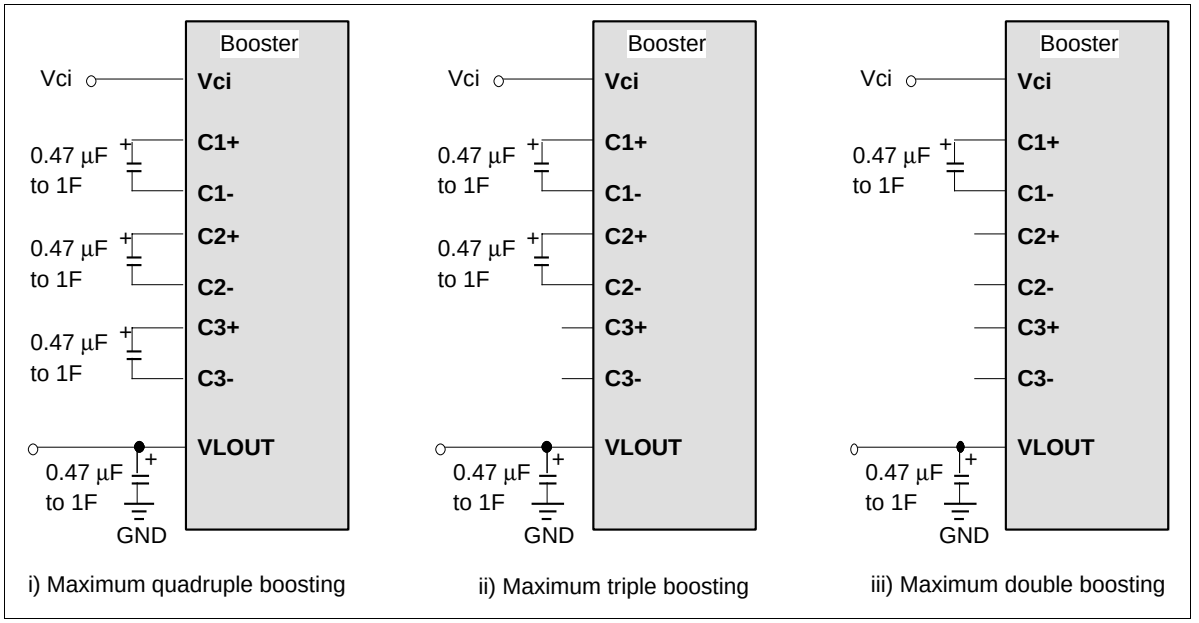


Figure 39 Booster Output Multiplying Factor Switching

Contrast Adjuster

Software can adjust contrast for an LCD by varying the liquid-crystal drive voltage (potential difference between V_{LCD} and V1) through the CT bits of the contrast adjustment register (electron volume function). The value of a variable resistor (VR) can be adjusted within a range from 0.1 x R through 3.2 x R, where R is a reference resistance obtained by dividing the total resistance between V_{LCD} and V1.

The HD66732 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder resistors, which generate different liquid-crystal drive voltages. Thus, CT4-0 bits must be adjusted so that the potential difference between V_{LCD} and V1 is 0.1 V or higher, and ones between V4 and GND and between V2 and GND are 1.4 V or higher when liquid-crystal drives.

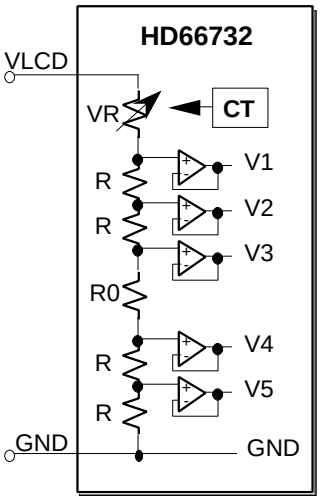


Figure 40 Contrast Adjuster

Table 46 Contrast Adjustment Bits (CT) and Variable Resistor Values

CT Set Value					Variable Resistor Value (VR)	Potential Difference between V1 and GND	Display Color
CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	3.2 x R	(Small)	(Light)
0	0	0	0	1	3.1 x R		
0	0	0	1	0	3.0 x R		
0	0	0	1	1	2.9 x R		
0	0	1	0	0	2.8 x R		
0	0	1	0	1	2.7 x R		
0	0	1	1	0	2.6 x R		
0	0	1	1	1	2.5 x R		
0	1	0	0	0	2.4 x R		
0	1	0	0	1	2.3 x R		
0	1	0	1	0	2.2 x R		
0	1	0	1	1	2.1 x R		
0	1	1	0	0	2.0 x R		
0	1	1	0	1	1.9 x R		
0	1	1	1	0	1.8 x R		
0	1	1	1	1	1.7 x R		
1	0	0	0	0	1.6 x R		
1	0	0	0	1	1.5 x R		
1	0	0	1	0	1.4 x R		
1	0	0	1	1	1.3 x R		
1	0	1	0	0	1.2 x R		
1	0	1	0	1	1.1 x R		
1	0	1	1	0	1.0 x R		
1	0	1	1	1	0.9 x R		
1	1	0	0	0	0.8 x R		
1	1	0	0	1	0.7 x R		
1	1	0	1	0	0.6 x R		
1	1	0	1	1	0.5 x R		
1	1	1	0	0	0.4 x R		
1	1	1	0	1	0.3 x R		
1	1	1	1	0	0.2 x R		
1	1	1	1	1	0.1 x R	(Large)	(Deep)

Table 47 Contrast Adjustment per Bias Drive Voltage

Bias	LCD drive voltage: V_{DR}	Contrast adjustment range
1/8 bias drive	$\frac{8 \times R}{8 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.714 \times (V_{LCD}-GND) \le V_{DR} \le 0.988 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{8 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{8 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/7 bias drive	$\frac{7 \times R}{7 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.686 \times (V_{LCD}-GND) \le V_{DR} \le 0.986 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{7 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{7 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/6 bias drive	$\frac{6 \times R}{6 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.652 \times (V_{LCD}-GND) \le V_{DR} \le 0.984 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{6 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{6 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/5.5 bias drive	$\frac{5.5 \times R}{5.5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.632 \times (V_{LCD}-GND) \le V_{DR} \le 0.982 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{5.5 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{5.5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/5 bias drive	$\frac{5 \times R}{5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.610 \times (V_{LCD}-GND) \le V_{DR} \le 0.980 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{5 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/4.5 bias drive	$\frac{4.5 \times R}{4.5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.556 \times (V_{LCD}-GND) \le V_{DR} \le 0.978 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{4.5 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{4.5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/4 bias drive	$\frac{4 \times R}{4 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.556 \times (V_{LCD}-GND) \le V_{DR} \le 0.976 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{4 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{4 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/2 bias drive	$\frac{2 \times R}{2 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.385 \times (V_{LCD}-GND) \le V_{DR} \le 0.952 \times (V_{LCD}-GND)$ - Limit of potential difference between V2 and GND : $\frac{2 \times R}{2 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{2 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]

LCD Drive Bias Selector

An optimum liquid crystal display bias value can be selected using BS2-0 bits, according to the liquid crystal drive duty ratio setting (NL2-0 bits). Liquid crystal display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is an ideal value where the optimum contrast is obtained. Driving by using a lower value than the optimum bias value provides lower contrast and lower liquid crystal display voltage (potential difference between V1 and GND). When the liquid crystal display voltage is insufficient even if a quadruple booster is used or output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid crystal bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT4-0 bits) and selecting the booster output level (BT1/0 bits).

$$\text{Optimum bias value for 1/N duty ratio drive voltage} = \frac{1}{\sqrt{N} + 1}$$

Table 48 Optimum Drive Bias Values

LCD drive duty ratio (NL2-0 set value)	1/54 duty ratio (NL2-0 = 100)	1/41 duty ratio (NL2-0 = 011)	1/28 duty ratio (NL2-0 = 010)	1/15 duty ratio (NL2-0 = 001)	1/2 duty ratio (NL2-0 = 000)
Optimum drive bias value (BS2-0 set value)	1/8 bias (BS2-0 = 000)	1/7 bias (BS2-0 = 001)	1/6 bias (BS2-0 = 010)	1/4.5 bias (BS2-0 = 101)	1/2 bias (BS2-0 = 111)

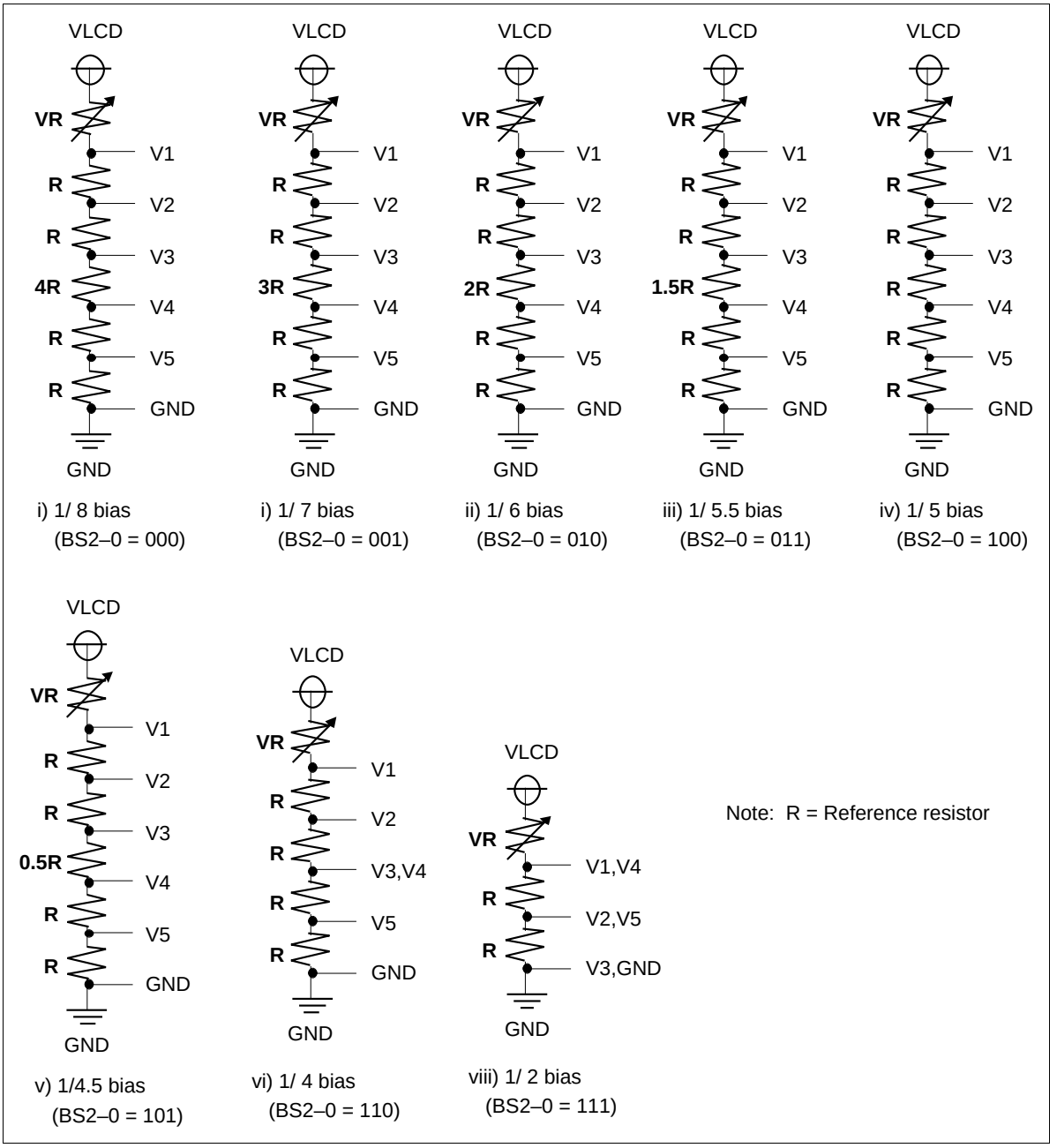


Figure 41 Liquid Crystal Display Drive Bias Circuit

LCD Panel Interface

The HD66732 has a function for changing the common driver/segment driver output shift direction using the CMS bit and SGS bit to meet the chip mounting positions of the HD66732. This is to facilitate the interface wiring to the LCD panel with COG or TCP installed.

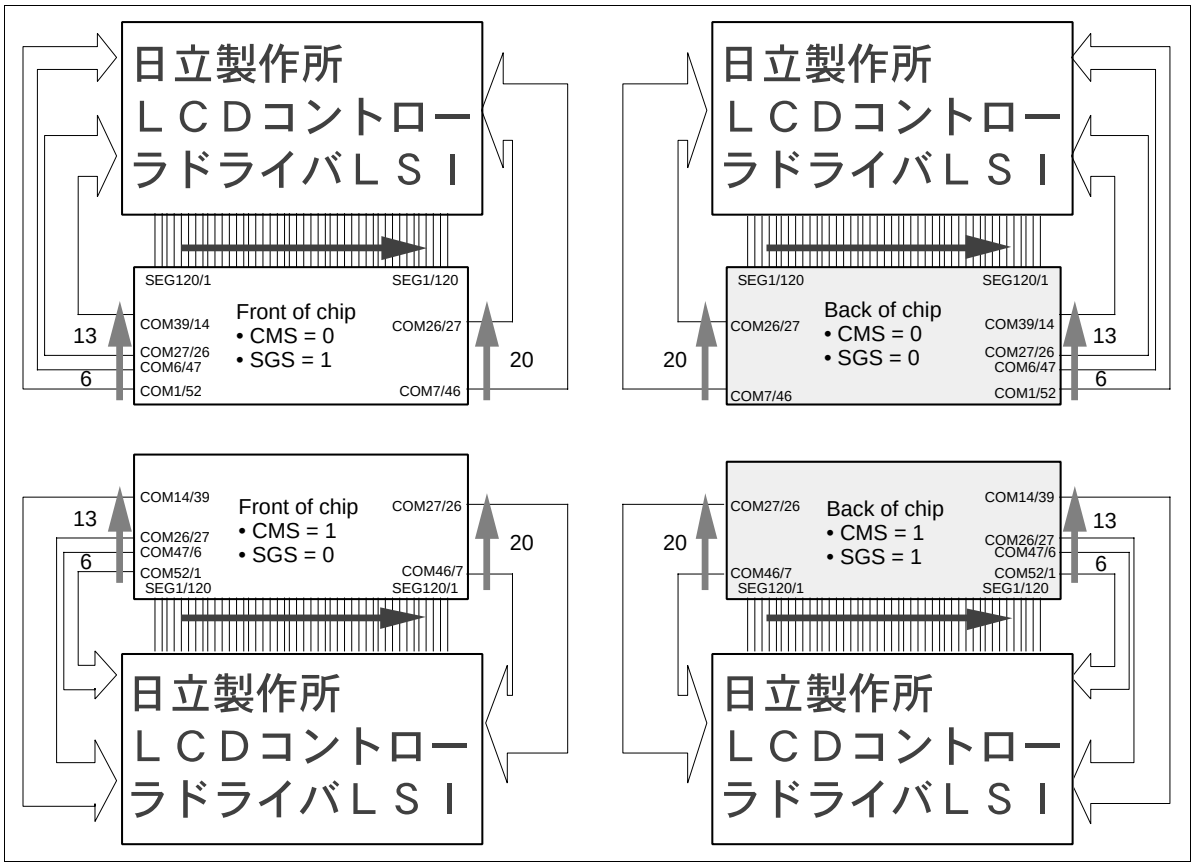


Figure 42 3-line Display Pattern Wiring

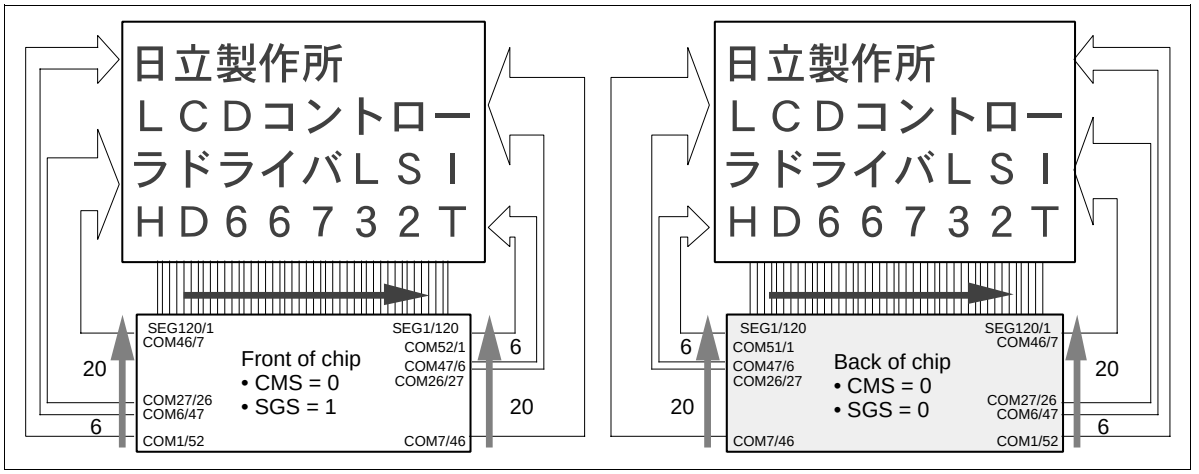


Figure 43 4-line Display Pattern Wiring

Combined Display of Full-size and Half-size Characters

The HD66732 creates a display from the left edge of the display area combining 12-dot full-size (font size: 11 x 12 dots) and 6-dot half-size characters (font size: 5 x 12 dots). There will be a one-dot space between these fonts.

The most significant bit in the data (8 bits) in the DDRAM is allocated to the designation bit indicating a full-size or half-size character. When this MSB is 0, the full-size character is selected, and when 1, the half-size character is selected.

When the full-size character is selected, two bytes of DDRAM are linked and used as a 16-bit code. In this case, the lower byte is written into the smaller DDRAM address. 13 bits of this 16-bit code are used as character codes. Since up to 8,192 character codes can be specified, symbols can be used as well as the JIS Level-1 and Level-2 Kanji Sets. In addition, two of the remaining bits can be allocated to a display-attribute code and can designate a black-white reversed display for individual characters. For details, refer to the Display Attribute Designation section.

Table 50 shows the relationship between the 16-bit designated JIS code and the HD66732 13-bit character code. The 8-bit data designating half-size characters are used as an 8-bit code. Specifically, 7 bits of the 8-bit half-size characters become the character codes, so that a total of 128 characters can be displayed (alphanumeric characters and symbols can be displayed as half-size characters). These 128 CGROMs (HCGROMs) for half-size fonts have two memory banks and incorporate a total of 256 half-size fonts. These memory banks are switched in a display-line unit by bits RL1–RL4 in the half-size ROM select register (RA). A half-size font display attribute is designated by the half-size display attribute register (RB) in a display-line unit. Note that the same display attribute in a character unit such as the full-size font cannot be specified.

User fonts can be displayed using the CGRAM. Special symbols not included in the internal CGROM can be displayed as needed. Since the display font size of the CGRAM is 12 x 13 dots, CGRAM fonts can be displayed to the right, left, top, or bottom, in order to be used to display double-size characters. In the super-imposed display mode, which displays the combined character display mode and graphics display mode, this CGRAM becomes the bit map memory for the graphics display and cannot be used as the user font for characters.

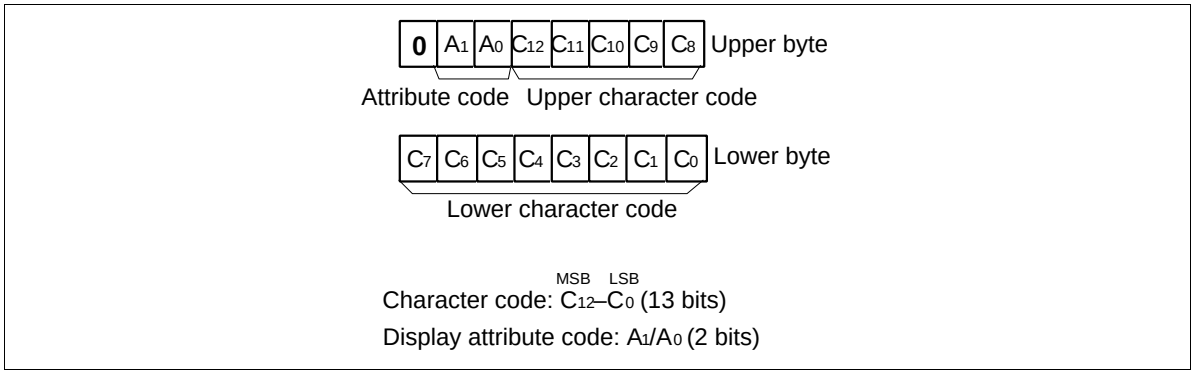


Figure 44 Full-size Code Format

Table 49 Attribute Code and Display Contents

A1	A0	Display Contents
0	0	Normal display
0	1	Black-white reversed display
1	0	Blinking display
1	1	Black-white reversed blinking display

Table 50 JIS Code and HD66732 Character Code

- JIS Level-1 byte code: b7–b1 (7 bits)
- JIS Level-2 byte code: a7–a1 (7 bits)
- CGRAM code for user fonts: u6–u1 (6 bits)

JIS Code				HD66732 Character Code													
	b7	b6	b5	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
Non-kanji	**0**	**1**	**0**	0	a7	a6	b3	b2	b1	0	0	a5	a4	a3	a2	a1
Level-1 Kanji	**0**	**1**	**1**	0	b7	b4	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1
	1	**0**	**0**	0	b7	b4	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1
Level-2 Kanji	**1**	**0**	**1**	1	b6	b4	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1
	1	**1**	**0**	1	b6	b4	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1
	1	**1**	**1**	1	a7	a6	b3	b2	b1	0	0	a5	a4	a3	a2	a1
User Font	—	—	—	u6	0	0	0	0	0	0	0	u5	u4	u3	u2	u1

Upper byte Lower byte

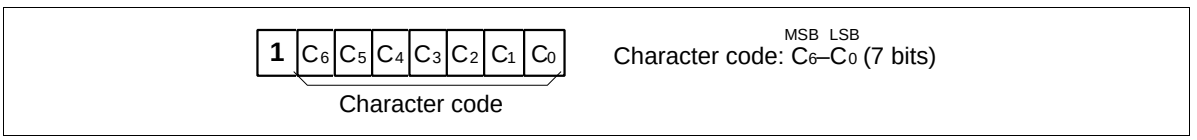


Figure 45 Half-size Code Format

An example of how to display full-size and half-size characters together is explained here.

The full-size character display conforms to the JIS code (16 bits). According to the relationship between the 13-bit JIS code, the code is converted from 16 bits to 13 bits, and the data of two bytes/character is written to the DDRAM. Write the lower byte to the smaller DDRAM address (table 51). When displaying a half-size character, refer to the HD66732 half-size font list (table 52) and write the one byte/character data to the DDRAM.

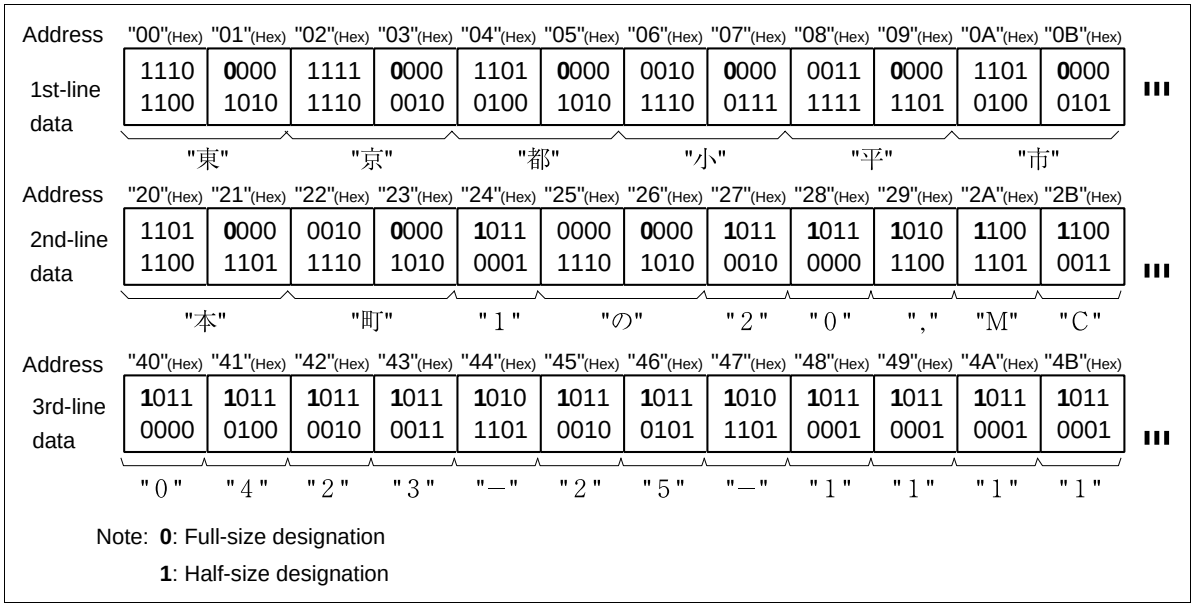
Figure 46 shows how to set data to the DDRAM when performing a 3-line 6-character display and figure 47 shows the resulting LCD display example.

Table 51 Example of Full-size Character Code Conversion

Displayed Character	JIS Code (first/second byte)	Character Code (C_{11}–C_0)
東	45/6C (Hex)	AEC (Hex)
京	35/7E (Hex)	2FE (Hex)
都	45/54 (Hex)	AD4 (Hex)
小	3E/2E (Hex)	72E (Hex)
平	4A/3F (Hex)	D3F (Hex)
市	3B/54 (Hex)	5D4 (Hex)
本	4B/5C (Hex)	DDC (Hex)
町	44/2E (Hex)	A2C (Hex)
の	24/4E (Hex)	A0E (Hex)

Table 52 Example of Half-size Character Code

Display Character	Character Code (C_6–C_0)	Display Character	Character Code (C_6–C_0)
1	31 (Hex)	0	30 (Hex)
2	32 (Hex)	4	34 (Hex)
0	30 (Hex)	2	32 (Hex)
,	2C (Hex)	3	33 (Hex)
M	4D (Hex)	5	35 (Hex)
C	43 (Hex)	1	31 (Hex)



Note: **0**: Full-size designation
1: Half-size designation

Figure 46 Example of Character Code Setting to DDRAM (3-line Mode, 1/41 Duty)

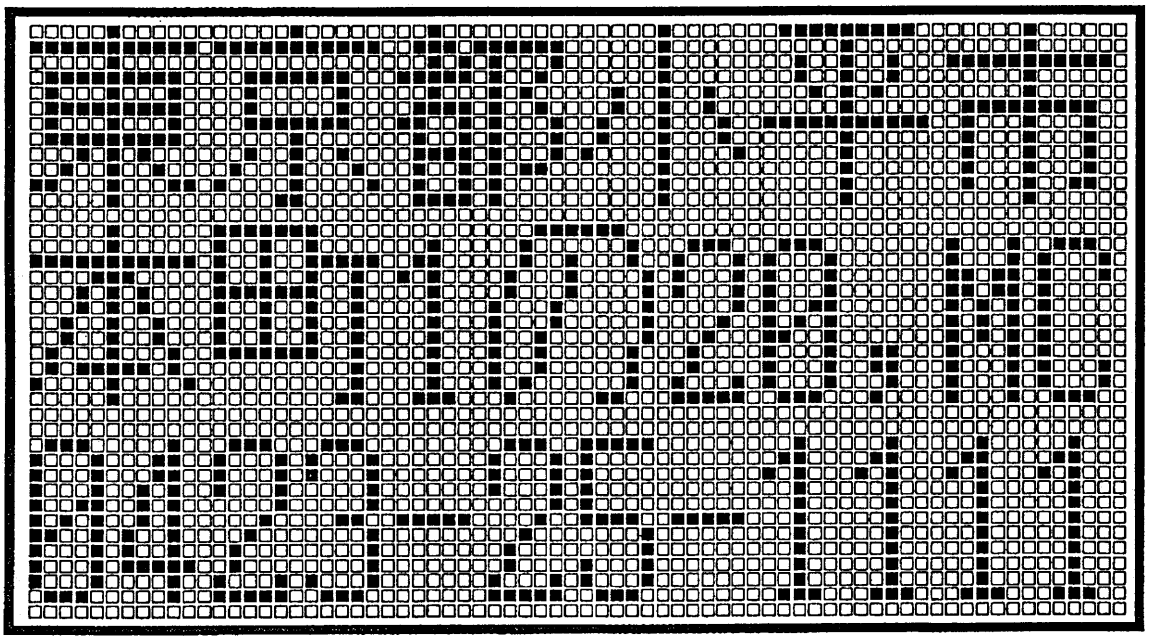


Figure 47 Example of Liquid Crystal Display (3-line 6-character Display)

Display Attribute Designation

The HD66732 allocates 12 bits of the full-size 16-bit code character to an abbreviated character code and 2 bits to a display-attribute code. A black-white reversed display, blinking display, and black-white reversed blinking display can be designated for each full-size character. Display attribute control is performed for a 12 x 13 dot matrix unit that includes a 11 x 12 dot full-size character and a column of dots to the right and a row of dots at the bottom. The blinking cycle for the blinking display and black-white reversed blinking display is 64 frames. The blinking display is provided by changing the display pattern every 32 frames.

The display attribute can be designated by the half-size display attribute register (RC) in each display-line unit although the display attribute cannot be designated by the 8-bit half-size character code. The half-size fonts in the same display line have the same display attributes.

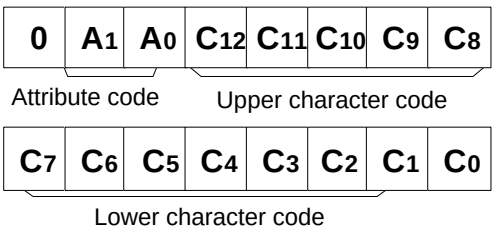


Figure 48 Full-size Code Format

Table 53 Full-size Display Attribute Designation

A1	A0	Display State
0	0	Normal display
0	1	Black-white reversed display
1	0	Blinking display
1	1	Black-white blinking display

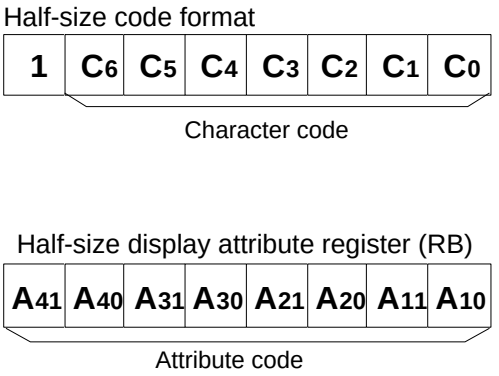


Figure 49 Half-size Code Format and RB

Table 54 Half-size Display Attribute Designation

A11	A10	Display State
0	0	Normal display of all half-size characters in the 1st line
0	1	Black-white reversed display of all half-size characters in the 1st line
1	0	Blinking display of all half-size characters in the 1st line
1	1	Black-white blinking display of all half-size characters in the 1st line

A21	A20	Display State
0	0	Normal display of all half-size characters in the 2nd line
0	1	Black-white reversed display of all half-size characters in the 2nd line
1	0	Blinking display of all half-size characters in the 2nd line
1	1	Black-white blinking display of all half-size characters in the 2nd line

A31	A30	Display State
0	0	Normal display of all half-size characters in the 3rd line
0	1	Black-white reversed display of all half-size characters in the 3rd line
1	0	Blinking display of all half-size characters in the 3rd line
1	1	Black-white blinking display of all half-size characters in the 3rd line

A41	A40	Display State
0	0	Normal display of all half-size characters in the 4th line
0	1	Black-white reversed display of all half-size characters in the 4th line
1	0	Blinking display of all half-size characters in the 4th line
1	1	Black-white blinking display of all half-size characters in the 4th line

Setting Codes in the DDRAM and Display Examples

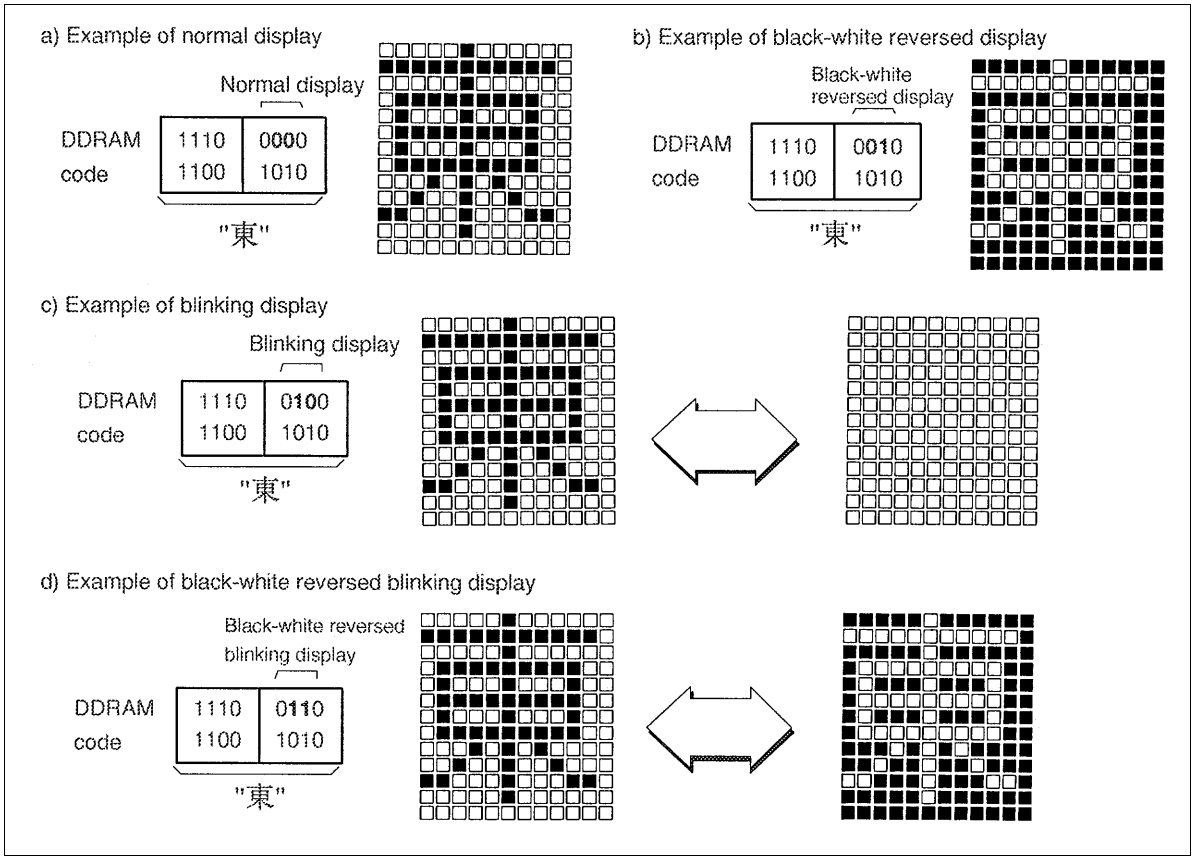
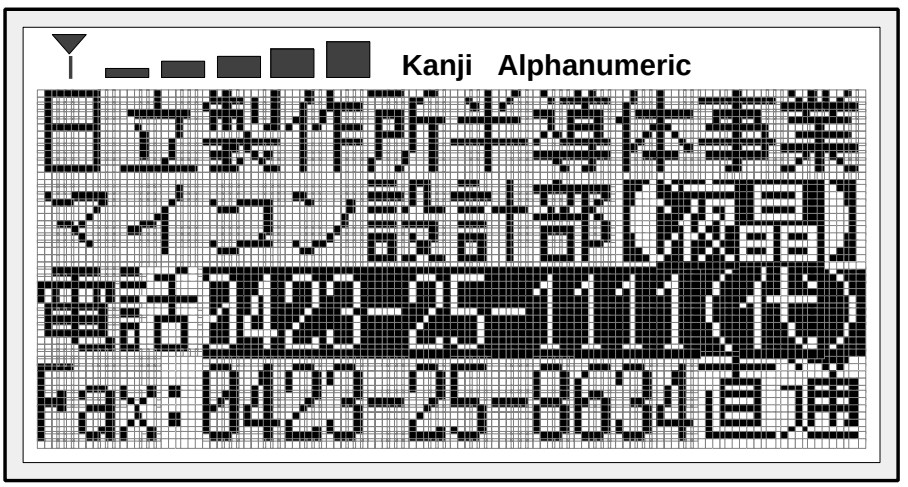


Figure 50 Example of Full-size Character Display at Display Attribute Designation



i) Black-white reversed display of full-size "液晶"
- A1 = 0
- A0 = 1

ii) Black-white reversed display of half-size characters in the 3rd line
- A31 = 0
- A30 = 1

iii) Black-white reversed display of full-size "代"
- A1 = 0
- A0 = 1

Figure 51 Example of Black-white Reversed Character Display

Character Display Functions and Graphics Display Functions

The HD66732 has a character display mode (GR = 0) where the CGRAM or CGROM is used to display font patterns, a graphics display mode (GR = 1) where the bit pattern data is set to the CGRAM to display given patterns, and a super-imposed display mode (SPR = 1) which displays both display modes combined. In the character display mode, kanji characters can easily be provided by sending two-byte-per-character character codes to the DDRAM. For example, when an LCD panel which displays 4-line 10-character kanji is rewritten, the LCD display can be easily provided simply by transferring 80-byte character codes. This reduces the microcomputer software processing needed to develop kanji fonts. In addition, since the 30 user fonts can be registered by using the CGRAM, kanji characters other than JIS Level-1 or Level-2, symbols, or marks which are not included in the CGROM can be displayed.

In the graphics display mode, all bit pattern data to be displayed need to be sent. However, up to a 120 x 52-dot display is possible using the CGRAM. The GR bit can switch these modes not only when characters such as kanji are displayed but also when graphics such as maps or games are used.

Figure 52 Example of Kanji Display in the Character Display Mode (GR = 0)

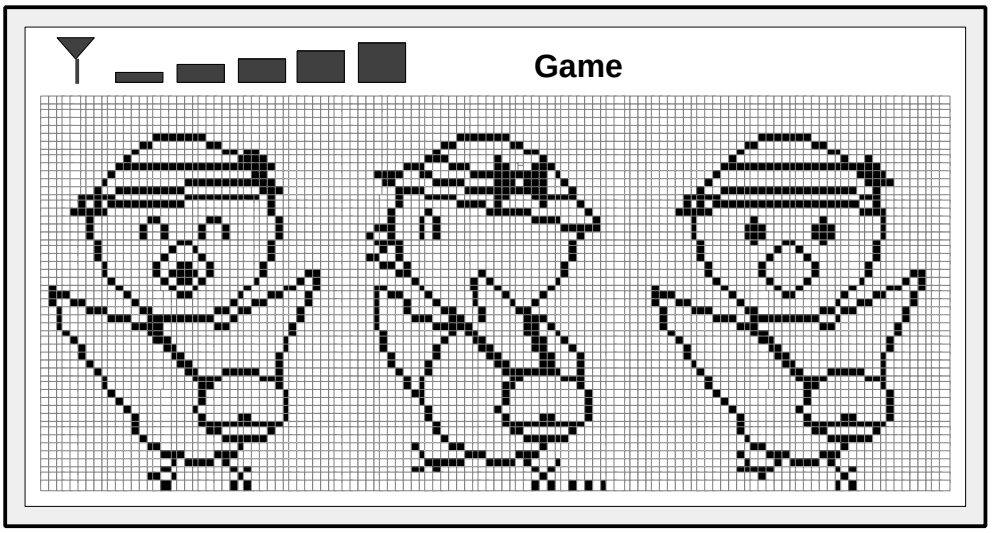


Figure 53 Example of Graphics Display in the Graphics Display Mode (GR = 1)

Super-imposed Display Function

The HD66732 has a super-imposed display mode (SPR = 1) which displays two modes combined: the character display mode where the full-size and half-size CGROM is used to display font patterns, and the graphics display mode where the bit pattern data is set to the CGRAM to display given patterns. The super-imposed mode can be supplied with an easy character display mode and various graphics display modes, enabling a flexible high-quality display. For example, this mode is available to insert graphics such as maps or to create facial images in an address book which otherwise only uses characters.

When characters are displayed in this mode, user fonts cannot be displayed by using the CGRAM. The CGRAM is used as the RAM for the graphics display.

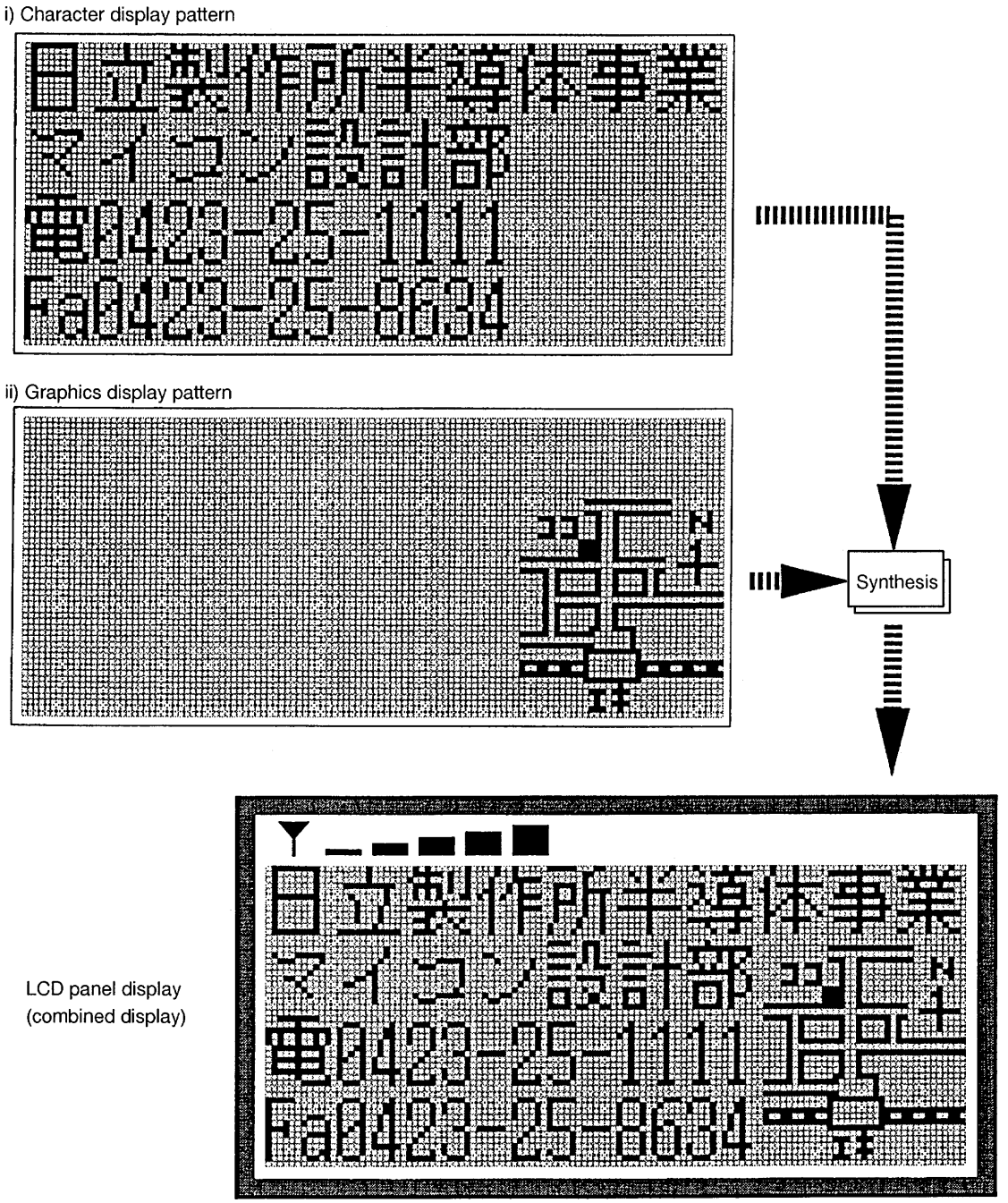


Figure 54 Example of Super-imposed Display

Vertical Smooth Scroll

The HD66732 can scroll vertically in units of one dot. Vertical smooth scrolling is enabled for the character display, graphics display, and super-imposed display modes. In vertical scrolling, the display start position is controlled in one-raster-row units by incrementing or decrementing the display start line (SN1/0) and display-start raster-row (SL3/2/1/0). However, segment icons (marks) displayed by using the SEGRAM are not scrolled.

If the response speed of the liquid crystal is slow and cannot keep up with one-raster-row scrolling, scroll multiple raster-row units together. Moreover, if vertical smooth scrolling is performed with a four-line display (1/54 duty), the display raster-row that has scrolled out of the display will appear again from the bottom (or the top) (this function is called lap-around). In this case, confirm the display line position (NF1/0) and display raster-row position (LF3–0) flags in the status register, and update the display data in the DDRAM or CGRAM while LCD driving is not performed.

i) Not scrolled
• SN1/0 = 00
• SL3–0 = 0000

ii) 4 raster-row scrolled up
• SN1/0 = 00
• SL3–0 = 0100

iii) 8 raster-row scrolled up
• SN1/0 = 00
• SL3–0 = 1000

iv) 13 raster-row scrolled up
• SN1/0 = 01
• SL3–0 = 0000

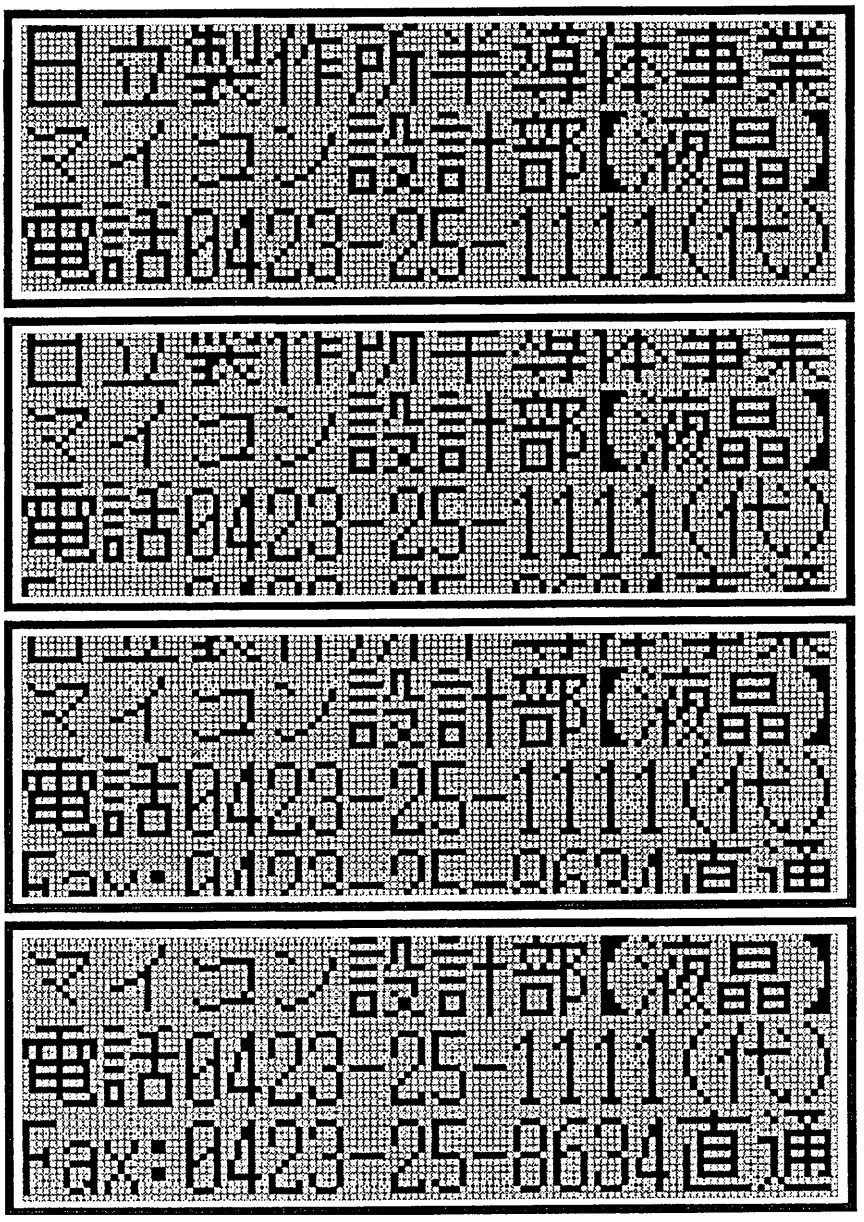
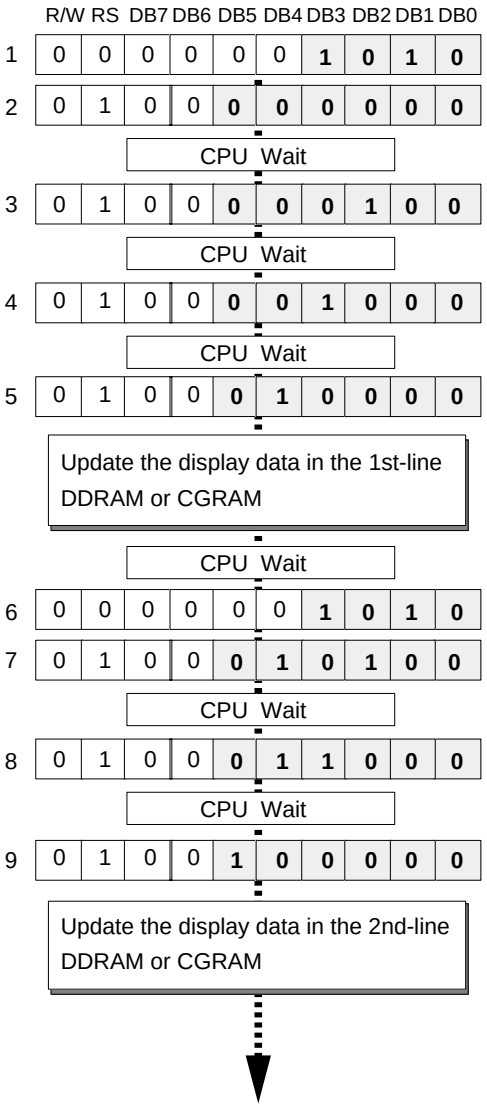


Figure 55 Example of Vertical Smooth Scroll Display

Vertical Smooth Scroll at 3-line Display (NL2–0 = 011)



Notes:
1. The DDRAM or CGRAM has only four-line RAM capacity. After the 13th raster-row in the fourth line is displayed, the first raster-row in the first line is lap-around displayed again.
2. In four-line display (NL2–0 = 100), all areas of the DDRAM and CGRAM are used and displayed. Therefore, update the contents of the DDRAM or CGRAM after checking the flags of the display line position (NF1/0) and display raster-row position (LF3–0) in the status register while the LCD driving is not performed. LCD driving is performed by time sharing from the first raster-row in the first line. For example, when the display data in the first line is updated, start driving when the LCD driving line enters the second line by the status register, and complete by the beginning of the 13th raster-row driving in the fourth line.

Figure 56 Vertical Scroll Control

Reversed Display Function

The HD66732 can display character/graphics display sections by black-white reversal except for the segment/icon display sections. Black-white reversal can be easily displayed without rewriting the data in the RAM when REV is set to 1. The segment and icon sections are not black-white reversed and do not depend on the REV bit setting.

Figure 57 Example of Reversed Display

Blink Mark Display

The HD66732 has a grayscale display and blink display based on 200 individual segments (marks). Forty of these are for grayscale display and the remainder are for blink display.

These 40 segments can also control the grayscale display, providing simple grayscale on specific pictograms or marks. The above display uses a curtailed frame grayscale system, and flicker may result in quick-response liquid crystal materials. Table 57 shows the relationship between set data in the SEGRAM and the effective applied voltage during the frame curtailing operation. These grayscale control segments are driven with the same grayscale data when COMS1 and COMS2 are selected.

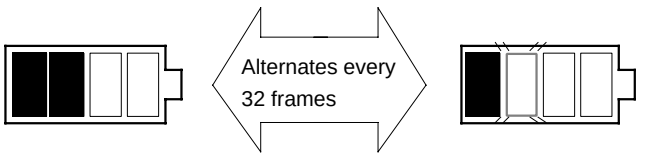
The remaining 160 segments are responsible for normal blinking and double-speed blinking. Normal blinking (black and white) is achieved by repeatedly turning on each segment for 32 frames and turning it off for the next 32 frames. Double-speed blinking (black and white) is achieved by repeatedly turning each segment on and off every 16 frames. These blinking control segments are driven by the independent blinking data when COMS1 and COMS2 are selected.

Table 55 Relationship between Segment Driver Output Pin and Segment Display Function

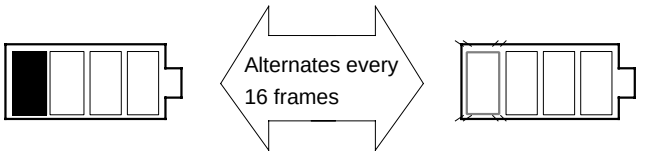
When SGS = 0	When SGS = 1	Remarks
SEG1/120, SEG4/117, SEG7/114, SEG10/111, SEG13/108, SEG16/105, SEG19/102, SEG22/99, SEG25/96, SEG28/93, SEG31/90, SEG34/87, SEG37/84, SEG40/81, SEG43/78, SEG46/75, SEG49/72, SEG52/69, SEG55/66, SEG58/63, SEG61/60, SEG64/57, SEG67/54, SEG70/51, SEG73/48, SEG76/45, SEG79/42, SEG82/39, SEG85/36, SEG88/33, SEG91/30, SEG94/27, SEG97/24, SEG100/21, SEG103/18, SEG106/15, SEG109/12, SEG112/9, SEG115/6, SEG118/3	SEG120/1, SEG117/4, SEG114/7, SEG111/10, SEG108/13, SEG105/16, SEG102/19, SEG99/22, SEG96/25, SEG93/28, SEG90/31, SEG87/34, SEG84/37, SEG81/40, SEG78/43, SEG75/46, SEG72/49, SEG69/52, SEG66/55, SEG63/58, SEG60/61, SEG57/64, SEG54/67, SEG51/70, SEG48/73, SEG45/76, SEG42/79, SEG39/82, SEG36/85, SEG33/88, SEG30/91, SEG27/94, SEG24/97, SEG21/100, SEG18/103, SEG15/106, SEG12/109, SEG9/112, SEG6/115, SEG3/118	The COMS1 and COMS2 outputs are controlled by the same grayscale. Total: 40 segments
Output pins other than above	Output pins other than above	The COMS1 and COMS2 outputs are independently controlled. Total: 80 x 2 = 160 segments

Table 56 Relationship between SEGRAM Data and Blinking Segment

SEGRAM Data Setting		LCD Display Control for	SEGRAM Data Setting		LCD Display Control for
DB5	DB4	COMS1 Segment	DB7	DB6	COMS2 Segment
0	0	Always unlit	0	0	Always unlit
0	1	Always lit	0	1	Always lit
1	0	Normal blinking (32-frame unit)	1	0	Normal blinking (32-frame unit)
1	1	Double-speed blinking (16-frame unit)	1	1	Double-speed blinking (16-frame unit)



i) Normal blinking display



ii) Double-speed blinking display

Figure 58 Blinking Segment Display

Table 57 Relationship between SEGRAM Data and Grayscale Segment Display

SEGRAM Data Setting				
DB7	**DB6**	**DB5**	**DB4**	**Effective Applied Voltage for COMS1 and COMS2 Outputs**
0	0	0	0	0 (Always unlit)
0	0	0	1	1 (Always lit)
0	0	1	0	0.34 (Grayscale display)
0	0	1	1	0.38 (Grayscale display)
0	1	0	0	0.41 (Grayscale display)
0	1	0	1	0.44 (Grayscale display)
0	1	1	0	0.47 (Grayscale display)
0	1	1	1	0.50 (Grayscale display)
1	0	0	0	(Blink display) *
1	0	0	1	0.53 (Grayscale display)
1	0	1	0	0.56 (Grayscale display)
1	0	1	1	0.59 (Grayscale display)
1	1	0	0	0.63 (Grayscale display)
1	1	0	1	0.66 (Grayscale display)
1	1	1	0	0.69 (Grayscale display)
1	1	1	1	0.72 (Grayscale display)

Note: Turn on the segment for 32 frames and turn it off for the next 32 frames.

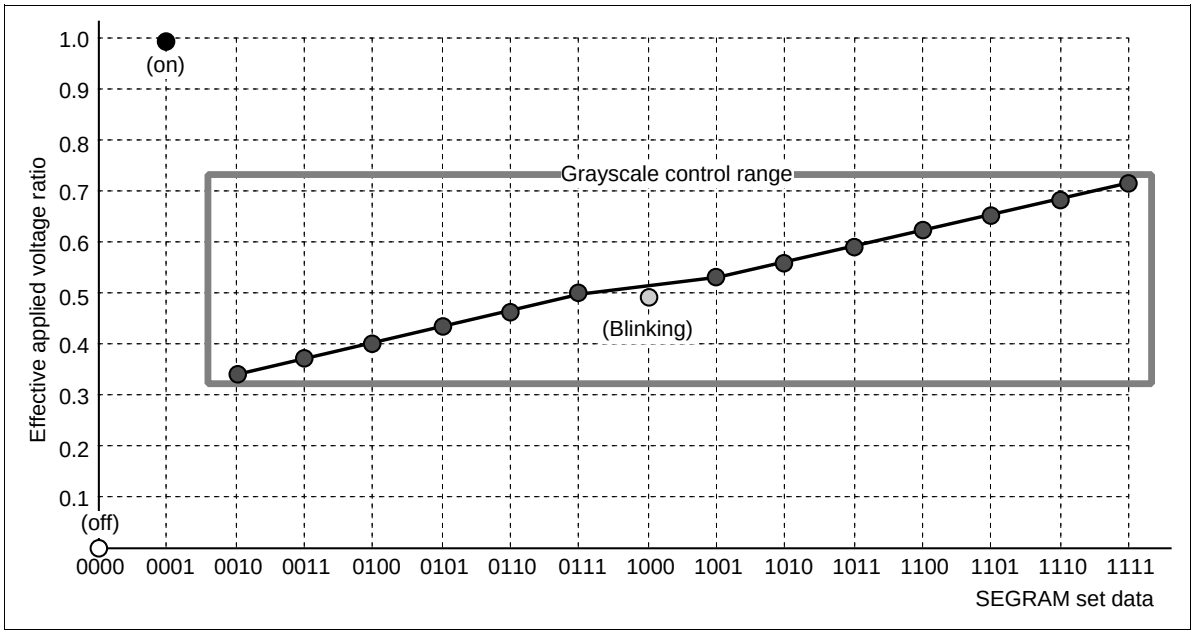


Figure 59 Relationship between SEGRAM Set Data and Effective Applied Voltage

Line-cursor Display

The HD66732 can assign a cursor attribute to an entire line corresponding to the address counter value by setting the LC bit to 1. One of three line-cursor modes can be selected: a black-white reversed cursor (B/W = 1), an underline cursor (C = 1), and a blink cursor (B = 1). The cycle for a blink cursor is 32 frames. These line-cursors are suitable for highlighting an index and/or marker, or for indicating an item in a menu with a cursor or an underline.

However, the black-white reversed display described above does not perform black-white blinking.

Table 58 Address Counter Value and Line Cursor

Address Counter Value (AC)	Selected Line for Line Cursor
00H to 13H	Entire 1st line (10 characters)
20H to 33H	Entire 2nd line (10 characters)
40H to 53H	Entire 3rd line (10 characters)
60H to 73H	Entire 4th line (10 characters)

Black-white Reserved Display (LC = 1, R/W = 1)

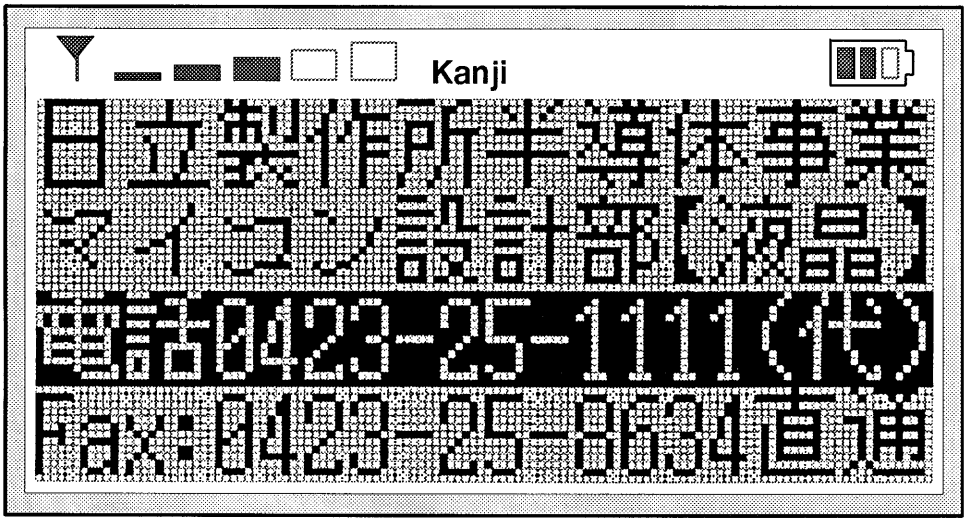


Figure 60 Black-white Reversed Cursor

Underline Cursor (LC = 1, C = 1)

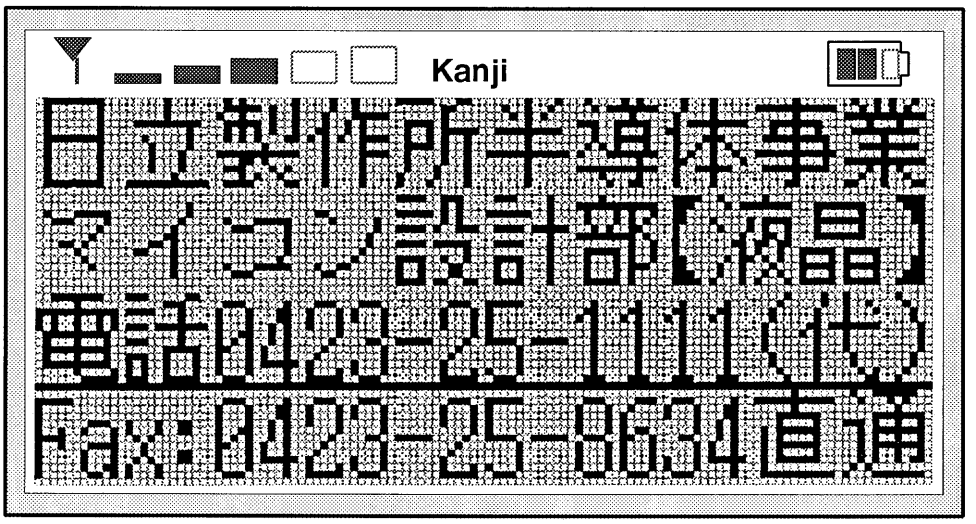


Figure 61 Underline Cursor

Blinking Display (LC = 1, B = 1)

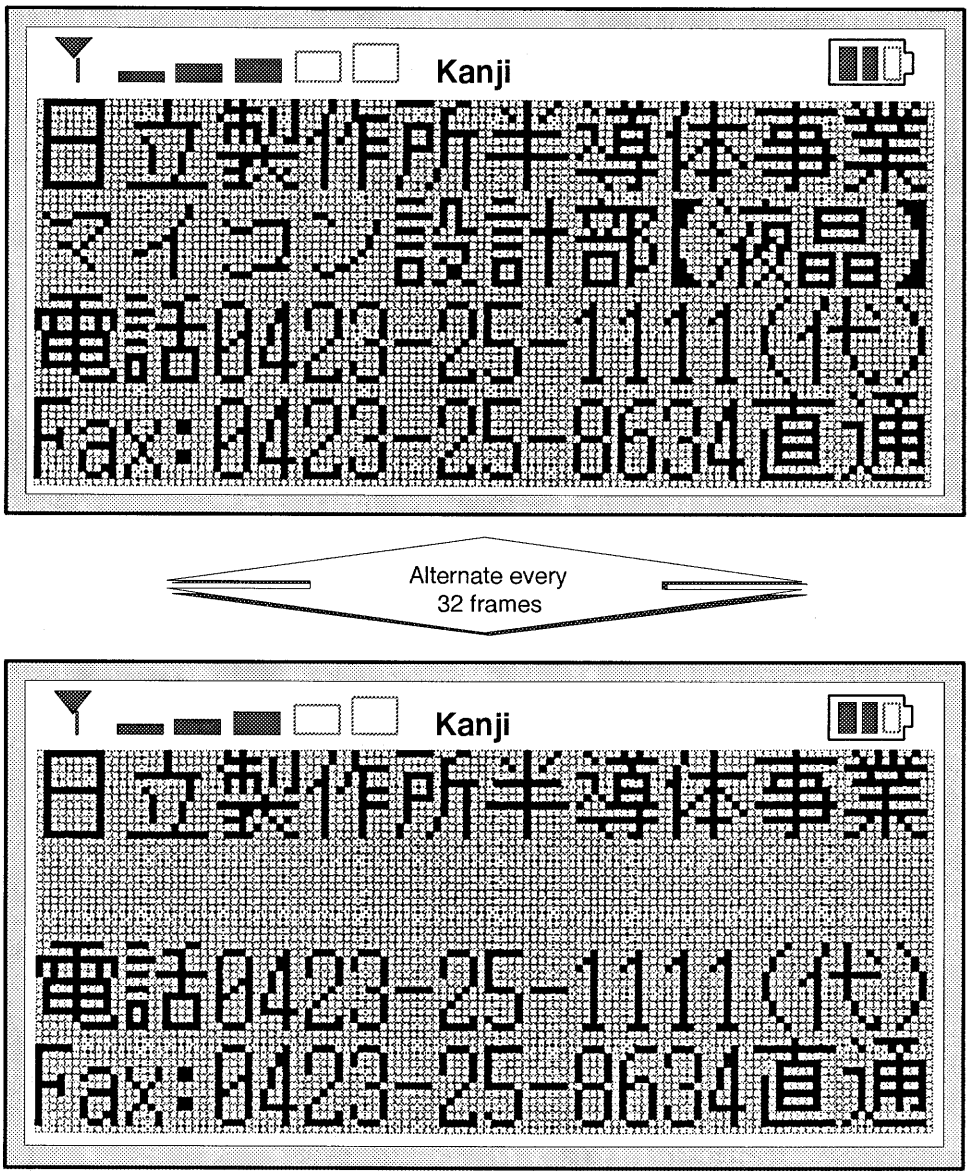


Figure 62 Blinking Display

Partial-display-on Function

The HD66732 can program the liquid crystal display drive duty ratio setting (NL2-0 bits), liquid crystal display drive bias value selection (BS2-0 bits), boost output level selection (BT1/0 bit) and contrast adjustment (CT4-0 bits). For example, in the four-line display mode (1/54 duty ratio), the HD66732 can drive only two lines in the center of the screen by combining these register functions and the centering display (CEN bit) function with the 1/28 duty ratio. This is called partial-display-on. Lowering the liquid crystal display drive duty ratio as required saves the liquid crystal display drive voltage, thus reducing internal current consumption. This is suitable for calendar or time display, which needs to be continuous in the system standby state with minimal current consumption. Here, the non-displayed lines are constantly driven by the unselected level voltage, thus turning off the LCD for the lines.

In general, lowering the liquid crystal display drive duty ratio decreases the optimum liquid crystal display drive voltage and liquid crystal display drive bias value.

Table 59 Partial-display-on Function (4-line Display)

Item	Normal 4-line Display	Partial-on Display	
Character/graphics display	4th line displayed	Only one line in the center of the screen	Only two lines in the center of the screen
LCD drive duty ratio	1/54 (NL2/1/0 = 100)	1/15 (NL2/1/0 = 001)	1/28 (NL2/1/0 = 010)
LCD drive bias value (optimum)	1/8 (BS2-0 = 000)	1/5 (BS2-0 = 100)	1/6 (BS2-0 = 010)
LCD drive voltage	Adjustable using BT1/0 and CT4-0	Adjustable using BT1/0 and CT4-0	Adjustable using BT1/0 and CT4-0
Frame frequency (fosc = 76 kHz)	70 Hz	71 Hz	70 Hz

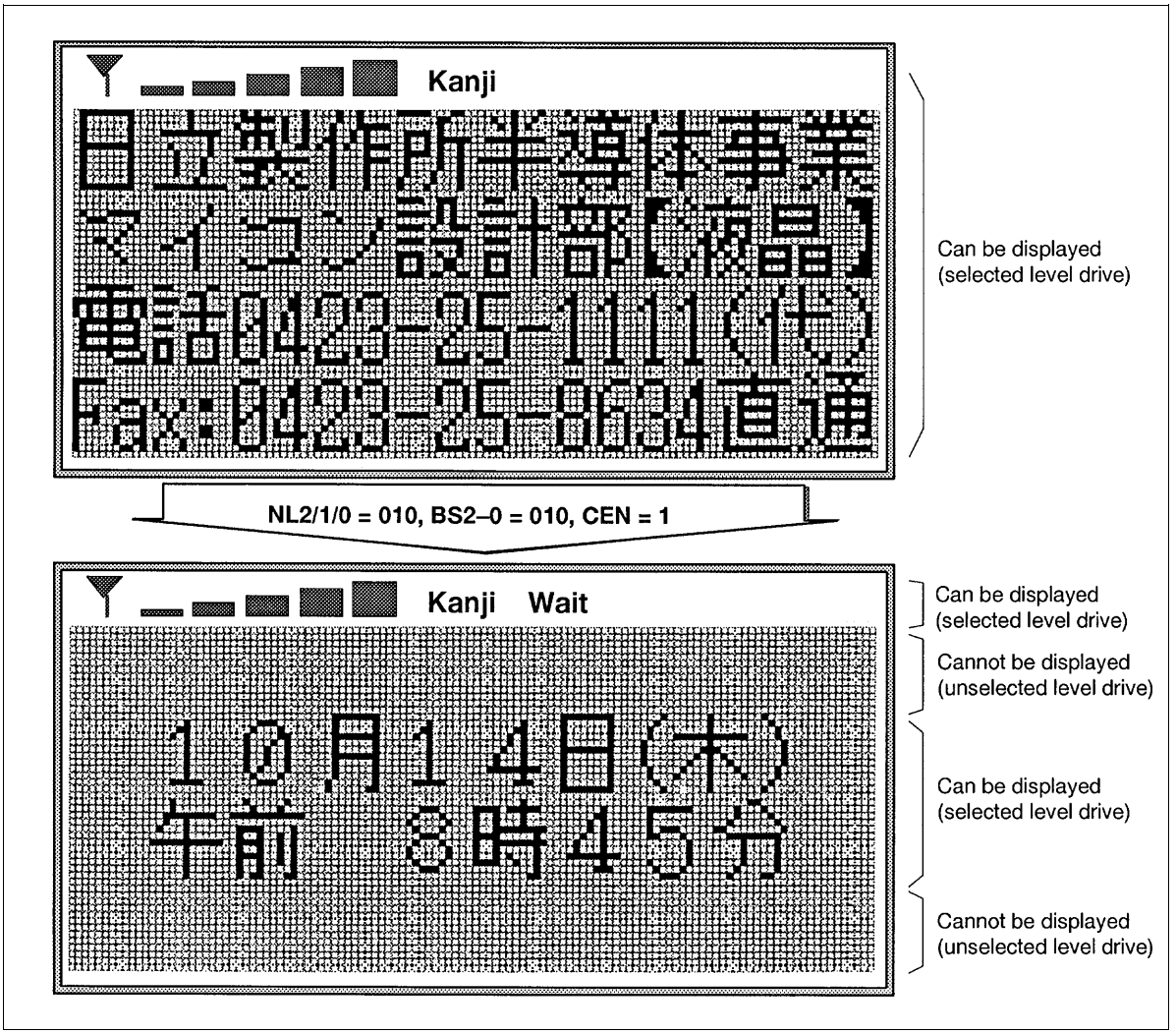


Figure 63 Partial-on Display (Date and Time Indicated)

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66732 in the sleep mode, where the device stops all internal display operations except for key scan operations, thus reducing current consumption. Specifically, LCD drive is completely halted. Here, all the SEG (SEG1 to SEG120) and COM (COM1 to COM52, COMS1/2) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

The key scan circuit operates normally in the sleep mode, thus allowing normal key scan and key scan interrupt generation. For details, see the Key Scan Control section and Key Scan Interrupt (Wake-up Function) section.

Table 60 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)	Key Standby Mode (KSB = 1)
Character display	Turned off	Turned off	Normally turned on
Segment display	Turned off	Turned off	Normally turned on
R-C oscillation circuit	Operates normally	Halted	Operates normally
Key scan circuit	Can operate normally	Halted but IRQ* can be generated	

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66732 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, character and segment displays, which are controlled by the multiplexing drive method, are completely halted. Here, all the SEG (SEG1 to SEG120) and COM (COM1 to COM52, COMS1/2) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than those for the start-oscillation instruction and the key scan interrupt generation enable instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.

Although key scan is halted in the standby mode, the HD66732 can detect key inputs, thus generating key scan interrupt (IRQ*). This means, the system can be activated from a completely inactive state. For details, see the Key Scan Interrupt (Wake-up Function) section.

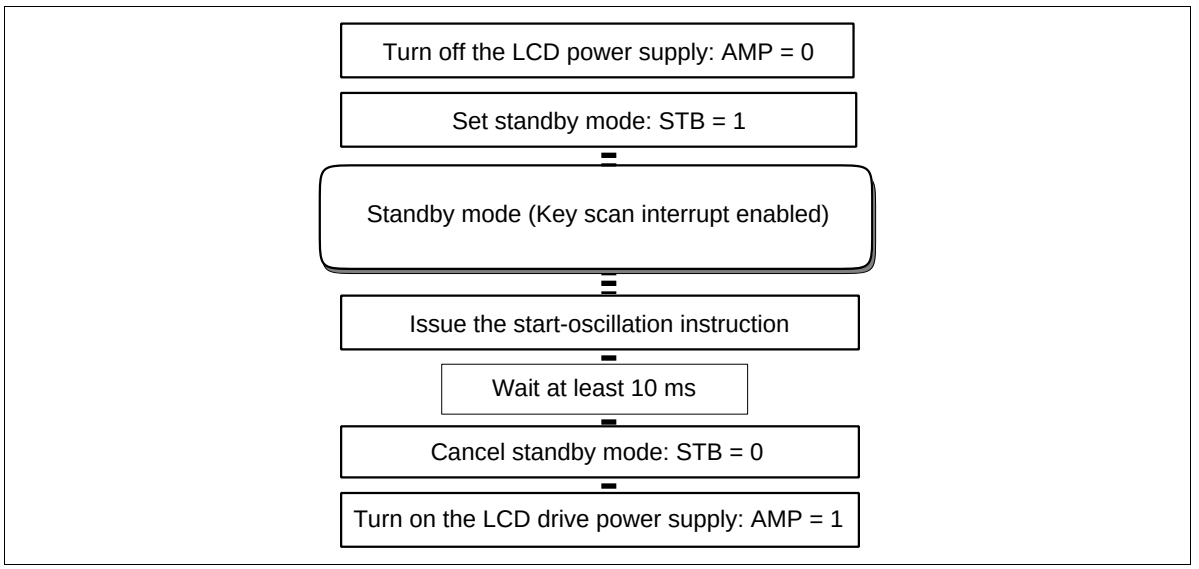


Figure 64 Procedure for Setting and Canceling Standby Mode

Key Standby Mode

When the key standby mode (KSB bit = "1") is set, only key-scan operations are selectively stopped. In this case, however, the display operation, including the internal CR oscillation circuit operation, continues as usual. Since noise generation can be suppressed by stopping unnecessary key-scan operations, the receiving sensitivity for such a wireless system can be improved.

In this case, although key-scan operations are stopped during standby mode, a key scan interrupt (IRQ*) can be generated by detecting the key being depressed, as can be done during the standby mode described above. For details, refer to the Key Scan Interrupt (Wake-up Function) section.

Absolute Maximum Ratings *

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{LCD} – GND	V	–0.3 to +15.0	1, 2
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	°C	–40 to +85	3
Storage temperature	Tstg	°C	–55 to +110	4

Note: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.4 to 5.5 V, Ta = –40 to +85°C*[3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V		5, 6
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 2.4 to 2.7 V	5, 6
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V	5, 6
Output high voltage (1) (SDA, DB0-7 pins)	V_{OH1}	0.75 V_{CC}	—	—	V	I_{OH} = –0.1 mA	5, 7
Output low voltage (1) (SDA, DB0-7 pins)	V_{OL1}	—	—	0.2 V_{CC}	V	V_{CC} = 2.4 to 2.7 V, I_{OL} = 0.1 mA	5
Output low voltage (1) (SDA, DB0-7 pins)	V_{OL1}	—	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V, I_{OL} = 0.1 mA	5
Output high voltage (2) (KST0-7, IRQ* pins)	V_{OH2}	0.7 V_{CC}	—	—	V	$–I_{OH}$ = 0.5 µA, V_{CC} = 3 V	5
Output low voltage (2) (KST0-7, IRQ* pins)	V_{OL2}	—	—	0.2 V_{CC}	V	I_{OL} = 0.1 mA	5
Output high voltage (3) (PORT0-2 pins)	V_{OH3}	0.75 V_{CC}	—	—	V	$-I_{OH}$ = 0.1mA	5
Output low voltage (3) (PORT0-2 pins)	V_{OL3}	—	—	0.2 V_{CC}	V	I_{OL} = 0.1mA	5
Driver ON resistance (COM pins)	R_{COM}	—	3	20	kΩ	±Id = 0.05 mA, V_{LCD} = 6 V	8
Driver ON resistance (SEG pins)	R_{SEG}	—	3	30	kΩ	±Id = 0.05 mA, V_{LCD} = 6 V	8
I/O leakage current	I_{Li}	–1	—	1	µA	Vin = 0 to V_{CC}	9
Pull-up MOS current (KIN0-7, DB0-7, SDA pins)	$-I_p$	1	10	40	µA	V_{CC} = 3 V, Vin = 0 V	5
Current consumption during normal operation (V_{CC}–GND)	I_{OP}	—	30	55	µA	R-C oscillation, V_{CC} = 3 V, f_{OSC} = 60 kHz (1/41 duty)	10, 11
Current consumption during sleep mode (V_{CC}–GND)	I_{SL}	—	13	—	µA	R-C oscillation, V_{CC} = 3 V, f_{OSC} = 60 kHz (1/41 duty)	10, 11
Current consumption during standby mode (V_{CC}–GND)	I_{ST}	—	0.1	5	µA	No R-C oscillation, V_{CC} = 3 V, Ta = 25°C	10, 11
LCD drive power supply current (V_{LCD}–GND)	I_{EE}	—	15	30	µA	V_{LCD} – GND = 8 V, f_{OSC} = 60 kHz, 1/7 bias, VTEST3 = "V_{CC}"	11
LCD drive voltage (V_{LCD} – GND)	V_{LCD}	4.5	—	13.0	V		12

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Double-boost output voltage (VLOUT pin)	V_{UP2}	5.5	5.9	6.0	V	V_{CC} = Vci = 3.0 V, I_O = 0.03 mA, C = 1 µF, f_{OSC} = 60 kHz, Ta = 25°C	15
Triple-boost output voltage (VLOUT pin)	V_{UP3}	8.5	8.9	9.0	V	V_{CC} = Vci = 3.0 V, I_O = 0.03 mA, C = 1 µF, f_{OSC} = 60 kHz, Ta = 25°C	15
Quadruple-boost output voltage (VLOUT pin)	V_{UP4}	11.5	11.8	12.0	V	V_{CC} = Vci = 3.0 V, I_O = 0.03 mA, C = 1 µF, f_{OSC} = 60 kHz, Ta = 25°C	15
Booster output voltage range	V_{UP}	V_{CC}	—	13.0	V	Vci ≤ V_{CC}	15, 16

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.4 to 5.5 V, Ta = –40 to +85°C*[3])

Clock Characteristics (V_{CC} = 2.4 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	40	60	100	kHz		13
External clock duty ratio	Duty	45	50	55	%		13
External clock rise time	trcp	—	—	0.2	µs		13
External clock fall time	tfcp	—	—	0.2	µs		13
Internal Rf oscillation frequency	t_{OSC}	45	60	75	kHz	Rf = 300 kΩ, V_{CC} = 3 V	14

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-system Bus Interface Timing Characteristics

(Vcc = 2.4 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	800	—	—	ns	Figure 71
	Read		1200	—	—		
Enable high-level pulse width	Write	PW_{EH}	150	—	—	ns	Figure 71
	Read		450	—	—		
Enable low-level pulse width	Write	PW_{EL}	300	—	—	ns	Figure 71
	Read		450	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 71
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns	Figure 71
Address hold time		t_{AHE}	20	—	—	ns	Figure 71
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 71
Write data hold time		t_{HE}	20	—	—	ns	Figure 71
Read data delay time		t_{DDRE}	—	—	400	ns	Figure 71
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 71

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	500	—	—	ns	Figure 71
	Read		700	—	—		
Enable high-level pulse width	Write	PW_{EH}	80	—	—	ns	Figure 71
	Read		300	—	—		
Enable low-level pulse width	Write	PW_{EL}	250	—	—	ns	Figure 71
	Read		320	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 71
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns	Figure 71
Address hold time		t_{AHE}	20	—	—	ns	Figure 71
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 71
Write data hold time		t_{HE}	20	—	—	ns	Figure 71
Read data delay time		t_{DDRE}	—	—	250	ns	Figure 71
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 71

80-system Bus Interface Timing Characteristics

(Vcc = 2.4 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	800	—	—	ns	Figure 72
	Read	t_{CYCR}	1200	—	—	ns	Figure 72
Write low-level pulse width		PW_{LW}	150	—	—	ns	Figure 72
Read low-level pulse width		PW_{LR}	450	—	—	ns	Figure 72
Write high-level pulse width		PW_{HW}	300	—	—	ns	Figure 72
Read high-level pulse width		PW_{HR}	450	—	—	ns	Figure 72
Write/Read rise/fall time		t_{WRr} , $_{WRf}$	—	—	25	ns	Figure 72
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 72
Address hold time		t_{AH}	20	—	—	ns	Figure 72
Write data setup time		t_{DSW}	60	—	—	ns	Figure 72
Write data hold time		t_{H}	20	—	—	ns	Figure 72
Read data delay time		t_{DDR}	—	—	400	ns	Figure 72
Read data hold time		t_{DHR}	5	—	—	ns	Figure 72

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	500	—	—	ns	Figure 72
	Read	t_{CYCR}	700	—	—	ns	Figure 72
Write low-level pulse width		PW_{LW}	80	—	—	ns	Figure 72
Read low-level pulse width		PW_{LR}	300	—	—	ns	Figure 72
Write high-level pulse width		PW_{HW}	250	—	—	ns	Figure 72
Read high-level pulse width		PW_{HR}	300	—	—	ns	Figure 72
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 72
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 72
Address hold time		t_{AH}	20	—	—	ns	Figure 72
Write data setup time		t_{DSW}	60	—	—	ns	Figure 72
Write data hold time		t_{H}	20	—	—	ns	Figure 72
Read data delay time		t_{DDR}	—	—	250	ns	Figure 72
Read data hold time		t_{DHR}	5	—	—	ns	Figure 72

Clock-synchronized Serial Interface Timing Characteristics (2.4 V)

(V_{CC} = 2.4 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	Write	t_{SCYC}	0.5	—	20	µs	Figure 73
	Read	t_{SCYC}	1	—	20	µs	Figure 73
Serial clock high-level width	Write	t_{SCH}	230	—	—	ns	Figure 73
	Read	t_{SCH}	480	—	—	ns	Figure 73
Serial clock low-level width	Write	t_{SCL}	230	—	—	ns	Figure 73
	Read	t_{SCL}	480	—	—	ns	Figure 73
Serial clock rise/fall time		t_{scf}, t_{scr}	—	—	20	ns	Figure 73
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 73
Chip select hold time		t_{CH}	200	—	—	ns	Figure 73
Serial input data setup time		t_{SISU}	100	—	—	ns	Figure 73
Serial input data hold time		t_{SIH}	100	—	—	ns	Figure 73
Serial output data delay time		t_{SOD}	—	—	400	ns	Figure 73
Serial output data hold time		t_{SOH}	5	—	—	ns	Figure 73

(V_{CC} = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	Write	t_{SCYC}	0.2	—	20	µs	Figure 73
	Read	t_{SCYC}	0.5	—	20	µs	Figure 73
Serial clock high-level width	Write	t_{SCH}	80	—	—	ns	Figure 73
	Read	t_{SCH}	230	—	—	ns	Figure 73
Serial clock low-level width	Write	t_{SCL}	80	—	—	ns	Figure 73
	Read	t_{SCL}	230	—	—	ns	Figure 73
Serial clock rise/fall time		t_{scf}, t_{scr}	—	—	20	ns	Figure 73
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 73
Chip select hold time		t_{CH}	200	—	—	ns	Figure 73
Serial input data setup time		t_{SISU}	40	—	—	ns	Figure 73
Serial input data hold time		t_{SIH}	40	—	—	ns	Figure 73
Serial output data delay time		t_{SOD}	—	—	200	ns	Figure 73
Serial output data hold time		t_{SOH}	5	—	—	ns	Figure 73

Reset Timing Characteristics (V_{CC} = 2.4 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 74

Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the given electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristics are exceeded, the LSI may malfunction or exhibit poor reliability.
2. VLCD > GND must be maintained.
3. For bare die products, specified up to 85˚C.
4. For bare die products, specified by the common die shipment specification.
5. The following three circuits are I/O pin configurations (figure 65).

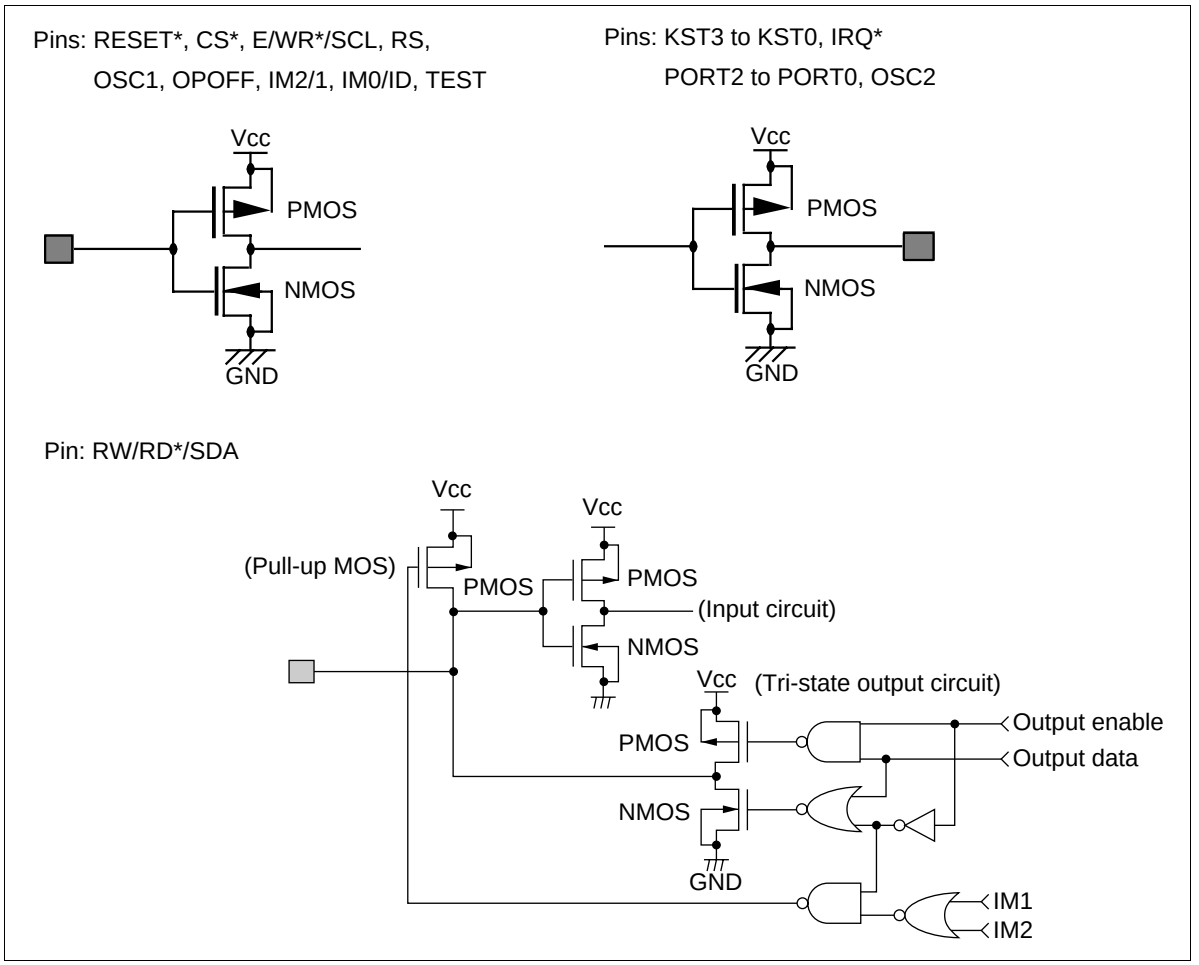


Figure 65 I/O Pin Configuration

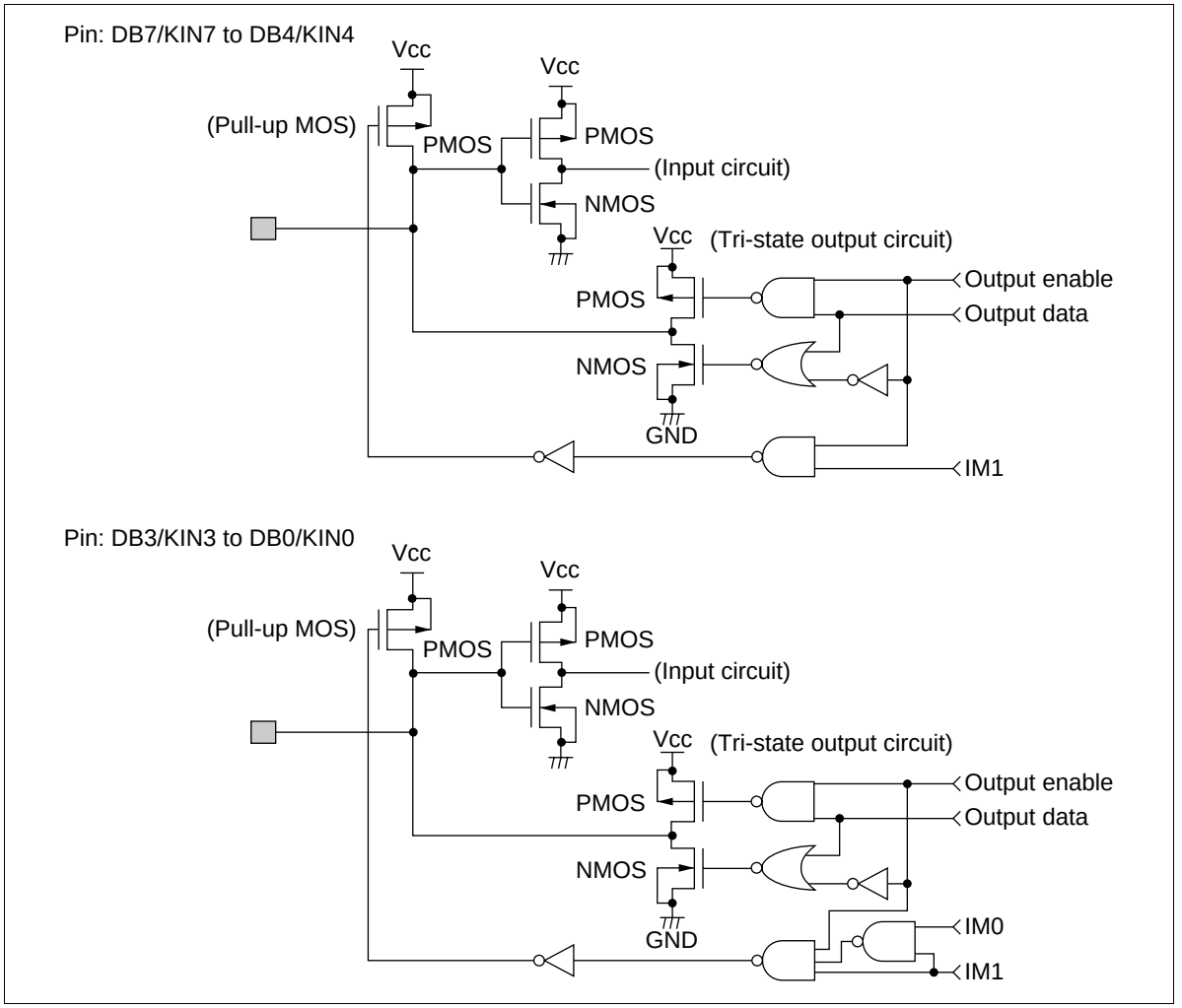


Figure 65 I/O Pin Configuration (cont)

6. The TEST pin must be grounded and the IM2/1, IM0/ID, and OPOFF pins must be grounded or connected to Vcc.
7. Corresponds to the high output for clock-synchronized serial interface.
8. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins (COM1 to COM52, COMS1 and COMS2), and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins (SEG1 to SEG120), when current Id is flown through all driver output pins.
9. This excludes the current flowing through pull-up MOSs and output drive MOSs.
10. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating.
11. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure 66).

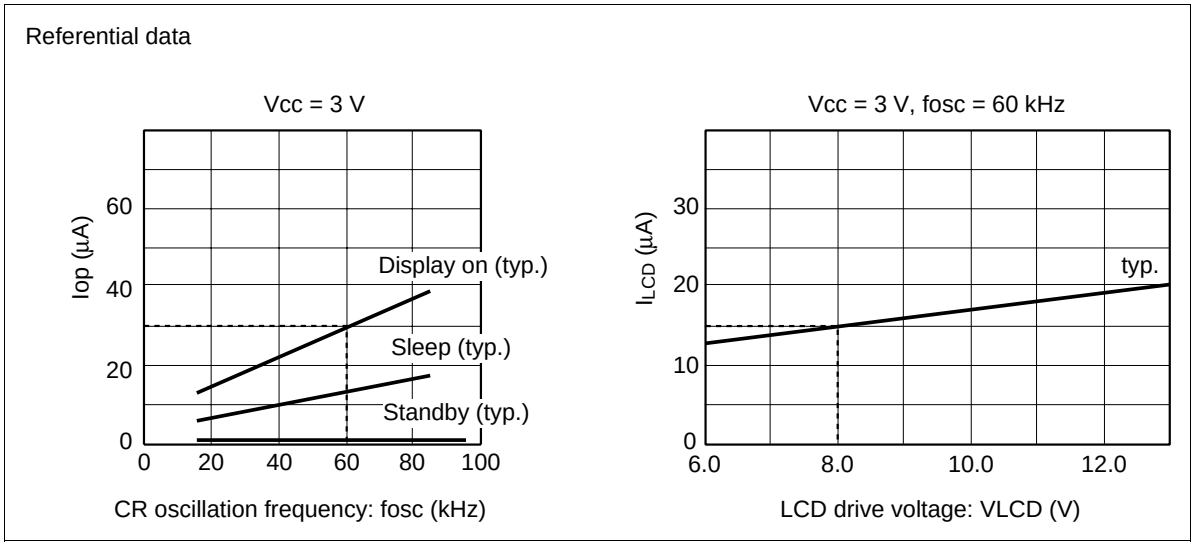


Figure 66 Relationship between the Operation Frequency and Current Consumption

12. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (Vcc, V1, V2, V3, V4, V5) when there is no load.

13. Applies to the external clock input (figure 67).

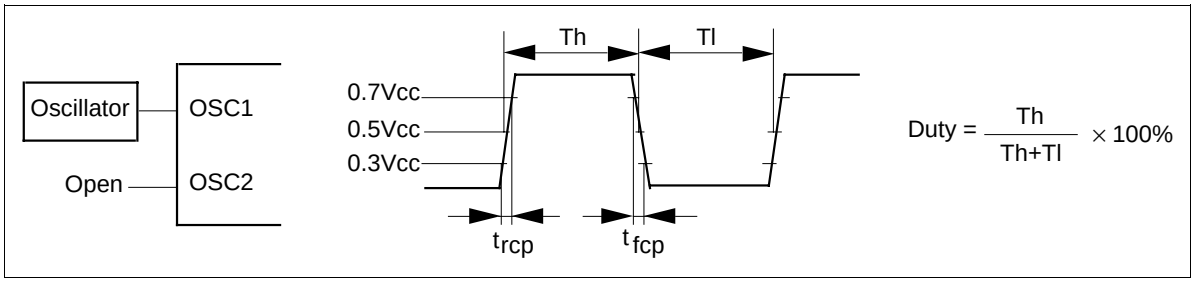
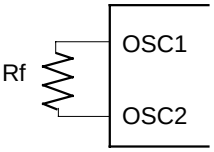


Figure 67 External Clock Supply

14. Applies to the internal oscillator operations using oscillation resistor Rf (figure 68).



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Referential data

External resistance (Rf)	CR oscillation frequency : fosc			
	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 4.0 V	Vcc = 5.0 V
120 kΩ	117 kHz	130 kHz	138 kHz	143 kHz
180 kΩ	73 kHz	85 kHz	93 kHz	98 kHz
240 kΩ	67 kHz	73 kHz	78 kHz	81 kHz
300 kΩ	56 kHz	60 kHz	62 kHz	63 kHz
390 kΩ	45 kHz	48 kHz	50 kHz	51 kHz
470 kΩ	37 kHz	40 kHz	42 kHz	43 kHz

Figure 68 Internal Oscillation

15. Booster characteristics test circuits are shown in figure 69.

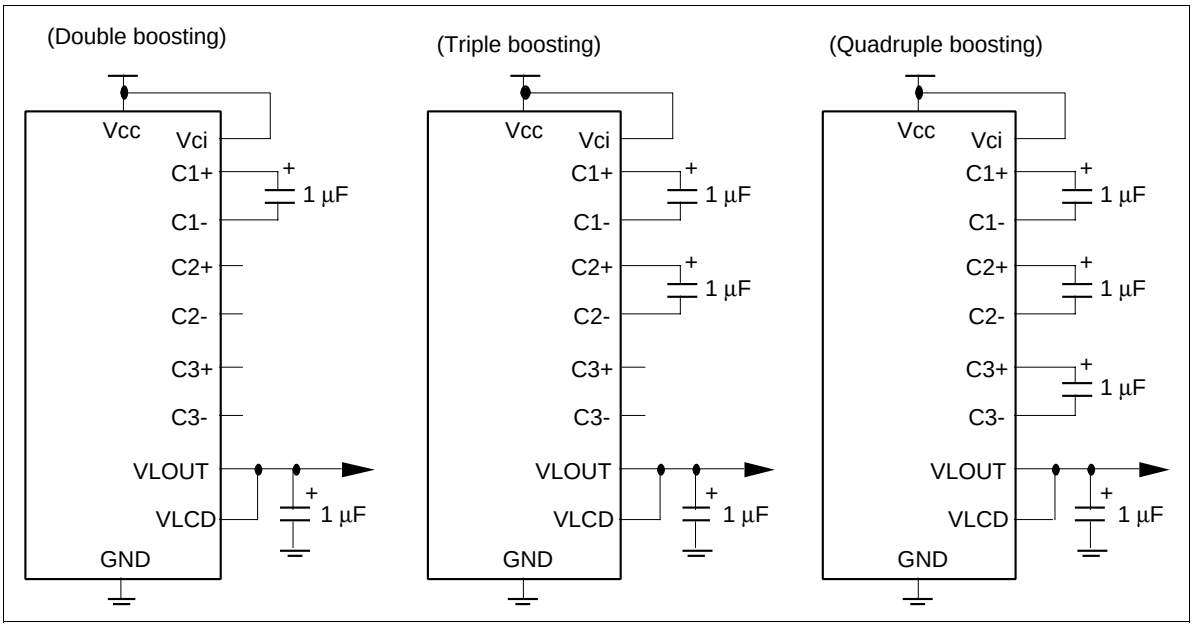
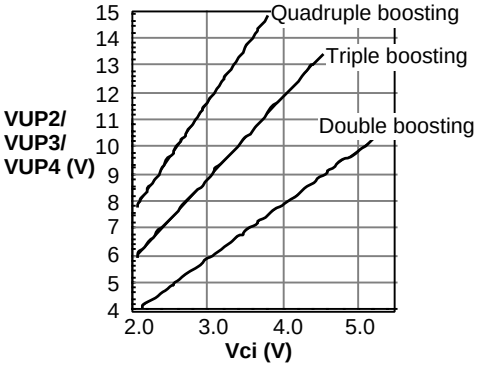


Figure 69 Booster

Referential data

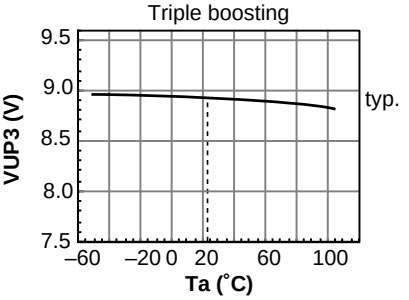
VUP2 = V_{LOUT} – GND; VUP3 = V_{LOUT} – GND; VUP4 = V_{LOUT} – GND

(i) Relation between the obtained voltage and input voltage



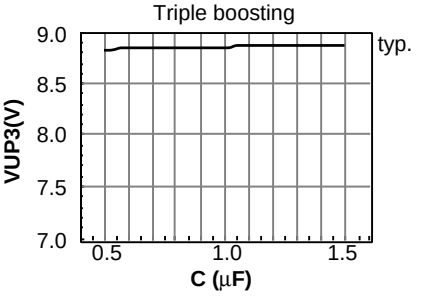
Vci = Vcc, fcp = 60 kHz, Ta = 25˚C

(ii) Relation between the obtained voltage and temperature

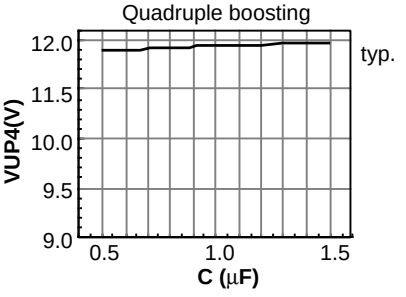


Vci = Vcc = 3.0 V, fosc = 60 kHz, Io = 30 µA

(iii) Relation between the obtained voltage and capacitance

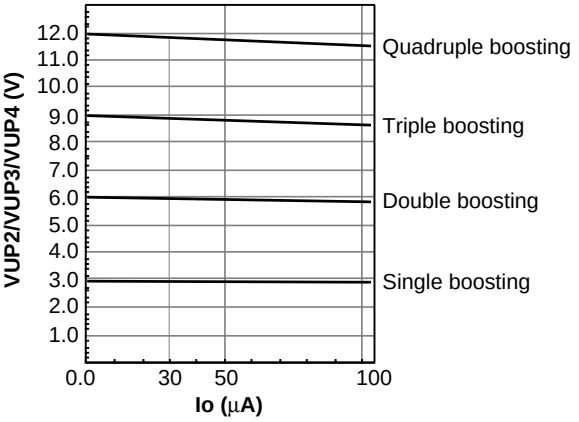


Vci = Vcc = 3.0 V, fosc = 60 kHz, Io = 30 µA



Vci = Vcc = 3.0 V, fosc = 60 kHz, Io = 30 µA

(iv) Relation between the obtained voltage and current



Vci = Vcc = 3.0 V, fosc = 60 kHz, Ta = 25°C

Figure 69 Booster (cont)

16. Vcc ≥ Vci must be maintained.

Load Circuits

AC Characteristics Test Load Circuits

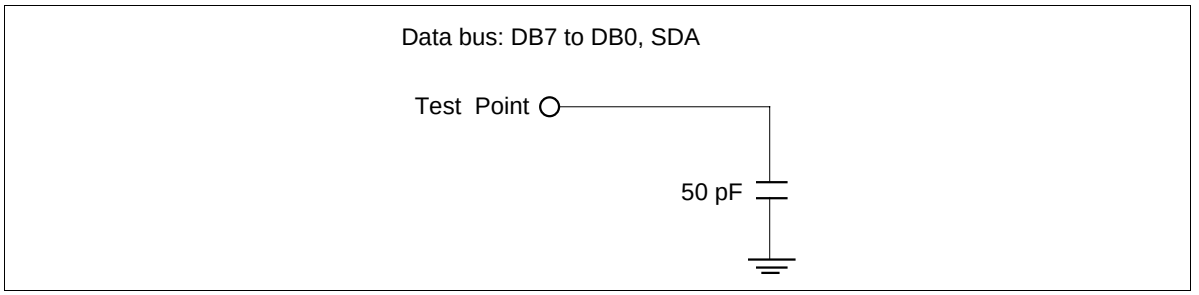
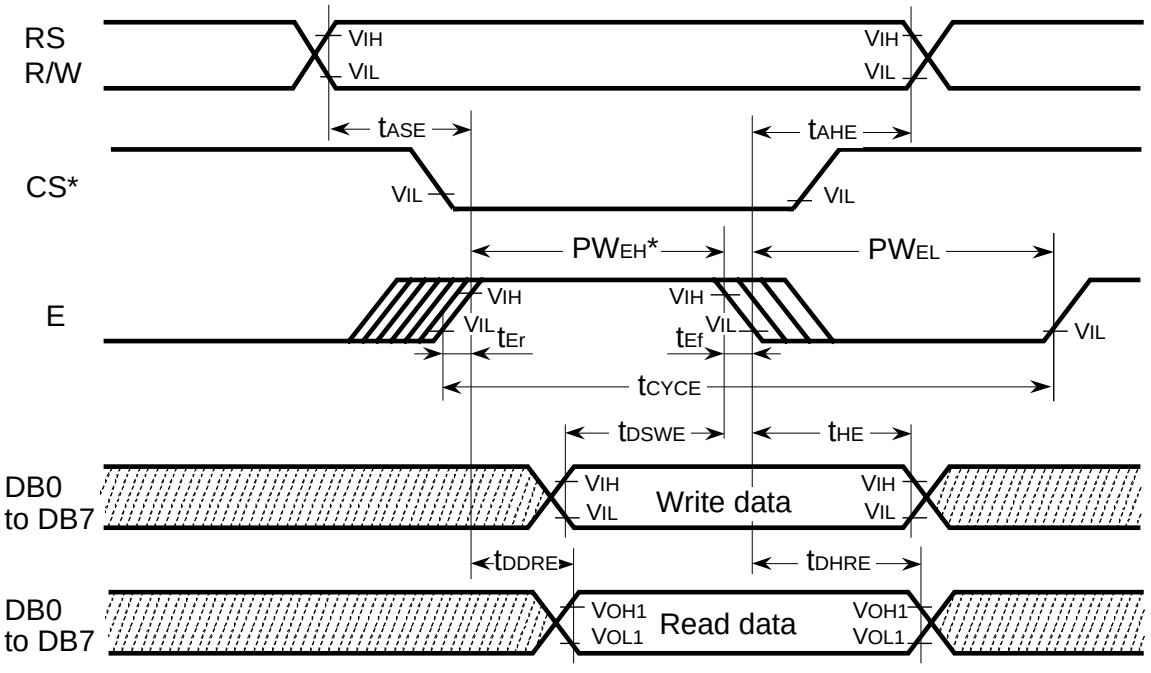


Figure 70 Load Circuit

Timing Characteristics

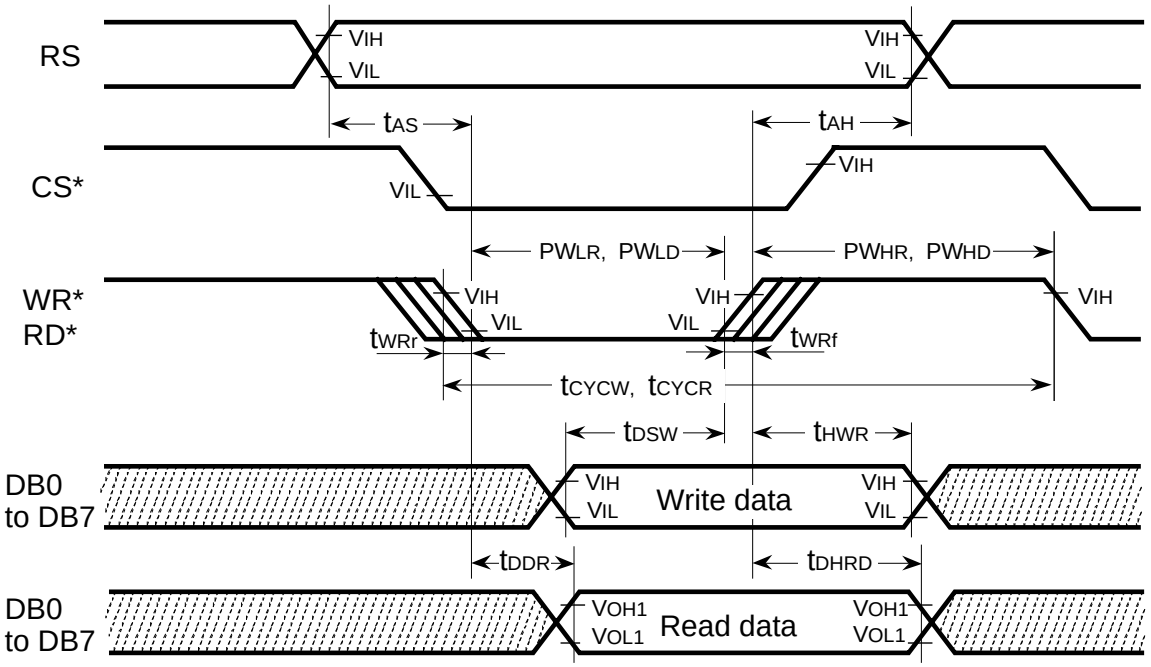
68-system Bus Operation



Note: PW_{EH} is defined as the overlapped period of CS* low-level and E high-level.

Figure 71 68-system Bus Timing

80-system Bus Operation



Note: PW_{LW} is defined as the overlapped period of CS* low-level and WR* low-level.
PW_{LR} is defined as the overlapped period of CS* low-level and RD* low-level.

Figure 72 80-system Bus Timing

Clock-synchronized Serial Operation

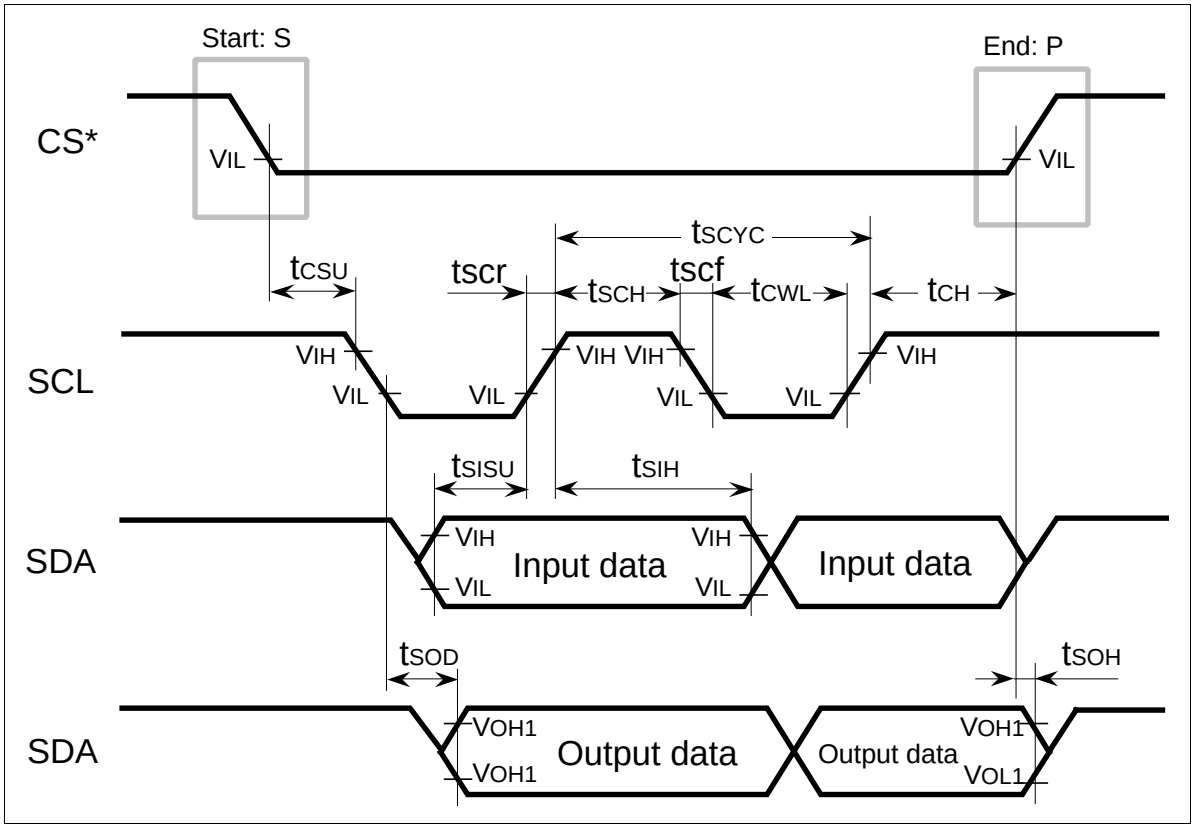


Figure 73 Clock-synchronized Serial Interface Timing

Reset Operation

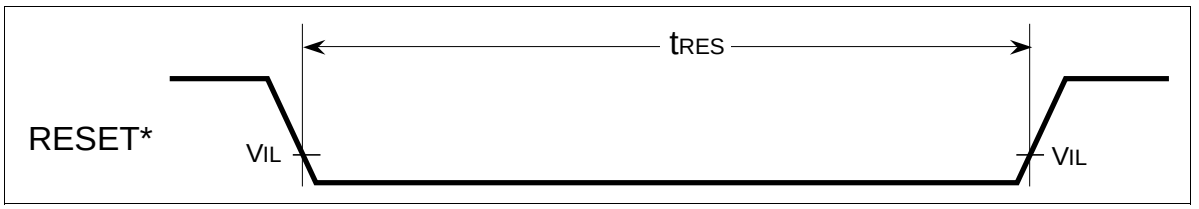


Figure 74 Reset Timing

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