HD66120T

(240-Channel Segment Driver for Dot-Matrix Graphic Liquid Crystal Display)

HITACHI

ADE-207-283(Z)
'99.9
Rev. 0.0

Description

The HD66120T is a segment driver for dot-matrix graphic liquid crystal display (LCD). It features a maximum driving voltage of 40V, enabling a high duty cycle. This driver operates at about 3V, making it suitable for battery-driven applications that make use of the low power dissipation of liquid crystal elements. The HD66120T, packaged in a fine-pitch slim tape carrier package (TCP), helps to reduce the size of the frame around an LCD panel.

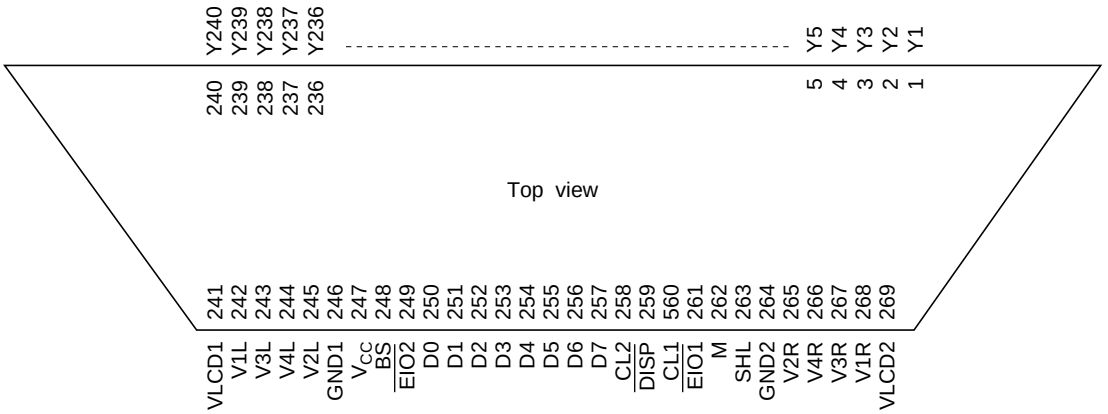
Features

- Duty cycle: 1/100 to 1/480
- High LCD driving voltage: 14 to 40V
- 240 LCD drive circuits
- Low operating voltage: 2.7 to 5.5V
- 4- and 8-bit data bus interface
- High-speed shift clocks
  - 10 MHz (max) at 3-V operation
  - 20 MHz (max) at 5-V operation
- Display off function
- Slim-TCP package
- Fine output lead pitch: 70 µm/74 µm
- Compact user area : 7.3 mm (when output lead pitch is 70 µm)
  : 7.6 mm (when output lead pitch is 74 µm)
- Internal chip enable signal generator
- Standby function

Ordering Information

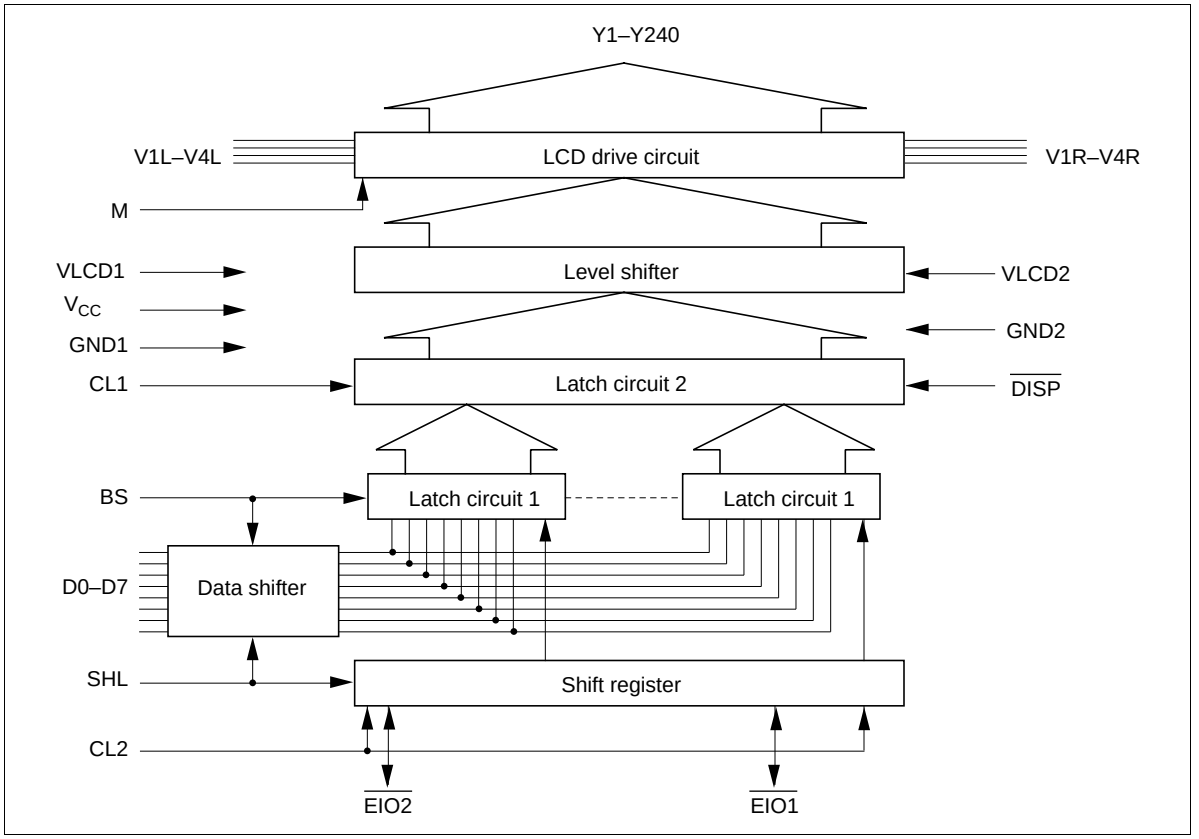
Type No.	Outer Lead Pitch (μm)
HD66120TA3	70
HD66120TA4	74

Pin Arrangement



Note: This figure does not specify the TCP dimensions; other TCP shapes are also possible.

Block Diagram



Block Functions

LCD Drive Circuit

The 240-bit LCD drive circuit generates four voltage levels V1, V2, V3, and V4, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on the combination of the M signal and the data in latch circuit 2.

Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

Latch Circuit 2

240-bit latch circuit 2 latches data input from latch circuit 1, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

Latch Circuit 1

240-bit latch circuit 1 latches 4-bit or 8-bit parallel data input via the D0 to D7 pins at the timing generated by the shift register.

Shift Register

The 60-bit shift register generates and outputs data latch signals for latch circuit 1 at the falling edge of each clock 2 (CL2) pulse.

Data Shifter

The data shifter shifts the destinations of display data output, when necessary.

Pin Description

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{CC}	247	V_{CC}	—	Power supply
GND1, GND2	246, 264	GND1, GND2	—	Power supply
VLCD1, VLCD2	241, 269	VLCD1, VLCD2	—	Power supply
V1L, V1R	242, 268	V1L, V1R	Input	Power supply
V2L, V2R	245, 265	V2L, V2R	Input	Power supply
V3L, V3R	243, 267	V3L, V3R	Input	Power supply
V4L, V4R	244, 266	V4L, V4R	Input	Power supply
CL1	260	Clock 1	Input	Control signal
CL2	258	Clock 2	Input	Control signal
M	262	M	Input	Control signal
D0–D7	250–257	Data 0–data 7	Input	Control signal
SHL	263	Shift left	Input	Control signal
$\overline{EIO1}$, $\overline{EIO2}$	261, 249	Enable IO 1, enable IO 2	Input/output	Control signal
$\overline{DISP}$	259	Display off	Input	Control signal
BS	248	Bus select	Input	Control signal
Y1–Y240	1–240	Y1–Y240	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, VLCD, GND: V_{CC}–GND1, GND2 supplies power to the internal logic circuits. VLCD–GND supplies power to the LCD drive circuits. See Figure 1.

V1L, V1R, V2L, V2R, V3L, V3R, V4L, V4R: Supply different levels of power to drive the LCD. V1 and V2 are selected levels, and V3 and V4 are non-selected levels.

Control Signals

CL1: Inputs display data latch pulses for latch circuit 2. Latch circuit 2 latches display data input from latch circuit 1, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for latch circuit 1. Latch circuit 1 latches display data input via D0–D7 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D0–D7: Input display data. High-voltage level (V_{CC} level) of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level (GND level) data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output, and determines which chip enable pin ($\overline{EIO1}$ or $\overline{EIO2}$) is an input and which is an output. See Figure 2.

$\overline{EIO1}$, $\overline{EIO2}$: If SHL is V_{CC} level, $\overline{EIO1}$ inputs the chip enable signal, and $\overline{EIO2}$ outputs the signal. If SHL is GND level, $\overline{EIO1}$ outputs the chip enable signal, and $\overline{EIO2}$ inputs the signal. The chip enable input pin of the first HD66120T must be grounded, and those of the other HD66120Ts must be connected to the chip enable output pin of the previous HD66120T. The chip enable output pin of the last HD66120T must be open.

$\overline{DISP}$: A low $\overline{DISP}$ sets LCD drive outputs Y1–Y240 to V2 level.

BS: Selects either the 4-bit or 8-bit display data bus interface. If BS is V_{CC} level, the 8-bit bus is selected, and if BS is GND level, the 4-bit bus is selected. In 4-bit bus mode, data is latched via D0–D3; D4–D7 must be grounded.

LCD Drive Output

Y1–Y240: Each Y outputs one of the four voltage levels V1, V2, V3, or V4, depending on the combination of the M signal and display data levels. See Figure 3.

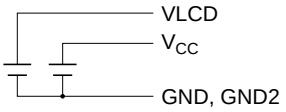


Figure 1 Power Supply for Logic and LCD Drive Circuits

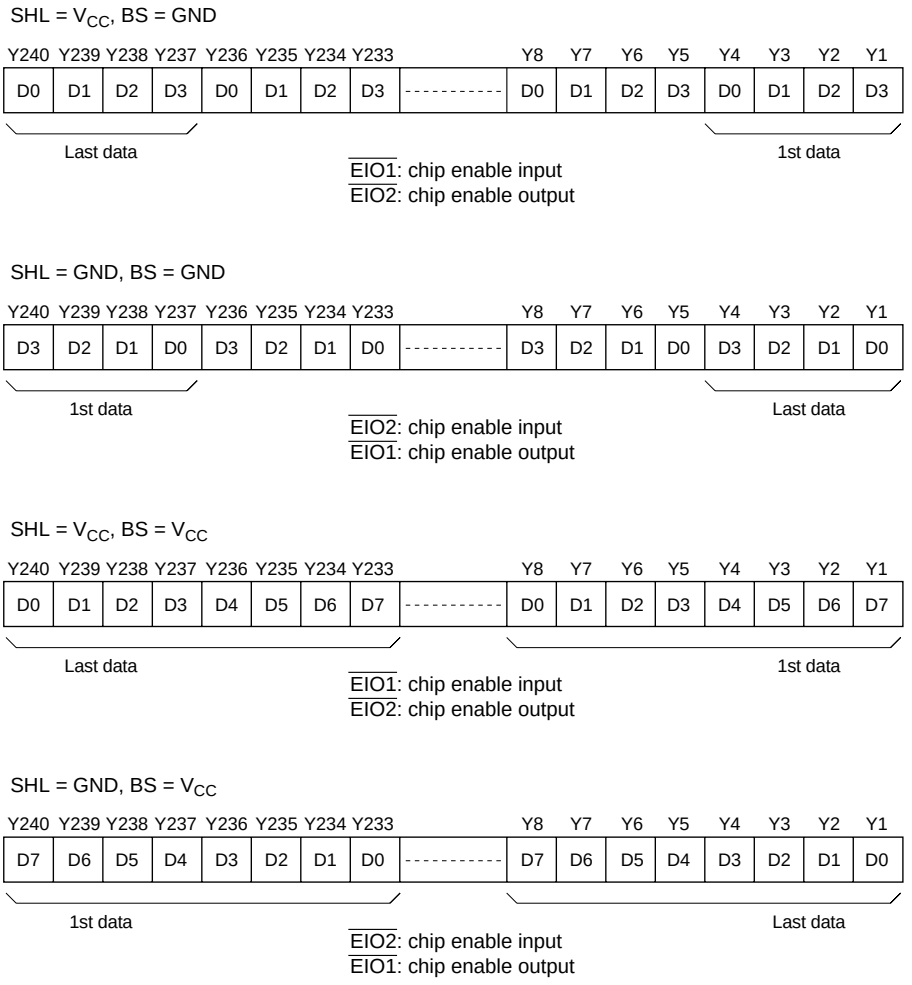


Figure 2 Selection of Destinations of Display Data Output

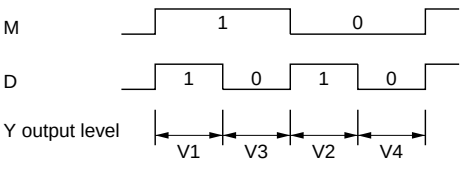


Figure 3 Selection of LCD Drive Output Level

Operation Timing

4-Bit Bus Mode (BS = GND)

Figure 4 shows 4-bit data latch timing when SHL = GND, that is, the $\overline{EIO2}$ pin is a chip enable input and $\overline{EIO1}$ pin is a chip enable output. When SHL = V_{CC}, the $\overline{EIO1}$ pin is a chip enable input and $\overline{EIO2}$ pin is a chip enable input.

When a low chip enable signal is input via the $\overline{EIO1}$ pin, the HD66120T is first released from data standby state, and, at the falling edge of the following CL2 pulse, it is released entirely from standby state and starts latching data. It simultaneously latches 4 bits of data at the falling edge of each CL2 pulse. When it has latched 236 bits of data, it sets the $\overline{EIO2}$ signal low. When it has latched 240 bits of data, it automatically stops and enters standby state, initiating the next HD66120T, as long as its $\overline{EIO2}$ pin is connected to the $\overline{EIO1}$ pin of the next HD66120T.

The HD66120Ts output one line of data from the Y1–Y240 pins at the falling edge of each CL1 pulse. Data d1 is output from Y1, and d240 from Y240 when SHL = GND, and d1 is output from Y240, and d240 from Y1 when SHL = V_{CC}. Data output level is either VLCD, V2, V3, or V4 depending on the combination of the M signal and the data level.

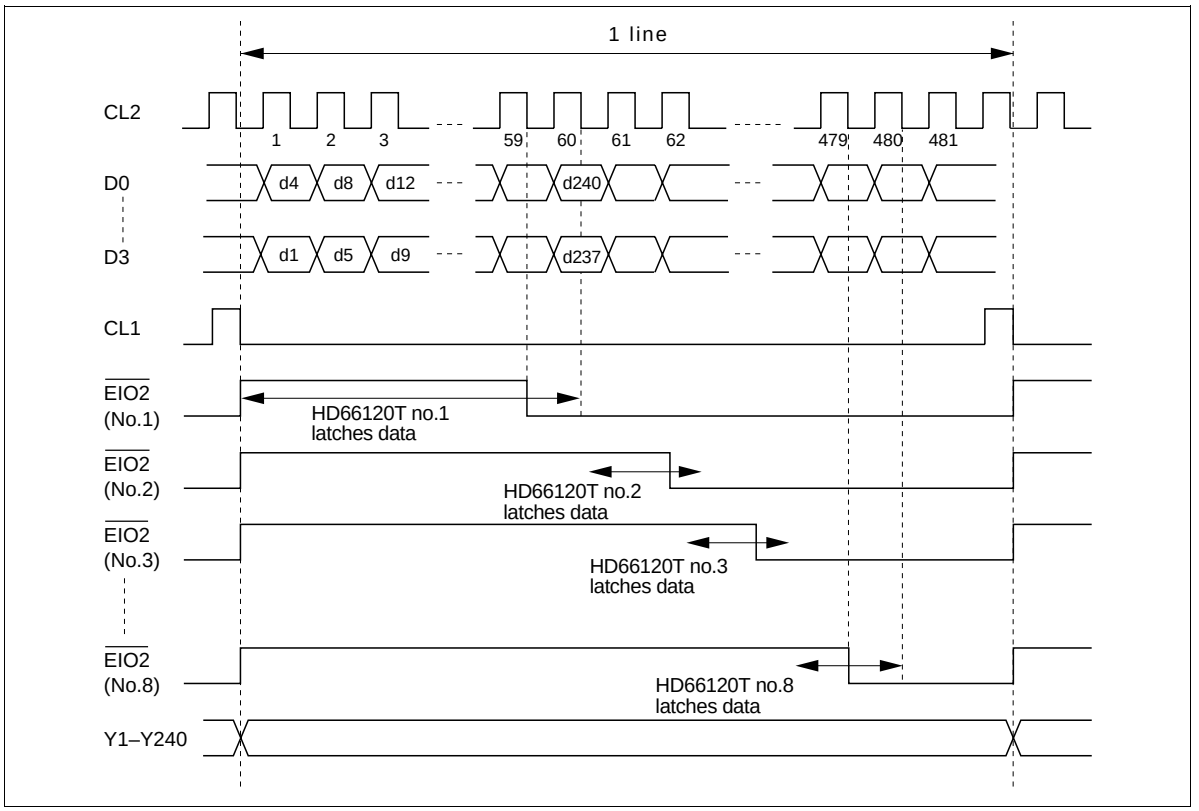


Figure 4 4-Bit Data Latch Timing (BS = GND, 1 Line: 640-by-3 Dots)

8-Bit Bus Mode (BS = V_{CC})

The operation is the same as that in 4-bit bus mode except that 8 bits of data are latched simultaneously.

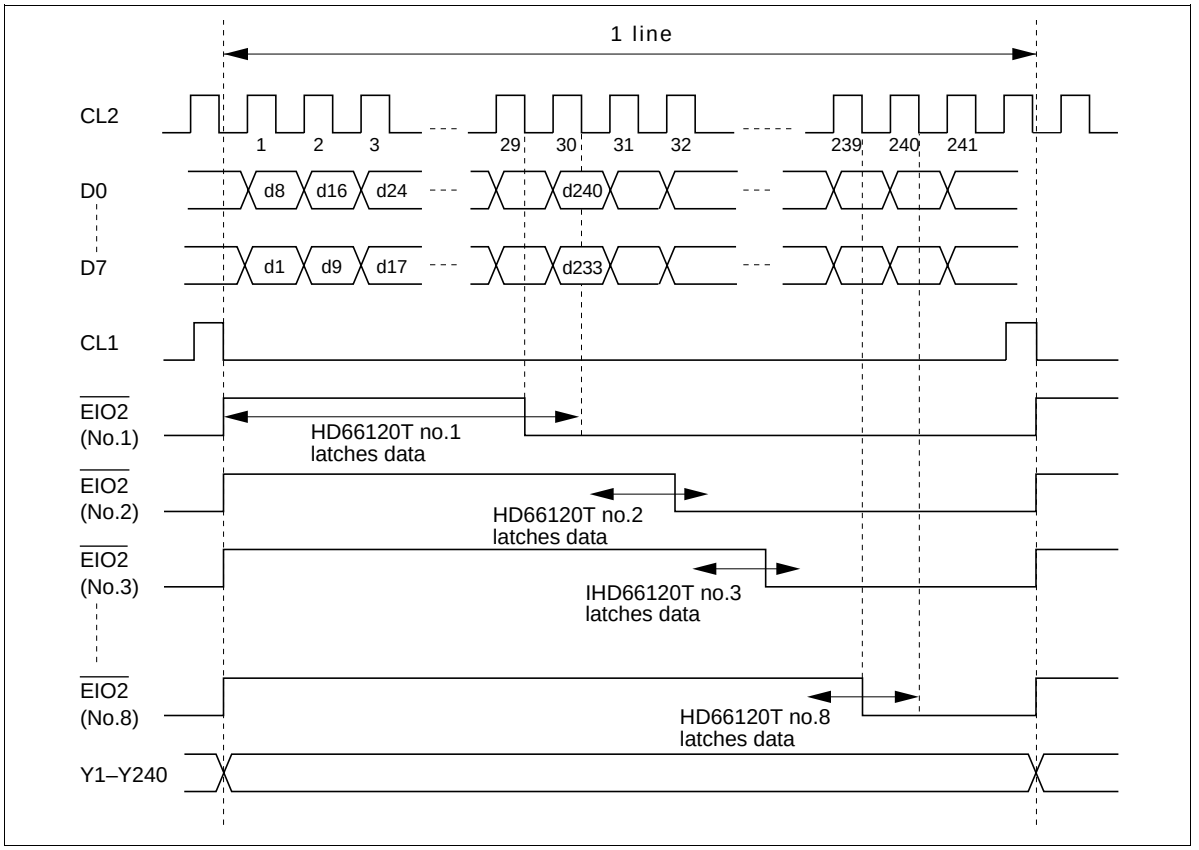
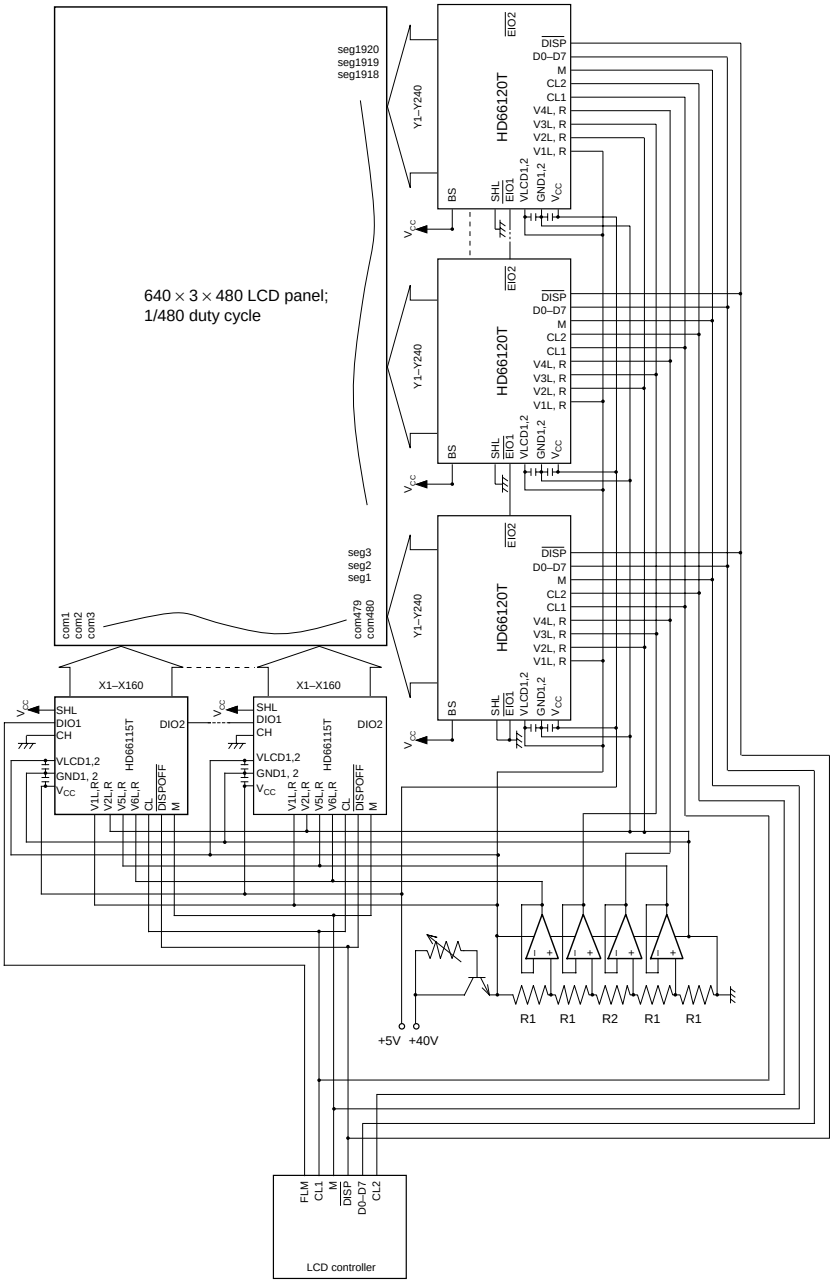


Figure 5 8-Bit Data Latch Timing (BS = V_{CC}, 1 Line: 640-by-3 Dots)

Application Example



Notes: 1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/20 bias, R1 and R2 must be 3 kΩ and 48 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/20.

2. To stabilize the power supply, place two 0.1-µF capacitors near each HD66120T, one between the V_{CC} and GND pins, and the other between the VLCD and GND pins.

3. The load must be less than 30 pF between the $\overline{EIO2}$ and $\overline{EIO1}$ connections of HD66120Ts.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to + 7.0	V	1, 4
Power supply voltage for LCD drive circuits	VLCD	–0.3 to + 42	V	1, 4
Input voltage 1	VT1	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	VT2	–0.3 to VLCD + 0.3	V	1, 3
Operating temperature	T_{opr}	–30 to +75	°C	
Storage temperature	T_{stg}	–55 to +110	°C	

Notes:
1. The reference point is GND (0V).
2. Applies to input pins for logic circuits.
3. Applies to V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R pins.
4. Power should be applied to V_{CC}–GND first, and then VLCD–GND. It should be disconnected in the reverse way.
5. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 2.7 to 4.5V, VLCD–GND = 14 to 40V, and Ta = –30 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Test Condition	Notes
Input high voltage	VIH	1	$0.8 \times V_{CC}$	V_{CC}	V		
Input low voltage	VIL	1	0	$0.2 \times V_{CC}$	V		
Output high voltage	VOH	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	VOL	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	3.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5.0	5.0	µA	VIN = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–100	100	µA	VIN = VLCD to GND	2
Current consumption 1	I_{CC}	—	—	3.3	mA	V_{CC} = 3.0V f_{CL2} = 10 MHz f_{CL1}= 36 kHz f_M = 75 Hz	2
Current consumption 2	I_{LCD}	—	—	3.8	mA	Same as above	2
Current consumption 3	I_{ST}	—	—	0.45	mA	Same as above	2, 3

Pins and notes at the end of the DC characteristics 2 table.

DC Characteristics 2 (V_{CC} = 5V ± 10%, VLCD–GND = 14 to 40V, and Ta = –30 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Test Condition	Notes
Input high voltage	VIH	1	$0.8 \times V_{CC}$	V_{CC}	V		
Input low voltage	VIL	1	0	$0.2 \times V_{CC}$	V		
Output high voltage	VOH	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	VOL	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	3.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5.0	5.0	µA	VIN = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–100	100	µA	VIN = VLCD to GND	2
Current consumption 1	I_{CC}	247	—	10	mA	f_{CL2} = 12 MHz f_{CL1} = 36 kHz f_M = 75 Hz	2
Current consumption 2	I_{LCD}	241, 269	—	3.8	mA	Same as above	2
Current consumption 3	I_{ST}	247	—	1.0	mA	Same as above	2, 3

Pins: 1. CL1, CL2, M, SHL, BS, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISP}$, D0–D7
2. $\overline{EIO1}$, $\overline{EIO2}$
3. Y1–Y240, VLCD1, VLCD2, V1L, V1R, V2L, V2R, V3L, V3R, V4L, V4R
4. V1L, V1R, V2L, V2R, V3L, V3R, V4L, V4R

Notes: 1. Indicates the resistance between one pin from Y1–Y240 and another pin from V1–V4, when load current is applied to the Y pin; defined under the following conditions.

VLCD–GND = 40V

V1, V3 = VLCD – {1/20(VLCD–GND)}

V2, V4 = GND + {1/20(VLCD–GND)}

V1 and V3 should be near VLCD level, and V2 and V4 should be near GND level (Figure 6). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage VLCD–GND (Figure 7).

2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, VIH and VIL must be held to V_{CC} and GND levels, respectively.
3. Applies to standby mode.

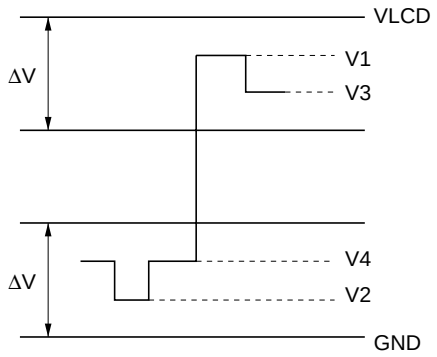


Figure 6 Relation between Driver Output Waveform and Level Voltages

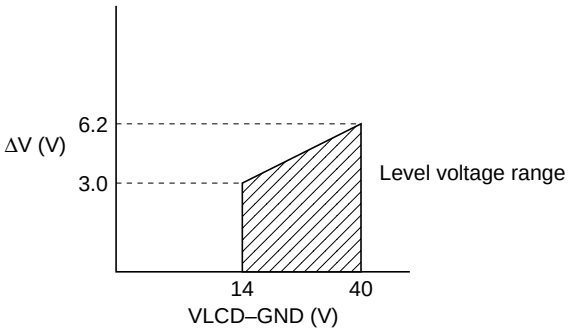


Figure 7 Relation between VLCD–GND and ΔV

AC Characteristics 1 (V_{CC} = 2.7 to 4.5V, VLCD–GND = 14 to 40V, and Ta = –30 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	100	—	ns
Clock high-level width 1	t_{CWH2}	CL2	37	—	ns
Clock low-level width 1	t_{CWL2}	CL2	37	—	ns
Clock high-level width 2	t_{CWH1}	CL1	50	—	ns
Clock setup time	t_{SCL}	CL1, CL2	100	—	ns
Clock hold time	t_{HCL}	CL1, CL2	100	—	ns
Clock rise time	t_r	CL1, CL2	—	50*[1]	ns
Clock fall time	t_f	CL1, CL2	—	50*[1]	ns
Data setup time	t_{DS}	D0–D7, CL2	35	—	ns
Data hold time	t_{DH}	D0–D7, CL2	35	—	ns
M phase difference time	t_{CM}	M, CL1	—	300	ns
Output delay time 1	t_{pd1}	CL1, Y1–Y240	—	1.2	µs
Output delay time 2	t_{pd2}	M, Y1–Y240	—	1.2	µs

Notes at the end of the AC characteristics 2 table.

AC Characteristics 2 (V_{CC} = 5V ± 10%, VLCD–GND = 14 to 40V, and Ta = –30 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	50	—	ns
Clock high-level width 1	t_{CWH2}	CL2	15	—	ns
Clock low-level width 1	t_{CWL2}	CL2	15	—	ns
Clock high-level width 2	t_{CWH1}	CL1	15	—	ns
Clock setup time	t_{SCL}	CL1, CL2	100	—	ns
Clock hold time	t_{HCL}	CL1, CL2	100	—	ns
Clock rise time	t_r	CL1, CL2	—	50*[1]	ns
Clock fall time	t_f	CL1, CL2	—	50*[1]	ns
Data setup time	t_{DS}	D0–D7, CL2	5	—	ns
Data hold time	t_{DH}	D0–D7, CL2	15	—	ns
M phase difference time	t_{CM}	M, CL1	—	300	ns
Output delay time 1	t_{pd1}	CL1, Y1–Y240	—	0.7	µs
Output delay time 2	t_{pd2}	M, Y1–Y240	—	0.7	µs

Notes: 1. The clock rise and fall times (t_r, t_f) must satisfy the following relationships:
t_r, $t_f < (t_{CYC} – t_{CWH2} – t_{CWL2})/2$
t_r, $t_f \leq 50$ ns
2. The load must be less than 30 pF between the $\overline{EIO2}$ and $\overline{EIO1}$ connections of HD66120Ts.

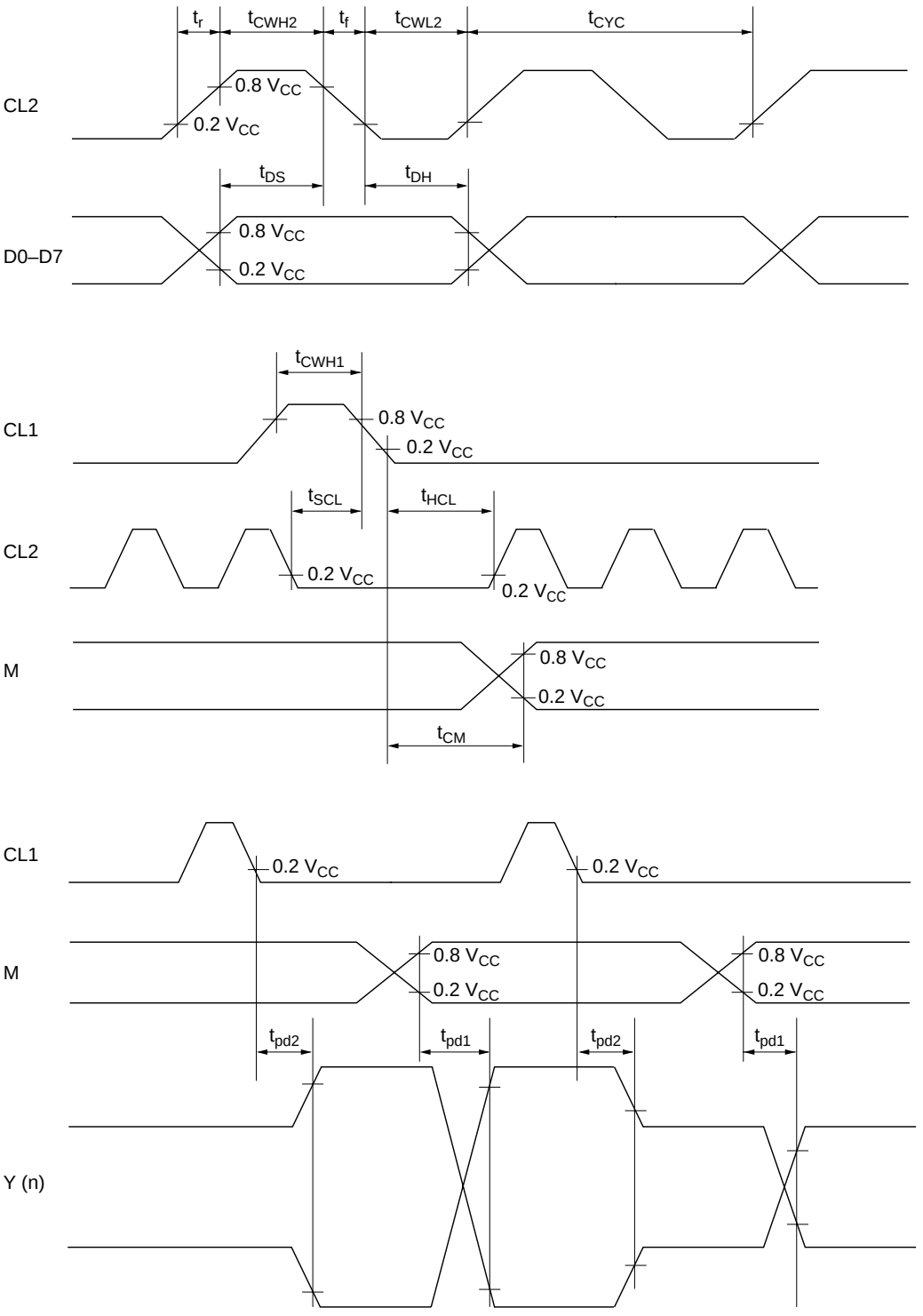


Figure 8 LCD Controller Interface Timing

LCD Driver LSI Power Supply Pin Connection

A feature of the LCD driver is the LCD drive power supply. As the number of pixel drives per LSI increases, so does the voltage and number of outputs.

Consequently, if multi-output CMOS circuits are switched simultaneously, a wiring voltage drop may occurs due to transient currents, and the potential between the LCD drive circuit power supply (V_{LCD}) and LCD drive level power supplies (V1, V6, and V3) or GND and the LCD level power supplies (V2, $\overline{V5}$, and V4) may be inverted, resulting in latchup breakdown. To prevent this, it is recommended that, when designing the LCD drive power supply and board power supply wiring, the power supply wiring be designed as low-impedance and capacitors be inserted in the wiring between V_{LCD} and V1, V3, V6, and between V2, V4, V5 and GND. In set evaluation, it is recommended that a check be carried out to confirm that there is no inversion of the LCD drive power supply and level power supplies in the period between when the LCD drive power supply is turned on and turned off.

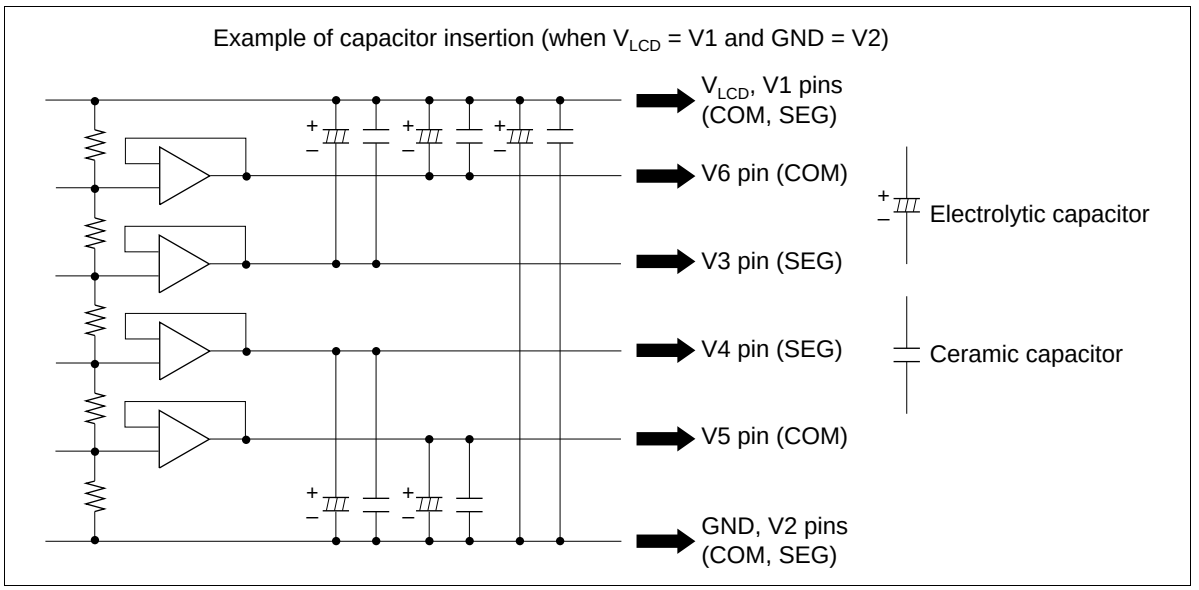


Figure 9 Example of Capacitor Insertion

Notes on Power-On/Off of the LCD Driver

To prevent an LCD driver display error at power on/off, the sequence for power-on signal activation must be as follows (see figure 10):

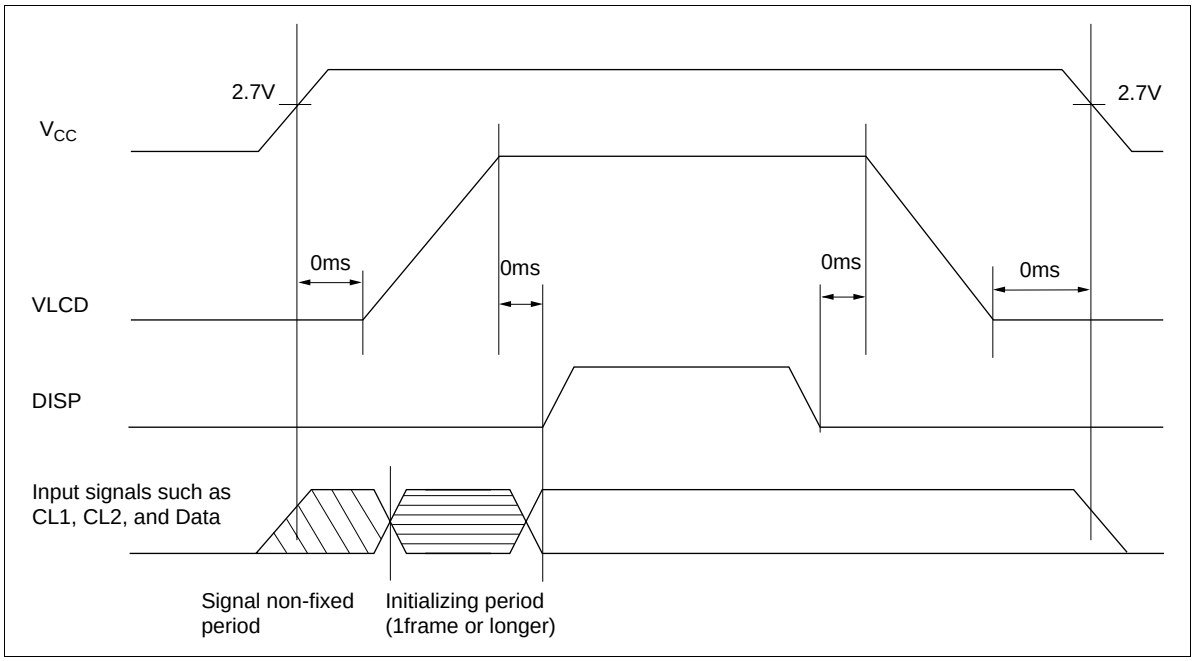


Figure 10 Sequence of Power-On/Off

At Power On

(1) Power on V_{CC}. At this time, input 0 to the $\overline{DISP}$ pin.
(2) Display-off function forces the LCD driver to output a V2 level (lowest level).
(3) Display-off function takes priority even if the input signal status becomes irregular immediately after V_{CC} power-on.
(4) Input the specified signals to initialize registers of the LCD driver. Its period must be 1 frame or longer.
(5) Set the $\overline{DISP}$ level to 1 to cancel display-off function after steps (1) to (4). At this time, VLCD and each V pin input must be at the specified levels.

At Power Off

Basically, the power-off procedure is the reverse of the power-on procedure.

(1) Set the $\overline{DISP}$ level to 0.
(2) Lower LCD driver power supply to 0V
(3) Lower V_{CC} and each input signals to 0V

At this time, each V pin input must be at 0V. Display-off function stops when V_{CC} falls to 0V, and therefore, the LCD driver may output a level other than V2 (lowest level). As a result, a display error may be caused at power-off or power-on.

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