HD66717

(Low-Power Dot-Matrix Liquid Crystal Display Controller/Driver)

HITACHI

ADE-207-307(Z)
'99.9
Rev. 0.0

Description

The HD66717 dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, katakana, hiragana, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of an I^2C bus, a clock-synchronized serial, or a 4- or 8-bit microprocessor. A single HD66717 is capable of displaying a maximum of four 12-character lines, 40 segments, and 10 annunciators. The HD66717 incorporates all the functions required for driving a dot-matrix liquid crystal display such as display RAM, character generator, and liquid crystal drivers, and a booster for LCD power supply.

The HD66717 provides various functions to reduce the power consumption of an LCD system such as low-voltage operation of 2.4V or less, a booster for generating a maximum of triple LCD drive voltage from the supplied voltage, and voltage-followers for decreasing the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions such as standby and sleep modes allows a fine power control. The HD66717, with the above functions, is suitable for any portable battery-driven product requiring long-term driving capabilities and small size.

Features

- 5×8-dot matrix LCD drive
- Four 12-character lines, 40 segments, and 10 annunciators
- Low-power operation support:
  - — 2.4 to 5.5V (low voltage)
  - — Double or triple booster for liquid crystal drive voltage
  - — Electron volume function and voltage-followers for decreasing the direct current flow in the LCD drive bleeder-resistors
  - — Standby mode and sleep mode
  - — Displays up to 10 static annunciators
- I^2C bus or clock-synchronized serial interface; 4- or 8-bit parallel bus interface
- 60×8-bit display data RAM (60 characters max)
- 9,600-bit character generator ROM
  - — 240 characters (5×8 dots)

- 32 × 5-bit character generator RAM
  - — 4 characters (5 × 8 dots)
- 8 × 5-bit segment RAM
  - — 40 segment-icons and marks max
- 60-segment × 34-common liquid crystal display driver
- Programmable display sizes and duty ratios (see List1)
- Vertical smooth scroll
- Double-height display
- Wide range of instruction functions:
  - — Display clear, display on/off, icon and mark control, character blink, white-black inverting blinking cursor, icon and mark blink, cursor home, cursor on/off, white-black inverting raster-row
- Hardware reset
- Internal oscillation with an external resistor
- Wide range of LCD drive voltages
  - — 3.0V to 13.0V
- Slim chip with/without bump (for COB) and tape carrier package (TCP)

List 1 Programmable Display Sizes and Duty Ratios

Display Size	Duty Ratio	Oscillation Frequency	Current Consumption	Multi-plexed-Drive Segments	Static-Drive Annunciators
1 line × 12 characters	1/10	40 kHz	8 µA	40	10
2 lines × 12 characters	1/18	80 kHz	15 µA	40	10
3 lines × 12 characters	1/26	120 kHz	23 µA	40	10
4 lines × 12 characters	1/34	160 kHz	30 µA	40	10

Note: Current consumption excludes that for LCD power supply source; V_{CC} = 3V.

Ordering Information

Type Name	External Dimension	Special spec.	Internal Font
HD66717A03TA0	TCP-153		Japanese and European fonts
HD66717A03TA1L	TCP-149	1/4 bias driving	
HD66717A03TA2L	TCP-149	1/6 bias driving	
HCD66717A03	Bare chip		
HCD66717A03BP	Au-bumped chip		
HD66717LA03TA0	TCP-153	Built-in Low power op-amp.	
HCD66717LA03	Bare chip	Built-in Low power op-amp.	
HCD66717LA03BP	Au-bumped chip	Built-in Low power op-amp.	
HD66717A13TA0L	TCP-153		Up-side-down pattern of A03
HCD66717A13BP	Au-bumped chip		
HCD66717LA13BP	Au-bumped chip	Built-in Low power op-amp.	
HD66717A02TA0L	TCP-153		European font
HCD66717A02	Bare chip		(ROM code : A02)
HCD66717A02BP	Au-bumped chip		
HD66717A12TA0L	TCP-153		Up-side-down pattern of A02
HCD66717A12BP	Au-bumped chip		

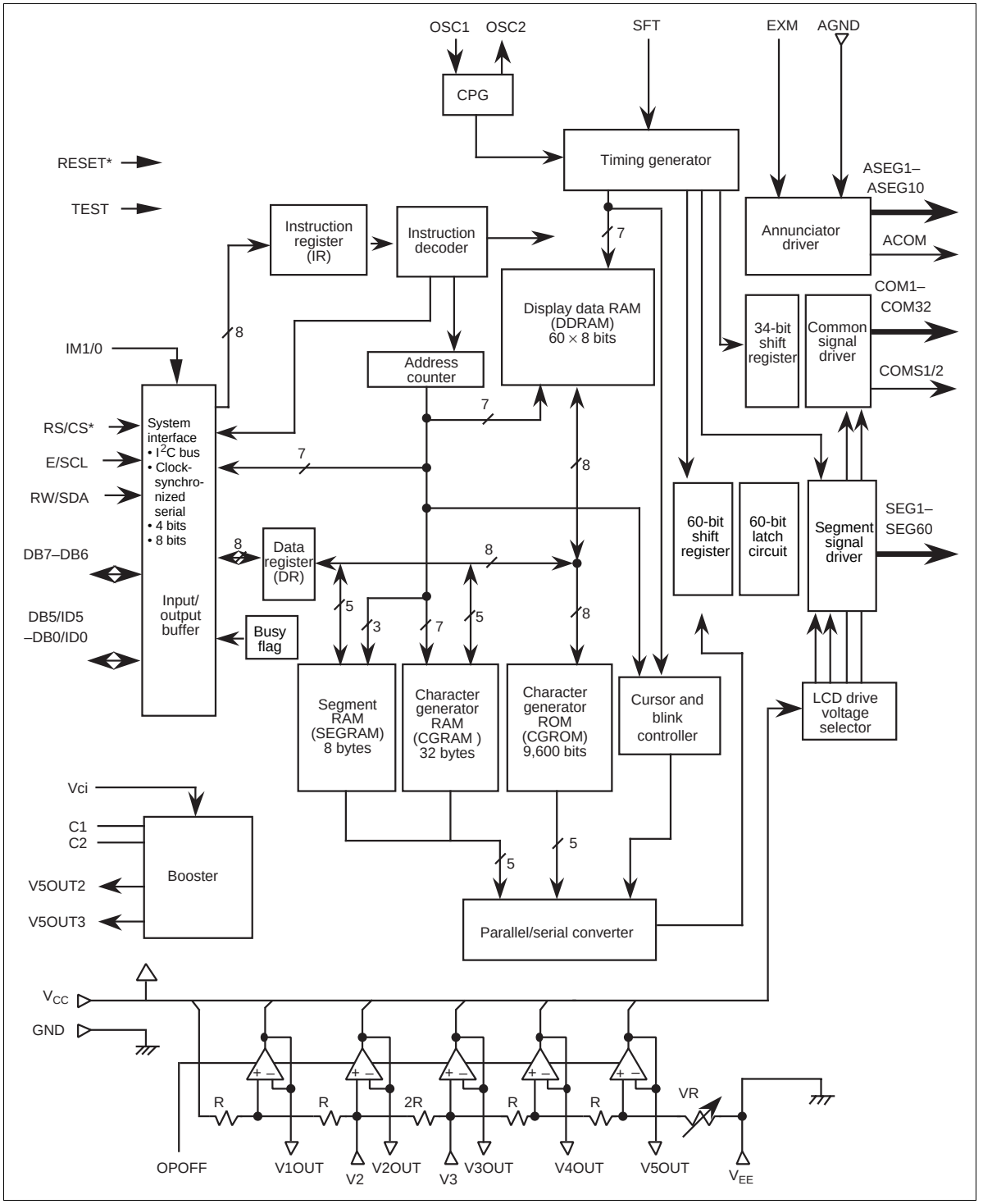
LCD-II Family Comparison

Item	LCD-II (HD44780U)	HD66702R	HD66710	HD66712U
Power supply voltage	2.7V to 5.5V	5V ± 10% (standard) 2.7V to 5.5V (low voltage)	2.7V to 5.5V	2.7V to 5.5V
Liquid crystal drive voltage	3.0 to 11.0V	3.0V to 8.3V	3.0 to 13.0V	2.7 to 11.0V
Maximum display - characters per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters × 4 lines	24 characters × 2 lines/ 12 characters × 4 lines
Segment display	None	None	40	60 (extended to 80)
Display duty ratio	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/17 and 1/33	1/17 and 1/33
CGROM	9,920 bits (208 5-×-8 dot characters and 32 5-×-10 dot characters)	7,200 bits (160 5-×-7 dot characters and 32 5-×-10 dot characters)	9,600 bits (240 5-×-8 dot characters)	9,600 bits (240 5-×-8 dot characters)
CGRAM	64 bytes	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes	80 bytes
SEGRAM	None	None	8 bytes	16 bytes
Segment signals	40	100	40	60
Common signals	16	16	33	34
Liquid crystal drive waveform	A	B	B	B
Clock source	External resistor or external clock	External resistor or external clock	External resistor or external clock	External resistor or external clock
Rf oscillation frequency	270 kHz ± 30%	320 kHz ± 30%	270 kHz ± 30%	270 kHz ± 30%
Liquid crystal voltage booster circuit	None	None	Double or triple booster circuit	Double or triple booster circuit
Liquid crystal drive operational amplifier	None	None	None	None
Bleeder-resistor for liquid crystal drive	External	External	External	External
Liquid crystal contrast adjuster	None	None	None	None
Key scan circuit	None	None	None	None
Extension driver control signal	Independent control signal	Independent control signal	Used in common with a driver output pin	Independent control signal
Reset function	Internal reset circuit	Internal reset circuit	Internal reset circuit	Internal reset circuit or reset input
Horizontal smooth scroll	Impossible	Impossible	Dot unit	Dot unit and line unit
Vertical smooth scroll	Impossible	Impossible	Impossible	Impossible
Number of displayed lines	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4
Low power control	None	None	Low power mode	Low power mode
Bus interface	4 or 8 bits	4 or 8 bits	4 or 8 bits	Serial, 4, or 8 bits
Package	80-pin QFP1420 80-pin TQFP1414 80-pin bare chip	144-pin FQFP2020 144-pin bare chip	100-pin QFP1420 100-pin TQFP1414 100-pin bare chip	128-pin TCP 128-pin bare chip

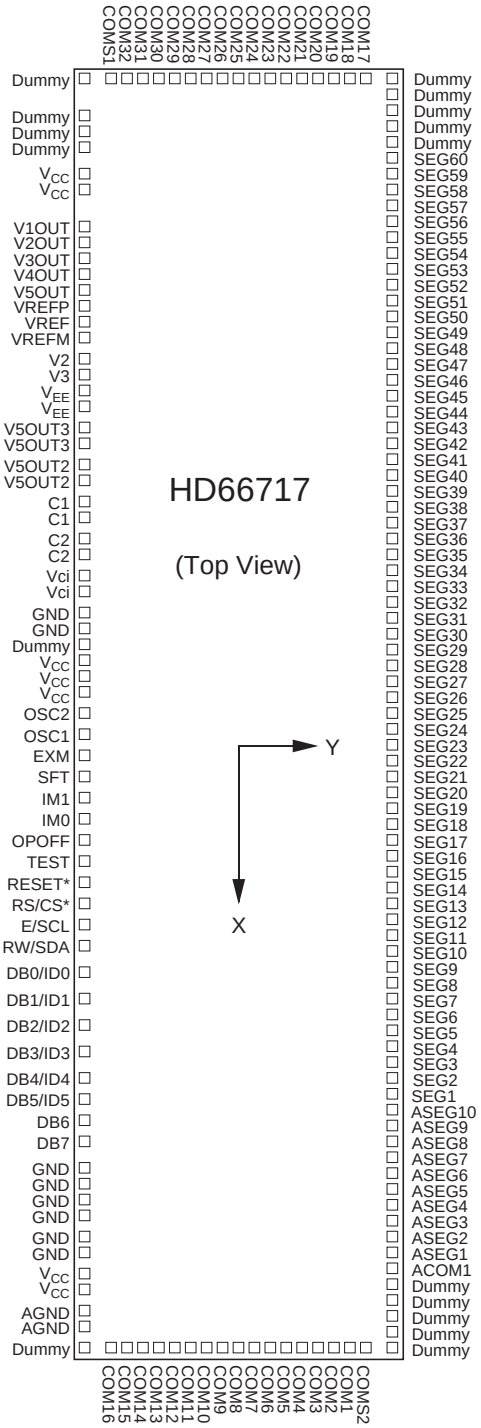
LCD-II Family Comparison (cont)

Item	HD66720	HD66717	HD66727
Power supply voltage	2.7V to 5.5V	2.4V to 5.5V	2.4V to 5.5V
Liquid crystal drive voltage	3.0 to 11.0V	3.0 to 13.0V	3.0 to 13.0V
Maximum display characters per chip	10 characters × 1 line/ 8 characters × 2 lines	12 characters × 1 line/2 lines/3 lines/4 lines	12 characters × 1 line/2 lines/3 lines/4 lines
Segment display	42 (extended to 80)	40 (and 10 annunciators)	40 (and 12 annunciators)
Display duty ratio	1/9 and 1/17	1/10, 1/18, 1/26, and 1/34	1/10, 1/18, 1/26, and 1/34
CGROM	9,600 bits (240 5-×-8 dot characters)	9,600 bits (240 5-×-8 dot characters)	11,520 bits (240 6-×-8 dot characters)
CGRAM	64 bytes	32 bytes	32 bytes
DDRAM	40 bytes	60 bytes	60 bytes
SEGRAM	16 bytes	8 bytes	8 bytes
Segment signals	42	60	60
Common signals	17	34	34
Liquid crystal drive waveform	B	B	B
Clock source	External resistor or external clock	External resistor or external clock	External resistor or external clock
Rf oscillation frequency	160 kHz ± 30%	1-line mode: 40 kHz ± 30% 2-line mode: 80 kHz ± 30% 3-line mode: 120 kHz ± 30% 4-line mode: 160 kHz ± 30%	1-line mode: 40 kHz ± 30% 2-line mode: 80 kHz ± 30% 3-line mode: 120 kHz ± 30% 4-line mode: 160 kHz ± 30%
Liquid crystal voltage booster circuit	Double or triple booster circuit	Double or triple booster circuit	Double or triple booster circuit
Liquid crystal drive operational amplifier	None	Built-in for each V1 to V5	Built-in for each V1 to V5
Bleeder-resistor for liquid crystal drive	External	Internal 1/4 and 1/6 bias resistors	Internal 1/4 and 1/6 bias resistors
Liquid crystal contrast adjuster	None	Incorporated	Incorporated
Key scan circuit	5 × 6 = 30 keys	None	4 × 8 = 32 keys
Extension driver control signal	Independent control signal	None	None
Reset function	Internal reset circuit or reset input	Reset input	Reset input
Horizontal smooth scroll	Dot unit and line unit	Impossible	Impossible
Vertical smooth scroll	Impossible	Dot (raster-row) unit	Dot (raster-row) unit
Number of displayed lines	1 or 2	1, 2, 3, or 4	1, 2, 3, or 4
Low power control	Low power mode and sleep mode	Standby mode and sleep mode	Standby mode and sleep mode
Bus interface	Serial	I^2C, serial, 4, or 8 bits	I^2C or clock-synchronized serial
Package	100-pin QFP1420 100-pin TQFP1414 100-pin bare chip	Slim chip with/without bumps TCP	Slim chip with/without bumps TCP

HD66717 Block Diagram



HD66717 Pin Arrangement



HD66717 Pad Coordinate

No.	Pad Name	X	Y
—	Dummy	–5191	–1260
—	Dummy	–4891	–1260
—	Dummy	–4767	–1260
—	Dummy	–4643	–1260
1	V_{CC}	–4439	–1244
2	V_{CC}	–4315	–1244
3	V1OUT	–4034	–1169
4	V2OUT	–3913	–1169
5	V3OUT	–3793	–1169
6	V4OUT	–3672	–1169
7	V5OUT	–3552	–1169
8	VREFP	–3432	–1169
9	VREF	–3311	–1169
10	VREM	–3191	–1169
11	V2	–3045	–1168
12	V3	–2924	–1168
13	V_{EE}	–2803	–1168
14	V_{EE}	–2683	–1168
15	V5OUT3	–2526	–1168
16	V5OUT3	–2406	–1168
17	V5OUT2	–2225	–1168
18	V5OUT2	–2105	–1168
19	C1	–1955	–1168
20	C1	–1834	–1168
21	C2	–1683	–1168
22	C2	–1562	–1168
23	Vci	–1411	–1168
24	Vci	–1290	–1168
25	GND	–1139	–1168
26	GND	–1018	–1168
—	Dummy	–898	–1168
27	V_{CC}	–777	–1168
28	V_{CC}	–656	–1168
29	V_{CC}	–536	–1168
30	OSC2	–391	–1192
31	OSC1	–183	–1192
32	EXM	21	–1192
33	SFT	225	–1192
34	IM1	429	–1192
35	IM0	633	–1192
36	OPOFF	837	–1192
37	TEST	1041	–1192
38	RESET*	1245	–1192
39	RS/CS*	1449	–1192
40	E/SCL	1653	–1192
41	RW/SDA	1861	–1192
42	DB0/ID0	2073	–1192
43	DB1/ID1	2290	–1192
44	DB2/ID2	2507	–1192
45	DB3/ID3	2723	–1192
46	DB4/ID4	2940	–1192
47	DB5/ID5	3157	–1192
48	DB6	3374	–1192
49	DB7	3590	–1192
50	GND	3809	–1201
51	GND	3930	–1201
52	GND	4079	–1201
53	GND	4200	–1201
54	GND	4349	–1201
55	GND	4474	–1201
56	V_{CC}	4627	–1201
57	V_{CC}	4752	–1201
58	AGND	4905	–1201
59	AGND	5029	–1201
—	Dummy	5191	–1201
60	COM16	5191	–1020
61	COM15	5191	–896
62	COM14	5191	–772
63	COM13	5191	–647
64	COM12	5191	–523
65	COM11	5191	–398
66	COM10	5191	–274
67	COM9	5191	–149
68	COM8	5191	–25
69	COM7	5191	100
70	COM6	5191	224
71	COM5	5191	348
72	COM4	5191	473
73	COM3	5191	597
74	COM2	5191	722
75	COM1	5191	846
76	COMS2	5191	971
—	Dummy	5191	1191
—	Dummy	4939	1191
—	Dummy	4815	1191
—	Dummy	4690	1191
—	Dummy	4566	1191
77	ACOM	4442	1191
78	ASEG1	4317	1191
79	ASEG2	4193	1191
80	ASEG3	4068	1191
81	ASEG4	3944	1191
82	ASEG5	3819	1191
83	ASEG6	3695	1191
84	ASEG7	3571	1191
85	ASEG8	3446	1191
86	ASEG9	3322	1191
87	ASEG10	3197	1191
88	SEG1	2948	1196
89	SEG2	2824	1196
90	SEG3	2699	1196
91	SEG4	2575	1196
92	SEG5	2451	1196
93	SEG6	2326	1196
94	SEG7	2202	1196
95	SEG8	2077	1196
96	SEG9	1953	1196
97	SEG10	1828	1196
98	SEG11	1704	1196
99	SEG12	1579	1196
100	SEG13	1455	1196
101	SEG14	1331	1196
102	SEG15	1206	1196
103	SEG16	1082	1196
104	SEG17	957	1196
105	SEG18	833	1196
106	SEG19	708	1196
107	SEG20	584	1196
108	SEG21	460	1196
109	SEG22	335	1196
110	SEG23	211	1196
111	SEG24	86	1196
112	SEG25	–38	1196
113	SEG26	–163	1196
114	SEG27	–287	1196
115	SEG28	–412	1196
116	SEG29	–536	1196
117	SEG30	–660	1196
118	SEG31	–785	1196
119	SEG32	–909	1196
120	SEG33	–1034	1196
121	SEG34	–1158	1196
122	SEG35	–1283	1196
123	SEG36	–1407	1196
124	SEG37	–1532	1196
125	SEG38	–1656	1196
126	SEG39	–1780	1196
127	SEG40	–1905	1196
128	SEG41	–2029	1196
129	SEG42	–2154	1196
130	SEG43	–2278	1196
131	SEG44	–2403	1196
132	SEG45	–2527	1196
133	SEG46	–2651	1196
134	SEG47	–2776	1196
135	SEG48	–2900	1196
136	SEG49	–3025	1196
137	SEG50	–3149	1196
138	SEG51	–3274	1196
139	SEG52	–3398	1196
140	SEG53	–3523	1196
141	SEG54	–3647	1196
142	SEG55	–3771	1196
143	SEG56	–3896	1196
144	SEG57	–4020	1196
145	SEG58	–4145	1196
146	SEG59	–4269	1196
147	SEG60	–4394	1196
—	Dummy	–4518	1196
—	Dummy	–4643	1196
—	Dummy	–4767	1196
—	Dummy	–4891	1196
—	Dummy	–5191	1196
148	COM17	–5191	970
149	COM18	–5191	845
150	COM19	–5191	721
151	COM20	–5191	596
152	COM21	–5191	472
153	COM22	–5191	348
154	COM23	–5191	223
155	COM24	–5191	99
156	COM25	–5191	–26
157	COM26	–5191	–150
158	COM27	–5191	–275
159	COM28	–5191	–399
160	COM29	–5191	–524
161	COM30	–5191	–648
162	COM31	–5191	–772
163	COM32	–5191	–897
164	COMS1	–5191	–1021

Die Specification

Chip size : $10.88 \times 2.89 mm^2$

Coordinate : Pad center

Origin : Chip center

Bump size : $70 \times 70\ \mu m^2$

Pad size : $90 \times 90\ \mu m^2$

Target Information

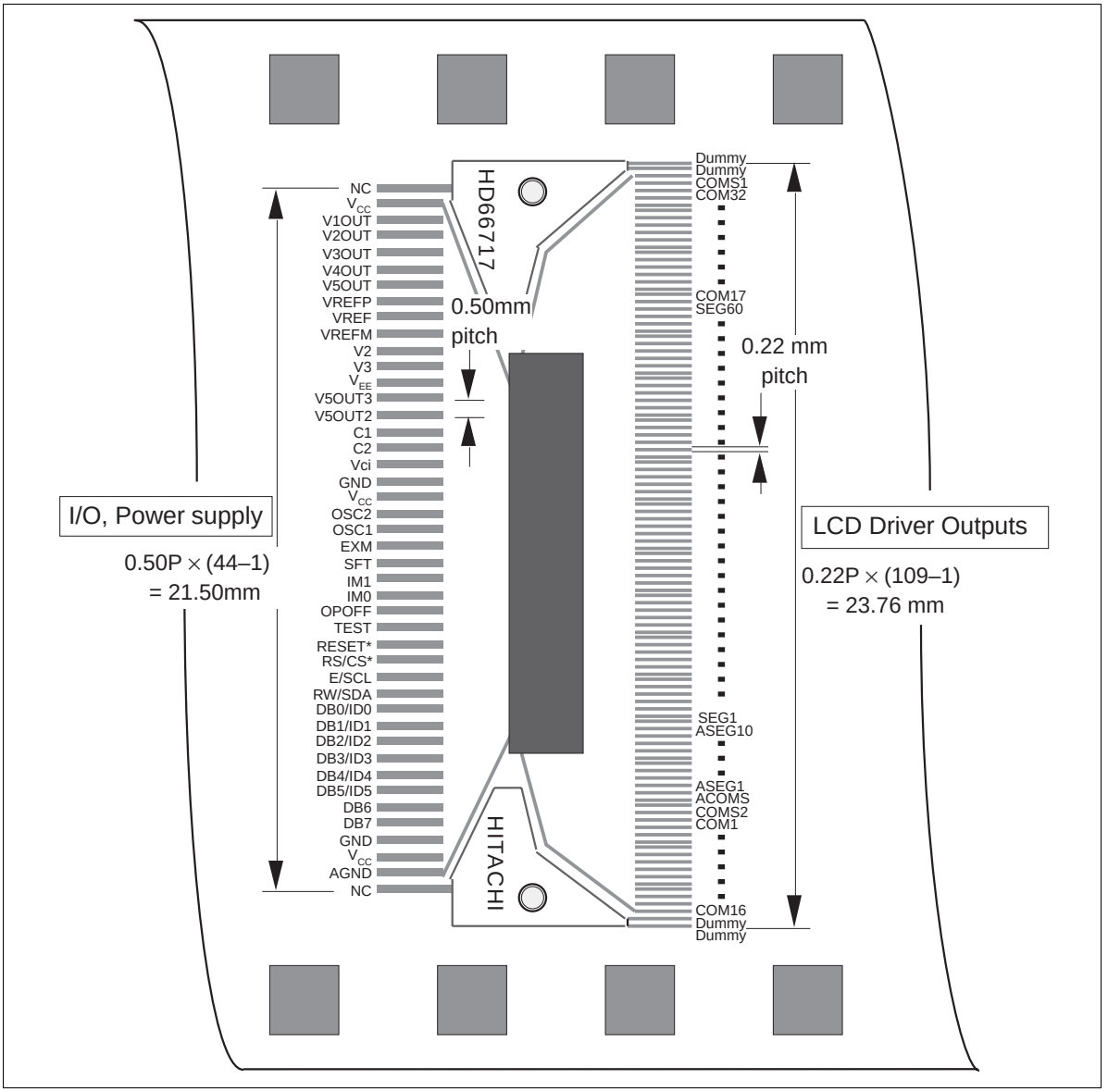
Target shape : Cross ("+")

Target center coordinate :
X = –5110, Y = –1206
X = +5115, Y = –1206
X = –5110, Y = +1206
X = +5115, Y = 1206

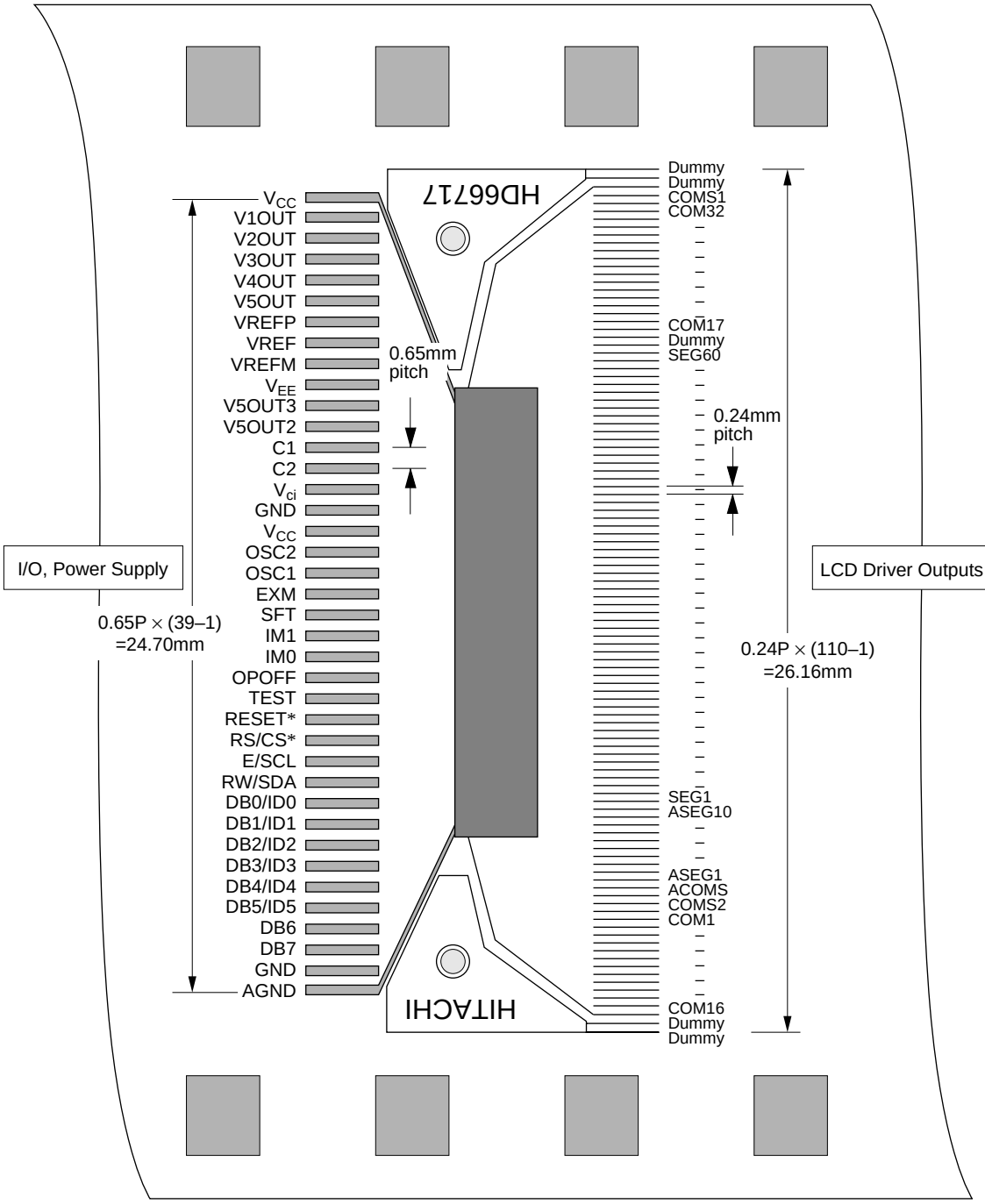
Target AL length : 26 μm

Target AL width : 8 μm

TCP Dimensions (TA0)



TCP Dimensions (TA1, TA2)



Note : TA1: V2 and V3 pins are short-circuited (1/4 bias driving)
TA2: V2 and V3 pins are open (1/6 bias driving)

Pin Functions

Table 1 Pin Functional Description

Signal	Number of Pins	I/O	Device Interfaced with	Function
IM1, IM0	2	I	V_{CC} or GND	Selects interface mode with the MPU: IM1, IM0 = GND, GND: I^2C bus mode (receive) IM1, IM0 = GND, V_{CC}: Clock-synchronized serial mode (receive) IM1, IM0 = V_{CC}, GND: 8-bit bus mode IM1, IM0 = V_{CC}, V_{CC}: 4-bit bus mode
RS/CS*	1	I	MPU	Selects the HD66717 during clock-synchronized serial mode: Low: HD66717 is selected and can be accessed High: HD66717 is not selected and cannot be accessed Selects the registers during 4- or 8-bit bus mode: Low: Instruction register (write); busy flag and address counter (read) High: Data registers (write/read) Must be grounded when I^2C bus mode
RW/SDA	1	I/O, I	MPU	Inputs serial (receive) data and outputs the acknowledge bit during I^2C bus mode; Inputs serial (receive) data during clock-synchronous serial mode; selects read/write during 4- or 8-bit bus mode: Low: Write High: Read
E/SCL	1	I	MPU	Inputs serial clock pulses during I^2C bus mode and clock-synchronized serial mode; enables data read/write during 4- or 8-bit bus mode
DB7, DB6, DB5/ID5 DB4/ID4	4	I, I/O	MPU	Inputs the HD66717's identification code (ID5, ID4) during I^2C bus mode and clock-synchronized serial mode;must be fixed to high or low (DB7 and DB6…). Four high-order bidirectional data bus pins for tristate data transfer during 8-bit bus mode. Bidirectional data bus pins during 4-bit bus mode.
DB3/ID3, DB2/ID2, DB1/ID1, DB0/ID0,	4	I, I/O	MPU	Inputs the HD66717's identification code (ID3 to ID0) during I^2C bus mode and clock-synchronized serial mode; must be fixed to high or low. Four low-order bidirectional data bus pins for tristate data transfer during 8-bit bus mode. Must be left disconnected during 4-bit bus mode since they are not used.
COMS1, COMS2	2	O	LCD	Common output signals for segment icon display.

Table 1 Pin Functional Description (cont)

Signal	Number of Pins	I/O	Device Interfaced with	Function
COM1 to COM32	32	O	LCD	Common output signals for character display: COM1 to COM8 for the first line, COM9 to COM16 for the second line, COM17 to COM24 for the third line, and COM25 to COM32 for the fourth line. All the unused pins output deselection waveforms. During sleep mode (SLP= 1) or standby mode (STB = 1), all pins output V_{CC} level.
SEG1 to SEG60	60	O	LCD	Segment output signals for segment icon display and character display. During sleep mode (SLP = 1) or standby mode (STB = 1), all pins output V_{CC} level.
ACOM	1	O	LCD	Common output signal for annunciator display; can drive display statically between V_{CC} and AGND levels; outputs V_{CC} level while annunciator display is turned off (DA = 0).
ASEG1 to ASEG10	10	O	LCD	Segment output signals for annunciator display; can drive display statically between V_{CC} and AGND levels; output V_{CC} level while annunciator display is turned off (DA = 0).
V2/V3	2	I	Open or Short-circuited	V2/V3 are voltage levels for the internal operational amplifiers; can drive LCD with 1/4 bias when V2 and V3 are short-circuited and with 1/6 bias when they are left disconnected.
V1OUT to V5OUT	5	I or O	—	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); when amplifiers' driving capability is insufficient, attach a capacitor to stabilize the output. Especially these capacitors for V1OUT and V4OUT must be attached in 1/26 duty and 1/34 duty. When the amplifiers are not used (OPOFF = V_{CC}); V1 to V5 voltages can be supplied to these pins externally.
VREFP, VREF, VREFM	3	I	Open or Short-circuited	Adjusts the driving capability of the internal operational amplifiers according to the LCD power supply voltage.
				LCD Power Supply Voltage (V_{CC}–V_{EE}) / **Pin Settings VREF, VREFP, and VREFM**
				V_{CC}–V_{EE}: 3V–5V / Only VREF and VREFP shorted
				V_{CC}–V_{EE}: 4V–6V / All pins open
				V_{CC}–V_{EE}: 5V–8V / All pins shorted
				V_{CC}–V_{EE}: 7V or more / Only VREF and VREFM shorted
V_{EE}	2	—	Power supply	GND power supply for LCD drive V_{CC}–V_{EE} = 13V max.
V_{CC}/GND	10	—	Power supply	V_{CC}: +2.4V to +5.5V, GND (logic): 0V
AGND	2	—	Power supply	Low level power supply for annunciator display; can adjust contrast of annunciators; AGND ≥ GND.
OSC1/ OSC2	2	—	Oscillation resistor/clock	For R-C oscillation, connect an external resistor For external clock supply, input clock pulses to OSC1.

Table 1 Pin Functional Description (cont)

Signal	Number of Pins	I/O	Device Interfaced with	Function
Vci	2	I	Power supply	Inputs a reference voltage and supplies power to the booster; generates the liquid crystal display drive voltage from the operating voltage.
V5OUT2	1	O	V_{EE} pin/ Booster capacitance	Voltage input to the Vci pin is boosted twice and output. When the voltage is boosted three times, the same capacitance as that of C1–C2 should be connected here.
V5OUT3	1	O	V_{EE} pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	2	—	Booster capacitance	External capacitance should be connected here when using the booster.
RESET*	1	I	—	Reset pin. Initializes the LSI when low.
EXM	1	I	MPU	External alternating signal used for annunciator display during standby mode. If annunciator display is not used, EXM must be fixed to V_{CC} or GND.
SFT	1	I	V_{CC} or GND	Selects the SEG output pin arrangement: when SFT = GND, SEG1 is connected to the far left of the LCD panel and when SFT = V_{CC}, SEG60 is connected to the far left of the LCD panel
OPOFF	1	I	V_{CC} or GND	Turns the internal operational amplifier off when OPOFF = V_{CC}, and turns it on when OPOFF = GND. If the amplifier is turned off (OPOFF = V_{CC}), V1 to V5 must be supplied to the V1OUT to V5OUT pins.
TEST	1	I	GND	Test pin. Must be grounded.

Block Function Description

System Interface

The HD66717 has four types of system interfaces: I^2C bus, clock-synchronized serial, 4-bit bus, and 8-bit bus. The interface mode is selected by the IM1 and IM0 pins.

The HD66717 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear, return home, and display control, and address information for the display data RAM (DDRAM), the character generator RAM (CGRAM), and the segment RAM (SEGRAM). The IR can only be written to by MPU and cannot be read from.

The DR temporarily stores data to be written into DDRAM, CGRAM, SEGRAM, or annunciator. Data written into the DR from the MPU is automatically written into DDRAM, CGRAM, SEGRAM, or annunciator by an internal operation. The DR is also used for data storage when reading data from DDRAM, CGRAM, or SEGRAM. When address information is written into the IR, data is read and then stored into the DR from DDRAM, CGRAM, or SEGRAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DDRAM, CGRAM, or SEGRAM at the next address is sent to the DR for the next read from the MPU.

These two registers can be selected by the register select (RS) signal in the 4/8-bit bus interface, and by the RS bit in I^2C bus or clock-synchronized serial interface (Table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66717 is in the internal operation mode, and the next instruction will not be accepted. When RS = low and R/W = high in 4/8-bit bus mode (Table 2), the busy flag is output from DB7. The next instruction must be written after ensuring that the busy flag is 0. The busy flag cannot be read in I^2C bus mode or clock-synchronized serial mode; data must be transferred in appropriate timing considering instruction execution times.

Address Counter (AC)

The address counter (AC) assigns addresses to DDRAM, CGRAM, or SEGRAM. When the address set instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DDRAM, CGRAM, and SEGRAM is also determined concurrently by the instruction.

After writing into (reading from) DDRAM, CGRAM, or SEGRAM, the AC is automatically incremented by 1 (or decremented by 1). The AC contents are then output to DB0 to DB6 when RS = low and R/W = high in 4/8-bit bus mode (Table 2).

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) read and address counter (DB0 to DB6) (4/8-bit bus interface)
1	0	DR write as an internal operation (DR to DDRAM, CGRAM, SEGRAM, or annunciator)
1	1	DR read as an internal operation (DDRAM, CGRAM, or SEGRAM to DR) (4/8-bit bus interface)

Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its capacity is 60 × 8 bits, or 60 characters, which is equivalent to an area of 12 characters × 5 lines. Any number of display lines (LCD drive duty ratio) from 1 to 4 can be selected by software. Here, assignment of DDRAM addresses is the same for all display modes (Table 3). The line to be displayed at the top of the display (display-start line) can also be selected by register settings. See Table 4.

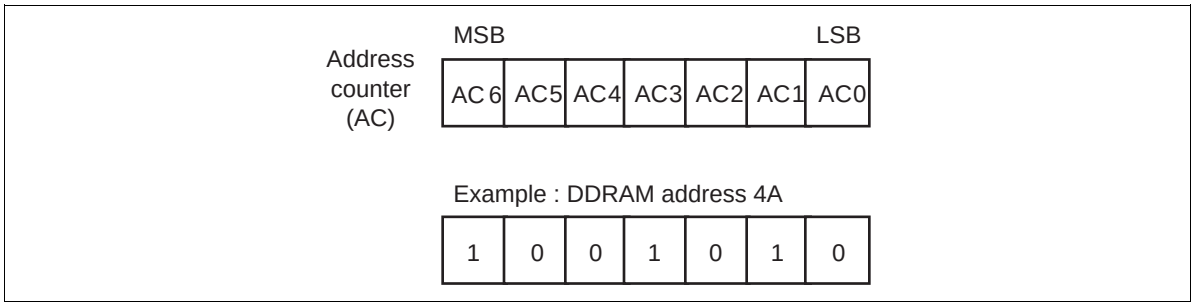


Figure 1 Address Counter and DDRAM Address

Table 3 DDRAM Addresses and Display Positions

Display Line	1st Char.	2nd Char.	3rd Char.	4th Char.	5th Char.	6th Char.	7th Char.	8th Char.	9th Char.	10th Char.	11th Char.	12th Char.
1st	00	01	02	03	04	05	06	07	08	09	0A	0B
2nd	10	11	12	13	14	15	16	17	18	19	1A	1B
3rd	20	21	22	23	24	25	26	27	28	29	2A	2B
4th	30	31	32	33	34	35	36	37	38	39	3A	3B
5th	40	41	42	43	44	45	46	47	48	49	4A	4B

Note: Char. indicates character position.

Table 4 Display-Line Modes, Display-Start Line, and DDRAM Addresses

Display-Line Mode	Duty Ratio	Common Pins	Display-Start Lines: 1st Line (SN = 000)	2nd Line (SN = 001)	3rd Line (SN = 010)	4th Line (SN = 011)	5th Line (SN = 100)
1-line (NL = 00)	1/10	COM1–COM8	00H–0BH	10H–1BH	20H–2BH	30H–3BH	40H–4BH
2-line (NL = 01)	1/18	COM1–COM8	00H–0BH	10H–1BH	20H–2BH	30H–3BH	40H–4BH
		COM9–COM16	10H–1BH	20H–2BH	30H–3BH	40H–4BH	00H–0BH
3-line (NL = 10)	1/26	COM1–COM8	00H–0BH	10H–1BH	20H–2BH	30H–3BH	40H–4BH
		COM9–COM16	10H–1BH	20H–2BH	30H–3BH	40H–4BH	00H–0BH
		COM17–COM24	20H–2BH	30H–3BH	40H–4BH	00H–0BH	10H–1BH
4-line (NL = 11)	1/34	COM1–COM8	00H–0BH	10H–1BH	20H–2BH	30H–3BH	40H–4BH
		COM9–COM16	10H–1BH	20H–2BH	30H–3BH	40H–4BH	00H–0BH
		COM17–COM24	20H–2BH	30H–3BH	40H–4BH	00H–0BH	10H–1BH
		COM25–COM32	30H–3BH	40H–4BH	00H–0BH	10H–1BH	20H–2BH

Character Generator ROM (CGROM)

The character generator ROM generates 5×8-dot character patterns from 8-bit character codes (Table 5). It can generate 240 5×8-dot character patterns. User-defined character patterns are also available using a mask-programmed ROM (see the Modifying Character Patterns section.)

Character Generator RAM (CGRAM)

The character generator RAM of 32×5 bits allows the user to redefine the character patterns for user fonts. In the case of 5×8-dot characters, up to four fonts may be redefined.

Write the character codes at addresses 00H to 03H into DDRAM to display the character patterns stored in CGRAM.

Segment RAM (SEGRAM)

The segment RAM is used to enable control of segments such as an icon and a mark by the user program. Segments and characters are driven by a multiplexing drive method.

SEGRAM has a capacity of 8×5 bits, for controlling the display of a maximum of 40 icons and marks. While COMS1 and COMS2 outputs are being selected, SEGRAM is read and segments (icons and marks) are displayed by a multiplexing drive method (20 segments each during COMS1 and COMS2 selection).

Bits in SEGRAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DDRAM and CGRAM.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM, CGRAM, and SEGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Cursor/Blink Control Circuit

The cursor/blink (or white-black inversion) control is used to produce a cursor or a flashing area on the display at a position corresponding to the location stored in the address counter (AC).

For example (Figure 2), when the address counter is 08H, a cursor is displayed at a position corresponding to DDRAM address (08)H.

Multiplexing Liquid Crystal Display Driver Circuit

The multiplexing liquid crystal display driver circuit consists of 34 common signal drivers (COM1 to COM32, COMS1, COMS2) and 60 segment signal drivers (SEG1 to SEG60). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output deselection waveforms.

Character pattern data is sent serially through a 60-bit shift register and latched when all needed data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs.

The shift direction of 60-bit data can be selected by the SFT pin; select the direction appropriate to the device mounting configuration.

When multiplexing drive is not used, or during standby or sleep mode, all common and segment signal drivers output the V_{CC} level, halting display.

Annunciator Driver Circuit

The static annunciator drivers, which are specially used for displaying icons and marks, consists of 1 common signal driver (ACOM) and 10 segment signal drivers (ASEG1 to ASEG10). Since this driver circuit operates at the logic operating voltage (V_{CC}–AGND), the LCD drive power supply circuit is not necessary, and low-power consumption can be achieved. It is suitable for mark indication during system standby because of its drive capability during standby and sleep modes. When multiplexing drive is not used, or during standby or sleep mode, all common and segment signal drivers output the V_{CC} level, halting display.

Booster

The booster doubles or triples a voltage input to the Vci pin. With this function, both the internal logic units and LCD drivers can be controlled with a single power supply.

Oscillator

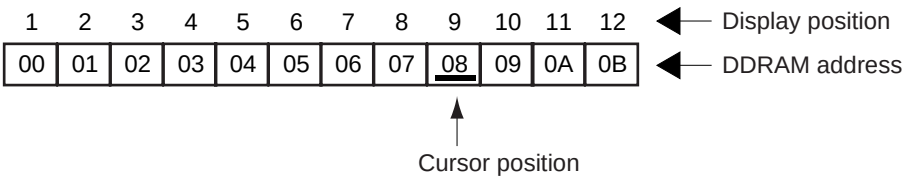
The HD66717 can provide R-C oscillation simply by adding an external oscillation resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation is halted during standby mode, current consumption can be reduced.

V-Pin Voltage-Followers

A voltage-follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. The voltage-followers can be turned off while multiplexing drive is not being used.

Contrast-Adjuster

The contrast-adjuster can adjust LCD contrast by varying LCD drive voltage by software. This function is suitable for selecting appropriate brightness of the LCD or for temperature compensation.



Note: The cursor/blink or white-black inversion control is also active when the address counter indicates the CGRAM or SEGRAM. However, it has no effect on the display.

Figure 2 Cursor Position and DDRAM Address

Table 5 Relation between Character Codes and Character Patterns (ROM code : A02)

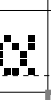
Upper bits / Lower bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	CG RAM (2)															
xxxx0010	CG RAM (3)															
xxxx0011	CG RAM (4)															
xxxx0100	CG RAM (5)															
xxxx0101	CG RAM (6)															
xxxx0110	CG RAM (7)															
xxxx0111	CG RAM (8)															
xxxx1000	CG RAM (1)															
xxxx1001	CG RAM (2)															
xxxx1010	CG RAM (3)															
xxxx1011	CG RAM (4)															
xxxx1100	CG RAM (5)															
xxxx1101	CG RAM (6)															
xxxx1110	CG RAM (7)															
xxxx1111	CG RAM (8)															

Table 6 Relation between Character Codes and Character Patterns (ROM code: A03)

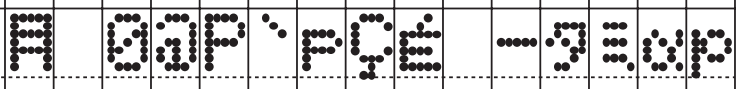
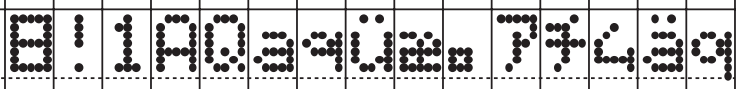
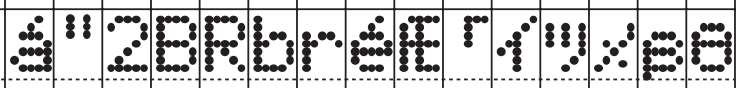
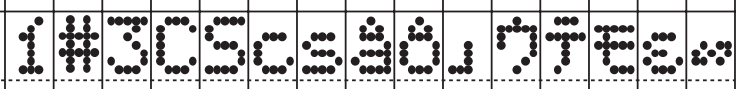
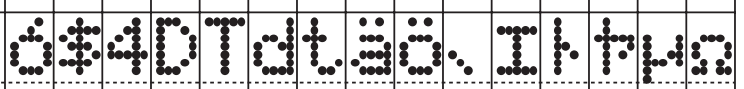
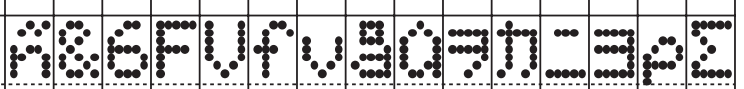
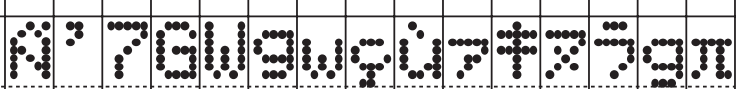
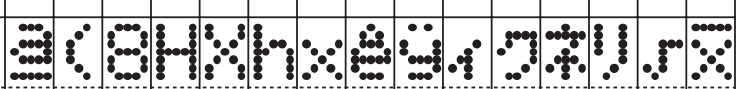
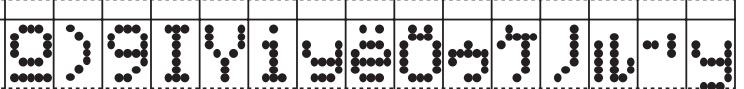
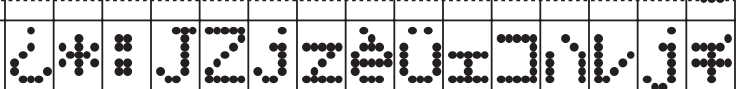
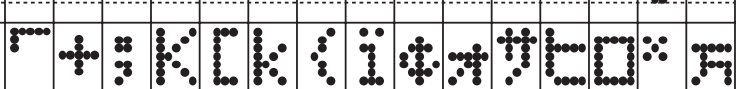
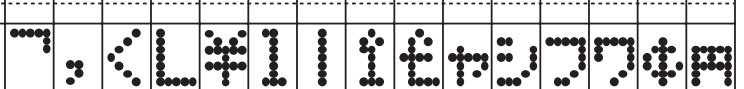
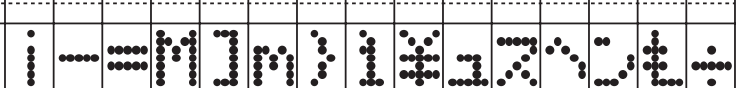
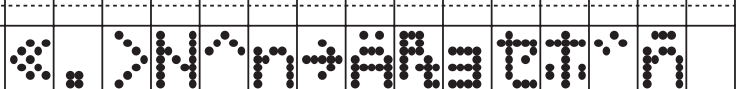
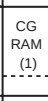
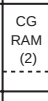
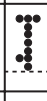
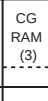
Lower bits \ Upper bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM (1)															
xxxx 0001	CG RAM (2)															
xxxx 0010	CG RAM (3)															
xxxx 0011	CG RAM (4)															
xxxx 0100	CG RAM (1)															
xxxx 0101	CG RAM (2)															
xxxx 0110	CG RAM (3)															
xxxx 0111	CG RAM (4)															
xxxx 1000	CG RAM (1)															
xxxx 1001	CG RAM (2)															
xxxx 1010	CG RAM (3)															
xxxx 1011	CG RAM (4)															
xxxx 1100	CG RAM (1)															
xxxx 1101	CG RAM (2)															
xxxx 1110	CG RAM (3)															
xxxx 1111	CG RAM (4)															

Table 7 Relation between Character Codes and Character Patterns (ROM code: A13)

Upper bits / Lower bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM (1)															
xxxx 0001	CG RAM (2)															
xxxx 0010	CG RAM (3)															
xxxx 0011	CG RAM (4)															
xxxx 0100	CG RAM (1)															
xxxx 0101	CG RAM (2)															
xxxx 0110	CG RAM (3)															
xxxx 0111	CG RAM (4)															
xxxx 1000	CG RAM (1)															
xxxx 1001	CG RAM (2)															
xxxx 1010	CG RAM (3)															
xxxx 1011	CG RAM (4)															
xxxx 1100	CG RAM (1)															
xxxx 1101	CG RAM (2)															
xxxx 1110	CG RAM (3)															
xxxx 1111	CG RAM (4)															

Note : This A13 font pattern is an upside-down pattern of A03.

Modifying Character Patterns

- Character pattern development procedure

  The following operations correspond to the numbers listed in Figure 3:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into an EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI will proceed at Hitachi.

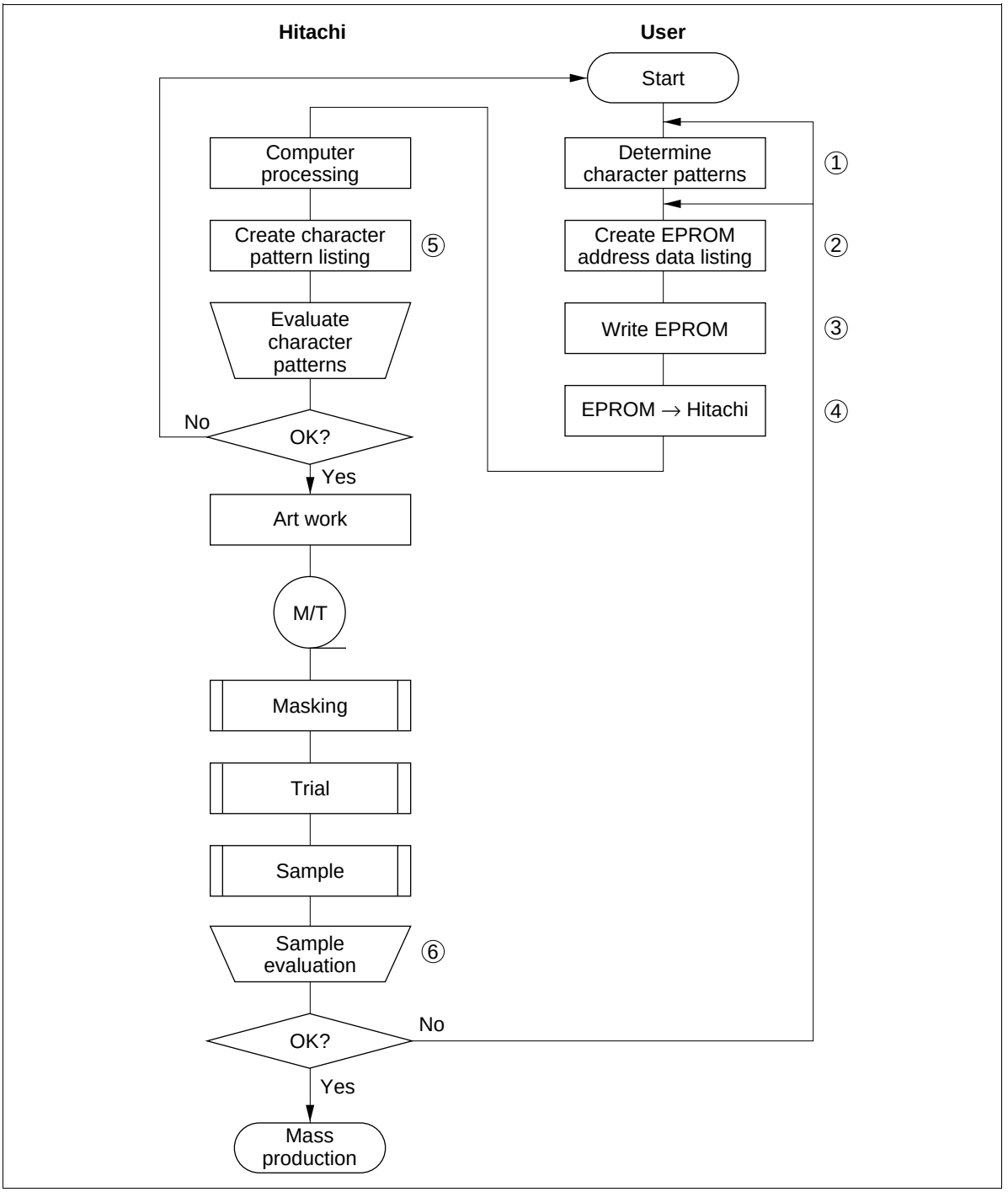


Figure 3 Character Pattern Development Procedure

Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM.

- Programming to EPROM

  The HD66717 character generator ROM can generate 240 5 × 8-dot character patterns. Table 8 shows correspondence between the EPROM address data and the character pattern.

Handling Unused Character Patterns

1. EPROM data outside the character pattern area: This is ignored by the character generator ROM for display operation so any data is acceptable.
2. EPROM data in CGRAM area: Always fill with zeros.
3. Treatment of unused user patterns in the HD66717 EPROM: According to the user application, these are handled in either of two ways:
   a. When unused character patterns are not programmed: If an unused character code is written into DDRAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.
   b. When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DDRAM. (This is equivalent to a space.)

Table 8 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 8 Dots)

EPROM Address												Data					
												MSB					LSB
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	O0	
0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1	
								0	0	0	1	1	0	0	0	1	
								0	0	1	0	1	0	0	0	1	
								0	0	1	1	0	1	0	1	0	
								0	1	0	0	0	0	1	0	0	
								0	1	0	1	0	0	1	0	0	
								0	1	1	0	0	0	1	0	0	
								0	1	1	1	0	0	0	0	0	
Character code								"0"	Line position								

Notes:
1. EPROM addresses A11 to A4 correspond to a character code.
2. EPROM addresses A2 to A0 specify the line position of the character pattern. EPROM address A3 should be set to 0.
3. EPROM data O4 to O0 correspond to character pattern data.
4. Areas which are lit (indicated by shading) are stored as 1, and unlit areas as 0.
5. The eighth raster-row is also stored in the CGROM, and should also be programmed. If the eighth raster-row is used for a cursor, this data should all be set to zero.
6. EPROM data bits O7 to O5 are invalid. 0 should be written in all bits.

Table 9 Example of Relationships between Character Code (DDRAM) and Character Pattern (CGRAM Data)

Character code (DDRAM data)								CGRAM address					MSB			CGRAM data					LSB	
D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	A0	O7	O6	O5	O4	O3	O2	O1	O0		
0	0	0	0	*	*	0	0	0	0	0	0	0	*	*	*	1	0	0	0	1		
										0	0	1	(Don't care)			1	0	0	0	1		
										0	1	0				1	0	0	0	1		
										0	1	1				0	1	0	1	0		Character pattern (1)
										1	0	0				0	0	1	0	0		
										1	0	1				0	0	1	0	0		
										1	1	0				0	0	1	0	0		
										1	1	1				0	0	0	0	0		
=								=		=								=				
0	0	0	0	*	*	1	1	1	1	0	0	0	*	*	*	1	0	0	0	1		
										0	0	1	(Don't care)			1	0	0	0	1		
										0	1	0				1	0	0	0	1		
										0	1	1				0	1	0	1	0		Character pattern (4)
										1	0	0				0	0	1	0	0		
										1	0	1				0	0	1	0	0		
										1	1	0				0	0	1	0	0		
										1	1	1				0	0	0	0	0		

Notes: 1. The lower 2 bits of the character code correspond to the upper two bits of the CGRAM address (2 bits: 4 types).

2. CGRAM address bits 0 to 2 designate the character pattern raster-row position. The 8th raster-row is the cursor position and its display is formed by a logical OR with the cursor.
3. The upper three bits of the CGRAM data are invalid; use the lower five bits.
4. When the upper four bits (bits 7 to 4) of the character code are 0, CGRAM is selected.
   Bits 3 and 2 of the character code are invalid (*). Therefore, for example, the character codes (00)H and (08)H correspond to the same CGRAM address.
5. A set bit in the CGRAM data corresponds to display selection, and 0 to non-selection.
   * Indicates no effect.

Table 10 Correspondence between Segment Display SEGRAM Addresses (ASEG) and Driver Signals

ASEG Address				Segment Signals								Common
MSB			LSB	D7	D6	D5	D4	D3	D2	D1	D0	Signal
1	0	0	0	*	*	*	SEG1, SEG21, SEG41	SEG2, SEG22, SEG42	SEG3, SEG23, SEG43	SEG4, SEG24, SEG44	SEG5, SEG25, SEG45	COMS1
1	0	0	1	*	*	*	SEG6, SEG26, SEG46	SEG7, SEG27, SEG47	SEG8, SEG28, SEG48	SEG9, SEG29, SEG49	SEG10, SEG30, SEG50	COMS1
1	0	1	0	*	*	*	SEG11, SEG31, SEG51	SEG12, SEG32, SEG52	SEG13, SEG33, SEG53	SEG14, SEG34, SEG54	SEG15, SEG35, SEG55	COMS1
1	0	1	1	*	*	*	SEG16, SEG36, SEG56	SEG17, SEG37, SEG57	SEG18, SEG38, SEG58	SEG19, SEG39, SEG59	SEG20, SEG40, SEG60	COMS1
1	1	0	0	*	*	*	SEG1, SEG21, SEG41	SEG2, SEG22, SEG42	SEG3, SEG23, SEG43	SEG4, SEG24, SEG44	SEG5, SEG25, SEG45	COMS2
1	1	0	1	*	*	*	SEG6, SEG26, SEG46	SEG7, SEG27, SEG47	SEG8, SEG28, SEG48	SEG9, SEG29, SEG49	SEG10, SEG30, SEG50	COMS2
1	1	1	0	*	*	*	SEG11, SEG31, SEG51	SEG12, SEG32, SEG52	SEG13, SEG33, SEG53	SEG14, SEG34, SEG54	SEG15, SEG35, SEG55	COMS2
1	1	1	1	*	*	*	SEG16, SEG36, SEG56	SEG17, SEG37, SEG57	SEG18, SEG38, SEG58	SEG19, SEG39, SEG59	SEG20, SEG40, SEG60	COMS2

Notes: 1. When the SFT pin is grounded, the SEG1 pin output is connected to the far left of the LCD panel, and when the SFT pin is high, the SEG60 pin output is connected to the far left.

2. SEG1 to SEG20 data is identical to SEG21 to SEG40 and SEG41 to SEG60 data.

3. The lower five bits (D4 to D0) of SEGRAM data determine on or off display of each segment. A segment is selected (turned on) when the corresponding data is 1, and is deselected (turned off) when the corresponding data is 0. The upper three bits (D7 to D5) are invalid.

Table 11 Correspondence between Annunciator Display Addresses (AAN) and Driver Signals

AAN Address				Annunciator Segment Signals								Common
MSB			LSB	D7	D6	D5	D4	D3	D2	D1	D0	Signal
0	0	0	0	ASEG1 Blink	ASEG1 Data	ASEG2 Blink	ASEG2 Data	ASEG3 Blink	ASEG3 Data	ASEG4 Blink	ASEG4 Data	ACOM
0	0	0	1	ASEG5 Blink	ASEG5 Data	ASEG6 Blink	ASEG6 Data	ASEG7 Blink	ASEG7 Data	ASEG8 Blink	ASEG8 Data	ACOM
0	0	1	0	ASEG9 Blink	ASEG9 Data	ASEG10 Blink	ASEG10 Data	— *	— *	— *	— *	ACOM

Notes: 1. The annunciator is turned on when the corresponding even bit (data) is 1, and is turned off when 0.

2. The turned-on annunciator blinks when the corresponding odd bit (blink) is 1. Blinking is provided by repeatedly turning on the annunciator for 32 frames and then turning it off for the next 32 frames.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66717 can be controlled by the MPU. Before starting internal operation of the HD66717, control information is temporarily stored in these registers to allow interfacing with various peripheral control devices or MPUs which operate at different speeds. The internal operation of the HD66717 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write (R/W), and the data bus (DB0 to DB7), make up the HD66717 instructions (Table 18). There are four categories of instructions that:

- Control display
- Control power management
- Set internal RAM addresses
- Perform data transfer with internal RAM

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66717 RAM addresses after each data write can lighten the program load of the MPU.

While an instruction is being executed for internal operation, or during reset, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU. If an instruction is sent without checking the busy flag, the time between the first instruction issue and next instruction issue must be longer than the instruction execution time itself. Refer to Table 16 for the list of each instruction execution cycles (clock pulses). The execution time depends on the operating clock frequency (oscillation frequency).

Instruction Description

Status Read

The status read instruction (Figure 4) reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CGRAM, DDRAM, and SEGRAM addresses, and its value is determined by the previous instruction.

Clear Display

The clear display instruction (Figure 5) writes space code (20)H (character pattern for character code (20)H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter. It also sets I/D to 1 (increment mode) in entry mode.

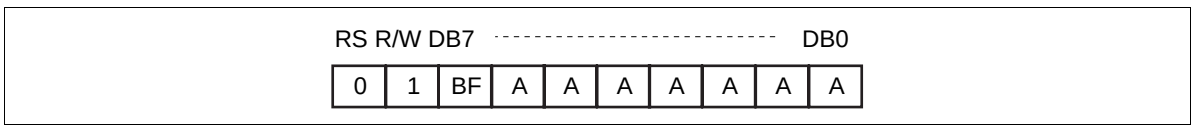


Figure 4 Status Read Instruction

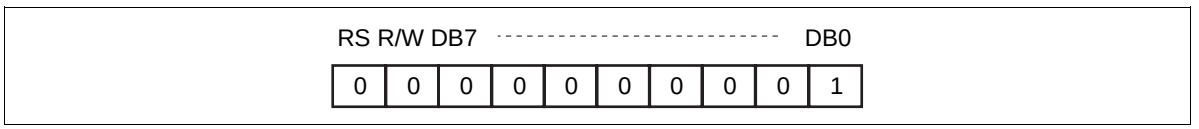


Figure 5 Clear Display Instruction

Return Home

The return home instruction (Figure 6) sets DDRAM address 0 into the address counter. The DDRAM contents do not change.The cursor or blinking goes to the top left of the display.

Start Oscillator

The start oscillator instruction (Figure 7) re-starts the oscillator from a halt state in standby mode. After issuing this instruction, wait at least 10 ms for oscillation to become stable before issuing the next instruction. (Refer to the Standby Mode section.)

Entry Mode

The entry mode instruction (Figure 8) includes the I/D and OSC bits.

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from DDRAM.The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CGRAM and SEGRAM.

OSC: Divides the external clock frequency by four (OSC = 1) using the resulting clock as an internal operating clock. The execution time for this instruction and subsequent ones is therefore quadrupled. The execution time of clearing this bit (OSC = 0) is also quadrupled. (For application of this instruction, refer to the Partial-Display-Off Function section.)

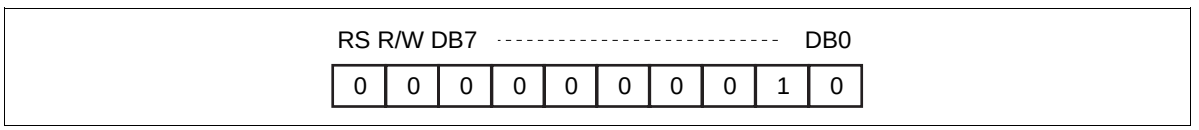


Figure 6 Return Home Instruction

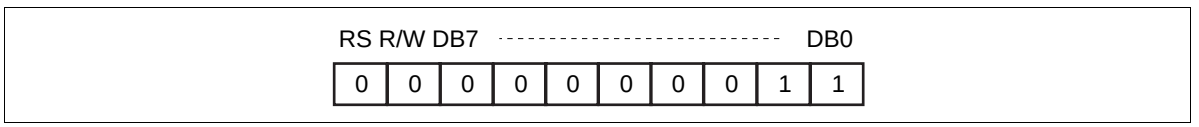


Figure 7 Start Oscillator Instruction

Cursor Control

The cursor control (Figure 9) includes the B/W, C, and B bits.

B/W: When B/W is 1, the character at the cursor position is cyclically (every 32 frames) displayed with black-white inversion.

C: The cursor is displayed on the 8th raster-row when C is 1. The cursor is displayed using 5 dots in the 8th raster-row for 5 × 8-dot character font.

B: The character indicated by the cursor blinks when B is 1. The blinking is displayed as switching between all black dots and displayed characters every 32 frames. The cursor and blinking can be set to display simultaneously. When LC and B = 1, the blinking is displayed as switching between all white dots and displayed characters.

Figure 10 shows cursor control examples.

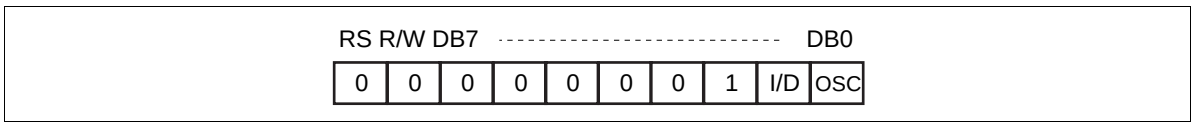


Figure 8 Entry Mode Instruction

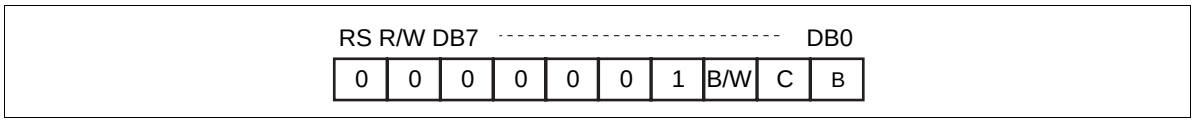


Figure 9 Cursor Control Instruction

Display On/Off Control

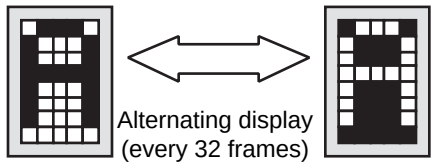
The display on/off control instruction (Figure 11) includes DC, DS, and LC bits.

DC: The character display is on when DC is 1 and off when DC is 0. When off, the display data remains in DDRAM, and can be displayed instantly by setting DC to 1.

DS: When DS = 1, segment display for icons and marks that is controlled by the multiplexing drive method is turned on and when DS = 0, it is turned off.

When both DC and DS = 0, multiplexing drive is halted, setting the outputs from SEG1 to SEG60, COM1 to COM32, and COMS1 and COMS2 to V_{CC} level to turn off the display. This can suppress current for LCD charging or discharging due to LCD driving operations.

LC: When LC = 1, a cursor attribute is assigned to the line that contains the address counter (AC) value. Cursor mode can be selected with the B/W, C, and B bits. Refer to the Line-Cursor Display section.



i) White-black inverting display example

ii) 8th raster-row cursor display

ii) Blink display example

Figure 10 Cursor Control Examples

RS	R/W	DB7						DB0
0	0	0	0	0	1	0	DC	DS	LC

Figure 11 Display On/Off Instruction

Power Control

The cursor control instruction (Figure 12) includes the AMP, SLP, and STB bits.

AMP: When AMP = 1, each voltage-follower for V1 to V5 pins and the booster are turned on. When AMP = 0, current consumption can be reduced while character or segment display controlled by the multiplexing drive method is not being used.

SLP: When SLP = 1, the HD66717 enters sleep mode, where all the internal operations are halted except for annunciator display function and the R-C oscillator, thus reducing current consumption. Refer to the Sleep Mode section. Only the following instructions can be executed during sleep mode.

a. Annunciator address set (AAN)
b. Annunciator data write
c. Annunciator display on or off (DA = 1 or 0)
d. Voltage-follower on or off (AMP = 1 or 0)
e. Standby mode set (STB = 1)
f. Sleep mode cancel (SLP = 0)

During sleep mode, other RAM data and instructions cannot be updated but they are retained.

STB: When STB = 1, the HD66717 enters standby mode, where the device completely stops, halting all the internal operations including the internal R-C oscillator and no external clock pulses are supplied. However, annunciator display alone is available when the alternating signal for annunciator-driving signals is supplied to the EXM pin. When the annunciator display is not needed, make sure to turn off display (DA = 0). Refer to the Standby Mode section. Only the following instructions can be executed during standby mode.

a. Annunciator address set (AAN)
b. Annunciator data write
c. Annunciator display on or off (DA = 1 or 0)
d. Voltage-follower on or off (AMP = 1 or 0)
e. Start oscillator
f. Standby mode cancel (STB = 0)

During standby mode, RAM data and other instructions may be lost; they must be set again after standby mode is cancelled.

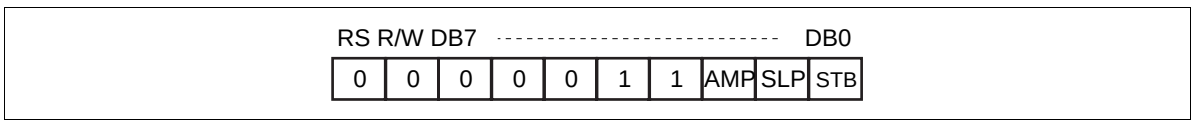


Figure 12 Power Control Instruction

Display Control

The display control instruction (Figure 13) includes the NL and DL bits.

NL1, NL0: Designates the number of display lines. This value determines the LCD drive multiplexing duty ratio (Table 12). The address assignment is the same for all display line modes.

DL3–DL1: Doubles the height of characters on a specified line. The first, second, or third line is doubled in height when DL1, DL2, or DL3 = 1, respectively. Two lines can be simultaneously doubled in a 4-line display. Refer to the Double-Height Display section.

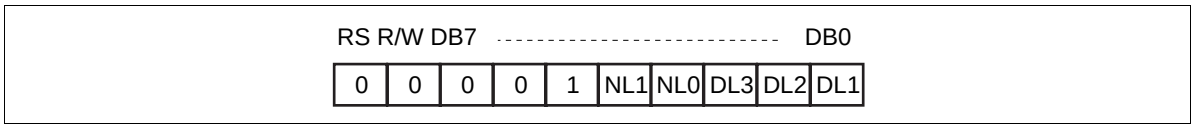


Figure 13 Display Control Instruction

Table 12 NL Bits and Display Lines

NL1	NL0	Number of Display Lines	LCD Drive Multiplexing Duty Ratio
0	0	1	1/10
0	1	2	1/18
1	0	3	1/26
1	1	4	1/34

Contrast Control

The contrast control instruction (Figure 14) includes the SN and CT bits.

SN2: Combined with the SN1 and SN0 bits described in the Scroll Control section to select the first line to be scrolled (display-start line).

CT3–CT0: Controls the LCD drive voltage (potential difference between V_{CC} and V5) to adjust contrast (Figure 15 and Table 13). Refer to the Contrast Adjuster section.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	SN2	CT3	CT2	CT1	CT0

Figure 14 Contrast Control Instruction

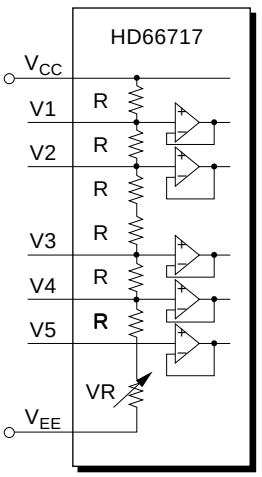


Figure 15 Contrast Adjuster

Scroll Control

The scroll control instruction (Figure 16) includes the SN and SL bits.

SN1, SN0: Combined with the SN2 bit described in the Contrast Control section to select the top line to be displayed (display-start line) through the data output from the COM1 pin (Table 14). After first five lines are displayed from the top line, the cycle is repeated and scrolling continues.

Table 13 CT Bits and Variable Resistor Value of Contrast Adjuster

CT3	CT2	CT1	CT0	Variable Resistor Value (VR)
0	0	0	0	6.4 x R
0	0	0	1	6.0 x R
0	0	1	0	5.6 x R
0	0	1	1	5.2 x R
0	1	0	0	4.8 x R
0	1	0	1	4.4 x R
0	1	1	0	4.0 x R
0	1	1	1	3.6 x R
1	0	0	0	3.2 x R
1	0	0	1	2.8 x R
1	0	1	0	2.4 x R
1	0	1	1	2.0 x R
1	1	0	0	1.6 x R
1	1	0	1	1.2 x R
1	1	1	0	0.8 x R
1	1	1	1	0.4 x R

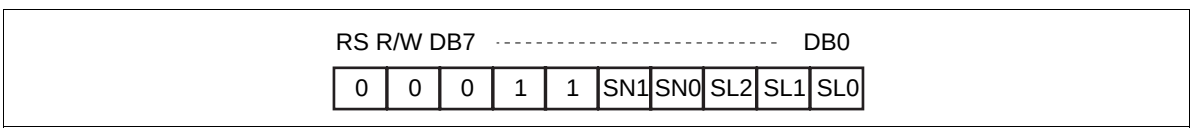


Figure 16 Scroll Control Instruction

SL2–SL0: Selects the top raster-row to be displayed (display-start raster-row) in the display-start line specified by SN2 to SN0. Any raster-row from the first to eighth can be selected (Table 15). This function is used to perform vertical smooth scroll together with SN2 to SN0. Refer to the Vertical Smooth Scroll section.

Table 14 SN Bits and Display-Start Lines

SN2	SN1	SN0	Display-Start Line
0	0	0	1st line
0	0	1	2nd line
0	1	0	3rd line
0	1	1	4th line
1	0/1	0/1	5th line

Table 15 SN Bits and Display-Start Raster-Rows

SL2	SN1	SL0	Display-Start Raster-Row
0	0	0	1st raster-row
0	0	1	2nd raster-row
0	1	0	3rd raster-row
0	1	1	4th raster-row
1	0	0	5th raster-row
1	0	1	6th raster-row
1	1	0	7th raster-row
1	1	1	8th raster-row

Annunciator/SEGRAM Address Set

The annunciator/SEGRAM address set instruction (Figure 17) includes the DA and A bits.

DA: Turns annunciator display on or off. When DA = 1, annunciator display is turned on and driven statically. When DA = 0, annunciator display is turned off with ASEG1 to ASEG10 and ACOM pins held to V_{CC} level.

The internal operating clock supply is halted during standby mode; make sure to turn off display (DA = 0) if the external alternating signal is not supplied. Refer to the Segment Display and Annunciator Display section and the Standby Mode section.

AAAA: Used for setting the SEGRAM address in the address counter (AC) or for setting an annunciator address. The SEGRAM addresses range from 1000H to 1111H (8 addresses), while the annunciator addresses range from 0000H to 0010H (3 addresses).

The annunciator address is directly set without using the address counter, and consequently must be updated for each access. The annunciator address can be set even during sleep and standby modes.

Once the SEGRAM address is set, data in the SEGRAM can be accessed consecutively since the address counter is automatically incremented or decremented by one according to the I/D bit setting after each access. The SEGRAM address cannot be set during sleep or standby mode.

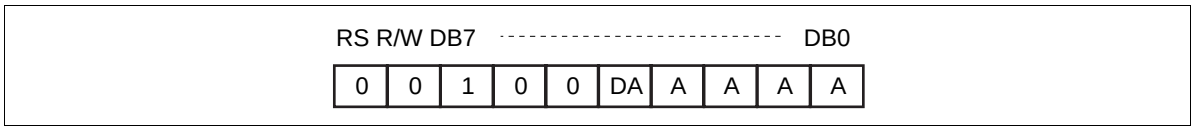


Figure 17 Annunciator/SEGRAM Address Set Instruction

CGRAM Address Set

The CGRAM address set instruction (Figure 18) includes the A bits.

AAAAA: Used for setting the CGRAM address in the address counter (AC). The CGRAM addresses range from 00H to 1FH (32 addresses) (Table 16).

Once the CGRAM address is set, data in the CGRAM can be accessed consecutively since the address counter is automatically incremented or decremented according to the I/D bit setting after each access. The CGRAM address cannot be set during sleep or standby mode.

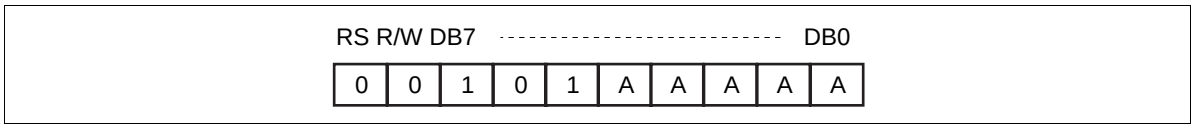


Figure 18 CGRAM Address Set Instruction

Table 16 CGRAM Addresses and Character Codes

Displayed Character	CGRAM Address	Character Codes
1st character	00H to 07H	00H
2nd character	08H to 0FH	01H
3rd character	10H to 17H	02H
4th character	18H to 1FH	03H

DDRAM Address Set

The DDRAM address set instruction (Figure 19) includes the A bits.

AAAAAAA: Used for setting the DDRAM address in the address counter (AC). The DDRAM addresses range from 00H to 4BH (60 addresses) (Table 17).

Once the DDRAM address is set, data in the DDRAM can be accessed consecutively since the address counter is automatically incremented or decremented according to the I/D bit setting after each access. Here, invalid addresses are automatically skipped. The DDRAM address cannot be set during sleep or standby mode.

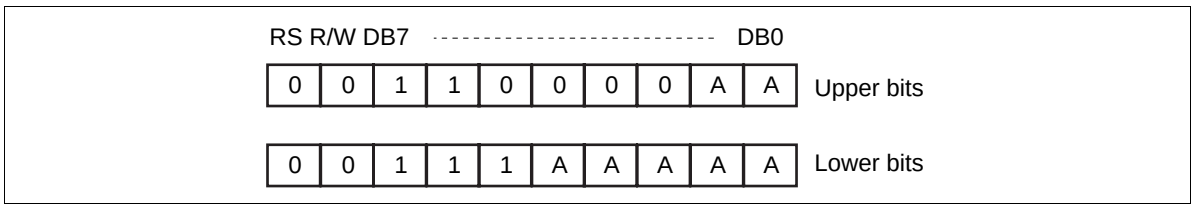


Figure 19 DDRAM Address Set Instruction

Table 17 DDRAM Addresses and Invalid Addresses

Displayed Line	DDRAM Address	Invalid Addresses
1st line	00H to 0BH	0CH to 0FH
2nd line	10H to 1BH	1CH to 1FH
3rd line	20H to 2BH	2CH to 2FH
4th line	30H to 3BH	3CH to 3FH
5th line	40H to 4BH	4CH and subsequent addresses

Write Data to RAM

The write data to RAM instruction (Figure 20) writes 8-bit data to annunciator or DDRAM, or lower 5-bit data to SEGRAM or CGRAM that is selected by the previous specification of the address set instruction (annunciator/SEGRAM address set, CGRAM address set, or DDRAM address set).

After a write, the address is automatically incremented or decremented by 1 according to the I/D bit setting in the entry mode instruction.

The annunciator address is not automatically updated; it must be specifically updated to write data to a different address. During sleep and standby modes, DDRAM, CGRAM, or SEGRAM cannot be accessed.

Read Data from RAM

The read data from RAM instruction (Figure 21), reads 8-bit data from DDRAM, or 5-bit binary data from CGRAM or SEGRAM that is selected by the previous specification of the address set instruction (SEGRAM address set, CGRAM address set, or DDRAM address set). The unused upper three bits of CGRAM or SEGRAM data are read as 000; annunciator data cannot be read. If no address is specified by the address set instruction just before this instruction, the first data read will be invalid. When executing serial read instructions, the next address is normally read from the next address.

After a read, the address is automatically incremented or decremented by 1 according to the I/D bit setting in the entry mode instruction.

Table 18 lists the above instructions.

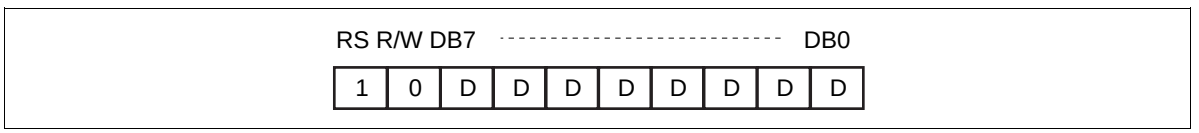


Figure 20 Write Data to RAM Instruction

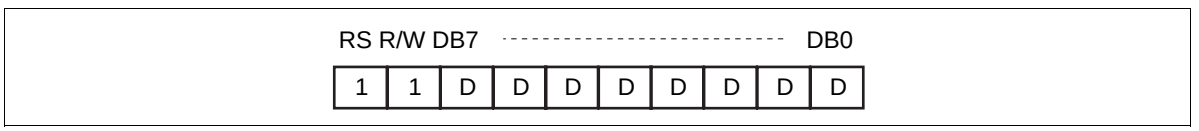


Figure 21 Read Data from RAM Instruction

Table 18 Instruction List

Instruction	No.	Code										Description	Execution Cycle *1
		R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Status	SR	1	0	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF), which indicates internal operations are being performed, and reads address counter (AC).	0
Clear display	CL	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	310
Return home	CH	0	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 in address counter.	10
Start oscillator	OS	0	0	0	0	0	0	0	0	1	1	Starts oscillation during standby mode.	—
Entry mode set	EM	0	0	0	0	0	0	0	1	I/D	OSC	Sets address update direction after RAM access (I/D), and system clock division (OSC).	10
Cursor control	CR	0	0	0	0	0	0	1	B/W	C	B	Sets black-white inverting cursor (B/W), 8th raster-row cursor (C), and blink cursor (B).	10
Display on/off control	DO	0	0	0	0	0	1	0	DC	DS	LC	Sets character display on/off (DC), segment display on/off (DS), and line-cursor on/off (LC).	10
Power control	PW	0	0	0	0	0	1	1	AMP	SLP	STB	Turns on voltage-follower and booster (AMP), and sets sleep mode (SLP) and standby mode (STB).	10
Display control	DC	0	0	0	0	1	NL1	NL0	DL3	DL2	DL1	Sets the number of display lines (NL) and the line to be doubled in height.	10
Contrast control	CN	0	0	0	1	0	SN2	CT3	CT2	CT1	CT0	Sets the display-start line (SN2) and contrast-adjusting value (CT).	10
Scroll control	SC	0	0	0	1	1	SN1	SN0	SL2	SL1	SL0	Sets the display-start line (SN) and display-start raster-row (SL).	10
Annunciator /SEGRAM address set	AS	0	0	1	0	0	DA	AAN/ A_{SEG3}	AAN/ A_{SEG2}	AAN/ A_{SEG1}	AAN/ A_{SEG0}	Turns on annunciator display and sets annunciator/SEGRAM address.	10
CGRAM address set	CA	0	0	1	0	1	A_{CG4}	A_{CG3}	A_{CG2}	A_{CG1}	A_{CG0}	Sets the initial CGRAM address to the address counter.	10
DDRAM address set (upper bits)	DA	0	0	1	1	0	0	0	0	A_{DD6}	A_{DD5}	Sets the initial higher DDRAM address to the address counter.	10
DDRAM address set (lower bits)	DA	0	0	1	1	1	A_{DD4}	A_{DD3}	A_{DD2}	A_{DD1}	A_{DD0}	Sets the initial lower DDRAM address to the address counter.	10

Table 18 Instruction List (cont)

Instruction	No.	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle *1
Write data to RAM	WD	0	1			Write data						Writes data to DDRAM, CGRAM, SEGRAM, or annunciator.	10
Read data from RAM	RD	1	1			Read data						Reads data from DDRAM, CGRAM, or SEGRAM.	10

BF = 1: Internally operating — AC: Address counter
I/D = 1: Increment — I/D = 0: Decrement
OSC = 1: System clock divided by four
B/W = 1: Black-white inverting cursor on — C = 1: 8th raster-row cursor on
B = 1: Blink cursor on
D = 1: Display on
DC = 1: Character display on — DS = 1: Segment display on
LC = 1: Line containing AC given cursor attribute
AMP = 1: Voltage-follower and booster on — SLP = 1: Sleep mode
STB = 1: Standby mode
NL1,NL0: Number of display lines [00: 1line (1/10 duty ratio), 01: 2 lines (1/18 duty ratio), 10: 3 lines (1/26 duty ratio),11:4 lines (1/34 duty ratio)]
DL3 – DL1: Double-height lines (DL1 = 1: 1st line, DL2 = 1: 2nd line, DL3 = 1: 3rd line)
CT3–CT0: Contrast adjustment
SN2 – SN0: Display-start line (000: 1st line, 001: 2nd line, 010: 3rd line, 011: 4th line, 100: 5th line)
SL2 – SL0: Display-start raster-row (000: 1st raster-row... 111: 8th raster-row)
DA = 1: Annunciator display on
AAN/A_{SEG} = 0000–0010: Annunciator address — AAN/A_{SEG} = 1000–1111: SEGRAM address
ACG4–ACG0: CGRAM address (00000–11111)
ADD6–ADD0: DDRAM address (0000000–1001011)

Note: 1. Represented by the number of operating clock pulses; the execution time depends on the supplied clock frequency or the internal oscillation frequency.

Reset Function

Initializing by Internal Reset Circuit

The HD66717 is internally initialized by RESET input. During reset, the system executes the instructions as described below. Here, the busy flag (BF) therefore indicates a busy state (BF = 1), accepting no instruction or RAM data access from the MPU. Here, reset input must be held at least 10 ms.

After releasing power-on reset, clear display instruction is operated, so wait for 1,000 clock-cycles or more.

Make sure to reset the HD66717 immediately after power-on reset in I^2C bus mode.

1. Instruction set initialization
   a. Clear display:
      Writes 20H to DDRAM after releasing reset
   b. Return home
      Sets the address counter (AC) to 00H to select the DDRAM
   c. Start oscillator
   d. Entry mode
      I/D = 1: Increment by 1
      OSC = 0: Clock frequency not divided
   e. Cursor control
      B/W = 0: White-black inverting cursor off
      C = 0: 8th raster-row cursor off
      B = 0: Blink cursor off
   f. Display on/off control
      DC = 0: Character display off
      DS = 0: Segment display off
      LC = 0: Line-cursor off
   g. Power control
      AMP = 0: LCD power supply off
      SLP = 0: Sleep mode off
      STB = 0: Standby mode off
   h. Display control
      NL1, NL0 = 11: 4-line display (1/34 multiplexing duty ratio)
      DL3–DL1 = 000: Double-height display off
   i. Contrast adjust
      CT = 0000: Weak contrast
   j. Scroll control
      SN2–SN0 = 000: First line displayed at the top
      SL2–SL0 = 000: First raster-row displayed at the top of the first line

k. Annunciator control

DA = 0: Annunciator display off

2. RAM data initialization

a. DDRAM

All addresses are initialized to 20H by the clear display instruction

b. CGRAM/SEGRAM

Not automatically initialized by reset input; must be initialized by software while display is off (DC and DS = 0)

c. Annunciator data

Not automatically initialized by reset input; must be initialized by software while display is off (DA= 0)

3. Output pin initialization

a. LCD driver output pins (SEG/COM, ASEG/ACOM): Outputs V_{CC} level

b. Booster output pins (V5OUT2 and V5OUT3): Outputs GND level

c. Oscillator output pin (OSC2): Outputs oscillation signal

Transferring Serial Data

I²C Bus Interface

Grounding the IM1 and IM0 pins (interface mode pins) allows serial data transfer conforming to the I²C bus interface over the serial data line (SDA) and serial transfer clock line (SCL). Here, the HD66717 operates in an exclusive-receive slave mode.

The HD66717 initiates serial data transfer by transferring the first byte when a high SCL level at the falling edge of the SDA input is sampled; it ends serial data transfer when a high SCL level at the rising edge of the SDA input is sampled.

The HD66717 is selected when the higher six bits of the 7-bit slave address in the first byte transferred from the master device match the 6-bit device identification code assigned to the HD66717. The HD66717, when selected, receives the subsequent data strings. Any identification code can be assigned by the DB5/ID5 to DB0/ID0 pins; select an appropriate code that is not assigned to any other slave device. The higher four bits (ID5 to ID2) of this identification code is recommended as 0111. Two different slave addresses must be assigned to a single HD66717 because the least significant bit (LSB) of the slave address is used as a register select bit (RS): when RS = 0, an instruction can be issued and when RS = 1, data can be written to a RAM. The eighth bit of the first byte (R/W bit) must be 0 since the HD66717 exclusively receives data.

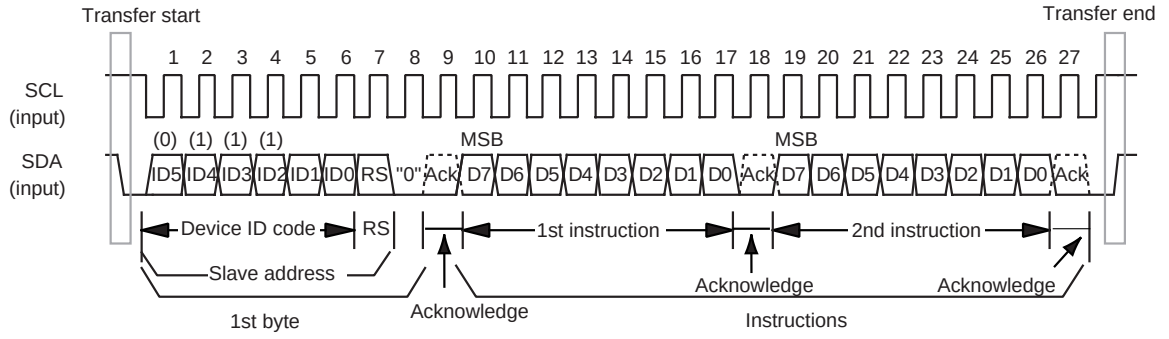
The ninth bit of the first byte is a receive-data acknowledge bit (ACK). When the received slave address matches the device ID code, the HD66717 pulls down the ACK bit to a low level. Therefore, the ACK output buffer is an open-drain structure, only allowing low-level output. However, the ACK bit is undetermined immediately after power-on; make sure to initialize the LSI using the RESET* input.

After identifying the address in the first byte, the HD66717 receives the subsequent data as an HD66717 instruction or as RAM data. Having received 8-bit data normally, the HD66717 pulls down the ninth bit (ACK) to a low level. Therefore, if the ACK is not returned, the data must be transferred again. Multiple bytes of data can be consecutively transferred until the transfer-end condition is satisfied. Here, when the serial data transfer rate is longer than that of the HD66717 instruction execution cycle, effective data transfer is possible without retransmission (see Table 18, Instruction List). Note that the display-clear instruction alone requires longer execution time than the others.

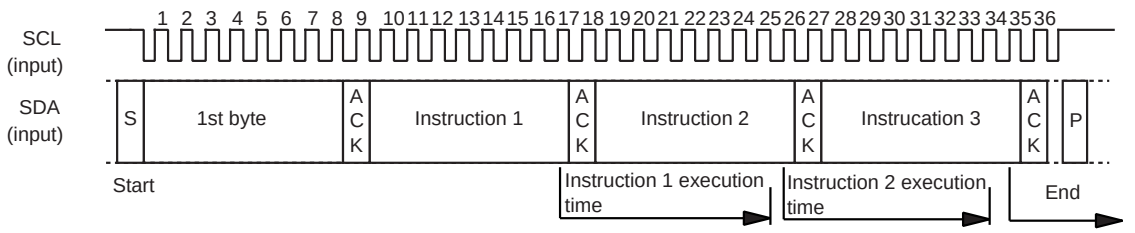
Table 19 illustrates the first bytes of I²C bus interface data and Figure 22 shows the I²C bus interface timing sequence .

Table 19 First Bytes of I²C Bus Interface Data

	Transferred Bit String								
First Byte	**S**	**Bit 1**	**Bit 2**	**Bit 3**	**Bit 4**	**Bit 5**	**Bit 6**	**Bit 7**	**Bit 8**	**Bit 9**
I²C bus system	Transfer start	I²C slave address							R/W	ACK
		A6	A5	A4	A3	A2	A1	A0		
HD66717	Transfer start	Device ID code						RS	0	ACK
		ID5	ID4	ID3	ID2	ID1	ID0			
		0	1	1	1					



a) Basic data transfer (receive) timing



b) Consecutive data transfer timing

Note: Transfer the instruction 2 ACK after instruction 1 has been executed.

Figure 22 I²C Bus Interface Timing Sequence

Clock-Synchronized Serial Interface

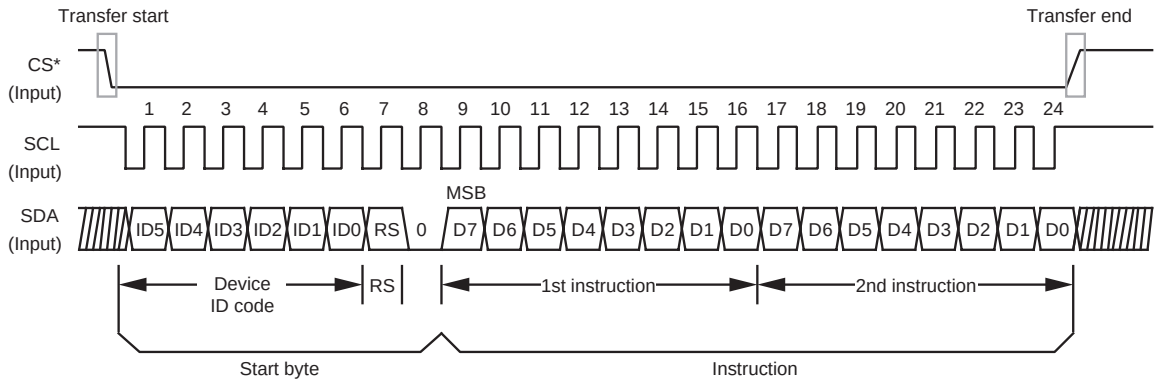
Setting the IM1 and IM0 pins (interface mode pins) to the GND and high levels, respectively, allows standard clock-synchronized serial data transfer, using the chip select (CS*), SDA, and SCL lines. Here, the HD66717 exclusively receives data.

The HD66717 initiates serial data transfer by transferring the start byte at the falling edge of the CS* input. It ends serial data transfer at the rising edge of the CS* input.

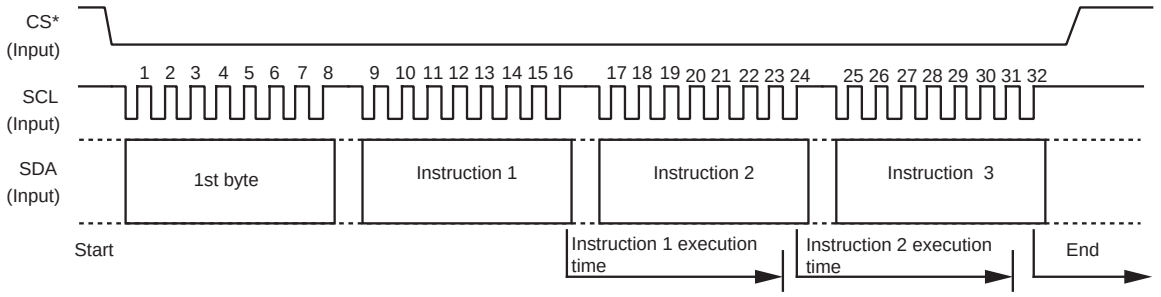
The HD66717 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit (device) identification code assigned to the HD66717. The HD66717, when selected, receives the subsequent data strings. Any identification code can be assigned by the DB5/ID5 to DB0/ID0 pins. Two different chip addresses must be assigned to a single HD66717 because the seventh bit of the start byte is used as a register select bit (RS): when RS = 0, an instruction can be issued and when RS = 1, data can be written to a RAM. The eighth bit of the start byte must be 0.

After receiving the start byte, the HD66717 receives the subsequent data as an HD66717 instruction or as RAM data. Data is transferred with the MSB first. To transfer data consecutively, adjust the data transfer rate so that the HD66717 can complete the current instruction before the eighth bit of the next instruction is transferred. See Table 18, Instruction List. If the next instruction is received during execution of the previous instruction, the next instruction will be ignored. Note that the display-clear instruction alone requires longer execution time than the others.

Figure 23 shows the clock-synchronised serial interface timing sequence.



(a) Basic data transfer (receive) timing



(b) Consecutive data transfer timing

Note: Adjust the transfer rate so that the HD66717 can complete instruction 1 before the 8th bit of instruction 2 is transferred.

Figure 23 Clock-Synchronized Serial Interface Timing Sequence

Transferring Parallel Data

Interface with an 8-Bit MPU

Eight-bit data can be transferred in parallel by setting the IM1 and IM0 pins to the V_{CC} and GND levels, respectively (Figure 24). The HD66717 can interface directly with an 8-bit bus synchronized with the E clock, or with an 8-bit MCU through an I/O port (Figure 25). When the number of I/O lines or chip packaging size is limited, a 4-bit bus interface or even serial data transfer should be used.

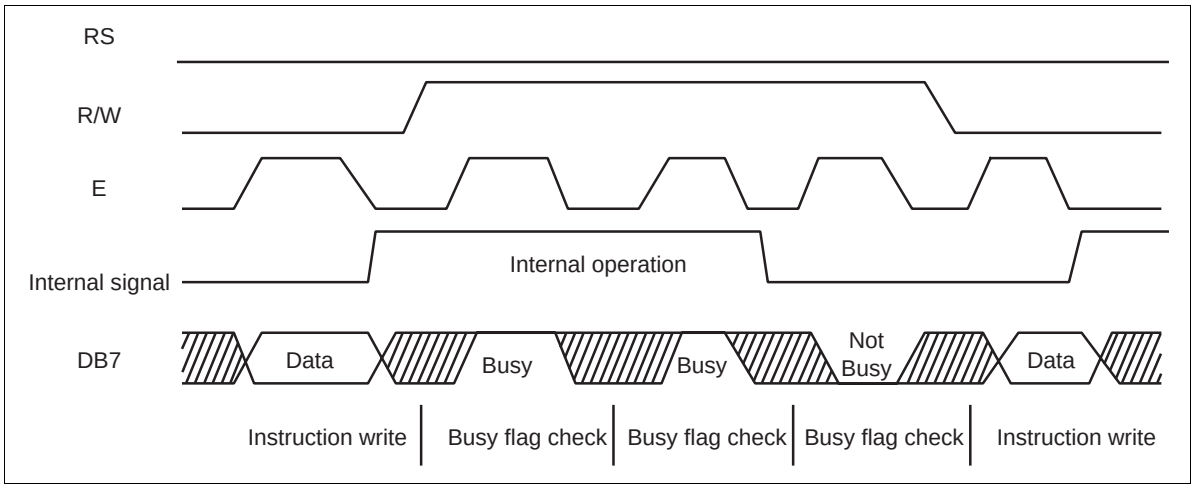


Figure 24 8-Bit Parallel Data Transfer Timing Sequence

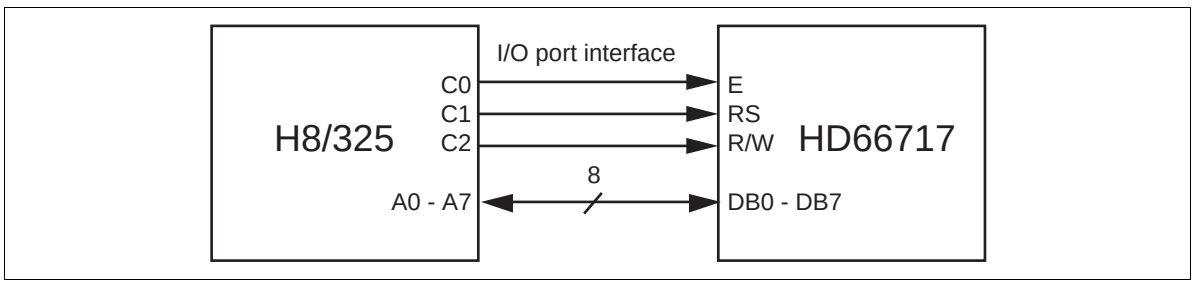


Figure 25 8-Bit MPU Interface

Interface with a 4-Bit MPU

Four-bit data can be transferred in parallel by setting both the IM1 and IM0 pins to the V_{CC} level (Figure 26). Four-bit data representing higher or lower bits of 8-bit instructions or 8-bit RAM data can be transferred in that order.

The HD66717 can forcibly reset the counter that counts the number of higher and lower 4-bit data transfers in a 4-bit bus interface. This function, called transfer-syncronization, can be performed by writing a special instruction containing 0000 four consecutive times after return home (Figure 27). For example, when a data transfer sequence becomes disordered due to noise or some undesired factor, this function resets the counter and thus enables resuming data transfer from the higher 4 bits. Using this function at specified intervals prevents display-system crash.
This transfer-synchronization must be performed after power-on reset.

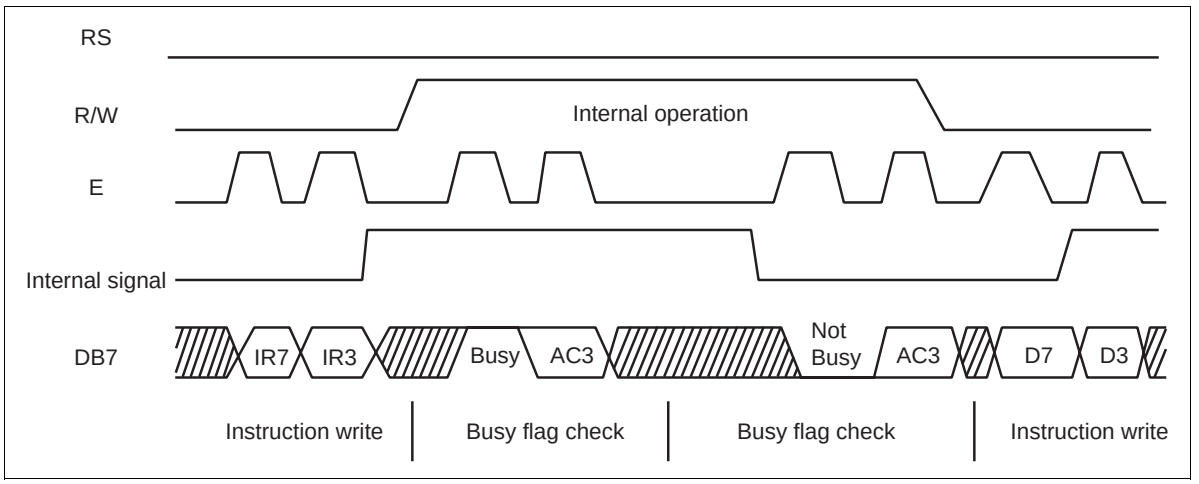
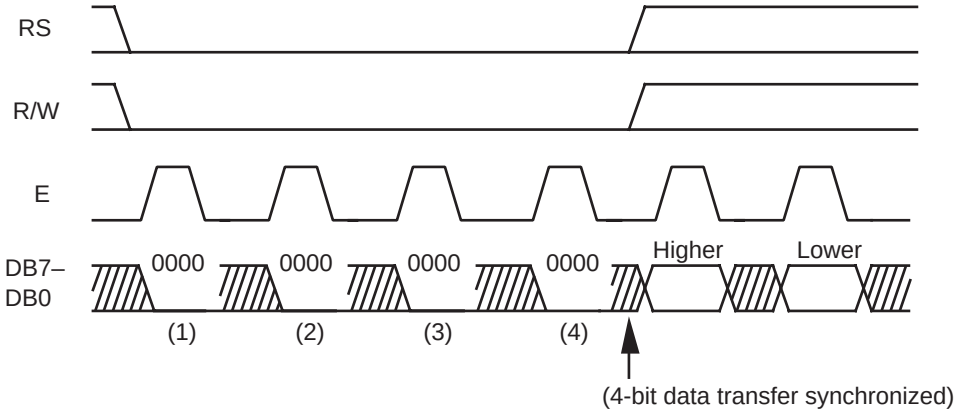


Figure 26 4-Bit Parallel Data Transfer Timing Sequence



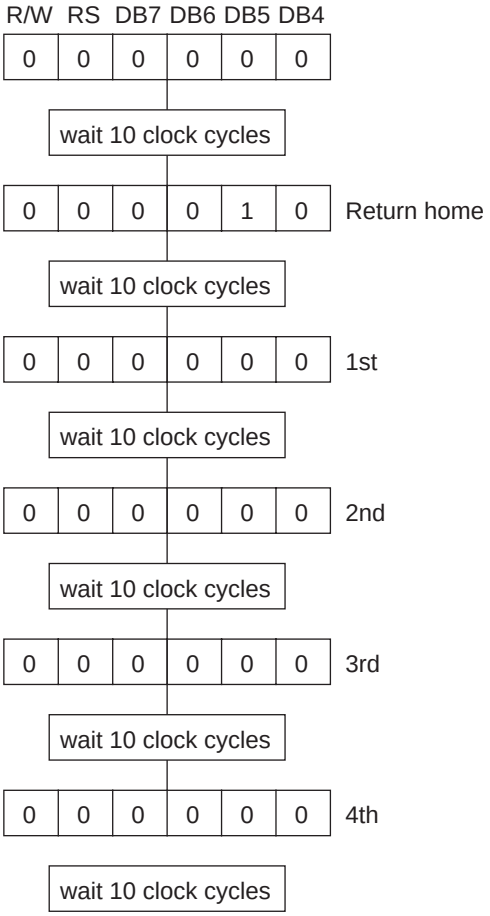


Figure 27 4-Bit Data Transfer Synchronization

Oscillator Circuit

The HD66717 can either be supplied with operating clock pulses externally (external clock mode) or oscillate using an internal R-C oscillator and an external oscillator-resistor (internal oscillation mode), as shown in Figure 28. An appropriate oscillator-resistor must be used to obtain the optimum clock frequency according to the number of display lines (Table 20). Instruction execution times change in proportion to the operating clock frequency or R-C oscillation frequency; MPU data transfer rate must be appropriately adjusted (see Table 18, Instruction List). Figure 29 shows a sample LCD drive output waveform, where 4-lines are displayed with 1/34 multiplexing duty ratio.

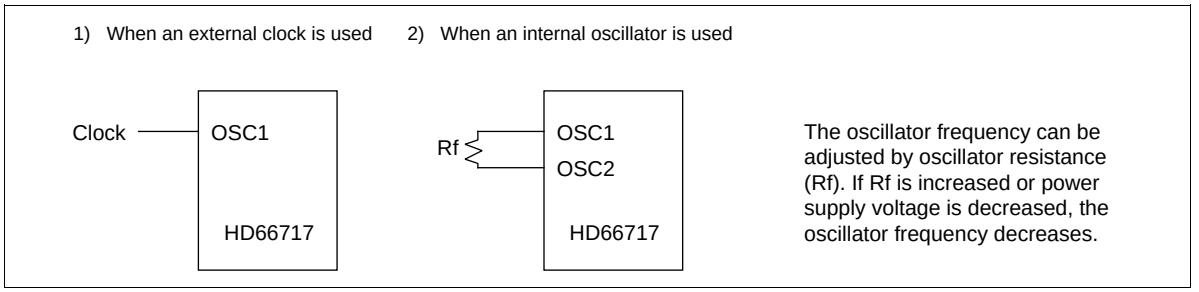


Figure 28 Oscillator Circuit

Table 20 Oscillation Frequency and LCD Frame Frequency

Item		1-Line Display NL1, NL0 = 00	2-Line Display NL1, NL0 = 01	3-Line Display NL1, NL0 = 10	4-Line Display NL1, NL0 = 11
Multiplexing duty ratio		1/10	1/18	1/26	1/34
Oscillator resistance (R_f)	V_{CC} = 3V	620 kΩ	300 kΩ	200 kΩ	150 kΩ
CR oscillator frequency		40 kHz	85 kHz	120 kHz	160 kHz
Frame frequency		67 Hz	79 Hz	77 Hz	78Hz

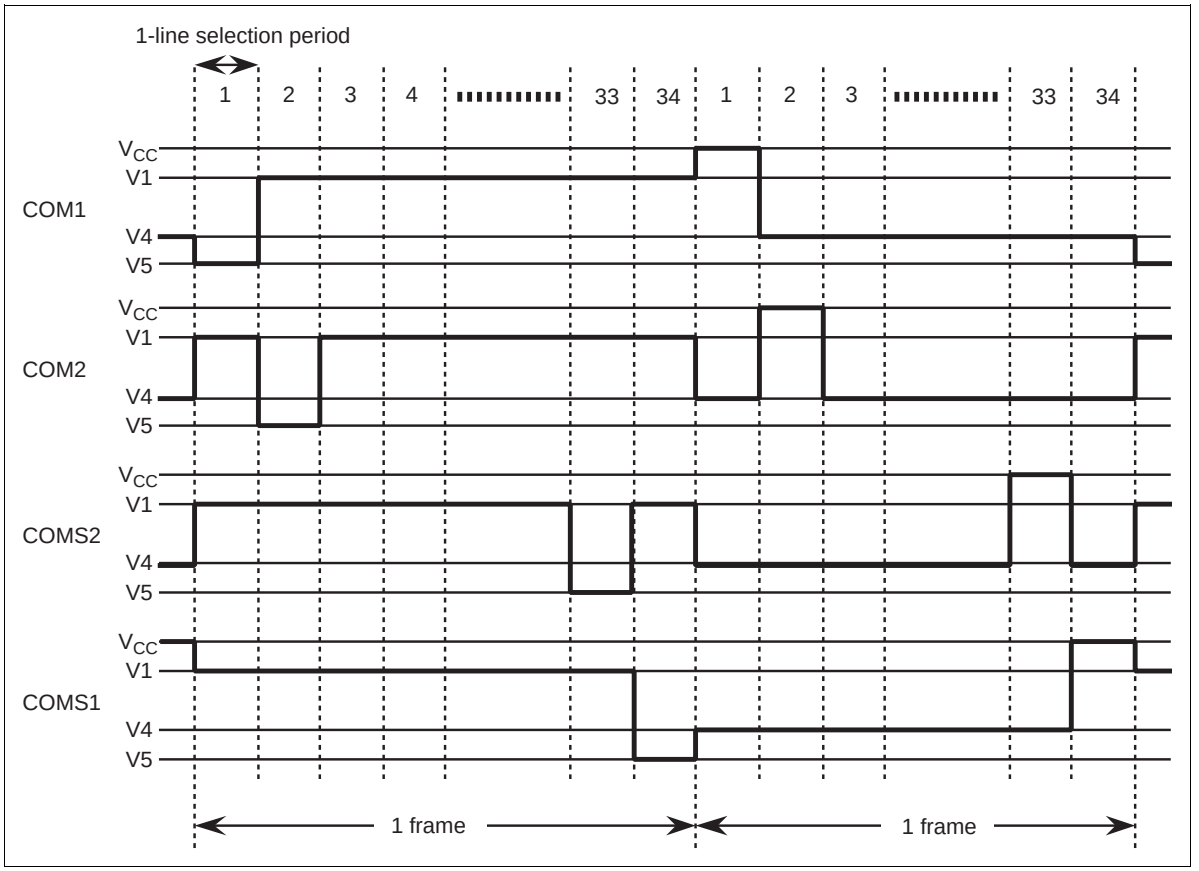


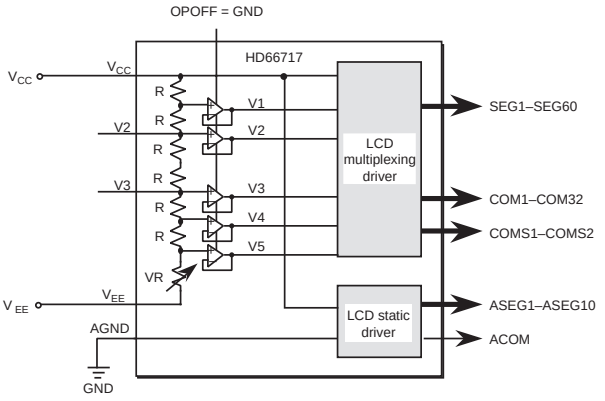
Figure 29 LCD Drive Output Waveform Example (4-line display with 1/34 multiplexing duty ratio)

Power Supply for Liquid Crystal Display Drive

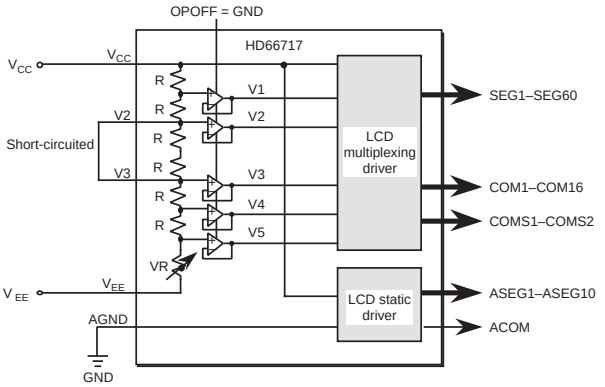
When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal booster, circuits should be connected as shown in Figure 30. Here, contrast can be adjusted through the CT bits of the contrast-control instruction.

The HD66717 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential differences between V_{CC} and V1 and between V_{EE} and V5 must be 0.4V or greater. Note that the OPOFF pin must be grounded when using the operational amplifiers.



a) 3- or 4-line display with 1/6 bias



b) 1- or 2-line display with 1/4 bias

Note: 1. Potential differences between V_{CC} and V1 and between V5 and V_{EE} must be 0.4V or greater, particularly for low-duty drive such as 1-line display.
2. When the internal operational amplifiers cannot fully drive the LCD panel used, an appropriate capacitor must be inserted between each output of V1OUT to V5OUT and V_{CC} to stabilize the operational amplifier output.

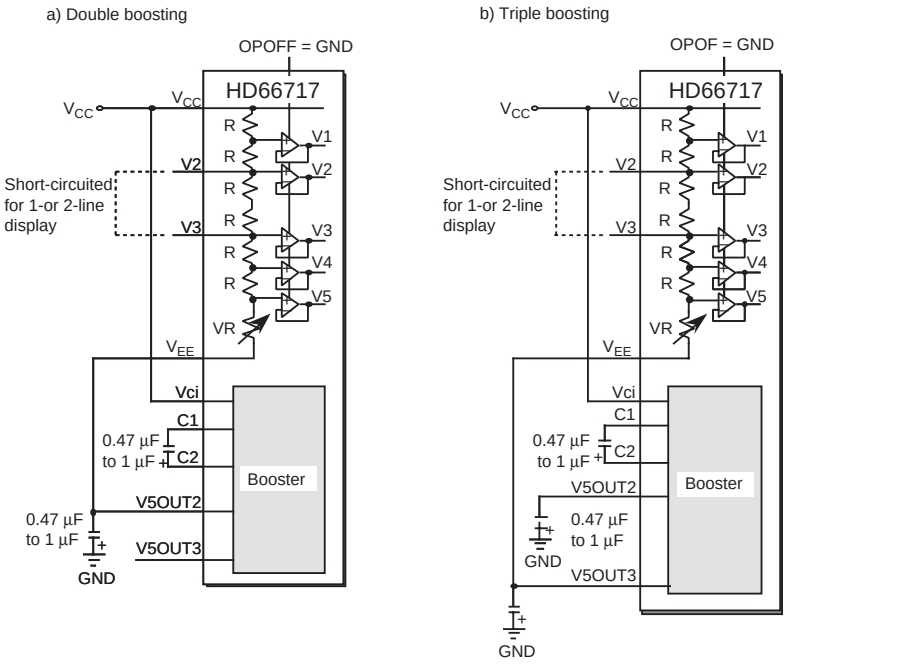
Figure 30 External Power Supply Circuit Example for LCD Drive Voltage Generation

When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal booster, circuits should be connected as shown in Figure 31. Here, contrast can be adjusted through the CT bits of the contrast-control instruction. Temperature can be compensated either through the CT bits or by controlling the reference voltage for the booster (Vci pin) using a thermistor.

Note that Vci is both a reference voltage and power supply for the booster; the reference voltage must therefore be adjusted using an emitter-follower or a similar element so that sufficient current can be supplied. In this case, Vci must be equal to or smaller than the V_{CC} level.

The HD66717 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential differences between V_{CC} and V1 and between V_{EE} and V5 must be 0.4V or greater. Note that the OPOFF pin must be grounded when using the operational amplifiers.



Note: 1. The reference voltage input (Vci) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating of the liquid-crystal power supply voltage (15V). Particularly, Vci must be 5 V or less for triple boosting.
2. Vci is both a reference voltage and power supply for the booster; connect it to V_{CC} directly or combine it with a transistor so that sufficient current can be obtained.
3. Vci must be smaller than V_{CC}.
4. To operate the voltage-follower correctly, potential differences between V_{CC} and V1 and between V5 and V_{EE} must be 0.4V or greater, particularly for low-duty drive such as 1-line display.
5. Polarized capacitors must be connected correclty.
6. Circuits for temperature compensation should be designed based on the sample circuit shown in Figure 32.

Figure 31 Internal Power Supply Circuit Example for LCD Drive Voltage Generation

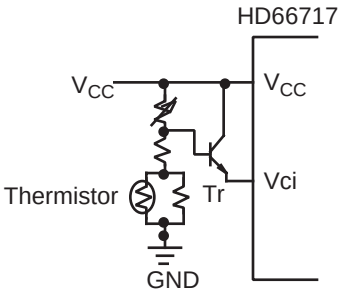
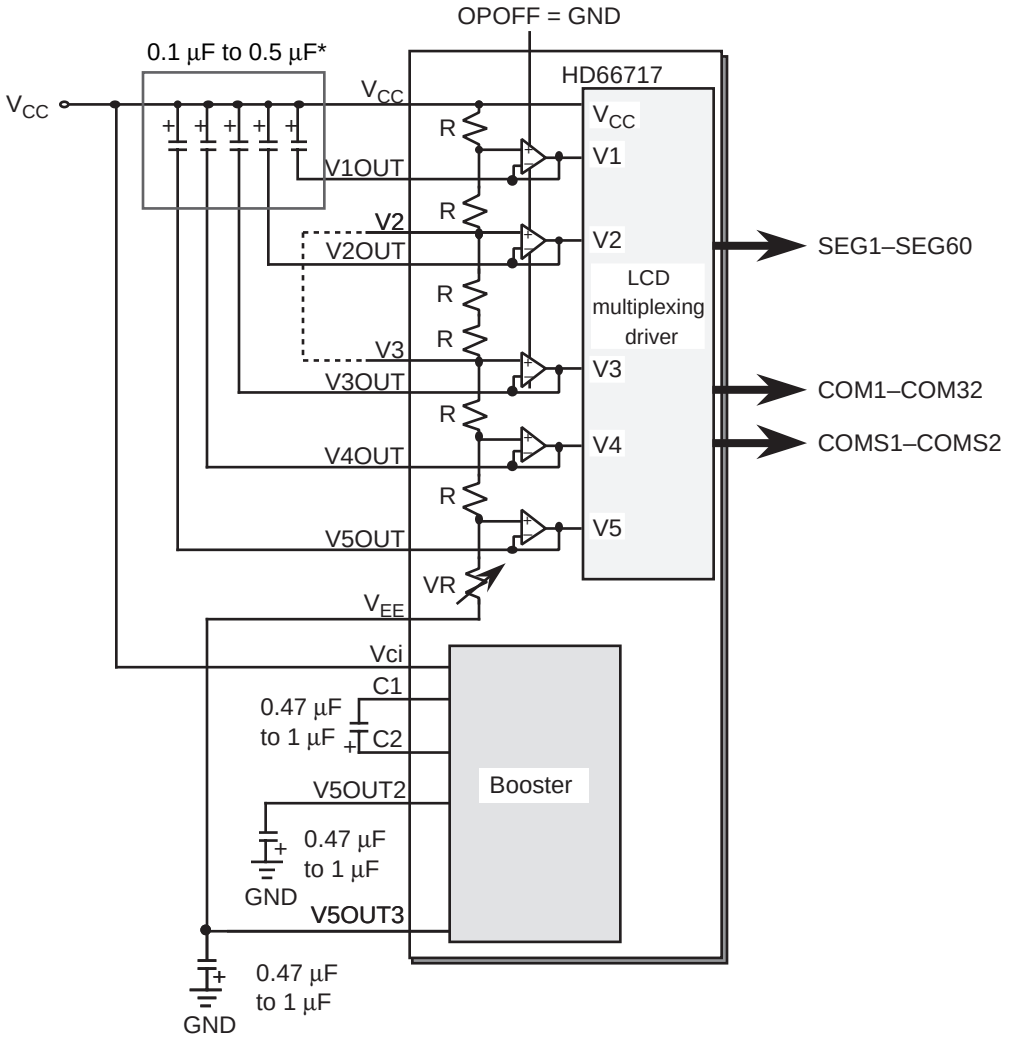


Figure 32 Temperature Compensation Circuit Example

The HD66717's internal operational amplifiers have a reduced drive current to save current consumption; when the internal operational amplifiers cannot fully drive the LCD panel used, an appropriate capacitors must be inserted between each output of V1OUT to V5OUT and V_{CC} to stabilize the operational amplifier output (Figure 33). Especially, the capacitors for V1OUT and V4OUT must be inserted when 1/26 duty or 1/34 duty drives.

The L version (HD66717L) saves the driving current.



Note : The capacitors for V1OUT and V4OUT must be inserted when 1/26 duty or 1/34 duty drives.

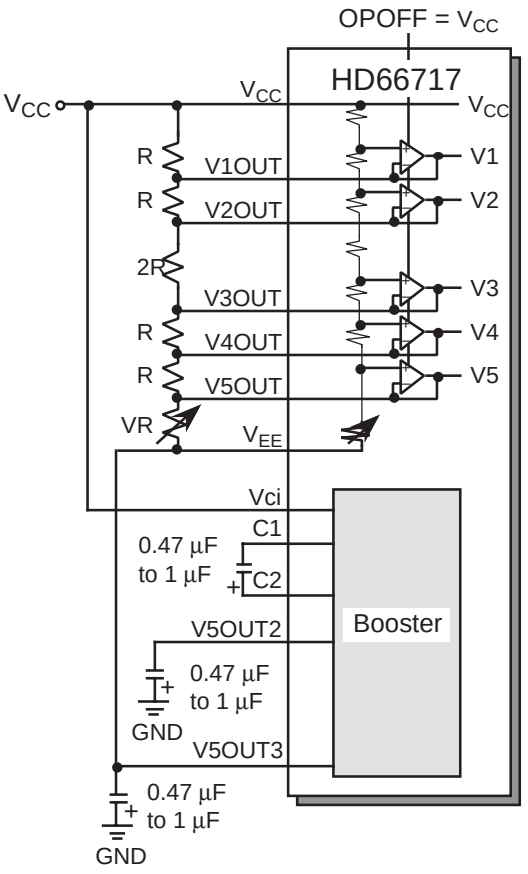
Figure 33 Operational Amplifier Output Stabilization Circuit Example

LCD driving current (I_{EE})*2	When 1/10, 1/18-duty drive (1 line, 2 lines)	When 1/26, 1/34-duty drive (3 lines, 4 lines)
When $I_{EE} \leq 15$ μA	Capacitors for V1OUT to V5OUT must be inserted.	Capacitors for V1OUT to V5OUT must be inserted.
When 15 μA $\leq I_{EE} \leq$ 40 μA	Capacitors for V1OUT and V4OUT must be inserted.	Capacitors for V1OUT and V4OUT must be inserted.
When $I_{EE} \geq 40$ μA	Capacitors for V1OUT and V4OUT may be inserted after confirming the display quality.	And additional capacitors for other VnOUTs may be inserted after confirming the display quality.

Notes:
1. These relationships between LCD driving current (I_{EE}) and the external capacitors are applied to designing LCM, but they cannot guarantee the practical display quality. This display quality depends on LCD panel size and LCD material used, and it must be checked and confirmed with your LCD panel.
2. These LCD driving currents (I_{EE}) depend on the LCD driving voltage between V_{CC} and V_{EE}, and setting of VREF, VREFP and VREFP pins.
3. Especially the capacitors for V1OUT and V4OUT are most efficient for display quality.
4. This condition is an example when the frame frequency is 60Hz to 100Hz. If higher frame frequency is used, these external capacitors should be enhanced to prevent the cross-talk.

When an Internal Booster and External Bleeder-Resistors are Used

When the internal operational amplifiers cannot fully drive the LCD panel used, V1 to V5 voltages can be supplied through external bleeder-resistors (Figure 34). Here, the OPOFF pin must be set to the V_{CC} level to turn off the internal operational amplifiers. Since the internal contrast adjuster is disabled in this case, contrast must be adjusted externally. Double- and triple-boosters can be used as they are.



Note: 1. Resistance of each external bleeder resistor should be 5 kΩ to 15 kΩ.
2. The bias current value for driving liquid-crystals can be varied by adjusting the resistance (2R) between the V2OUT and V3OUT pins.
3. The internal contrast-adjuster is disabled; contrast must be adjusted either by controlling the external variable resistor between V_{EE} and V5OUT or Vci for the booster.
4. Vci is both a reference voltage and power supply for the booster; connect it to V_{CC} directly or combine it with a transistor so that sufficient current can be obtained.
5. Vci must be smaller than V_{CC}.

Figure 34 External Bleeder-Resistor Example for LCD Drive Voltage Generation Power Supply Circuit

Contrast Adjuster

Multiplexing Drive System

Contrast for an LCD controlled by the multiplexing drive method can be adjusted by varying the liquid-crystal drive voltage (potential difference between V_{CC} and V5) through the CT bits of the contrast control instruction (electron volume function). See Figure 35 and Table 20. The value of a variable resistor (VR) can be adjusted within the range from 0.4R through 6.4R, where R is a reference resistance obtained by dividing the total resistance between V_{CC} and V5.

The HD66717 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential differences between V_{CC} and V1 and between V_{EE} and V5 must be 0.4V or greater. Note that the OPOFF pin must be grounded when using the operational amplifiers.

- 1/6 bias (V2 and V3 pins left open)
  - LCD drive voltage VLCD: $6R \times (V_{CC} - V_{EE})/(6R + VR)$ (VR = a value within the range from 0.4R to 6.4R)
  - VLCD adjustable range: $0.484 \times (V_{CC} - V_{EE}) \leq VLCD \leq 0.938 \times (V_{CC} - V_{EE})$
  - Potential difference between V_{CC} and V1: $R \times (V_{CC} - V_{EE})/(6R + VR) \geq 0.4$ (V)
  - Potential difference between V5 and V_{EE}: $VR \times (V_{CC} - V_{EE})/(6R + VR) \geq 0.4$ (V)
- 1/4 bias (V2 and V3 pins short-circuited)
  - LCD drive voltage VLCD: $4R \times (V_{CC} - V_{EE})/(4R + VR)$ (VR = a value within the range from 0.4R to 6.4R)
  - VLCD adjustable range: $0.385 \times (V_{CC} - V_{EE}) \leq VLCD \leq 0.909 \times (V_{CC} - V_{EE})$
  - Potential difference between V_{CC} and V1: $R \times (V_{CC} - V_{EE})/(4R + VR) \geq 0.4$ (V)
  - Potential difference between V5 and V_{EE}: $VR \times (V_{CC} - V_{EE})/(4R + VR) \geq 0.4$ (V)

Static Drive System

Contrast for a statically-driven LCD, that is, annunciator display, can be adjusted through the AGND pin. The annunciators are driven statically by the potential difference between V_{CC} and AGND. The AGND pin level must be equal to or greater than the GND level.

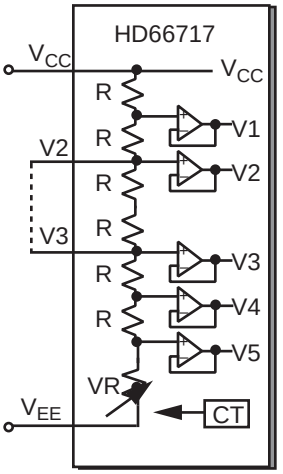


Figure 35 Contrast Adjuster

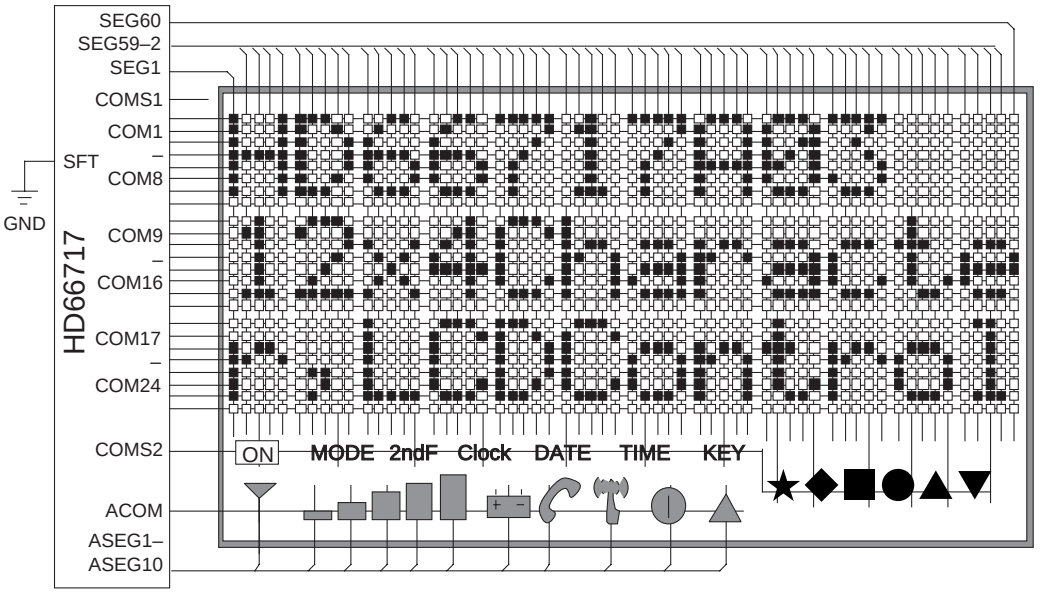
Table 21 Contrast-Adjust Bits (CT) and Variable Resistor Values

CT Register				
CT3	**CT2**	**CT1**	**CT0**	**Variable Resistor Value (VR)**
0	0	0	0	6.4 R
0	0	0	1	6.0 R
0	0	1	0	5.6 R
0	0	1	1	5.2 R
0	1	0	0	4.8 R
0	1	0	1	4.4 R
0	1	1	0	4.0 R
0	1	1	1	3.6 R
1	0	0	0	3.2 R
1	0	0	1	2.8 R
1	0	1	0	2.4 R
1	0	1	1	2.0 R
1	1	0	0	1.6 R
1	1	0	1	1.2 R
1	1	1	0	0.8 R
1	1	1	1	0.4 R

LCD Module Interface

Segment data output pins SEG1 to SEG60 can be connected either from left to right or right to left of an LCD panel according to the SFT pin level. When the SFT pin is grounded, SEG1 is connected to the far left of the panel, and when it is at the V_{CC} level, SEG60 is connected to the far left. Either connection mode can be selected according to the LCD module layout and routing on a printed-circuit board. Figures 36 shows two examples.

a) 12-character x 3-line display (SEG line above the panel : SFT = GND)



b) 12-character x 4-line display (SEG line below the panel : SFT = V_{CC})

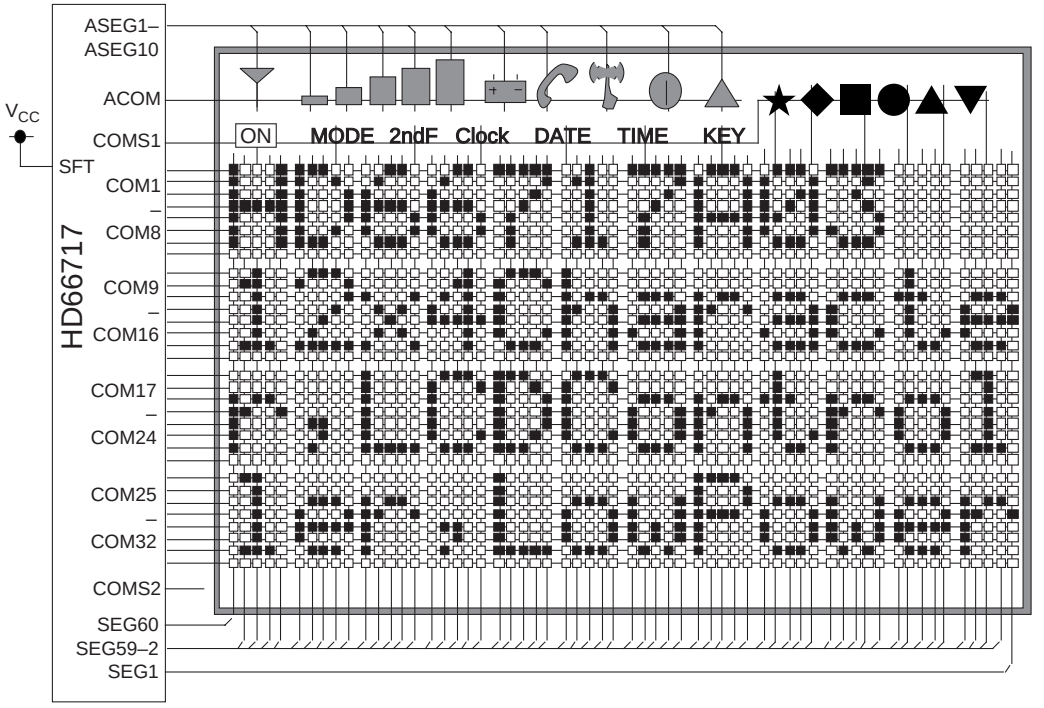


Figure 36 LCD Module Interface Examples

Segment Display and Annunciator Display

The HD66717 provides both segment display, which is driven by the multiplexing method, and annunciator display, which is driven statically. Annunciator display is driven at a logic operating voltage (V_{CC} – AGND) and is thus also available while the LCD drive power supply is turned off. Accordingly, annunciator display is suitable for displaying marks during system standby, when it is desirable to reduce current consumption. It is available in sleep mode, where internal multiplexing operations for character or segment display are halted. If an alternating signal is supplied to the EXM pin, it is also available in standby mode, where the internal R-C oscillator is halted. Here, AGND must be equal to or above the GND level.

Note that annunciator display cannot share character display drivers SEG and COM but require special drivers ASEG and ACOM that require long routing.

Tables 22 to 24 illustrates segment display and annunciator display.

Table 22 Comparison between Segment Display and Annunciator Display

Item	Segment Display	Annunciator Display
Number of driven elements	20 each by COMS1 and COMS2	10
Blinking	Impossible	Possible
Segment drivers	SEG1–SEG60 (shared with character display)	ASEG1–ASEG10 (independent of character display)
Common drivers	COMS1, COMS2	ACOM
LCD power supply	V_{CC} – V5 (LCD power supply necessary)	V_{CC} – AGND (LCD power supply unnecessary)
Normal mode display	Display possible together with character display by multiplexing drive	Display possible by static drive
Sleep mode display	Impossible (SEG and COM output V_{CC})	Possible by static drive
Standby mode display (without oscillation)	Impossible (SEG and COM output V_{CC})	Possible by supplying alternating signal to the EXM pin

Table 23 Correspondence between Segment Display SEGRAM Addresses (ASEG) and Driver Signals

ASEG Address				Common	Segment Signals				
MSB			LSB	Signal	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	0	COMS1	SEG1/21/41	SEG2/22/42	SEG3/23/43	SEG4/24/44	SEG5/25/45
1	0	0	1	COMS1	SEG6/26/46	SEG7/27/47	SEG8/28/48	SEG9/29/49	SEG10/30/50
1	0	1	0	COMS1	SEG11/31/51	SEG12/32/52	SEG13/33/53	SEG14/34/54	SEG15/35/55
1	0	1	1	COMS1	SEG16/36/56	SEG17/37/57	SEG18/38/58	SEG19/39/59	SEG20/40/60
1	1	0	0	COMS2	SEG1/21/41	SEG2/22/42	SEG3/23/43	SEG4/24/44	SEG5/25/45
1	1	0	1	COMS2	SEG6/26/46	SEG7/27/47	SEG8/28/48	SEG9/29/49	SEG10/30/50
1	1	1	0	COMS2	SEG11/31/51	SEG12/32/52	SEG13/33/53	SEG14/34/54	SEG15/35/55
1	1	1	1	COMS2	SEG16/36/56	SEG17/37/57	SEG18/38/58	SEG19/39/59	SEG20/40/60

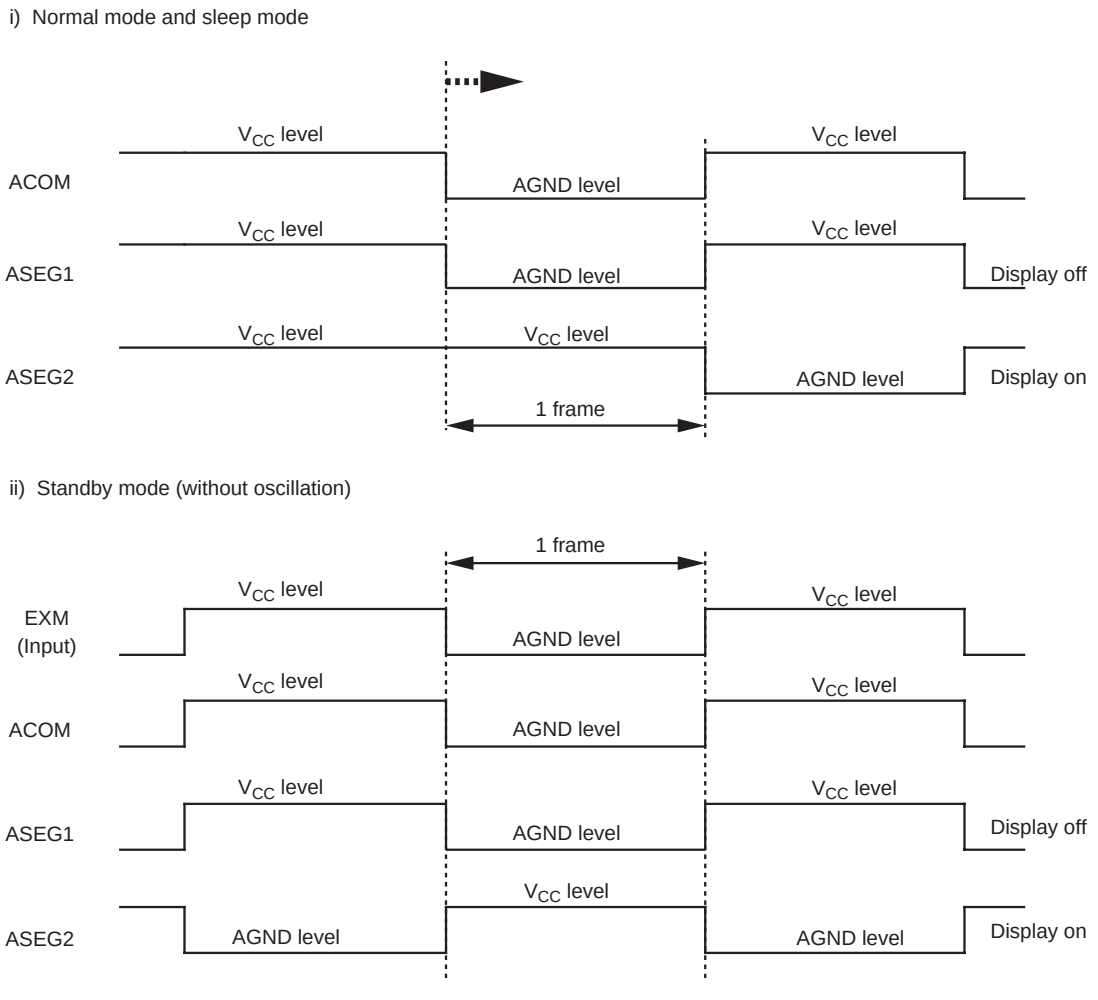
Table 24 Correspondence between Annunciator Display Addresses (AAN) and Driver Signals

AAN Address				Common	Segment Signals			
MSB			LSB	Signal	Bits 7, 6	Bits 5, 4	Bits 3, 2	Bits 1, 0
0	0	0	0	ACOM	ASEG1	ASEG2	ASEG3	ASEG4
0	0	0	1	ACOM	ASEG5	ASEG6	ASEG7	ASEG8
0	0	1	0	ACOM	ASEG9	ASEG10	—	—

Note: The annunciator is turned on when the corresponding even bit (bit 6, 4, 2, or 0) is 1, and the turned-on annunciator blinks when the corresponding odd bit (bit 7, 5, 3, or 1) is 1.

Annunciator Drive

Figure 37 shows annunciator drive output waveforms in two modes.



Note: If annunciator display is unnecessary during standby mode, make sure to fix the EXM pin to the V_{CC} or GND level and set the annunciator display ON bit (DA) to 0. This will prevent dark display and liquid-cell deterioration due to DC bias application on liquid crystal cells.

Figure 37 Annunciator Drive Output Waveforms

Vertical Smooth Scroll

The HD66717 can scroll in the vertical direction in units of raster-rows. This function is achieved by writing character codes into the DDRAM area that is not being used for display. In other words, since the DDRAM corresponds to a 5-line × 12-character display, one of the lines can be used to achieve continuous smooth vertical scroll even in a 4-line display. Here, after the fifth line is displayed, the first line is displayed again. Specifically, this function is controlled by incrementing or decrementing the value in the scroll-start line bits (SL2 to SL0) and scroll-start raster-row bits (SN2 to SN0) by 1. For example, to smoothly scroll up, first set SN2 to SN0 to 000, and increment SL2 to SL0 by 1 from 000 to 111 to scroll seven raster-rows. Then increment SN2 to SN0 to 001, and again increment SL2 to SL0 by 1 from 000 to 111. To start displaying and scrolling from the first raster-row of the second line, update the first line of DDRAM data as desired during its non-display period.

Figure 38 shows an example of vertical smooth scrolling and Figure 39 shows an example of setting instructions for vertically scrolling upward in a 4-line display (NL1 and NL0 = 11).

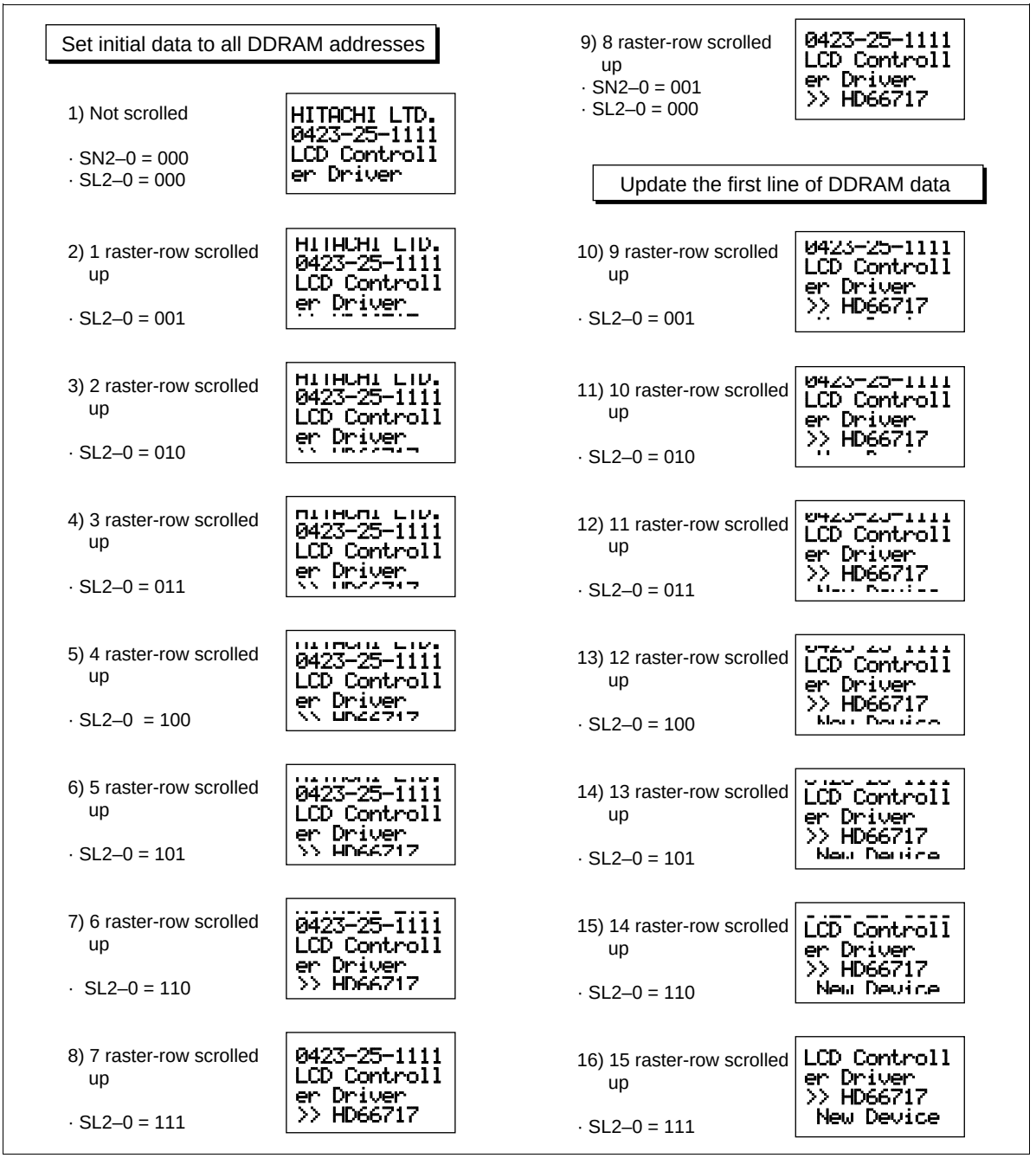


Figure 38 Example of Vertical Smooth Scrolling

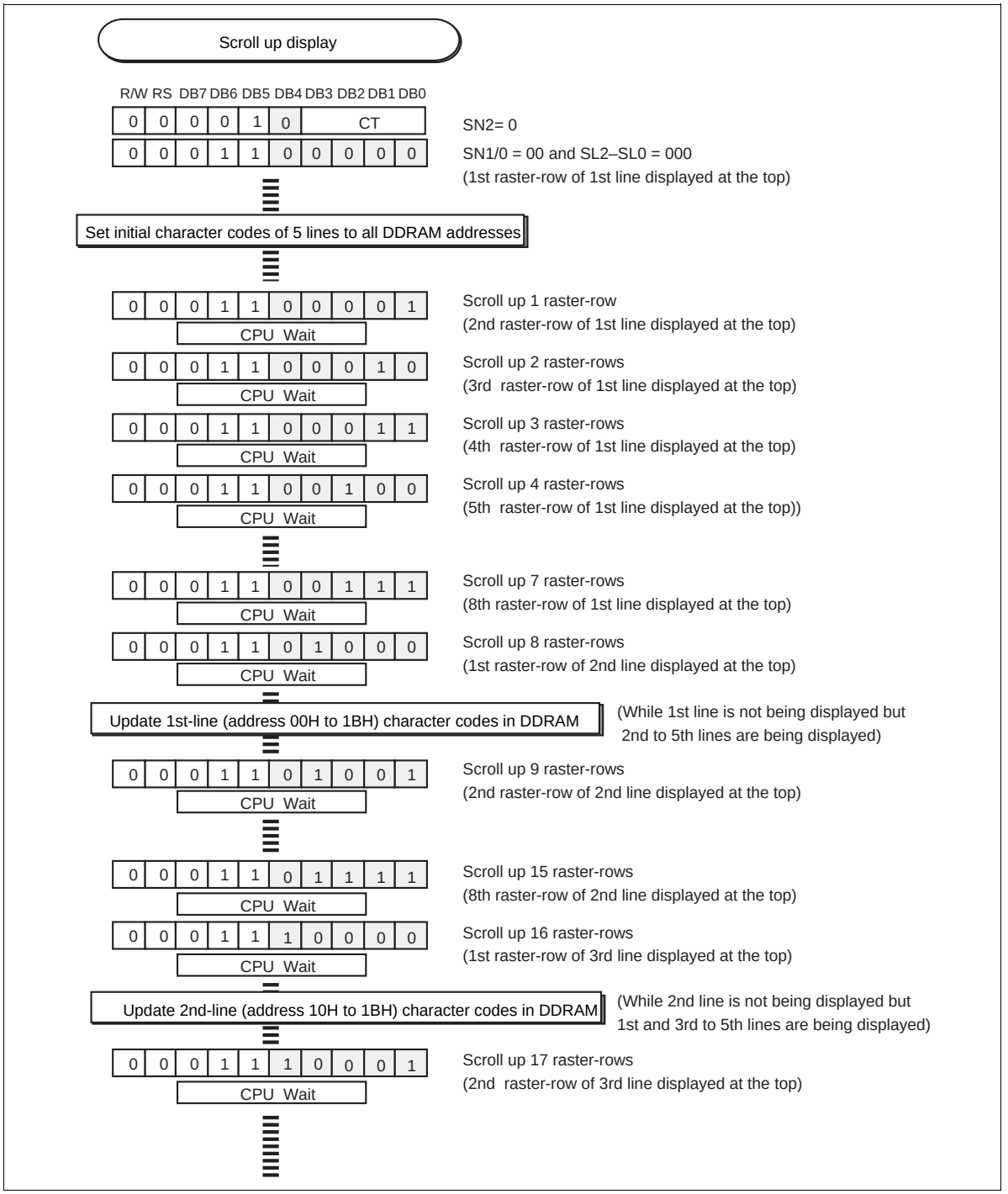


Figure 39 Example of Setting Instructions for Vertical Smooth Scroll (4-line display (NL1 and NL0 = 11))

Line-Cursor Display

The HD66717 can assign a cursor attribute to an entire line corresponding to the address counter value by setting the LC bit to 1 (Table 25). One of three line-cursor modes can be selected: a black-white inverting blink cursor (B/W = 1), an underline cursor (C = 1), and a blink cursor (B = 1). The blink cycle for a black-white inverting blink cursor and for a blink cursor is 32 frames. These line-cursors are suitable for highlighting an index and/or marker, and for indicating an item in a menu with a cursor or an underline.

Figures 40 to 42 show three line-cursor examples.

Table 25 Address Counter Value and Line-Cursor

Address Counter Value (AC)	Selected Line for Line-Cursor
00H to 0BH	Entire 1st line (12 digits)
10H to 1BH	Entire 2nd line (12 digits)
20H to 2BH	Entire 3rd line (12 digits)
30H to 3BH	Entire 4th line (12 digits)
40H to 4BH	Entire 5th line (12 digits)

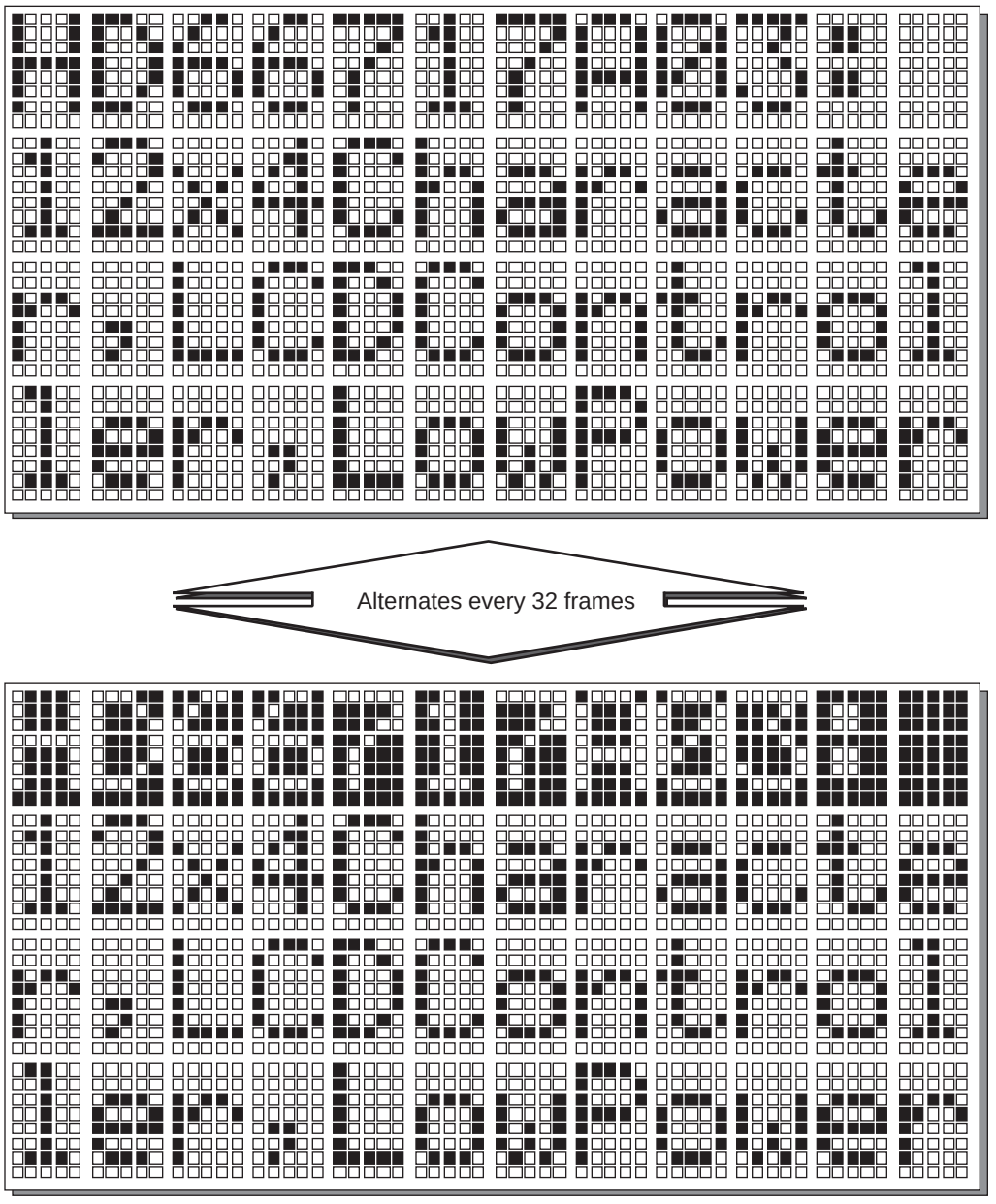


Figure 40 Example of Black-White Inverting Blink Cursor (LC = 1; B/W = 1)

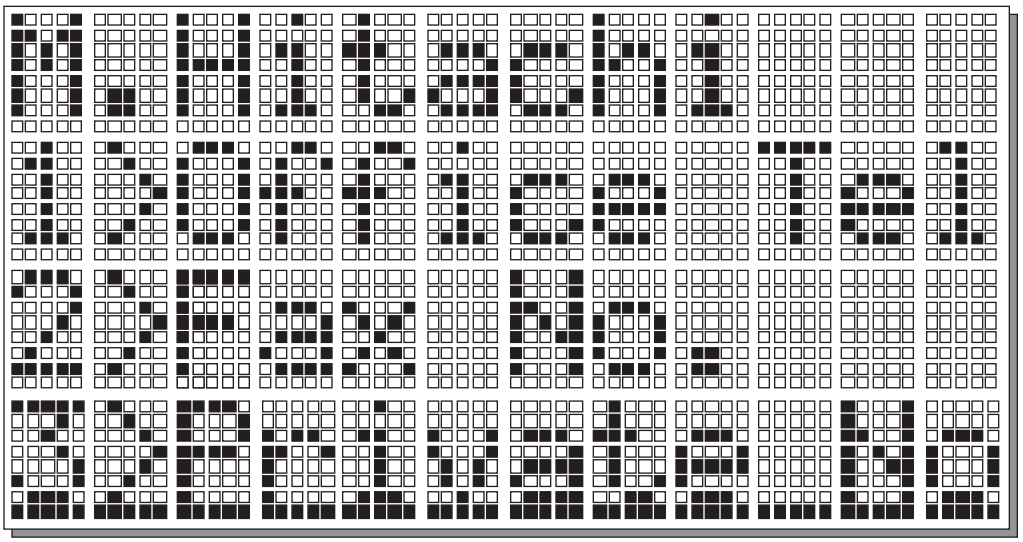


Figure 41 Example of Underline Cursor (LC = 1; C = 1)

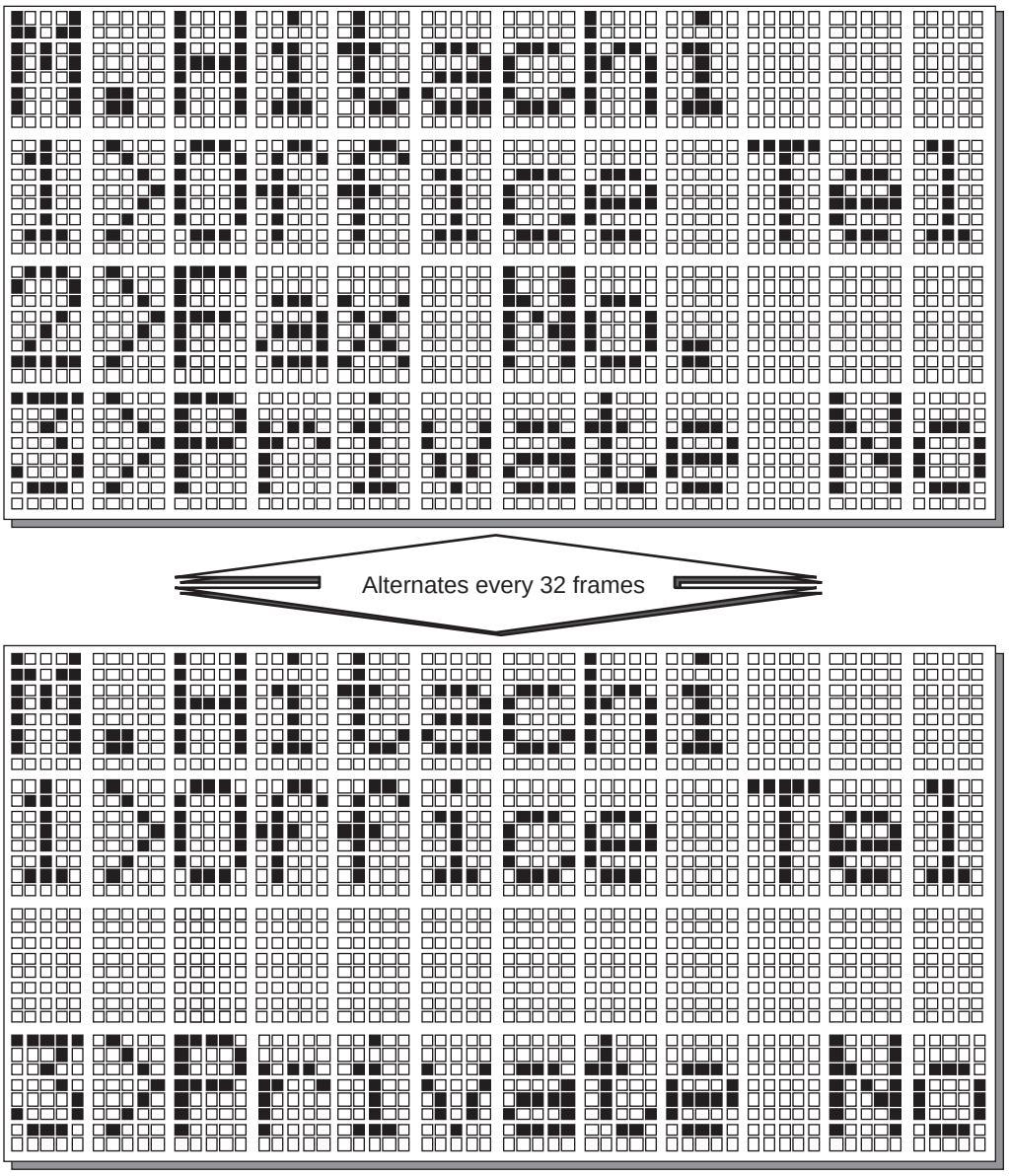


Figure 42 Example of Blink Cursor (LC = 1; B = 1)

Double-Height Display

The HD66717 can double the height of any desired line from the first to third lines. A line can be selected by the DL3 to DL1 bits as listed in Table 26. All the standard font characters stored in the CGROM and CGRAM can be doubled in height, providing an easy-to-see display. Note that there should be no space between lines for double-height display (Figure 43).

Table 26 Double-Height Display Specifications

DL3	DL2	DL1	2-Line Display (NL1, NL0 = 01)	3-Line Display (NL1, NL0 = 10)	4-Line Display (NL1, NL0 = 11)
0	0	0	1st & 2nd lines: normal	1st to 3rd lines: normal	1st to 4th lines: normal
0	0	1	1st line: double-height	1st line: double-height 2nd line: normal	1st line: double-height 2nd & 3rd lines: normal
0	1	0	Disabled	2nd line: double-height 1st line: normal	2nd line: double-height 1st & 3rd lines: normal
0	1	1	1st line: double-height	Disabled	1st & 2nd lines: double-height
1	0	0	1st & 2nd lines: normal	Disabled	3rd line: double-height 1st & 2nd lines: normal
1	0	1	1st line: double-height	1st line: double-height 2nd line: normal	Disabled
1	1	0	Disabled	2nd line: double-height 1st line: normal	Disabled
1	1	1	1st line: double-height	Disabled	1st & 2nd lines: double-height

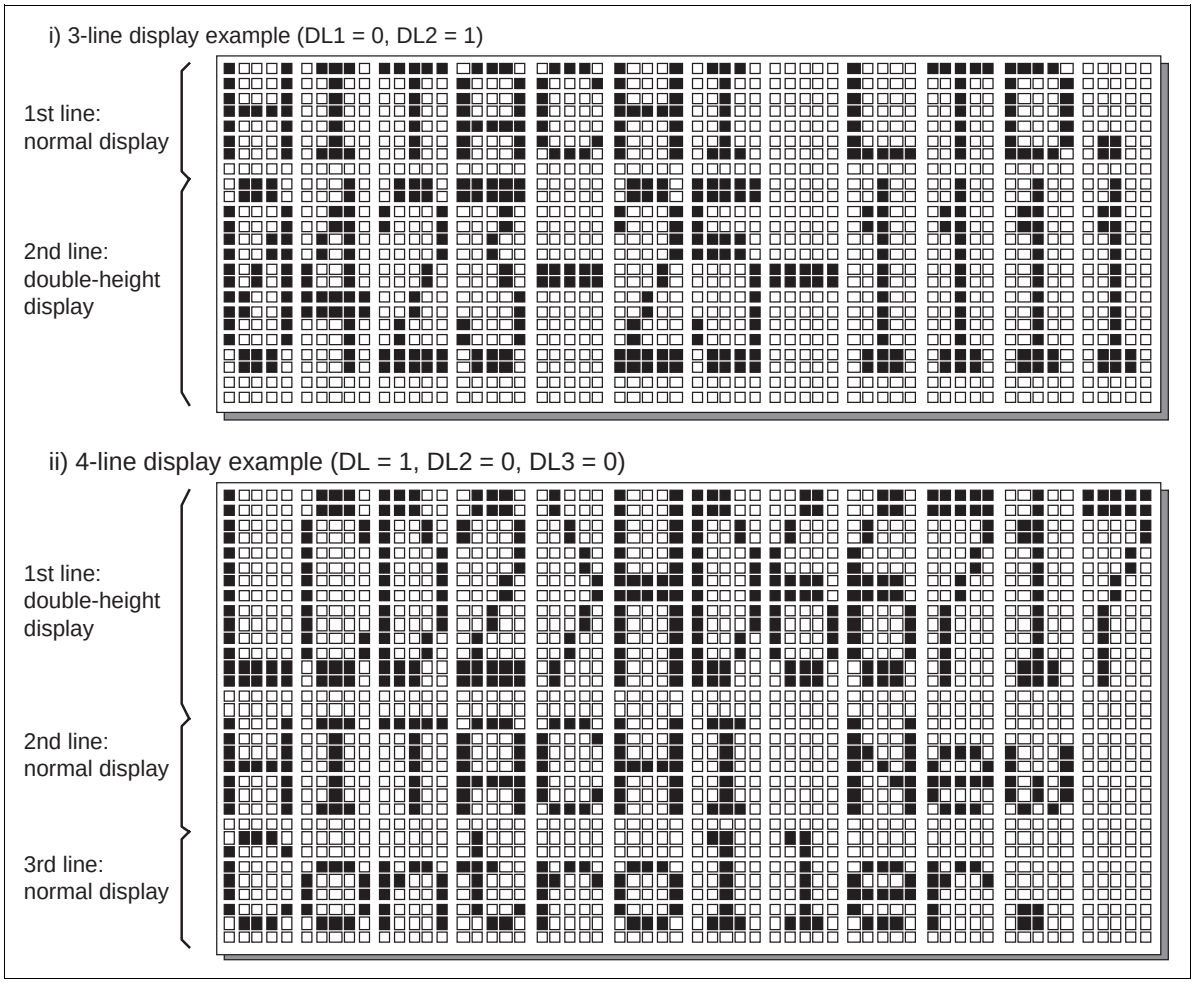


Figure 43 Double-Height Display Examples

Partial-Display-Off Function

The HD66717 can program the number of display lines (NL1 and NL0 bits), divide the internal operating frequency by four (OSC bit), and adjust the display contrast (CT bit). Combining these functions, the HD66717 can turn off the second and/or subsequent lines, displaying only the characters in the first line to reduce internal current consumption (partial-display-off function). This function is suitable for calendar or time display, which needs to be continuous during system standby with minimal current consumption. Here, the second to fourth non-displayed lines are constantly driven by the deselection level voltage, thus turning off the LCD for the lines.

Note that internal clock frequency is reduced to a quarter, quadrupling execution time of each instruction; MPU data transfer rate must be appropriately adjusted.

Table 27 lists partial-display-off function specifications and Figure 44 shows a sample display using the partial-display-off function.

Table 27 Partial Display Off Function

Function Item	Normal 4-Line Display	Partially-Off Display
Character display	1st to 4th lines displayed	Only 1st line displayed
Segment display	Possible	Possible
Annunciator display	Possible	Possible
R-C oscillation frequency	160 kHz	160 kHz
Internal operating frequency	160 kHz (OSC = 0)	40 kHz (OSC = 1)
LCD single-line drive frequency	2.7 kHz (1/34 duty ratio)	0.7 kHz (1/10 duty ratio)
Frame frequency	78 Hz	66 Hz

Note: Select an optimum LCD drive voltage (between V_{CC} and V5) for the multiplexing duty ratio used, using a reference voltage input pin (Vci) for the booster or the contrast-adjust bits (CT) .

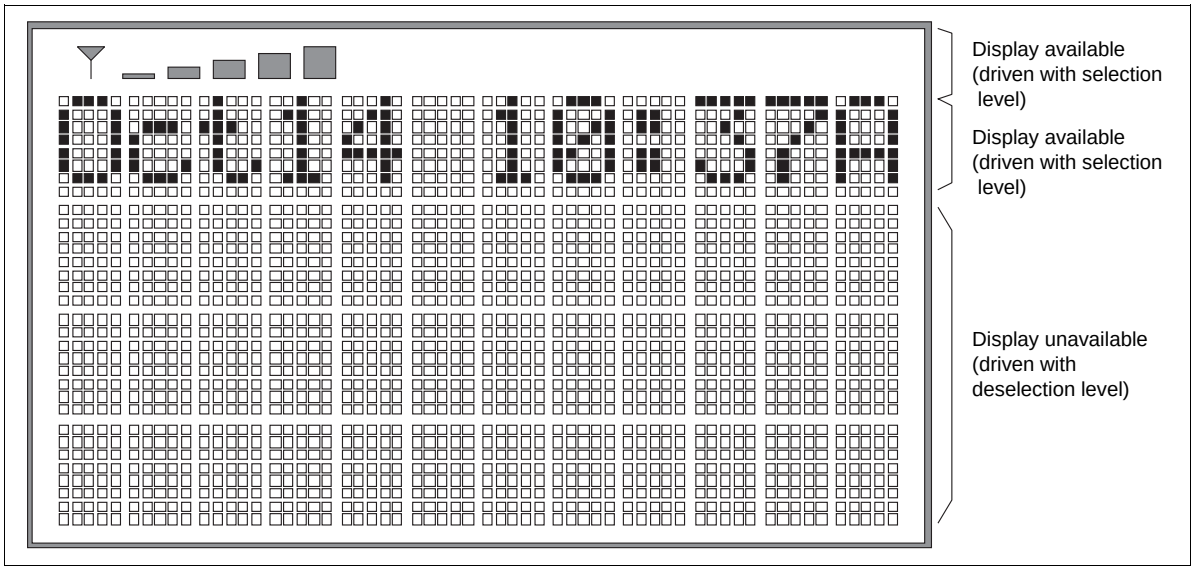


Figure 44 Example of Partially-Off Display (date and time indicated)

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66717 in sleep mode, where the device halts all the internal display operations except for annunciator display operations, thus reducing current consumption. Specifically, character and segment displays, which are controlled by the multiplexing drive method, are completely halted. Here, all the SEG (SEG1 to SEG60) and COM (COM1 to COM34) pins output the V_{CC} level, resulting in no display. If the AMP bit is set to 0 in sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Annunciators can be normally displayed in sleep mode. Since they are driven at logic operating power supply voltage (V_{CC} – AGND), they are available even if the LCD power supply is turned off (AMP = 0). This function allows time and alarm marker indication during system standby with reduced current consumption.

During sleep mode, no instructions can be accepted for character/segment display and neither DDRAM, CGRAM, nor SEGRAM can be accessed.

Table 28 compares the functions of sleep mode and standby mode.

Table 28 Comparison of Sleep Mode and Standby Mode

Function Item	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
Character display	Turned off	Turned off
Segment display	Turned off	Turned off
Annunciator display	Can be turned on	Can be turned on when an alternating signal is supplied to the EXM pin
R-C oscillation	Normally operates	Halted

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66717 in standby mode, where the device stops completely, halting all internal operations including the R-C oscillator, thus further reducing current consumption compared to that in sleep mode. Specifically, character and segment displays, which are controlled by the multiplexing drive method, are completely halted. Here, all the SEG (SEG1 to SEG60) and COM (COM4 to COM34) pins output the V_{CC} level, resulting in no display. If the AMP bit is set to 0 in standby mode, the LCD drive power supply can be turned off.

Annunciators can be displayed simply by supplying an approximately 40-Hz alternating signal for the LCD drive signals to the EXM pin externally. If annunciator display is unnecessary during standby mode, the EXM pin must be fixed to the V_{CC} or GND level and the annunciator display-on bit (DA) set to 0.

During standby mode, no instructions can be accepted other than those for annunciator display and the start-oscillator instruction. To cancel standby mode, issue the start-oscillator instruction to stabilize R-C oscillation before setting the STB bit to 0.

Figure 45 shows the procedure for setting and cancelling standby mode.

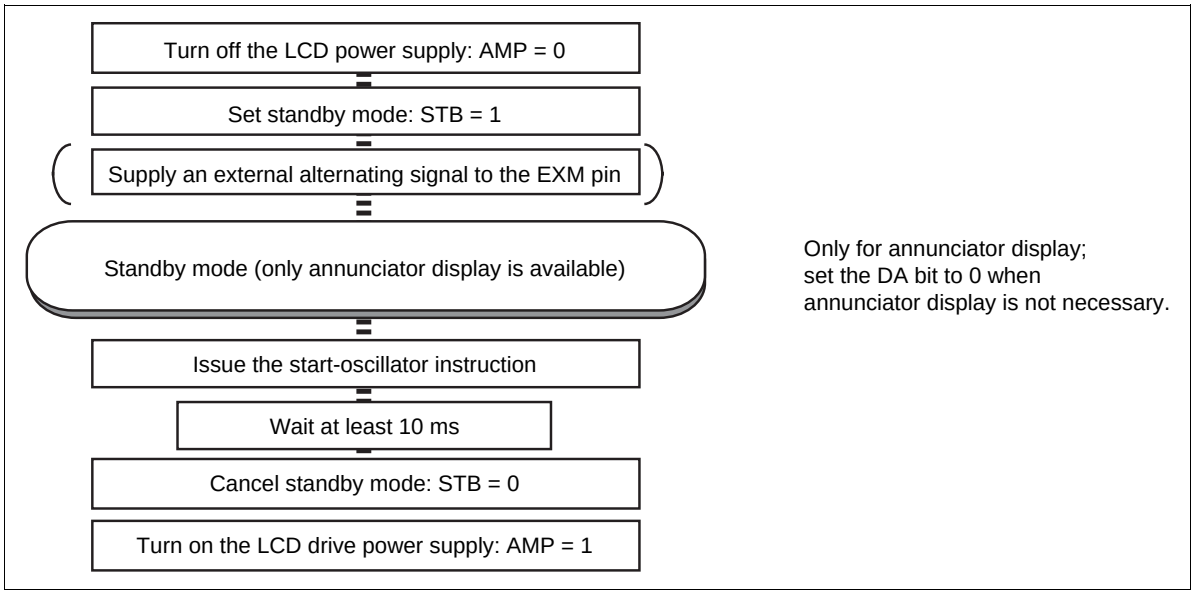


Figure 45 Procedure for Setting and Cancelling Standby Mode

Absolute Maximum Ratings*

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{CC}–V_{EE}	V	–0.3 to +15.0	1, 2
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	T_{opr}	°C	–30 to +75	
Storage temperature	T_{stg}	°C	–55 to +110	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.4V to 5.5V, T_a = –30 to +75°C*[3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage	VIH	$0.7V_{CC}$	—	V_{CC}	V		6
Input low voltage	VIL	–0.3	—	$0.15V_{CC}$	V	V_{CC} = 2.4 to 3.0V	6
		–0.3	—	0.6	V	V_{CC} = 3.0 to 5.5V	
Output high voltage (1) (DB0–DB7 pins)	VOH1	$0.75V_{CC}$	—	—	V	I_{OH} = –0.1 mA	
Output low voltage (1) (DB0–DB7 pins)	VOL1	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	
Output low voltage (2) (SDA pin)	VOL2	—	—	$0.2V_{CC}$	V	V_{CC} = 2.4 to 4.5V I_{OL} = 0.4 mA	7
		—	—	0.4	V	V_{CC} = 4.5 to 5.5V I_{OL} = 1.0 mA	
Driver ON resistance (COM pins)	R_{COM}	—	2	20	kΩ	±Id = 0.05 mA (COM) VLCD = 4V	8
Driver ON resistance (SEG pins)	R_{SEG}	—	2	30	kΩ	±Id = 0.05 mA (SEG) VLCD = 4V	8
I/O leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (RESET* pin)	–Ip	10	50	120	µA	V_{CC} = 3V Vin = 0V	
Current consumption during normal operation (V_{CC}–GND)	I_{OP}	—	30	60	µA	R_f oscillation, external clock, V_{CC} = 3V, f_{OSC} = 160 kHz, 1/34 duty	10, 11
Current consumption during sleep mode (V_{CC}–GND)	I_{SL}	—	25	—	µA	R_f oscillation, external clock, V_{CC} = 3V, f_{OSC} = 160 kHz	10, 11
Current consumption during standby mode (V_{CC}–GND)	I_{ST}	—	0.1	5	µA	No R_f oscillation, V_{CC} = 3V, Ta = 25°C	10, 11
LCD power supply current (V_{CC}–V_{EE})	I_{EE}	—	25	60	µA	V_{CC}–V_{EE} = 8V, f_{OSC} = 160 kHz VREF–VREFM: short-circuited	
LCD voltage with 1/4 bias (V_{CC}–V_{EE})	VLCD1	3.0	—	13.0	V	V2–V3 short-circuited	12
LCD voltage with 1/6 bias (V_{CC}–V_{EE})	VLCD2	3.0	—	13.0	V	V2–V3 open	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	VUP2	8.0	8.8	—	V	V_{CC} = Vci = 4.5V, I_0 = 0.1 mA, C = 1 µF, f_{OSC} = 160 kHz, T_a = 25°C	15
Output voltage (V5OUT3 pin)	VUP3	7.0	7.9	—	V	V_{CC} = Vci = 2.7V, I_0 = 0.1 mA, C = 1 µF, f_{OSC} = 160 kHz, T_a = 25°C	15
Input voltage	VCi	1.0	—	5.0	V	Vci ≤ V_{CC}	15

Note: * Refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.4V to 5.5V, T_a = –30 to +75°C*[3])

Clock Characteristics (V_{CC} = 2.4V to 5.5V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	20	160	350	kHz		13
	External clock duty ratio	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{fcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	120	160	200	kHz	R_f = 150 kΩ, V_{CC} = 3V	14

Note: * Refer to the Electrical Characteristics Notes section following these tables.

Read & Write Bus Interface Timing Characteristics with Read Operation (V_{CC} = 2.4V to 4.5V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figures 52 and 53
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/W to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	30	—	—		
Read data delay time	t_{DDR}	—	—	400	ns	Figure 53
Read data hold time	t_{DHR}	5	—	—		

Read & Write Bus Interface Timing Characteristics with Read Operation (V_{CC} = 4.5V to 5.5V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	500	—	—	ns	Figures 52 and 53
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	30	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_H	30	—	—		
Read data delay time	t_{DDR}	—	—	200	ns	Figure 53
Read data hold time	t_{DHR}	5	—	—		

Write Bus Interface Timing Characteristics without Read Operation (V_{CC} = 2.4V to 5.5V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time		t_{CYCE}	500	—	—	ns	Figure 52
Enable pulse width (“High” level)	V_{CC} = 2.4 to 3.0V	P_{WEH}	200	—	—		
	V_{CC} = 3.0 to 5.5V	P_{WEH}	150	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/W to E)		t_{AS}	60	—	—		
Address hold time		t_{AH}	20	—	—		
Data set-up time		t_{DSW}	140	—	—		
Data hold time		t_{H}	30	—	—		

Clock-Synchronized Serial Interface Operation (V_{CC} = 2.4V to 5.5V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	1	—	20	µs	Figure 54
Serial clock high-level width	t_{SCH}	400	—	—	ns	
Serial clock low-level width	t_{SCL}	400	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	200	—	—		
Serial input data set-up time	t_{SISU}	200	—	—		
Serial input data hold time	t_{SIH}	200	—	—		

I^2C bus Interface Operation (V_{CC} = 2.4V to 4.5V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
SCL clock cycle time	t_{SCL}	2	—	20	µs	Figure 55
SCL clock high-level width	t_{SCLH}	500	—	—	ns	
SCL clock low-level width	t_{SCLL}	1000	—	—		
SCL/SDA rise/fall time	t_{Sr}, t_{Sf}	—	—	300		
Bus free time	t_{BUF}	140	—	—		
Start hold time	t_{STAH}	500	—	—		
Retransmit start set-up time	t_{STAS}	500	—	—		
Stop set-up time	t_{STOS}	500	—	—		
SDA data set-up time	t_{SDAS}	140	—	—		
SDA data hold time	t_{SDAH}	0	—	—		

I2C bus Interface Operation (V_{CC} = 4.5V to 5.5V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
SCL clock cycle time	t_{SCL}	2	—	20	µs	Figure 55
SCL clock high-level width	t_{SCLH}	500	—	—	ns	
SCL clock low-level width	t_{SCLL}	1000	—	—		
SCL/SDA rise/fall time	t_{Sr}, t_{Sf}	—	—	300		
Bus free time	t_{BUF}	100	—	—		
Start hold time	t_{STAH}	500	—	—		
Retransmit start set-up time	t_{STAS}	500	—	—		
Stop set-up time	t_{STOS}	500	—	—		
SDA data set-up time	t_{SDAS}	100	—	—		
SDA data hold time	t_{SDAH}	0	—	—		

Reset Timing (V_{CC} = 2.4 V to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	10	—	—	ms	Figure 56

Electrical Characteristics Notes

1. All voltage values are referred to GND = 0V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the given electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristic are exceeded, the LSI may malfunction or exhibit poor reliability.
2. $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 > V_{EE}$ must be maintained.
3. For die products, specified at 75°C.
4. For die products, specified by the common die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output (Figure 46).

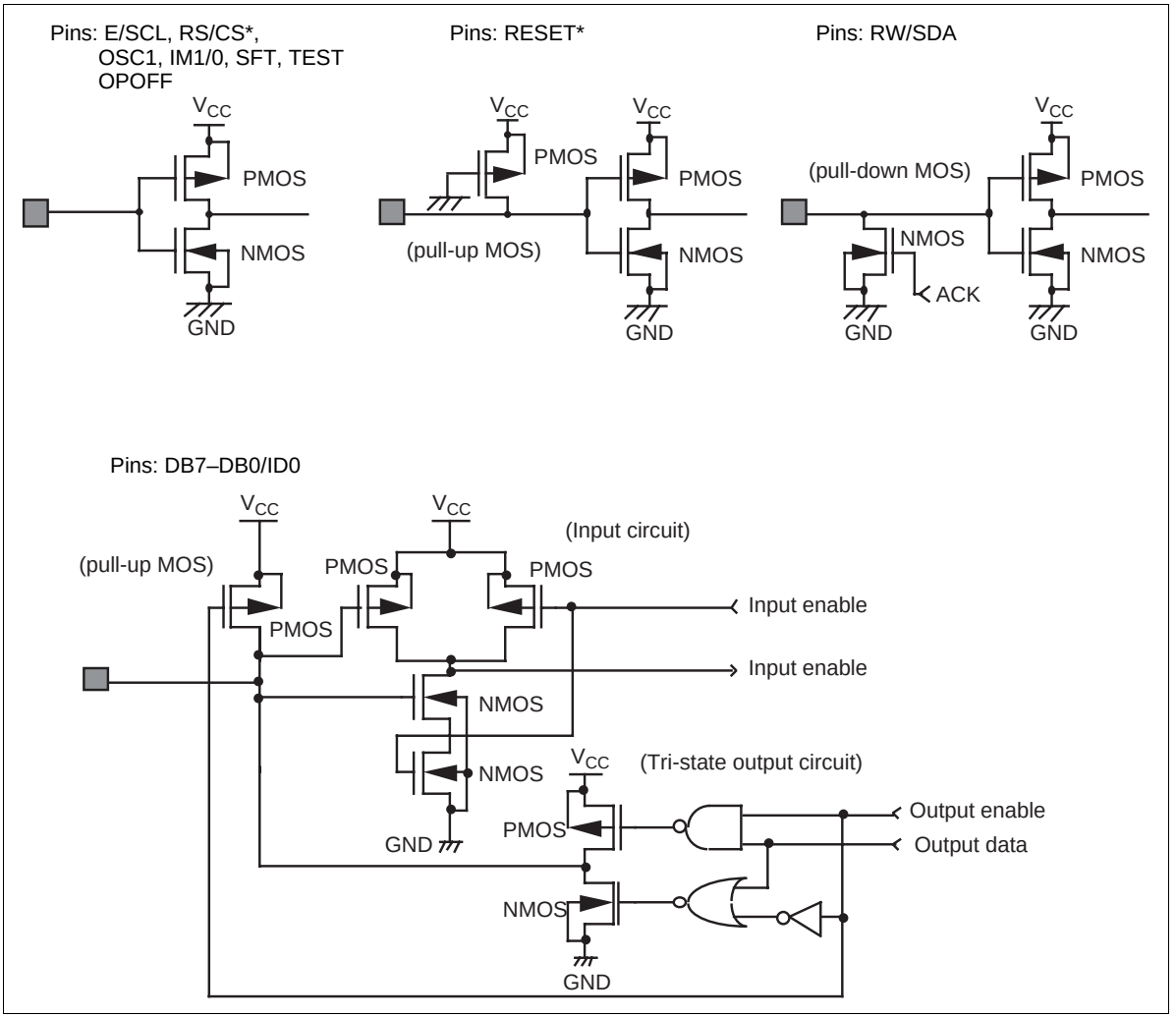


Figure 46 I/O Pin Configurations

6. The TEST pin must be grounded and the ID5 to ID0, IM1, IM0, SFT, EXM, and OPOFF pins must be grounded or connected to V_{CC}.
7. Applies to the ACK bit for I^2C bus interface.
8. Applies to resistor values (RCOM) between power supply pins V_{CC}, V1OUT, V4OUT, V5OUT and common signal pins (COM1 to COM32, COMS1, and COMS2), and resistor values (RSEG) between power supply pins V_{CC}, V2OUT, V3OUT, V5OUT and segment signal pins (SEG1 to SEG60).
9. This excludes the current flowing through pull-up MOSs and output drive MOSs.
10. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating.
11. The following shows the relationship between the operation frequency (f_{OSC}) and current consumption (I_{CC}) (Figure 47). The HD66717 is a normal current-consumption version, and the HD66717L is a low current-consumption version in the LCD power supply.

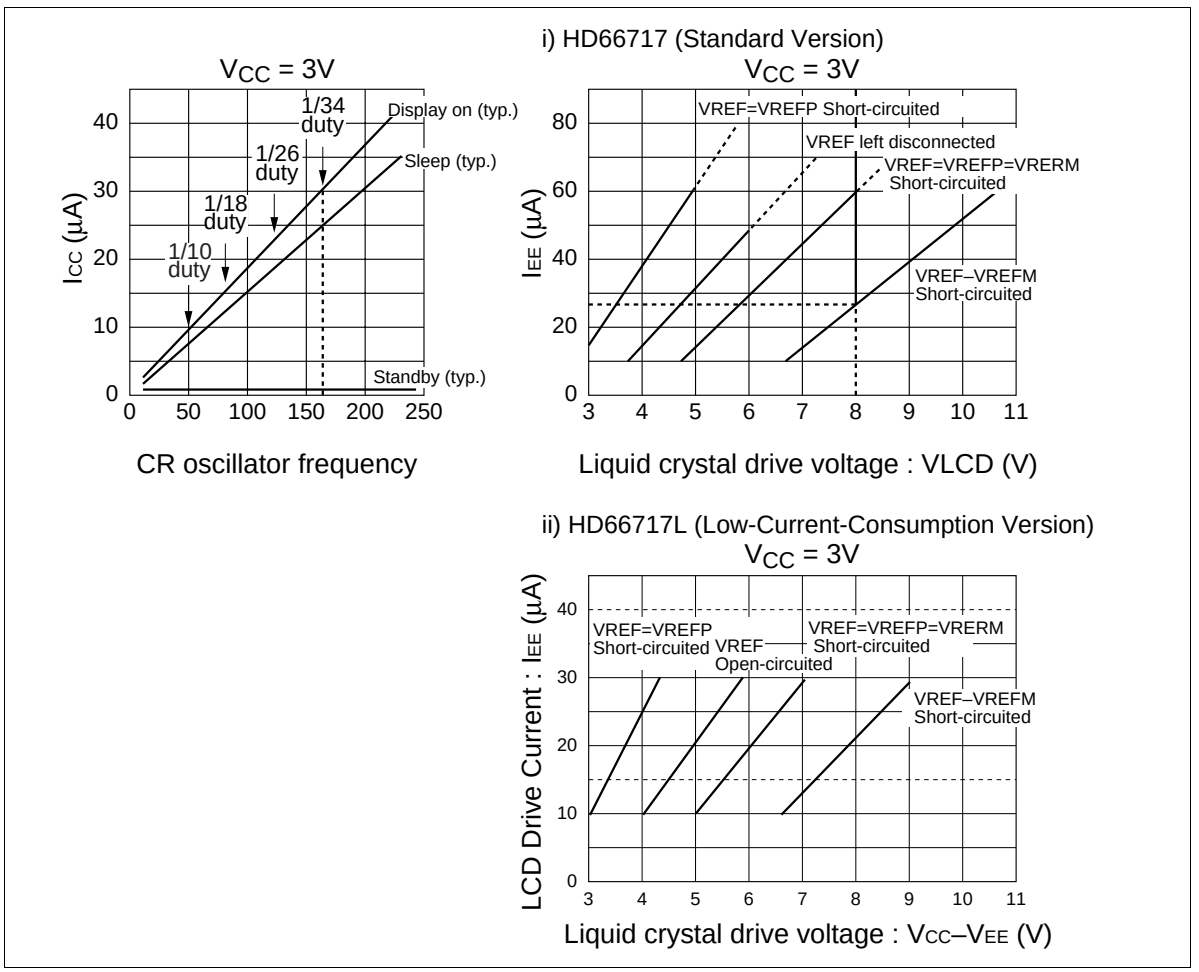


Figure 47 Relationship between the Operation Frequency and Current Consumption

12. Each COM and SEG output voltage is within ±0.15V of the LCD voltage (V_{CC}, V1, V2, V3, V4, V5) when there is no load.

13. Applies to the external clock input (Figure 48).

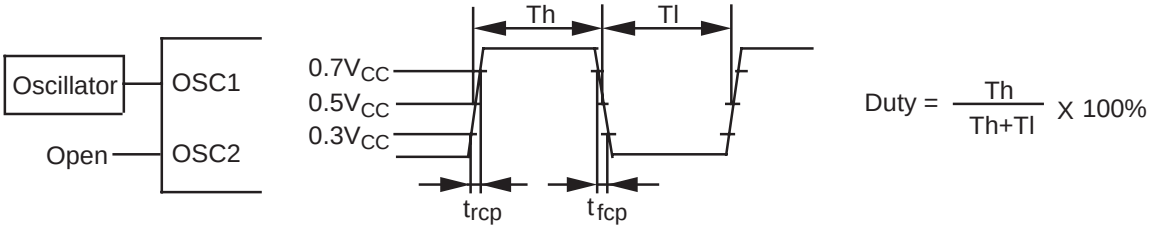
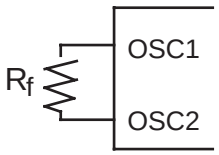


Figure 48 External Clock Supply

14. Applies to the internal oscillator operations using oscillation resistor R_f (Figure 49).



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Referential data

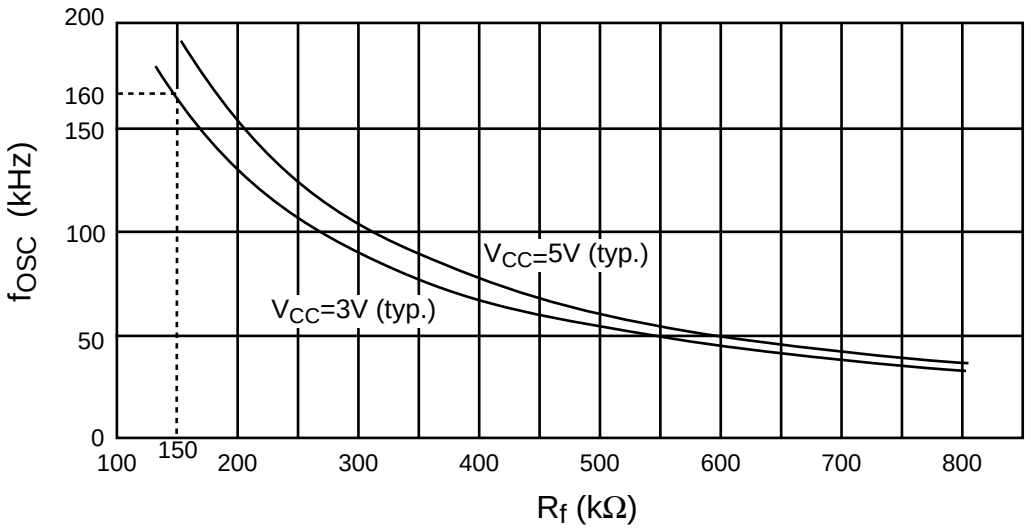


Figure 49 Internal Oscillation

15. Booster characteristics test circuits are shown in Figure 50.

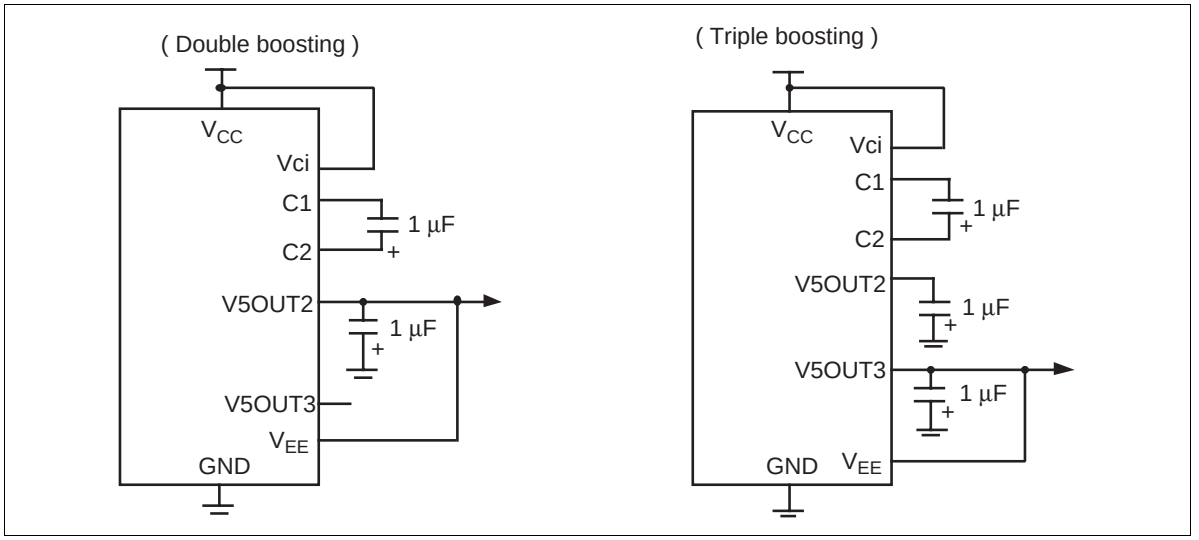
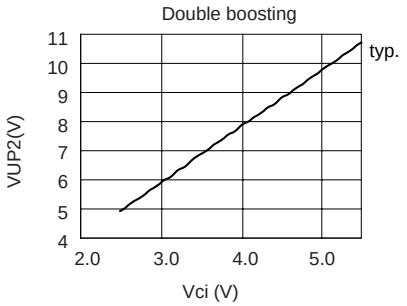


Figure 50 Booster

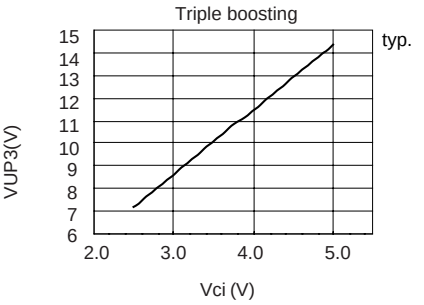
Referential data

VUP2 = V_{CC} – V5OUT2 VUP3 = V_{CC} – V5OUT3

(i) Relationship between the obtained voltage and input voltage

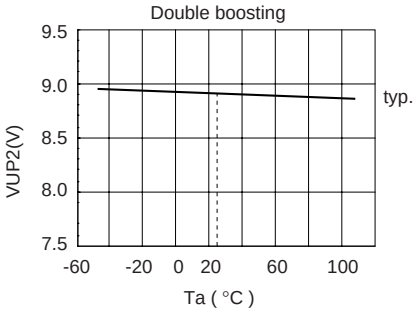


Vci = V_{CC}, fcp = 160kHz, Ta = 25°C

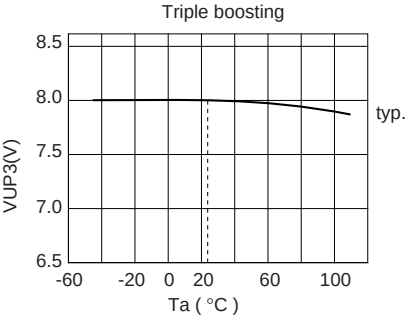


Vci = V_{CC}, fcp = 160kHz, Ta = 25°C

(ii) Relationship between the obtained voltage and temperature

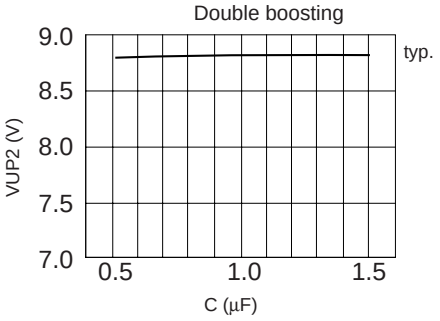


Vci = V_{CC} = 4.5V, R_f = 180kΩ,
I_O = 0.1mA

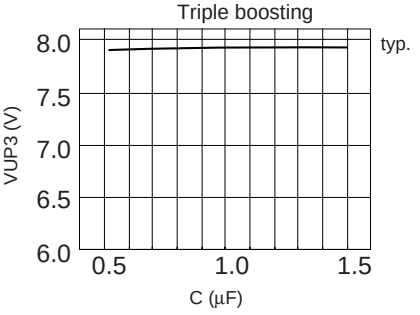


Vci = V_{CC} = 2.7V, R_f = 150kΩ,
I_O = 0.1mA

(iii) Relationship between the obtained voltage and capacitance



Vci = V_{CC} = 4.5V, R_f = 180kΩ,
I_O = 0.1mA



Vci = V_{CC} = 2.7V, R_f = 150kΩ,
I_O = 0.1mA

Figure 50 Booster (cont)

(iv) Relationship between the obtained voltage and the load current.

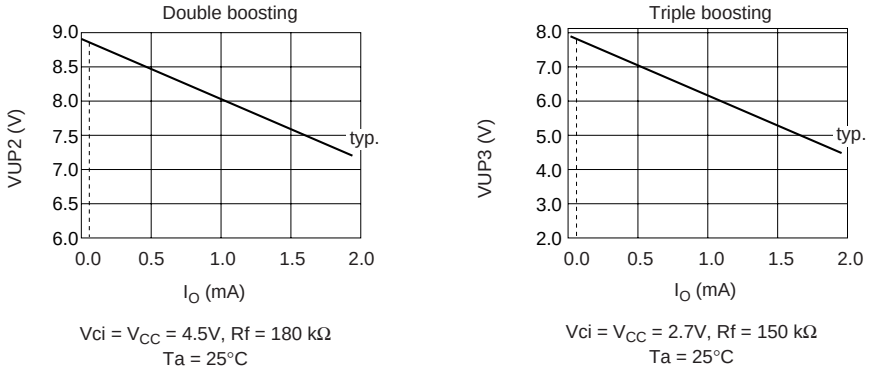


Figure 50 Booster (cont)

Load Circuits

AC Characteristics Test Load Circuits

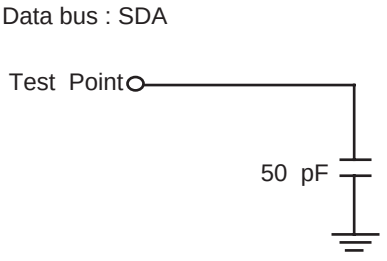


Figure 51 Load Circuit

Timing Characteristics

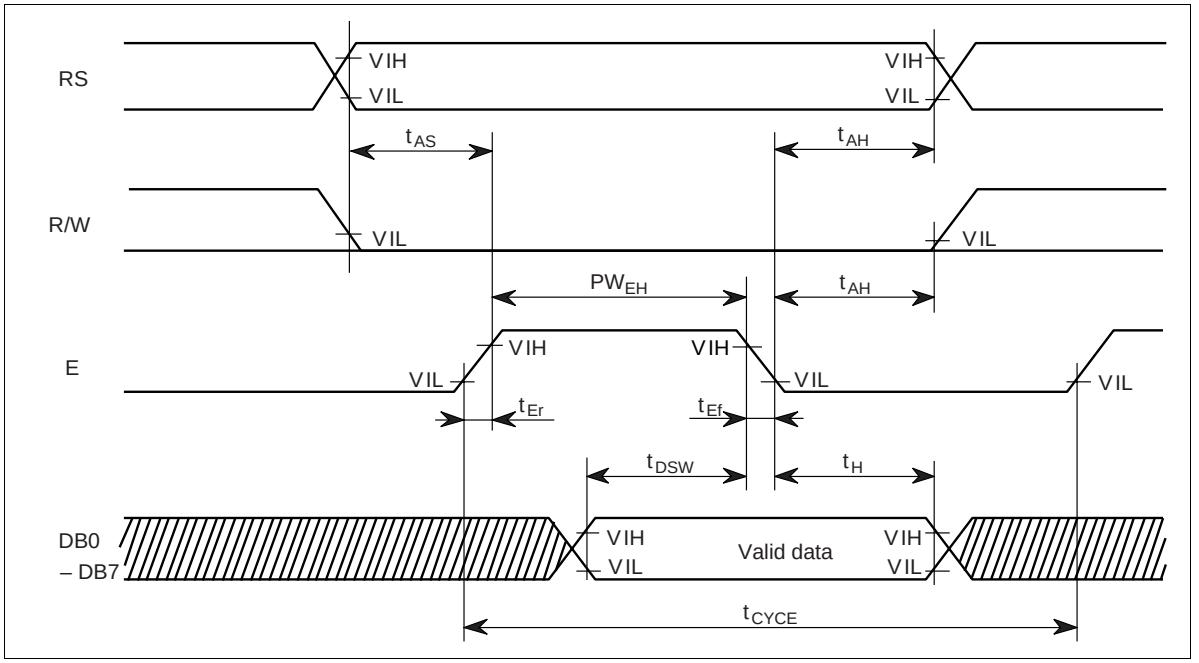


Figure 52 Bus Write Operation

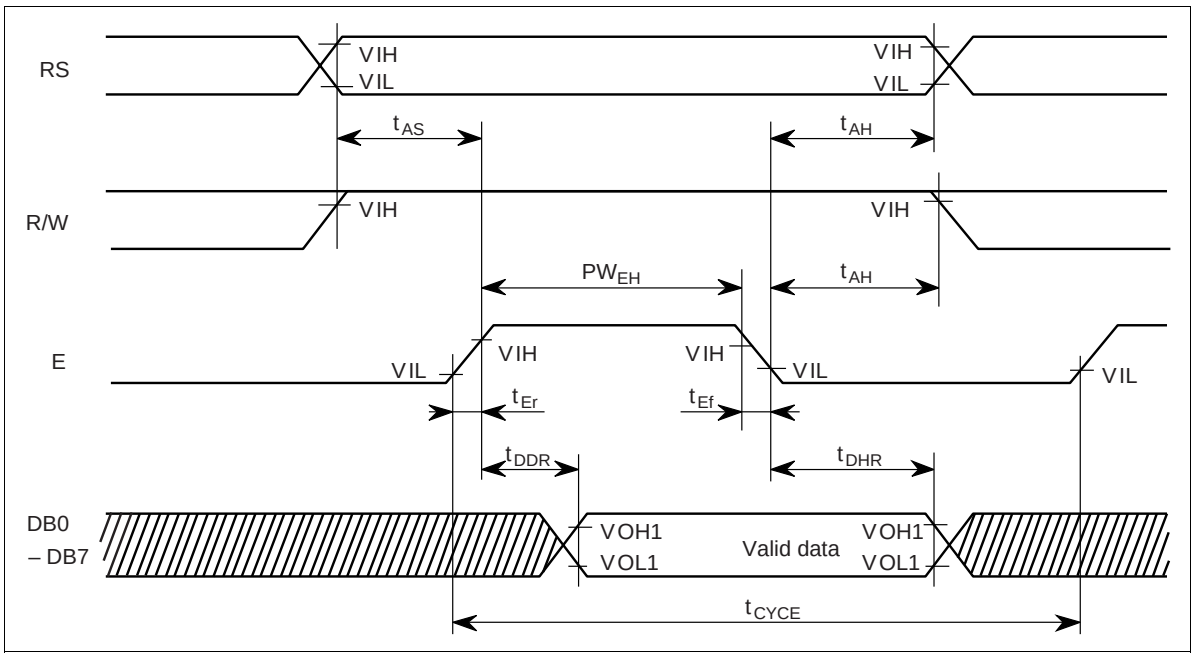


Figure 53 Bus Read Operation

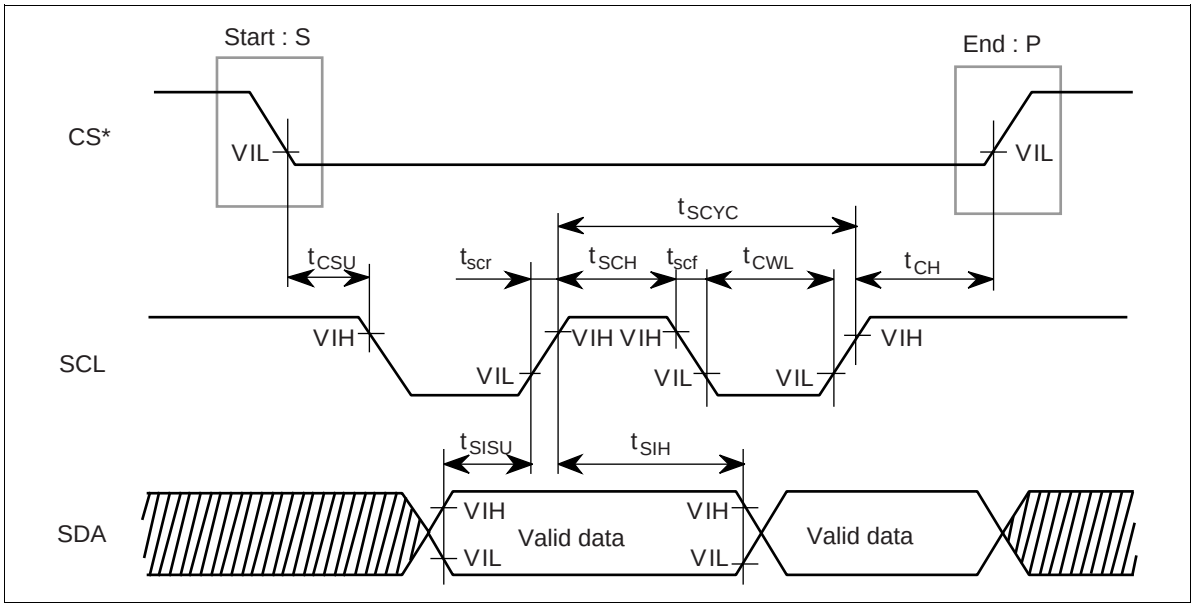


Figure 54 Clock-Synchronized Serial Interface Timing

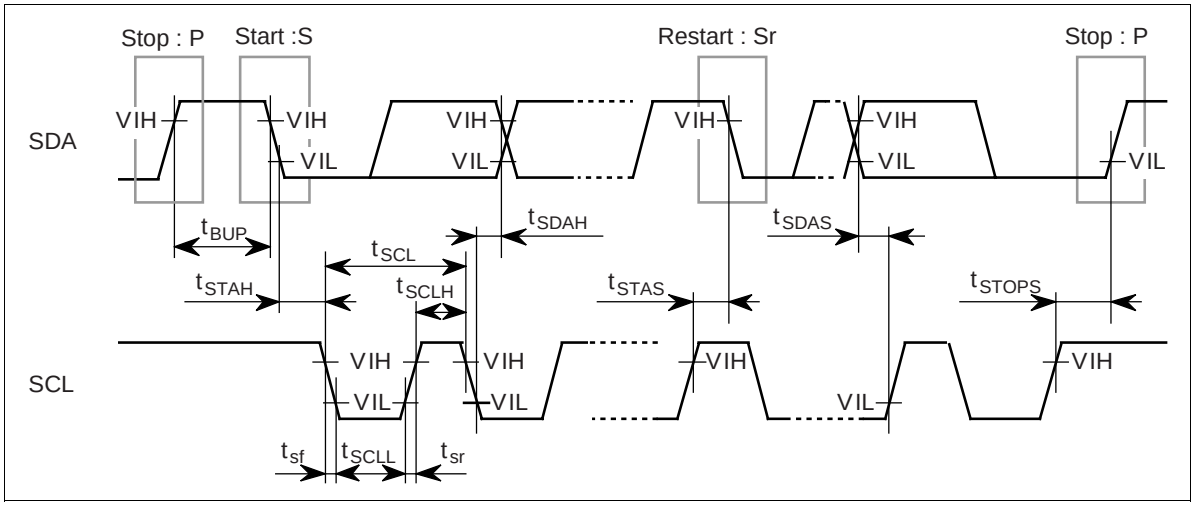


Figure 55 I²C Bus Interface Timing

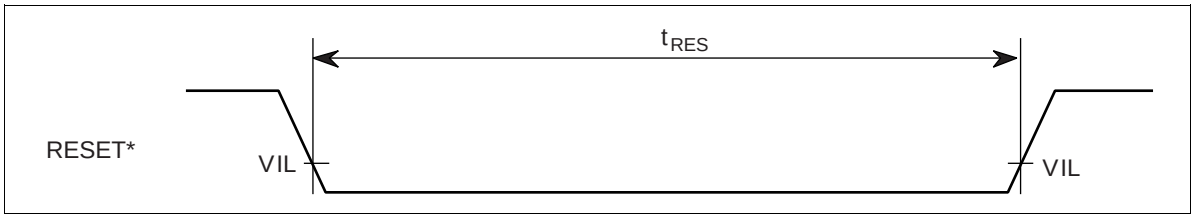


Figure 56 Reset Timing

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