HD66002

(80-Channel General-purpose Driver for Middle- or Small-sized Liquid Crystal Panel)

HITACHI

ADE-207-277(Z)
'99.9
Rev. 0.0

Description

The HD66002 is an 80-channel column driver, which drives a middle-or small-sized liquid crystal panel. This product can be used to expand the display of small portable equipment when connected to LCD-II controllers. In addition, it can be applied to middle-sized dot-matrix liquid crystal displays with sizes such as 128×240 or 128×480 dots.

Features

- Logic power supply voltage: 2.7 to 5.5V
- Display duty: 1/16 (1/5 bias) to 1/128
- 80 liquid crystal display drive circuits
- Liquid crystal display drive voltage: 6 to 17V
- Data transfer speed: 2.5 MHz max
- Serial/parallel conversion function
- Chip enable signal automatic generation
- Controllers that can be used with
  - HD44780U, HD66710, HD66712, HD66720, and HD66730 (LCD-II series)
  - HD61830B (LCDC series)
- Packages
  - FP-100A
  - TFP-100B
  - No package (bare chip)
- CMOS process

Ordering information

Type name	Package
HD66002FS	FP-100A
HD66002TE	TFP-100B
HCD66002	Bare chip

Pin Arrangement

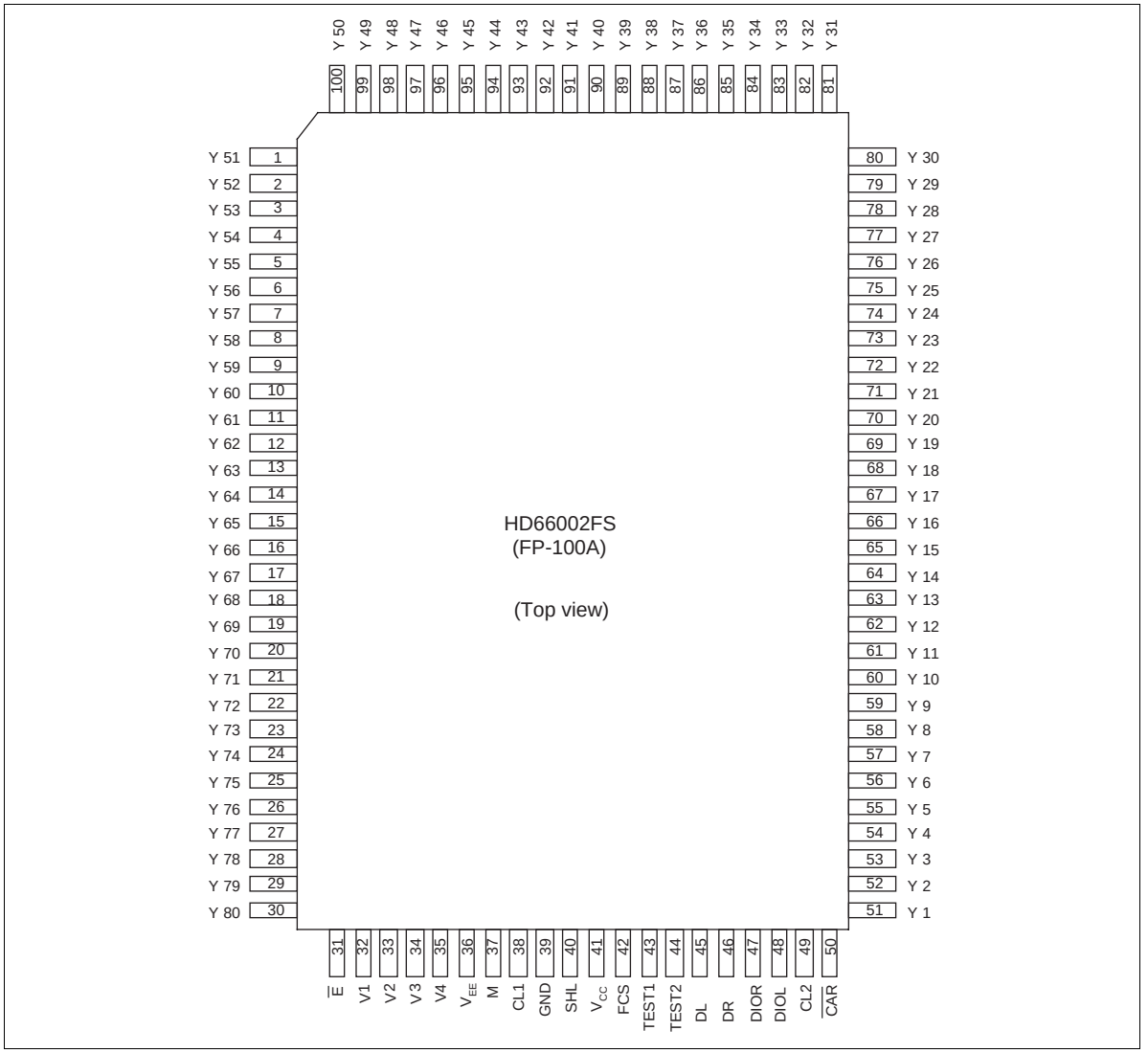

Figure 1 Pin Arrangement (HD66002FS)

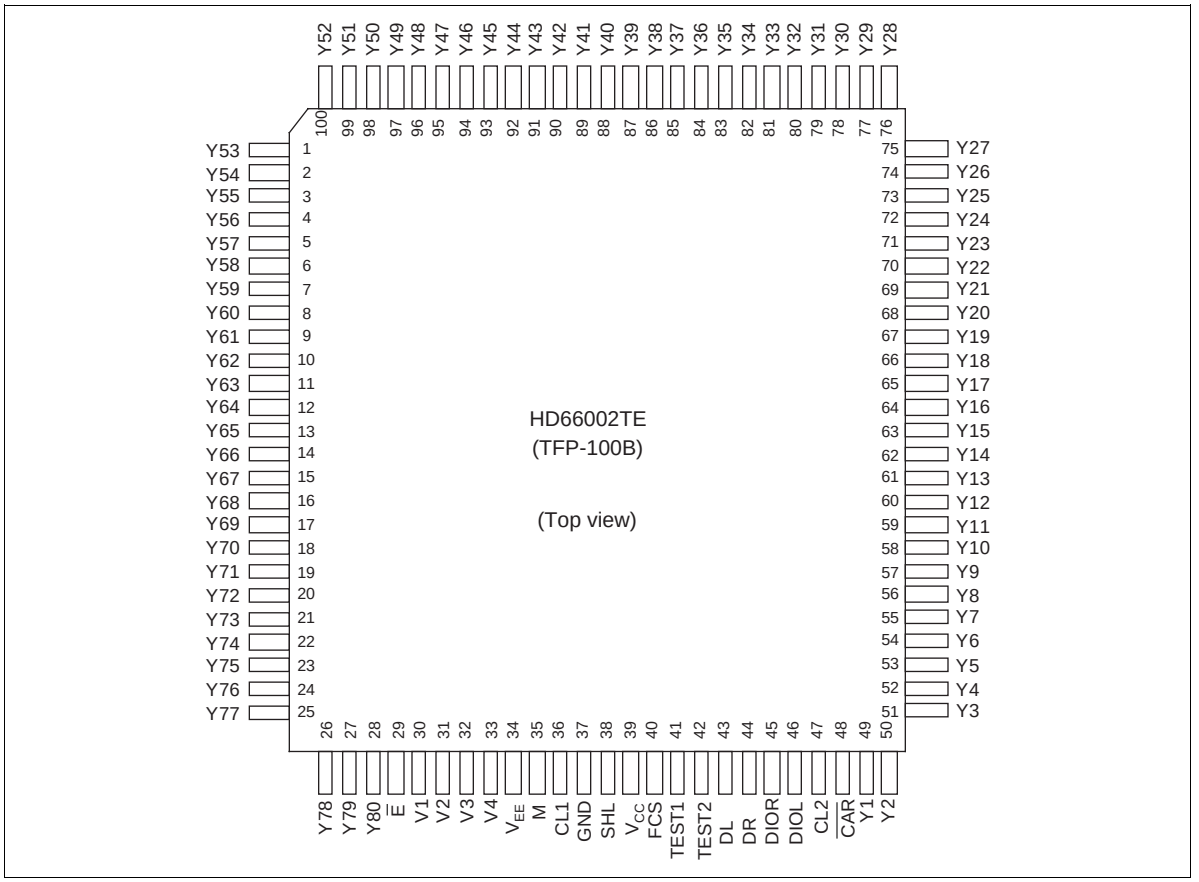

Figure 2 Pin Arrangement (HD66002TE)

Block Diagram

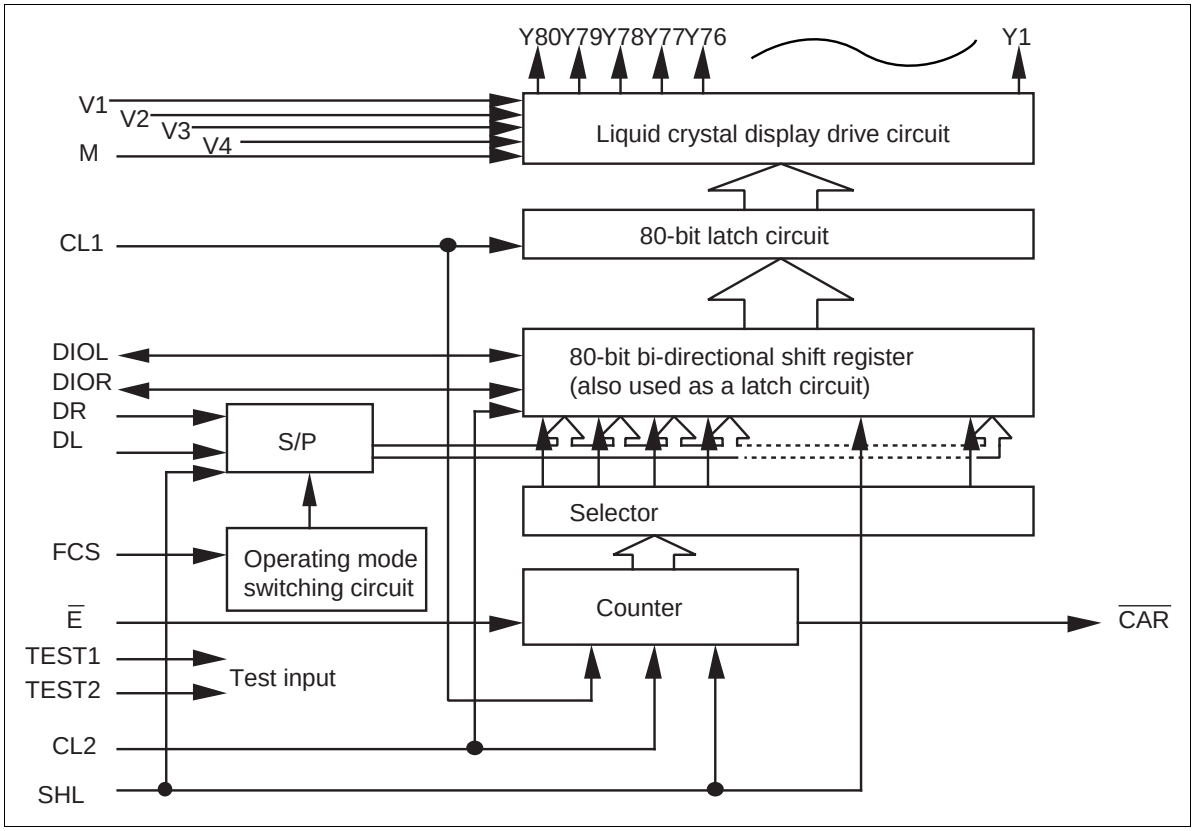

Figure 3 Block Diagram

Block Functions

Liquid crystal display drive circuit

Generates one of four levels V1 to V4 to the output pin to drive the liquid crystal display according to the combination of data of the 80-bit latch circuit and the M signal.

80-bit latch circuit

Latches data of the 80-bit bi-directional shift register (also used as a latch circuit) at the falling edge of CL1, and transmits it to the liquid crystal display drive circuit.

80-bit bi-directional shift register (also used as a latch circuit)

When FCS is low, this register functions as an 80-bit shift register. At this time, DIOL and DIOR are used as data input/output pins. When FCS is high, this register functions as a 20 × 4-bit latch circuit. At this time, data that is input in serial to data input pin DR or DL is converted to 4-bit data, and then is latched to this register according to the latch signal generated by the selector.

S/P

Converts serial data into 4-bit parallel data.

Selector

Decodes output data from the counter and generates a latch signal. Functions when latching data at serial-latch operation (when FCS is high). At this time, after 80 bits of data Y1 to Y80 are completely latched, the operation of the selector terminates. Even if input data changes, data in the latch circuit is maintained.

Operating mode switching circuit

Switches shift register operation (when FCS is low) and serial-latch operation (when FCS is high).

Pin Functions

Table 1 Pin Functions

Classification	Symbol	Pin No.	Pin Name	Input/ Output	Function
Power supply	V_{CC} GND V_{EE}	41 (39) 39 (37) 36 (34)	V_{CC} GND V_{EE}	—	V_{CC}–GND: Logic power supply V_{CC}–V_{EE}: Power supply for driving the liquid crystal display.
	V1 V2 V3 V4	32 (30) 33 (31) 34 (32) 35 (33)	V1 V2 V3 V4	Input	Power supply voltage for liquid crystal display drive level. See Figure 4.
Control signal	CL1	38 (36)	Clock 1	Input	Display data latch signal. Data is latched at the falling edge of this signal.
	CL2	49 (47)	Clock 2	Input	Display data latch and shift signal. This signal is valid at its falling edge.
	M	37 (35)	M	Input	AC conversion signal for liquid crystal display drive output.
	SHL	40 (38)	Shift left	Input	Control signal for inverting data output destination. 1. Operating mode: Serial-latch operation When serial data is input in order from D1 to D80, the relationship between data and output Y are as shown in Table 2. When SHL is low, data is input from the DL pin, and the DR pin is set low. When SHL is high, data is input from the DR pin, and DL pin is set low. 2. Operating mode: Shift register operation When serial data is input in order from D1 to D80, the relationship between data and output Y are as shown in Table 3. When SHL is low, data is input to the DIOL pin, and output from the DIOR pin. When SHL is high, the relationships between DIOL and DIOR are reverse.
	$\overline{E}$	31 (29)	Enable	Input	When FCS is high, data latch starts by setting the $\overline{E}$ signal low. When FCS is low, set the $\overline{E}$ signal high. The relationships between the $\overline{E}$ signal, the FCS signal, and data latch operation are as shown in Table 4.

Pin Functions

Table 1 Pin Functions (cont)

Classification	Symbol	Pin No.	Pin Name	Input/ Output	Function
Control signal	$\overline{CAR}$	50 (48)	Carry	Output	When FCS is high, a chip enable signal is transferred to the next IC from this pin. Connect this pin to the next IC. When FCS is low, open this pin.
	DIOL DIOR	48 (46) 47 (45)	Data I/O (L) Data I/O (R)	Input/ output	In serial-latch operation, DIOL, DIOR, DR, and DL are display data input and open pins. When the SHL pin is high, DL is low and DR is input, and when it is low, DL is input and DR is low. At this time, set the DIOL and DIOR pins low.
	DR DL	46 (44) 45 (43)	Data (R) Data (L)	Input	In shift register operation, DIOL, DIOR, DR, and DL are display data input and output pins. When the SHL pin is high, DIOL and DIOR are output and input, respectively, and vice versa when the SHL pin is low. At this time, set the DR and DL pins low. When display data is high, liquid crystal display drive output is selection level and the liquid crystal display is on, and when display data is low, they are non-selection and off, respectively.
	FCS	42 (40)	Function select	Input	Control signal to select each operating mode. When the FCS pin is low, the operating mode is shift register, and when it is high, the operating mode is serial latch.
	TEST1 TEST2	43 (41) 44 (42)	Test 1 Test 2	Input	Test pins. Set these pins high.
Liquid crystal display drive output	Y1 to Y80	51 to 100 (49 to 100) 1 to 30 (1 to 28)	Y1 to Y80	Output	Each Y pins outputs one of the four voltage levels V1, V2, V3, or V4 according to the combination of M and display data. The combination is differently between serial latch operation and shift register operation. See Figure 5. In case of using at display expanse of LCD-II family, use in shift register operation (FCS = L).

Note: Pin numbers of the HD66002TE are enclosed in parentheses ( ).

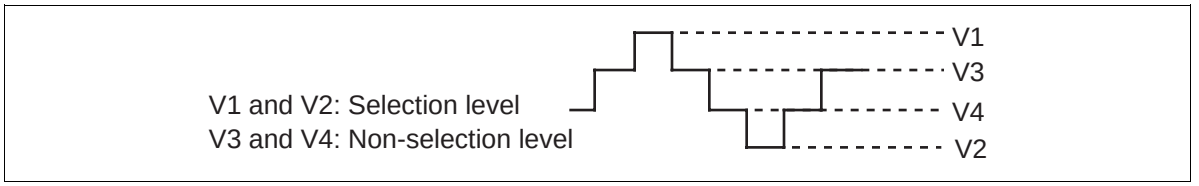

Figure 4 Liquid Crystal Display Drive level

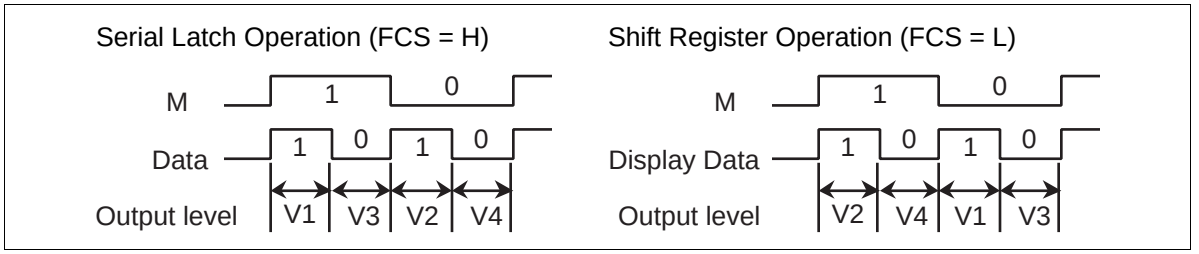

Figure 5 Liquid Crystal Display Drive Output

Table 2 Relationship between Data and Output Y in Serial-Latch Operation

SHL	Y1	Y2	.....	Y79	Y80
Low	D1	D2	.....	D79	D80
High	D80	D79	.....	D2	D1

Table 3 Relationship between Data and Output Y in Shift Register Operation

SHL	Y1	Y2	.....	Y79	Y80
Low	D80	D79	.....	D2	D1
High	D1	D2	.....	D79	D80

Table 4 Relationship between FCS, $\overline{E}$, and Data Latch Operation

FCS	$\overline{E}$	Data Latch Operation
High	Low	Enabled
	High	Disabled
Low	High	—

Application Examples

Example 1 (Shift Register Operating Mode 1)

Figure 6 shows an example when configuring the 16 × 200-dot LCD panel using the HD66002 (when using the HD44780U as a controller).

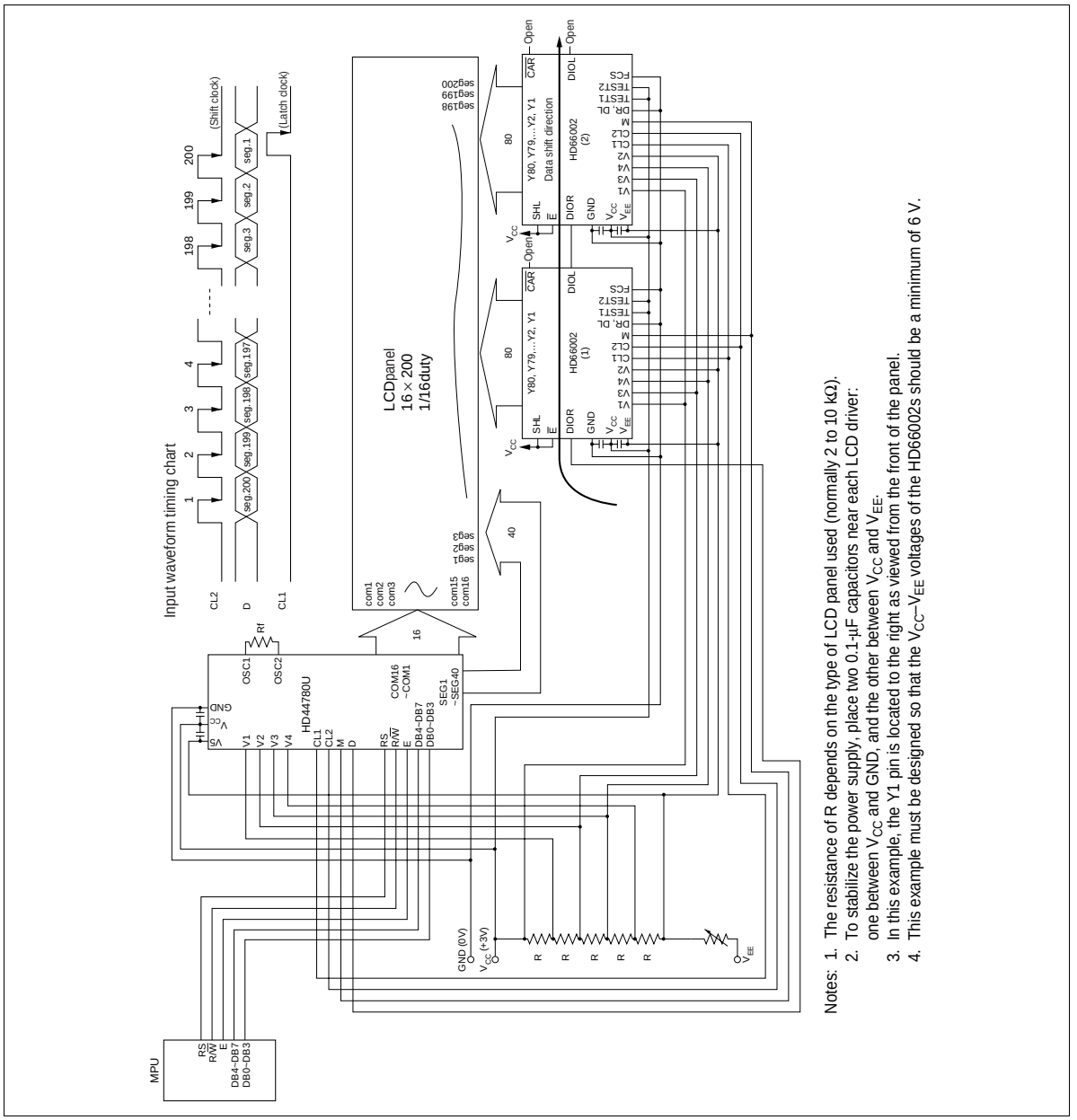

Figure 6 Application Example 1 (Shift Register Operating Mode 1)

Example 2 (Shift Register Operating Mode 2)

Figure 7 shows an example when configuring the 228 × 25-dot LCD panel using the HD66002 (when using the HD66730 as a controller).

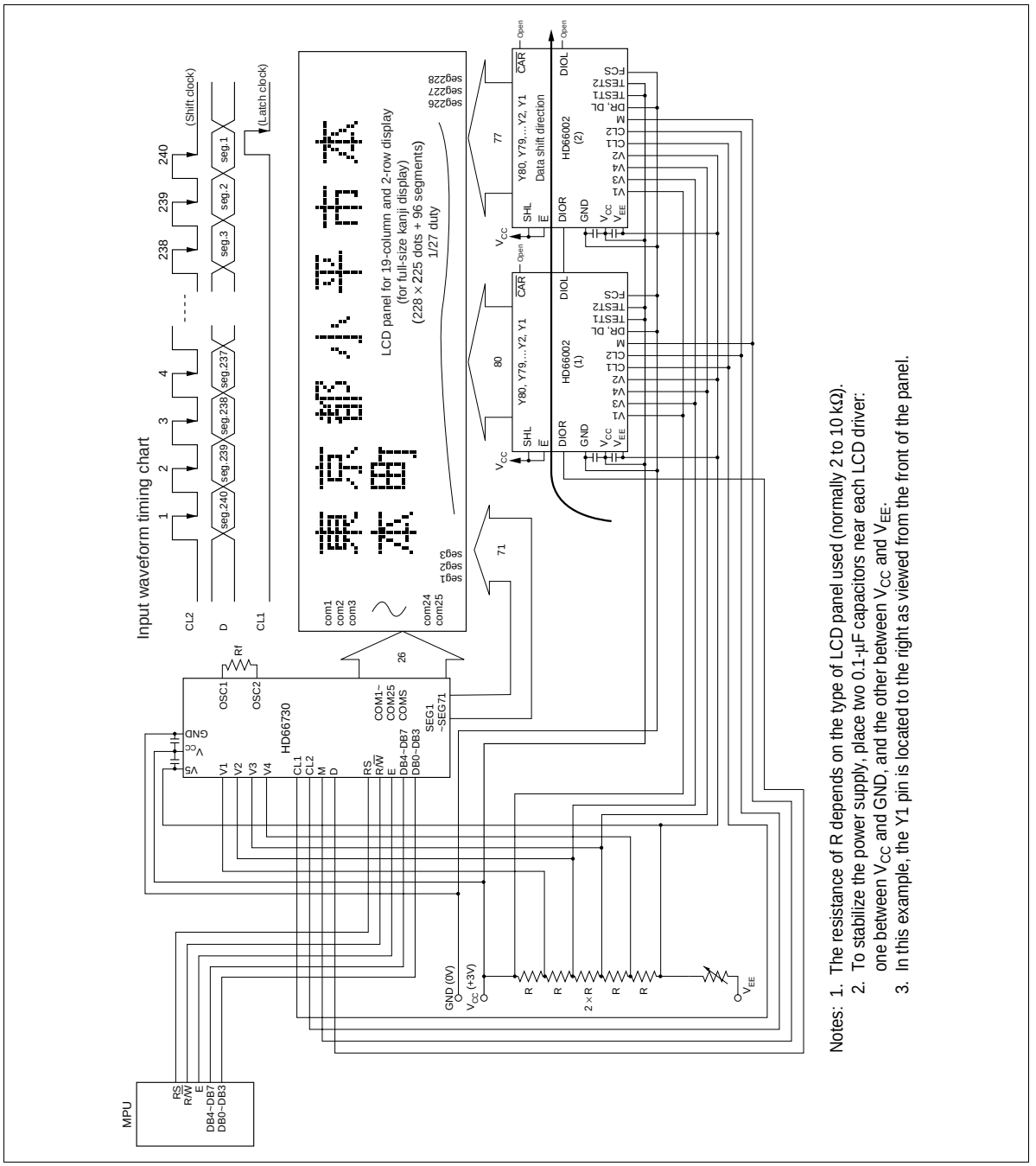

Figure 7 Application Example 2 (Shift Register Operating Mode 2)

Example 3 (Serial-Latch Operating Mode)

Figure 8 shows an example when configuring the 64 × 240-dot LCD panel using the HD66002 (when using the HD61203U as a common driver).

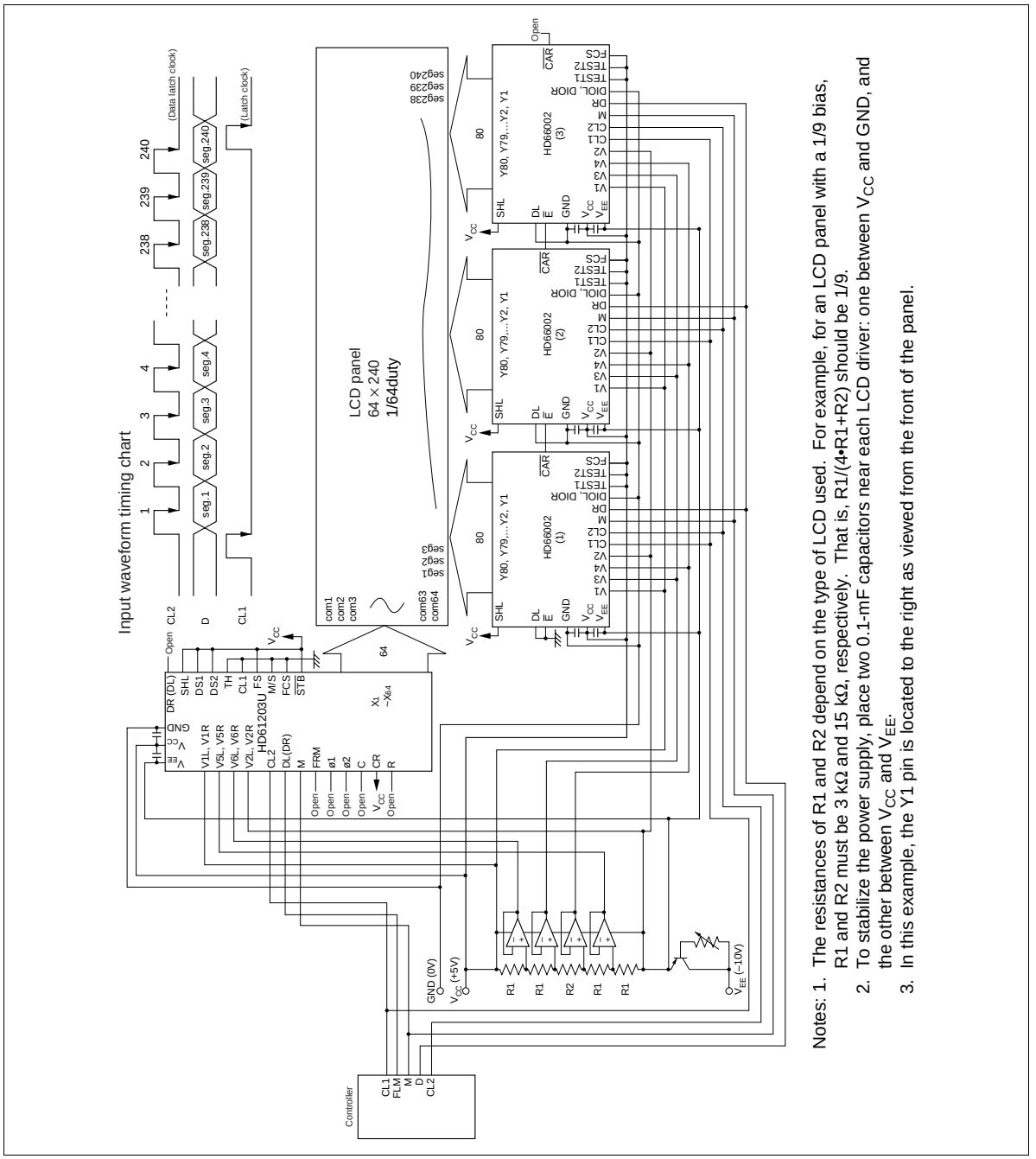

Figure 8 Application Example (Serial-Latch Operating Mode)

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Note
Power supply voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	Liquid crystal display drive circuit	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	
Input voltage (1)		VT1	–0.3 to V_{CC} + 0.3	V	1 and 2
Input voltage (2)		VT2	V_{EE} – 0.3 to V_{CC} + 0.3	V	1 and 3
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

Notes: 1. Measured relative to GND (0V).
2. Applies to CL1, CL2, M, SHL, $\overline{E}$, DIOL, DIOR, DR, DL, TEST1, TEST2, and FCS pins.
3. Applies to V1 to V4 pins.
4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.7 to 5.5V, GND = 0V, $V_{CC} - V_{EE}$ = 6 to 17V, and Ta = –20 to 75 °C, unless otherwise stated)

Item	Symbol	Applicable Pin	Min.	Typ.	Max.	Unit	Conditions	Note
Input high level voltage	VIH	CL1, CL2, M, SHL, $\overline{E}$, DIOL, DIOR, DR, DL, FCS, TEST1, and TEST2	$0.8 \times V_{CC}$	—	V_{CC}	V	V_{CC} = 2.7 to 4.5V	
			$0.7 \times V_{CC}$	—			V_{CC} = 4.5 to 5.5V	
Input low level voltage	VIL		0	—	$0.2 \times V_{CC}$		V_{CC} = 2.7 to 4.5V	
					$0.3 \times V_{CC}$		V_{CC} = 4.5 to 5.5V	
Output high level voltage	VOH	$\overline{CAR}$, DIOL, and DIOR	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low level voltage	VOL	$\overline{CAR}$, DIOL, and DIOR	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi-Yj on resistance	R_{ON1}	Y1 to Y80, and V1 to V4	—	—	20	kΩ	I_{ON} = 50 µA $V_{CC} - V_{EE}$ = 6 to 8V	1
	R_{ON2}		—	—	7.5	kΩ	I_{ON} = 100 µA $V_{CC} - V_{EE}$ = 8 to 17V	1
Input leakage current (1)	I_{IL1}	CL1, CL2, M, SHL, $\overline{E}$, DIOL, DIOR, DR, DL, FCS, TEST1, and TEST2	–5	—	5	µA	VIN = V_{CC}–GND	
Input leakage current (2)	I_{IL2}	V1 to V4	–25	—	25	µA	VIN = V_{CC}–V_{EE}	
Consumption current (1)	I_{GND1}	—	—	—	1.0	mA	f_{CL2} = 2.5 MHz f_{CL1} = 4.48 kHz f_M = 35 Hz V_{CC} = 3V $V_{CC} - V_{EE}$ = 17V FCS = high	2 and 3
Consumption current (2)	I_{EE1}	—	—	—	100	µA		2 and 3
Consumption current (3)	I_{GND2}	—	—	—	500	µA	f_{CL2} = 400 kHz f_{CL1} = 1 kHz V_{CC} = 3V $V_{CC} - V_{EE}$ = 13V FCS = low	2 and 4
Consumption current (4)	I_{EE2}	—	—	—	20	µA		2 and 4

Notes: 1. Indicates the resistance between one pin from Y1 to Y80 and another pin from V pins V1 to V4 (Figure 9), when a load current is applied to the Y pin; defined under the following conditions:
$V_{CC} - V_{EE}$ = 6 to 8V
V1 and V3 = V_{CC} – 2/5 ($V_{CC} - V_{EE}$)
V4 and V2 = V_{EE} + 2/5 ($V_{CC} - V_{EE}$)

V_{CC}–V_{EE} = 8 to 17V

V1 and V3 = V_{CC} – 2/7 (V_{CC} – V_{EE})

V4 and V2 = V_{EE} + 2/7 (V_{CC} – V_{EE})

V1 and V3 should be near the V_{CC} level, and V4 and V2 should be near the V_{EE} level. All these voltage pairs should be separated by less than Δ V, which is the range within which RON, the LCD drive circuits' output impedance, is stable. Note that Δ V depends on power supply voltage V_{CC} – V_{EE}. See Figure 10.

2. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, VIH and VIL must be held to V_{CC} and GND levels, respectively.
3. Applies to serial-latch operation.
4. Applies to shift register operation.

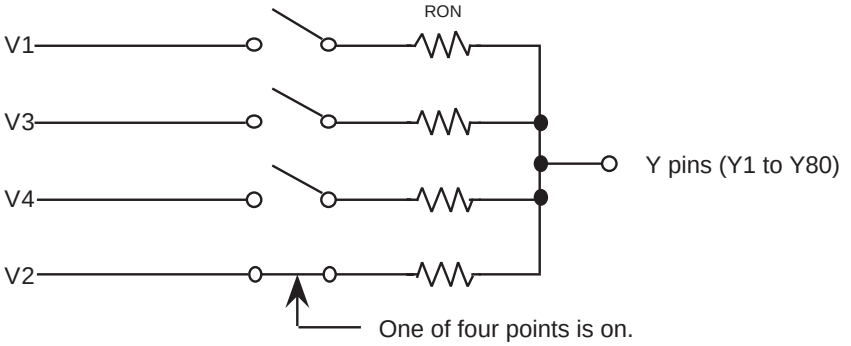

Figure 9 RON Resistance

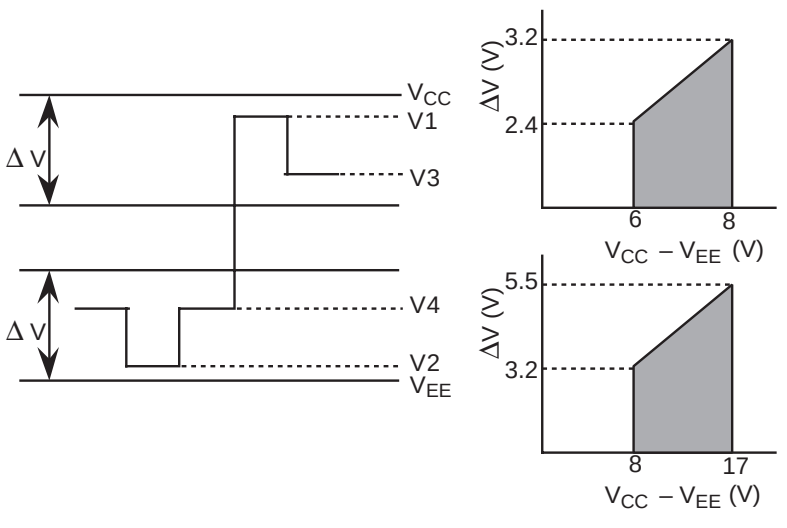

Figure 10 Relationship between Driver Output Waveform and Level Voltages

Pin Configuration

Each pin configuration is shown below.

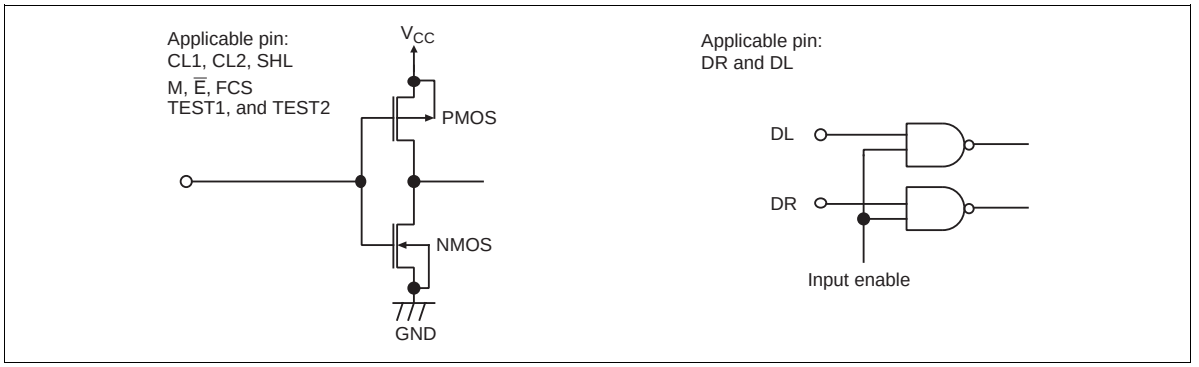

Figure 11 Input Pin Configuration

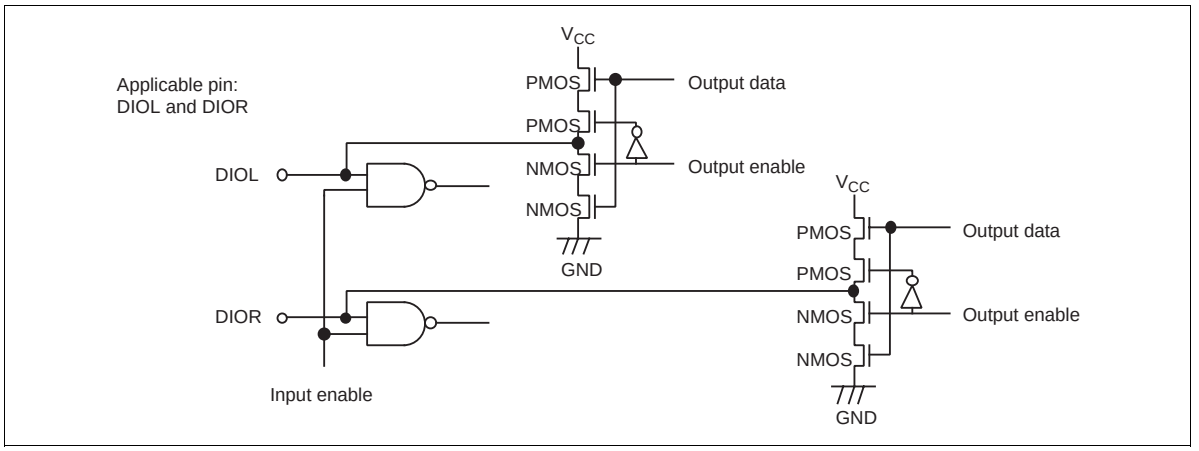

Figure 12 Input/Output Pin Configuration

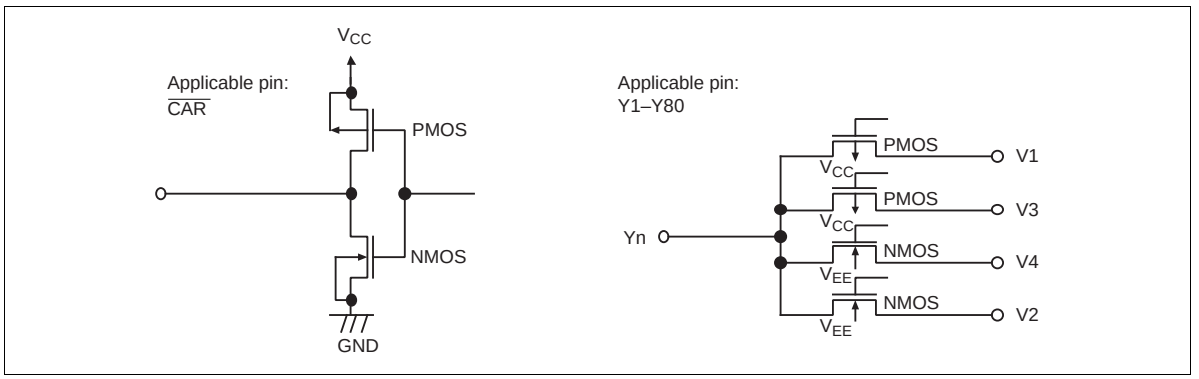

Figure 13 Output Pin Configuration

AC Characteristics 1 (In Serial-Latch Operation, FCS = V_{CC}) (V_{CC} = 2.7 to 5.5V, GND = 0V, $V_{CC} - V_{EE}$ = 8 to 17V, and Ta = –20 to +75 ° C, unless otherwise stated)

Item	Symbol	Applicable Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	400	—	ns	
Clock high level width	t_{CWH}	CL2 and CL1	150	—	ns	
Clock low level width	t_{CWL}	CL2	150	—	ns	
Clock setup time	t_{SCL}	CL1 and CL2	100	—	ns	
Clock hold time	t_{HCL}	CL1 and CL2	100	—	ns	
Clock rise and fall time	t_{ct}	CL1 and CL2	—	30	ns	
Clock phase difference	t_{CL}	CL1 and CL2	100	—	ns	
Data setup time	t_{DSU}	DR, DL and CL2	80	—	ns	
Data hold time	t_{DH}	DR, DL, and CL2	100	—	ns	
Enable setup time	t_{ESU}	$\overline{E}$ and CL2	200	—	ns	
Output delay time	t_{DCAR}	$\overline{CAR}$, CL2, CL1	—	300	ns	1
M phase difference	t_{CM}	M and CL1	—	300	ns	

Note: Defined by connecting the load circuit shown in Figure 14.

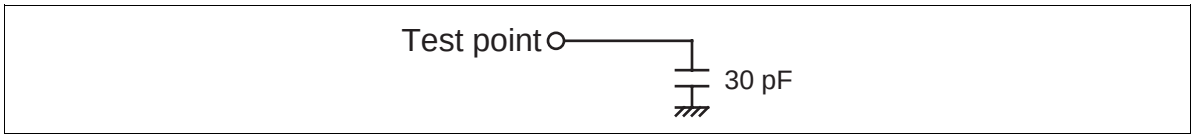

Figure 14 Load Circuit

AC Characteristics 2 (In Shift Register Operation, FCS = GND) (V_{CC} = 2.7 to 5.5V, GND = 0V, $V_{CC} - V_{EE}$ = 6 to 13V, and Ta = –20 to +75 ° C, unless otherwise stated)

Item	Symbol	Applicable pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	2.5	—	µs	
Clock high level width	t_{CWH}	CL2 and CL1	800	—	ns	
Clock low level width	t_{CWL}	CL2	800	—	ns	
Data setup time	t_{SU}	DIOL and DIOR	300	—	ns	
Data hold time	t_{DH}	DIOL and DIOR	300	—	ns	
Clock setup time	t_{SL}	CL1and CL2	500	—	ns	1
Clock setup time	t_{LS}	CL1and CL2	500	—	ns	2
Output delay time	t_{pd}	DIOL and DIOR	—	500	ns	3
Clock rise and fall time	t_{ct}	CL1and CL2	—	200	ns	

Notes: 1. Setup time from CL2 fall to CL1 fall.
2. Setup time from CL1 fall to CL2 fall
3. Defined by connecting the load circuit shown in Figure 15.

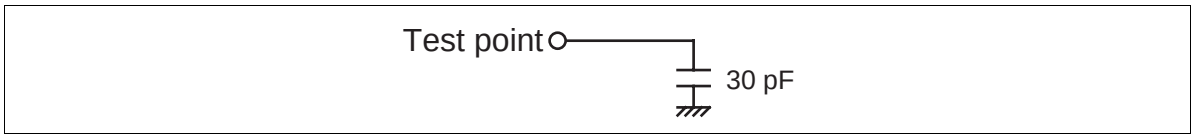

Figure 15 Load Circuit

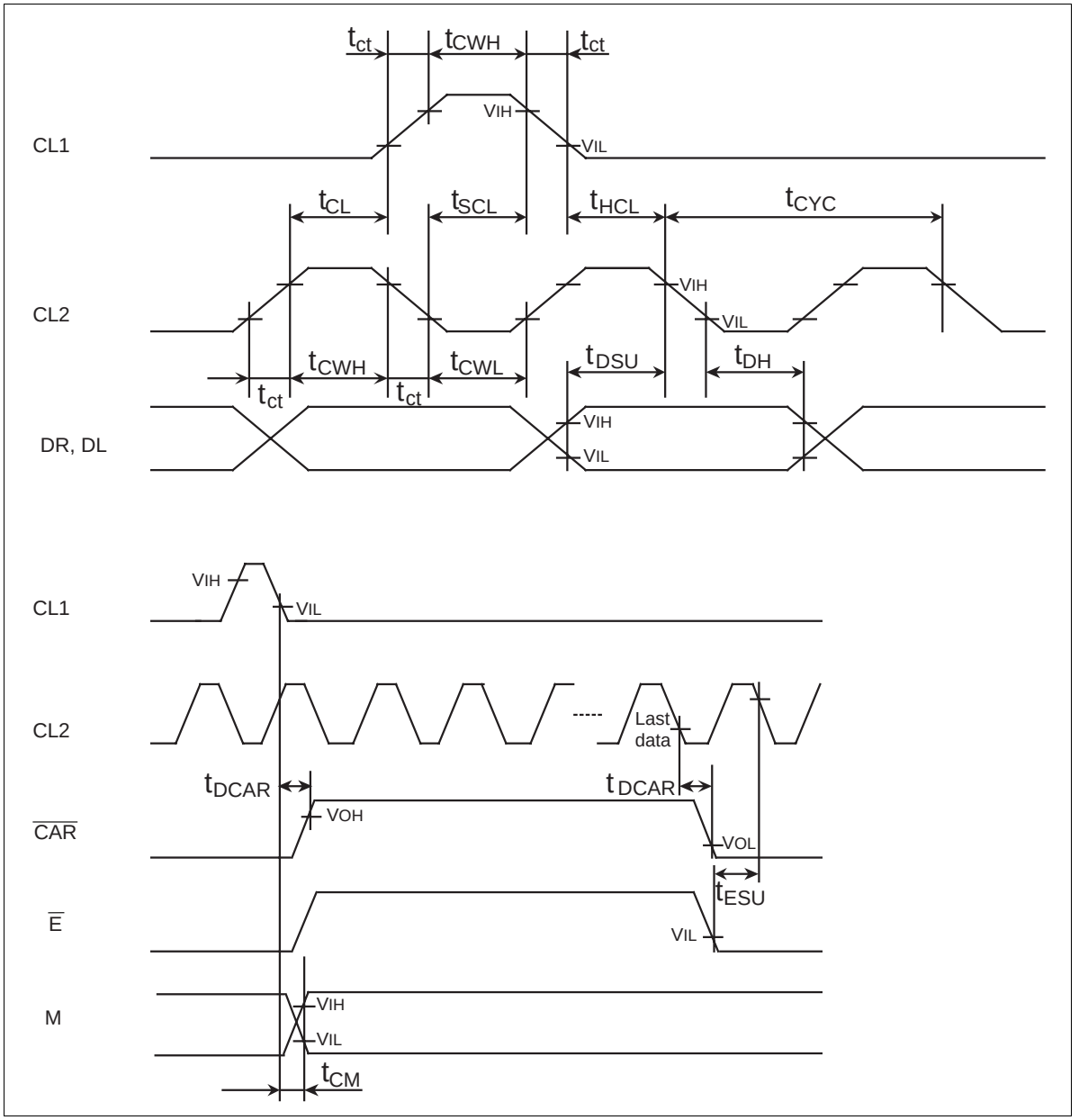

Figure 16 Serial-Latch Operation Timing

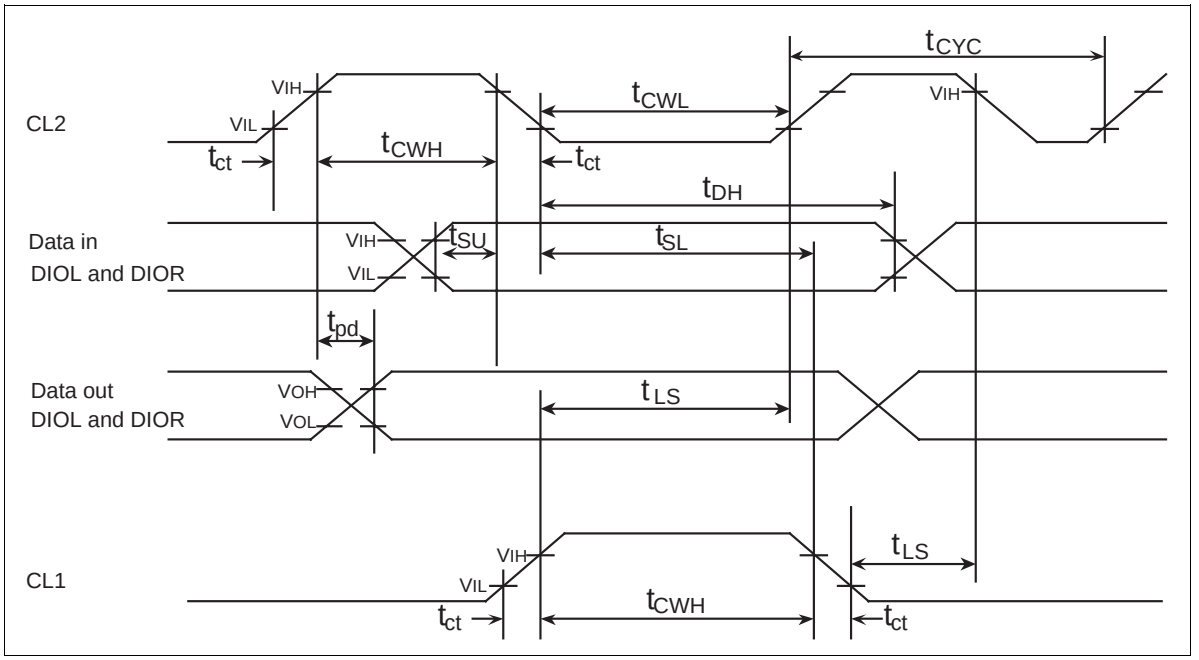

Figure 17 Shift Register Operation Timing

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