

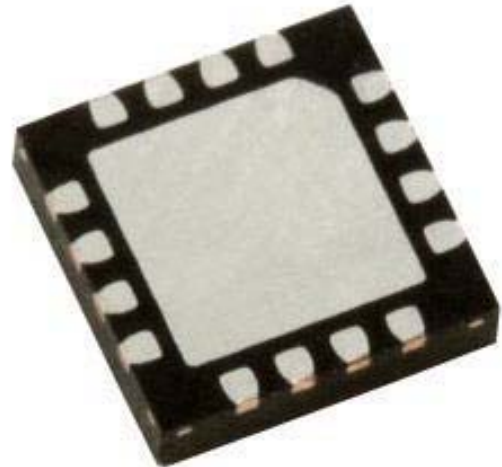
15.5 dB, DC-4GHz, 5 Bit Serial Digital Attenuator

Features

- Very Low DC Power Consumption
- Attenuation In Steps From 0.5 dB To 15.5 dB
- Single Or Dual Power Supply Voltages
- Serial Data Interface
- 50 Ohm Compatible Impedance
- Space Saving LPCC™ Surface Mount Packaging

Product Description

The Honeywell HRF-AT4511 is a 5-bit digital attenuator that is ideal for use in broadband communication system applications that require accuracy, speed and low power consumption. The HRF-AT4511 is manufactured with Honeywell's patented Silicon On Insulator (SOI) CMOS manufacturing technology, which provides the performance of GaAs with the economy and integration capabilities of conventional CMOS.



HRF-AT4511 in LPCC™ Package

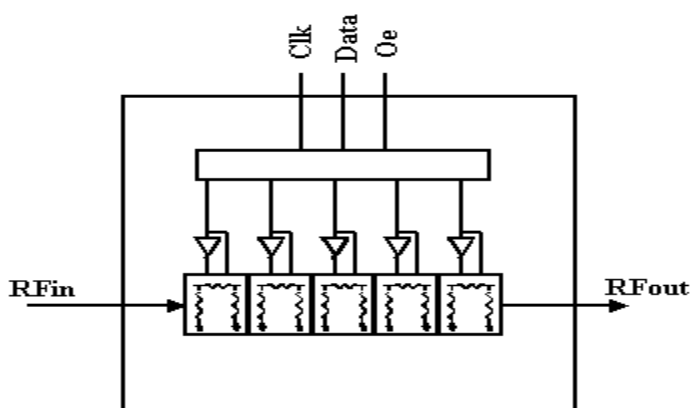
RF Electrical Specifications @ + 25°C

Parameter	Test Condition	Frequency	Minimum	Typical	Maximum	Units
Insertion Loss		DC – 0.5 GHz		1.60	1.80	dB
		2.0 GHz		2.00	2.10	dB
		3.0 GHz		2.20	2.40	dB
		4.0 GHz		3.60	3.80	dB
1dB Compression	VSS = 0V, Input Power	1.0 GHz		23.0		dBm
		2.0 GHz		21.5		dBm
1dB Compression	VSS = - 3, Input Power	1.0 GHz		29.0		dBm
		2.0 GHz		28.0		dBm
Input IP3	VSS = 0V Two-tone inputs Up To +5 dBm @ 0 dBm Attenuation	2.0 GHz		35.5		dBm
Input IP3	V _{ss} = - 3 Two-tone inputs Up To + 5 dBm @ 0 dBm Attenuation	2.0 GHz		37.0		dBm
Return Loss*	Any Bit or Combination of Bits	DC - 4.0 GHz	-11	-15		dB
Attenuation Accuracy	All attenuation states	1.0 GHz	+/- (0.17 + 3% of programmed IL)			dB
	All attenuation states	2.0 GHz	+/- (0.22 + 3% of programmed IL)			dB
	All attenuation states	3.0 GHz	+/- (0.33 + 3% of programmed IL)			dB
	All attenuation states	4.0 GHz	+/- (0.45 + 3% of programmed IL)			dB
Trise, Tfall*	10% To 90%			10		nS
Ton, Toff (Tpd)	50% Cntl To 90%/10%RF			15		nS
Transients	In-Band			30		mV
T clock Period (Tprd)*	T high / T low = ½ minimum clock period		50			nS
T data set up (Tsup)*	Set up to rising edge of clock		5			nS
T data hold (Thld)*	Data hold after rising edge of clock		2			nS
T latch set up (Tlsup)*	Data set up to falling edge of OE		5			nS

0.01uF Decoupling Capacitors Required On Power Supply Rails.

*Bv design

Functional Schematic



DC Electrical Specifications @ + 25°C

Parameter	Minimum	Typical	Maximum	Units
V_{DD}	3.3*	5.0		V
V_{SS}			-5.0	V
I_{DD} Power Supply Current			2	mA
CMOS Logic level (0)	0		0.8	V
CMOS Logic level (1)	$V_{DD} - 0.8$		V_{DD}	V
Input Leakage Current			2	uA

* Note, performance curves are for $V_{DD} = +5.0 \pm 10\%$

Absolute Maximum Ratings²

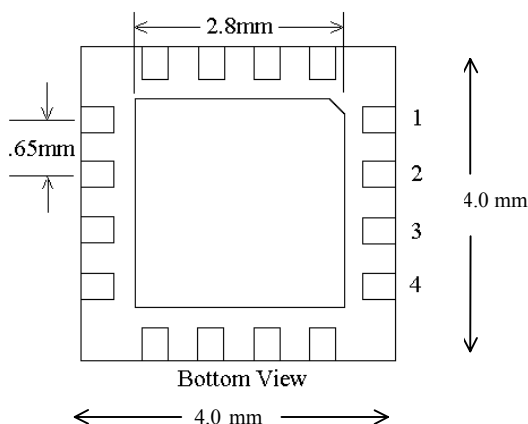
Parameter	Absolute Maximum	Units
Input Power	+ 35	dBm
V_{DD}	+6.0	V
V_{SS}	-5.5	V
ESD Voltage (Control Lines)	2K	V
Operating Temperature	-40 To +85	Degrees C
Storage Temperature	-65 To +125	Degrees C
Digital Inputs	$V_{DD} + 0.6$ max to $V_{SS} - 0.6$ min	V

(Note 2) Operation of this Device beyond any of these parameters may cause permanent damage.

Latch-Up: Unlike conventional CMOS digital attenuators, Honeywell's HRF-AT4511 is immune to latch-up.

ESD Protection: Although the HRF-AT4511 contains ESD protection circuitry on all digital inputs, conventional precautions should be taken to ensure that the Absolute Maximum Ratings are not exceeded.

Package Outline Drawing



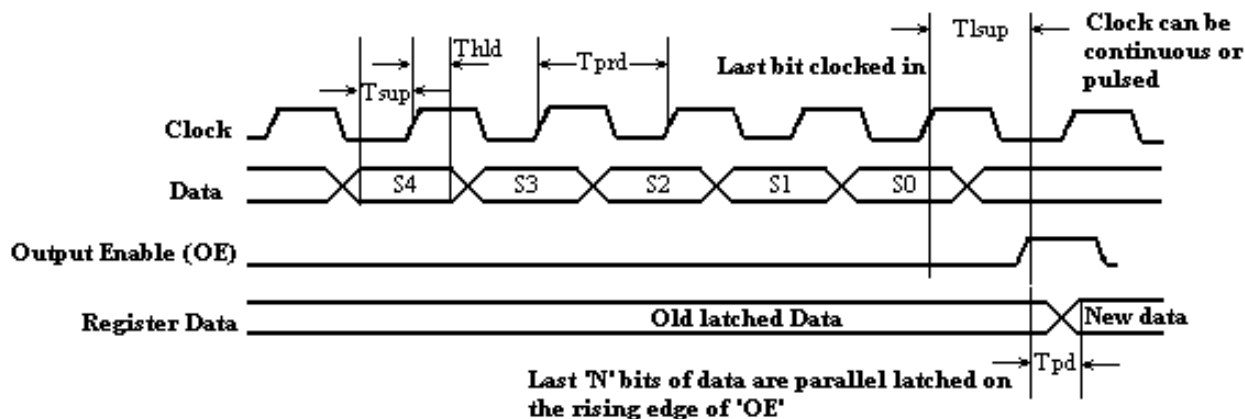
This package conforms to the LPCC™ 4 X 4 mm 16 lead body dimensions. See ASAT LPCC Marketing Outline Dwg. # DGMJ00004 Latest Rev. at <http://www.asat.com> for additional dimensional information.

Pin Configuration

Pin	Function	Pin	Function
1	VDD	9	GROUND
2	GROUND	10	RF OUTPUT
3	RF INPUT	11	GROUND
4	GROUND	12	VSS
5	GROUND	13	DIGITAL GROUND
6	GROUND	14	OE
7	GROUND	15	CLK
8	GROUND	16	DATA

Serial Data Load

Serial data is shifted into the register on the rising edge of clock, MSB first. The state of "OE" will not affect the shifting of data. The rising edge of the "OE" signal will be the clock for the transfer of shifted data. Latched new data occurs one prop delay after the rising edge of "OE". See the Electrical Spec Table for AC parameters.

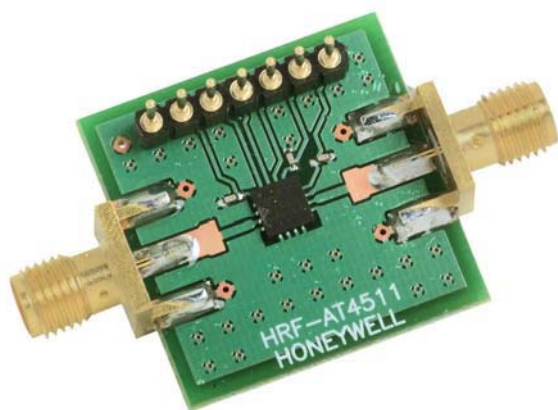


Truth Table

S4	S3	S2	S1	S0	Output
0	0	0	0	0	Reference Input
0	0	0	0	1	0.5 dB
0	0	0	1	0	1 dB
0	0	1	0	0	2 dB
0	1	0	0	0	4 dB
1	0	0	0	0	8 dB
1	1	1	1	1	15.5 dB

Operation: Data on serial input D is clocked into internal registers on the low to high transition of the Clock signal (CK). The register is sampled during the Output Enable (OE) low state and clocked into the register during the low-to-high transition

Evaluation Circuit Board



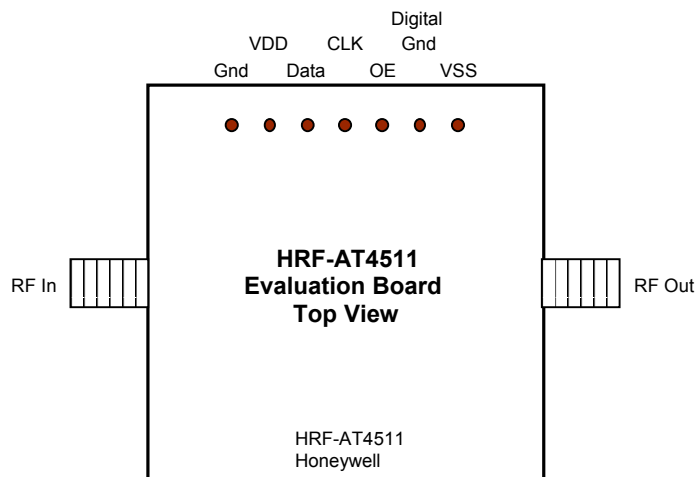
HRF-AT4511 Evaluation Board

Honeywell's evaluation board provides an easy to use method of evaluating the RF performance of our attenuator. Simply connect power, DC and RF signals to be measuring attenuator performance in less than 10 minutes.

Evaluation Circuit Board Layout Design Details

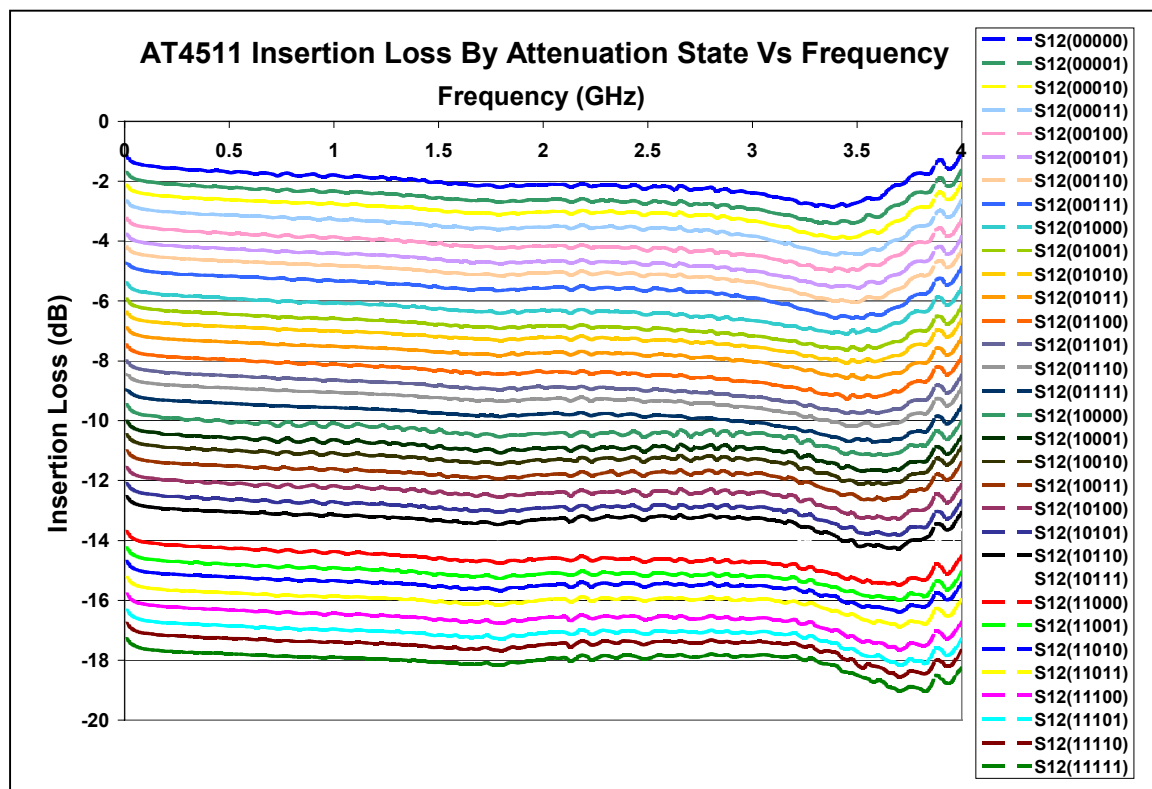
Item	Description
PCB	Impedance Matched Multi-Layer FR4
Attenuator	HRF-AT4511 Digital Attenuator
Chip Capacitor	Panasonic Model ECU-E1C103KBQ Capacitor, .01uf 0402 10% 16V
RF Connector	Johnson Connectors Model 142-0701-801 SMA RF Coaxial Connector
DC Pin	Mil-Max Model 800-10-064-10-001 Header Pins

Evaluation Circuit Board Connections

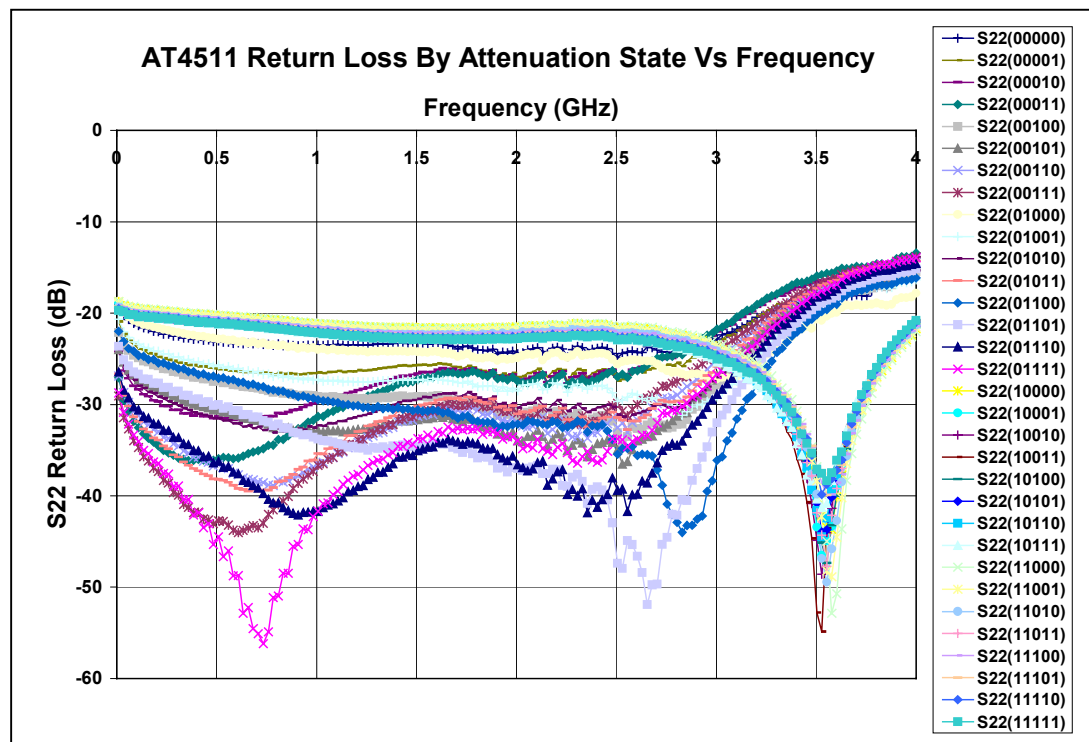
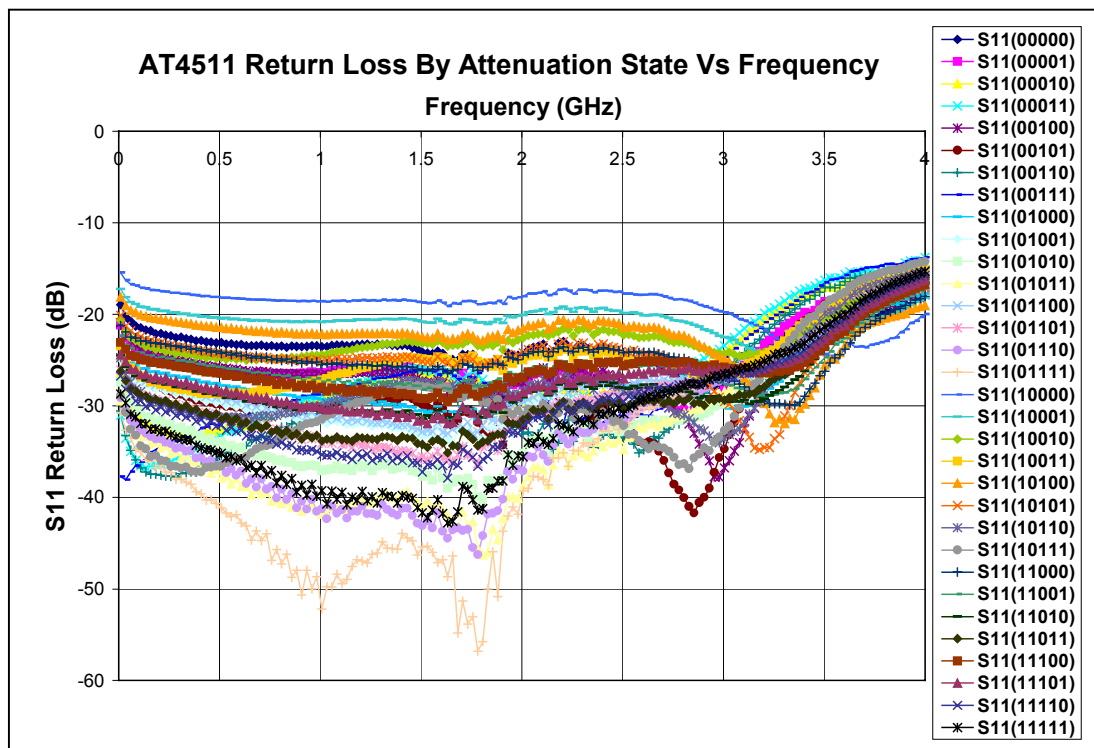


Performance Curves

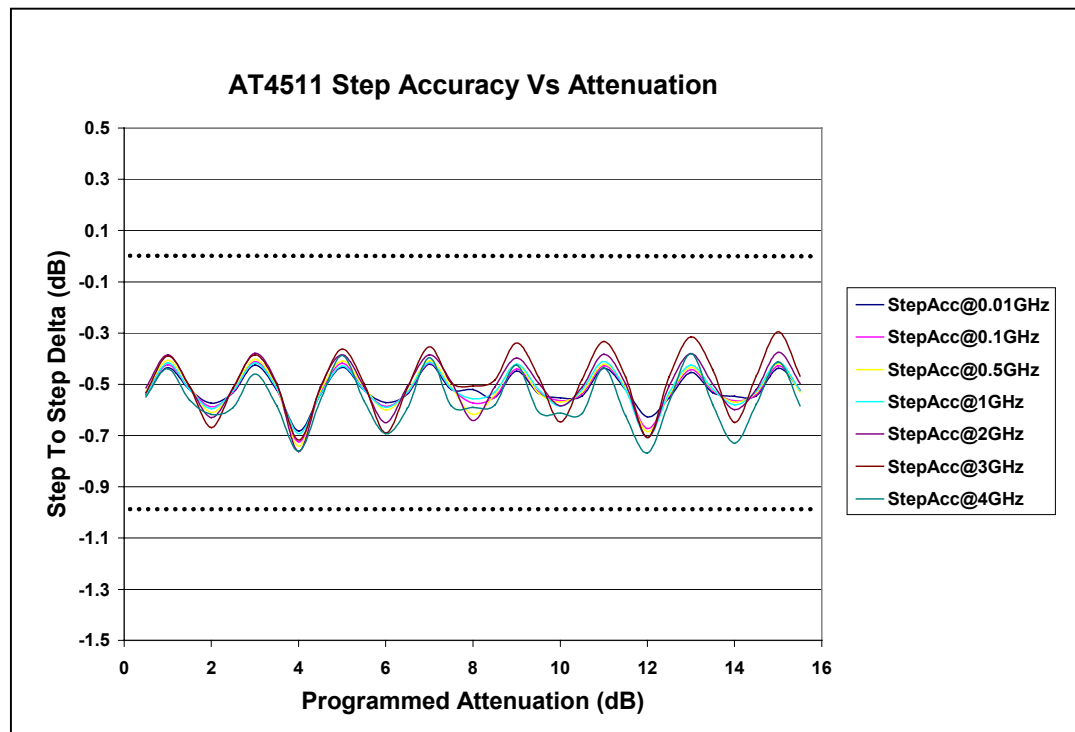
Insertion Loss



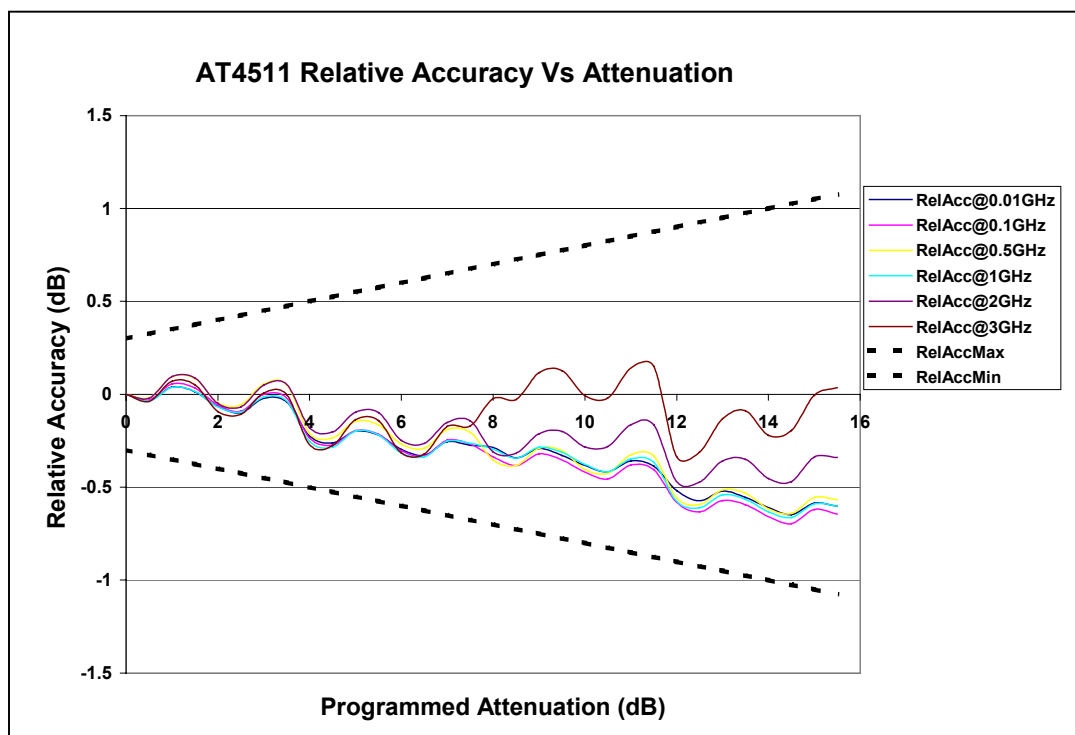
Return Loss



Step Accuracy



Relative Accuracy



Ordering Information

Ordering Number	Delivery Method	Units Per Shipment
HRF-AT4511-B	In Chip Tubes	Customer Specific, Usually Minimum
HRF-AT4511-TR	On Tape And Reel ³	Of 50 Per Chip Tube
HRF-AT4511-E	On Individual Engineering Evaluation Board	3000 Units Per Reel
		One Board Per Box

(Note 3) Call Honeywell for details

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