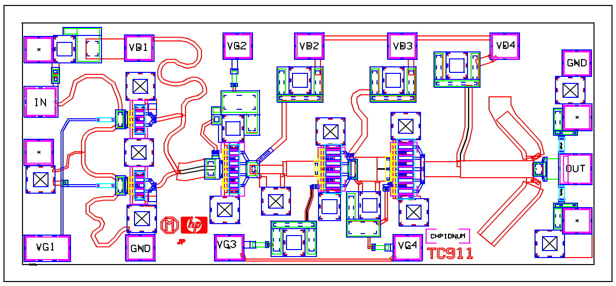
Agilent HMMC-5038
38 GHz LNA

Data Sheet



Chip Size:	1630 × 760 µm (64.2 × 29.9 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	80 × 80 µm (3.1 × 3.1 mils)

Features

- Low Noise Figure: 4.8 dB
- Frequency Range:
  37 - 40 GHz
- High Gain (Adjustable):
  3 v, 120 mA @ 23 dB Gain
  3 v, 80 mA @ 20 dB Gain
- 50Ω Input/Output Matching

Description

The HMMC-5038 MMIC is a high-gain low-noise amplifier (LNA) designed for communication receivers that operate from 37 GHz to 40 GHz. The gain of this four stage LNA can be adjusted by altering the gate bias of the output two, or three, stages while maintaining optimum noise figure bias for the input stage(s). Large FETs provide high power handing capability to avoid power compression. The backside of the chip is both RF and DC ground. This helps simplify the assembly process and reduce assembly related performance variations and costs.

The HMMC-5038 is fabricated using a PHEMT integrated circuit structure that provides good noise and gain performance.

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Min.	Max.	Units
$V_{D1,2\text{-}3\text{-}4}$	Drain Supply Voltages		5	Volts
$V_{G1,2,3\text{-}4}$	Gate Supply Voltages	-3.0	0	Volts
I_{DD}	Total Drain Current		300	mA
P_{in}	RF Input Power		15	dBm
T_{ch}	Channel Temperature[2]		160	°C
T_A	Backside Ambient Temperature	-55	+125	°C
T_{st}	Storage Temperature	-65	+165	°C
T_{max}	Max. Assembly Temperature		310	°C

[1]Absolute maximum ratings for continuous operation unless otherwise noted.
[2]Refer to *DC Specifications / Physical Properties* table for derating information.

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DC Specifications/Physical Properties[1]

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{D1,2\text{-}3\text{-}4}$	Low Noise Drain Supply Operating Voltages	2	3	5	Volts
I_{D1}	First Stage Drain Supply Current (V_{DD} = 3 V, $V_{G1} \cong$ -0.8 V)		22		mA
$I_{D2\text{-}3\text{-}4}$	Drain Supply Current for Stage 2, 3, and 4 Combined (V_{DD} = 3 V, $V_{GG} \cong$ -0.8 V)		98		mA
$V_{G1,2,3\text{-}4}$	Gate Supply Operating Voltages ($I_{DD} \cong$ 120 mA)		-0.8		Volts
V_P	Pinch-off Voltage (V_{DD} = 3 V, $I_{DD} \leq$ 10 mA)	-2	-1.2	-0.8	Volts
$\theta_{ch\text{-}bs}$	Thermal Resistance[2] (Channel-to-Backside at T_{ch} = 160°C)		62		°C/Watt
T_{ch}	Channel Temperature[3] (T_A = 125°C, MTTF > 10^6 hrs, V_{DD} = 3 V, I_{DD} = 120 mA)		150		°C

[1]Backside ambient operating temperature T_A = 25°C unless otherwise noted.
[2]Thermal resistance (°C/Watt) at a channel temperature T(°C) can be *estimated* using the equation:
$\theta(T) \cong 62 \times [T(°C)+273] / [160°C+273]$.
[3]De-rate MTTF by a factor of two for every 8°C above T_{ch}.

RF Specifications

(T_A = 25°C, V_{DD} = 3 V, I_{DD} = 120 mA, Z_0 = 50Ω)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
BW	Operating Bandwidth	37		40	GHz
Gain	Small Signal Gain[1]	20	23		dB
ΔGain	Small Signal Gain Flatness		±0.5		dB
$\Delta S_{21}/\Delta T$	Temperature Coefficient of Gain		-.04		dB/°C
$(RL_{in})_{MIN}$	Minimum Input Return Loss w/o external capacitive matching[2]	8	12		dB
$(RL_{out})_{MIN}$	Minimum Output Return Loss	12	18		dB
Isolation	Reverse Isolation		50		dB
P_{-1dB}	Output Power at 1dB Gain Compression		12		dBm
NF	Noise Figure[3]		4.8	5.5	dB
ΔNF/ΔT	Temperature Coefficient of NF		+.02		dB/°C

[1]Gain may be reduced by biasing for lower I_{DD}. Increasing I_{DD} will increase Gain.
[2]Minimum input return may be improved by approximately 3 dB by including a small capacitive (30 fF) stub on the input transmission line.
[3]Noise Figure may be further reduced by optimizing DC bias conditions.

Applications

The HMMC-5038 low noise amplifier (LNA) is designed for use in digital radio communication systems and point-to-multipoint links that operate within the 37 GHz to 40 GHz frequency band. High gain and low noise temperature make it ideally suited as a front-end gain stage in the receiver. The MMIC solution is a cost effective alternative to hybrid assemblies.

Biasing and Operation

The recommended DC bias condition is with all drains connected to single 3 volt supply and all gates connected to an adjustable negative voltage supply as shown in Figure 6. The gate voltage is adjusted for a total drain supply current of typically 120 mA. Reducing the current in stages 3 and 4 will reduce the overall gain. The gain can be adjusted further by altering the current through stage 2 with little affect on noise figure. Optimum noise figure is realized with V_{D1}= 3 to 4 volts and I_{D1} = 20 to 25 mA.

The second, third, and fourth stage DC drain bias lines are connected internally and therefore require only a single bond wire. An additional bond wire is needed for the first stage DC drain bias, V_{D1}.

The third and fourth stage DC gate bias lines are connected internally. A total of three DC gate bond wires are required: One for V_{G1}, one for V_{G2}, and one for the V_{G3}-to-V_{G4} connection as shown in Figure 6(b).

A DC blocking capacitor is needed in the RF input transmission line only if there is DC voltage present. The RF output is AC-coupled.

Optimum input match is achieved when an optional capacitive (30 fF) stub is included on the input transmission line. This capacitance complements the bond wire inductance to complete the input matching network.

No ground wires are needed because ground connections are made with plated through-holes to the backside of the device.

Assembly Techniques

It is recommended that the RF input and RF output connections be made using either 500 line/inch (or equivalent) gold wire mesh, or dual 0.7 mil diameter gold wire. The RF wires should be kept as short as possible to minimize inductance. The bias supply wires can be a 0.7 mil diameter gold.

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

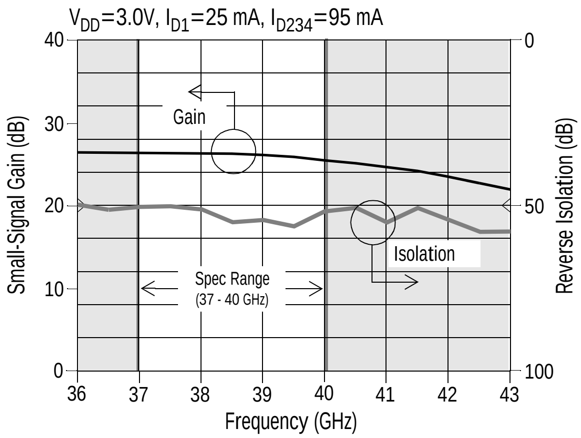


Figure 1.
Gain and Isolation versus Frequency

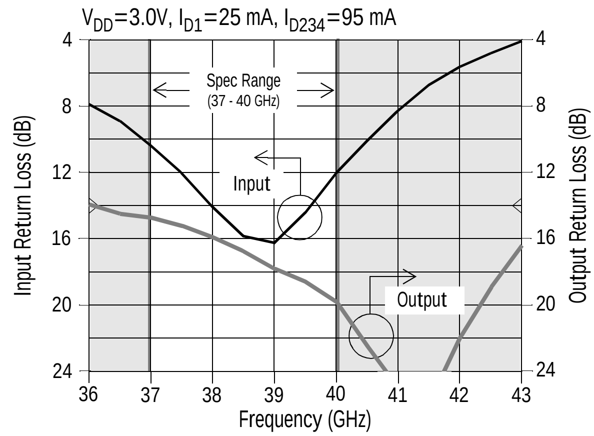


Figure 2.
Input and Output Return Loss versus Frequency

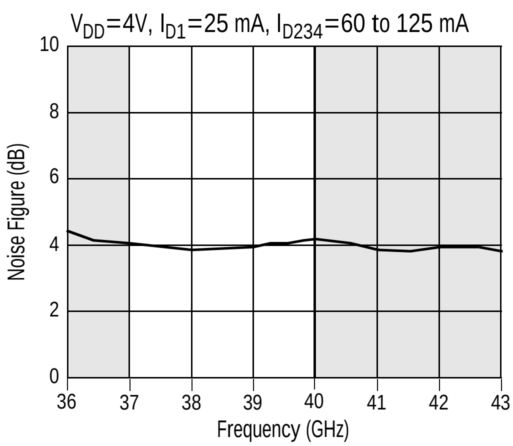


Figure 3.
Noise Figure versus Frequency

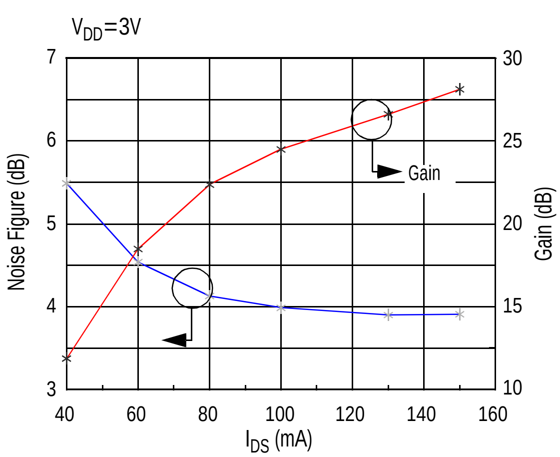


Figure 4.
38 GHz Noise Figure and Gain versus I_{DD}

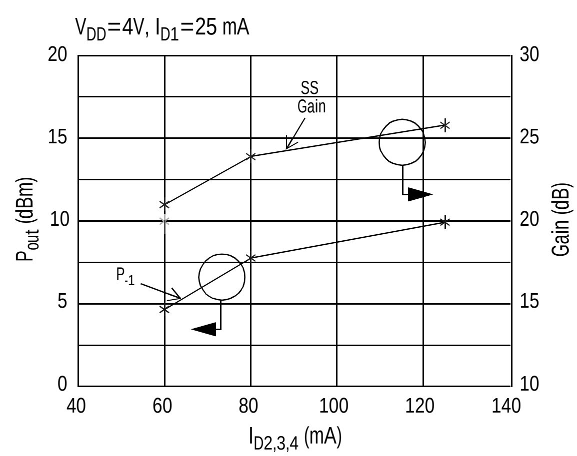
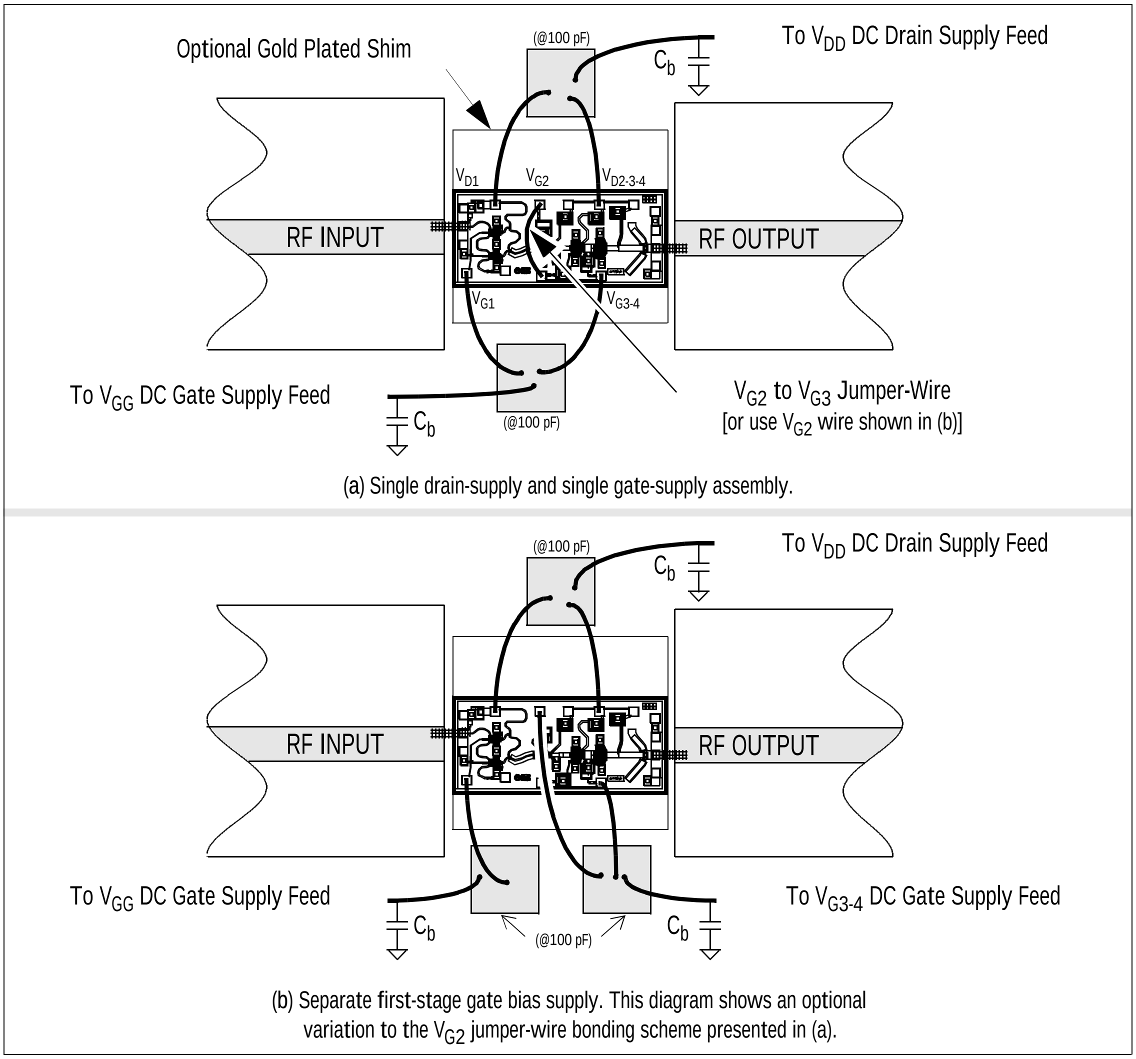


Figure 5.
38 GHz Gain and Power Performance versus I_{DD}



(a) Single drain-supply and single gate-supply assembly.

(b) Separate first-stage gate bias supply. This diagram shows an optional variation to the V_{G2} jumper-wire bonding scheme presented in (a).

Figure 6. Common Assembly Diagrams

(Note: To assure stable operation, bias supply feeds should be bypassed to ground with a capacitor, C_b > 100 nF typical.)

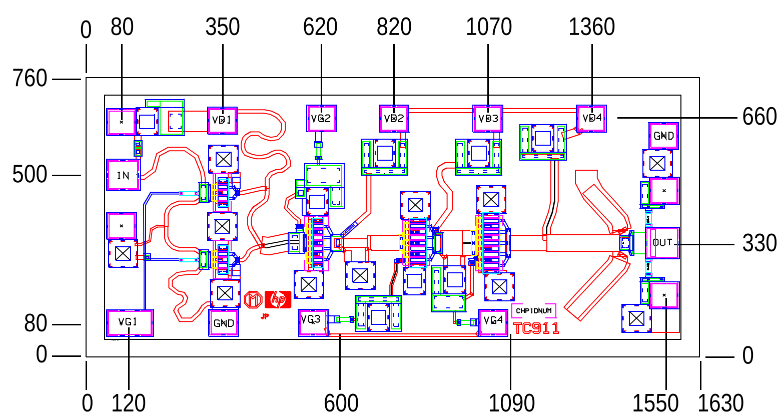


Figure 7. Bonding Pad Positions

(Dimensions are micrometers)

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local Agilent Technologies' sales representative.

Notes: