

April 1995

8-Bit, 75 MSPS Flash A/D Converter

Features

- Differential Linearity Error ± 0.5 LSB or Less
- Integral Linearity Error ± 0.5 LSB or Less
- Built-In Integral Linearity Compensation Circuit
- High-Speed Operation with Maximum Conversion Rate of 75 MSPS (Min)
- Low Input Capacitance 17pF (Typ)
- Wide Analog Input Bandwidth 150MHz (Min. for Full Scale Input)
- Single Power Supply -5.2V
- Low Power Consumption 580mW (Typ)
- Low Error Rate
- Operable at 50% Clock Duty Cycle
- Capable of Driving 50 Ω Loads

Applications

- Video Digitizing
- HDTV (High Definition TV)
- Direct RF Down-Conversion
- Communication Systems
- Radar Systems
- Digital Oscilloscopes

Description

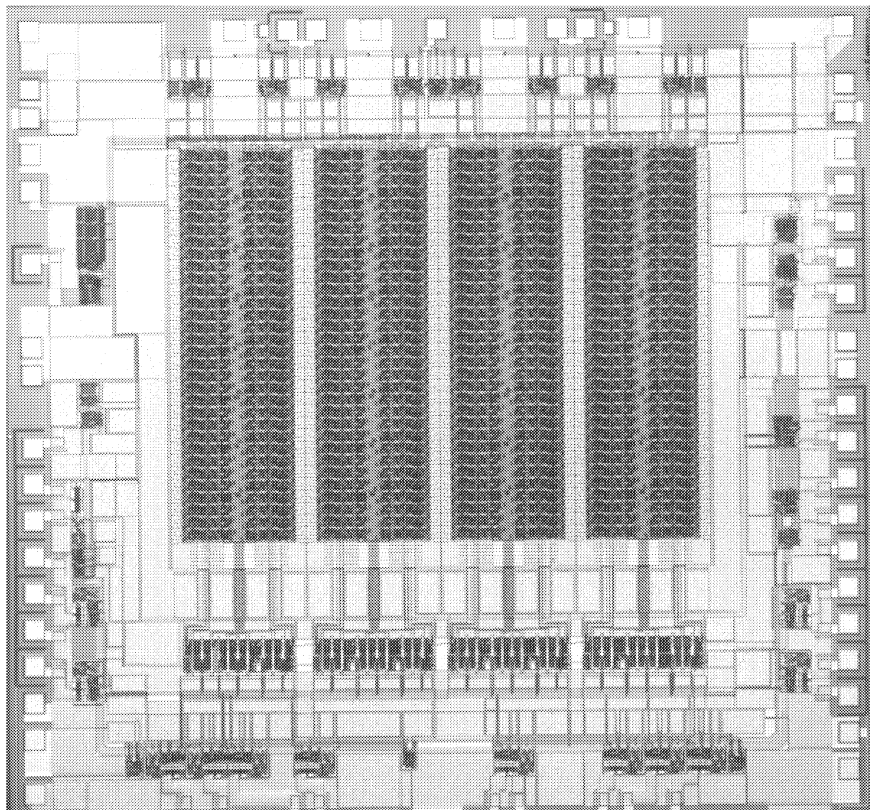
This is a specification that outlines the mechanical and electrical characteristics for the HI1386Y, 8-bit Flash A/D converter IC, in chip (die) form.

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
HI1386Y	+25°C	Die

- All performance parameters are for packaged devices when supplied by Intersil.

Die Metallization Layer



Specifications HI1386Y

Absolute Maximum Ratings $T_A = +25^{\circ}\text{C}$

Supply Voltage (AV_{EE} , DV_{EE})	-7V to +0.5V	V_{RM} Pin Input Current (I_{VRM})	-3mA to +3mA
Analog Input Voltage (V_{IN})	-2.7V to +0.5V	Digital Output Current (ID0 to ID7)	-30mA to 0mA
Reference Input Voltage		Storage Temperature Range (T_{STG})	-65°C to +150°C
V_{RT} , V_{RB} , V_{RM}	-2.7V to +0.5V		
$ V_{RT} - V_{RB} $	2.5V		
Digital Input Voltage			
CLK, $\overline{\text{CLK}}$, MINV, LINV	-4V to +0.5V		
$ \text{CLK} - \overline{\text{CLK}} $	2.7V		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage		Analog Input Voltage, V_{IN}	V_{RB} to V_{RT}
AV_{EE} , DV_{EE}	-5.5V to -4.95V	Pulse Width of Clock	
AV_{EE} - DV_{EE}	-0.05V to 0.05V	T_{PW1}	6.6ns Min.
AGND - DGND	-0.05V to 0.05V	T_{PW0}	6.6ns Min.
Reference Input Voltage			
V_{RT}	-0.1V to 0.1V		
V_{RB}	-2.2V to -1.8V		

Electrical Specifications $T_A = +25^{\circ}\text{C}$, $AV_{EE} = DV_{EE} = -5.2\text{V}$, $V_{RT} = 0\text{V}$, $V_{RB} = -2\text{V}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Differential Linearity Error (DNL) (00000000 to 11111111)		-0.5	0.5	LSB
Integral Linearity Error (INL) (00000000 to 11111111)		-0.5	0.5	LSB
Resolution		8	-	Bits
Input Bias Current, I_{IN}	$V_{IN} = -1.0\text{V}$	0	160	μA
Analog Input Resistance, R_{IN}	$V_{IN} = -1.0\text{V}$	100	1000	$\text{k}\Omega$
Resister-String Current, I_{REF}		-22	-16	mA
Reference Voltage, V_{RM}		-1.1	-0.9	V
Digital Input Current HI,	$H_i = -0.8\text{V}$	0	40	μA
Digital Input Current LO,	$L_o = -1.6\text{V}$	-30	30	μA
$\overline{\text{CLK}}$ Open Voltage, V_{OPN}	$\overline{\text{CLK}} = \text{Open}$	-1.4	-1.2	V
Leakage (1) D0 to D7, V_{LEAK}	$I = -10\mu\text{A}$	-0.8	-0.4	V
Leakage (2) D0 to D7, V_{IN} , LINV , MINV , CLK , $\overline{\text{CLK}}$, I_{LEAK}	$V = 0.3\text{V}$	-1.0	1.0	μA
Digital Output Voltage HI, V_{OH}	220 Ω to -5.2V	-1.095	-0.6	V
Digital Output Voltage LO, V_{OL}	220 Ω to -5.2V	-2	-1.64	V
Supply Current, I_{EE}		-140	-70	mA

Timing Diagram

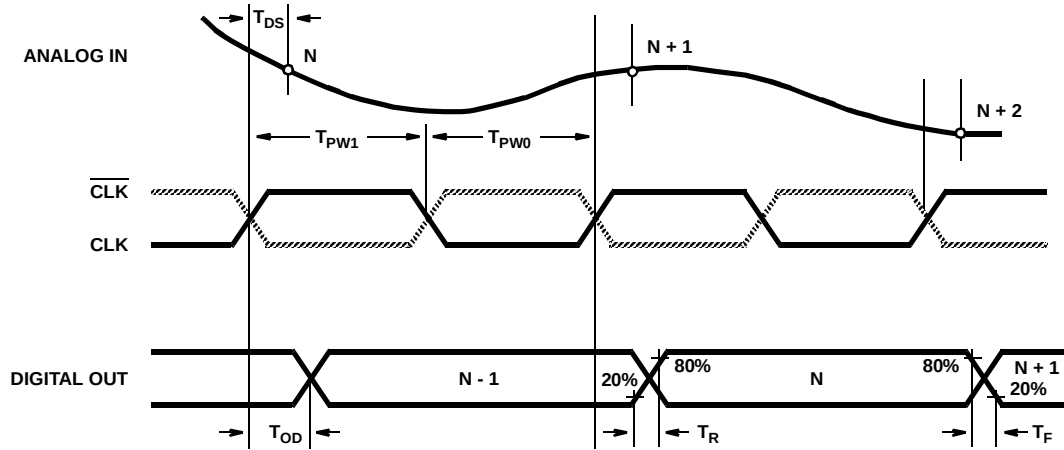
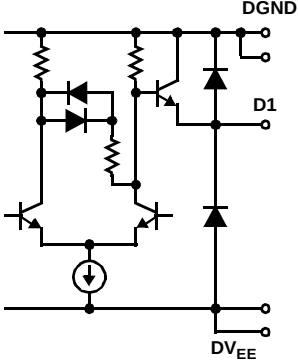
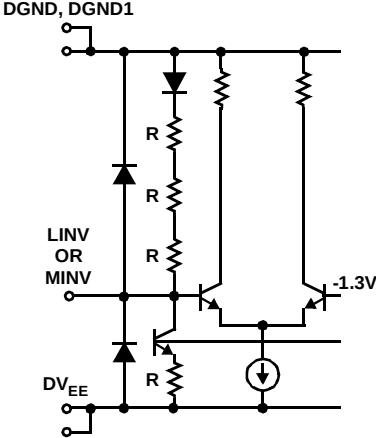
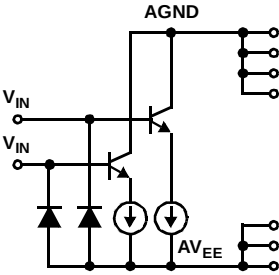


FIGURE 1.

Pad Descriptions

PAD NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
50, 53, 55, 58	AGND	-	0V		Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND, DGND1, and DGND2.
47, 48, 60, 61	AV _{EE}	-	-5.2V		Analog V _{EE} -5.2V (Typ.). Internally connected to DV _{EE} (Resistance: 4Ω to 6Ω). Bypass with 0.1μF to AGND.
39	CLK	I	ECL		CLK Input
38	$\overline{\text{CLK}}$				Input complementary to CLK. When open pulled down to -1.3V. Device is operable without CLK input, but use of complementary inputs of CLK and $\overline{\text{CLK}}$ is recommended to obtain stable high speed operation.
9, 29	DGND1	-	0V		Digital GND (used for internal circuits and output transistors).

Pad Descriptions (Continued)

PAD NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
10, 28	DGND2	-	0V		Digital GND (used for output buffers).
8, 30	DV _{EE}	-	-5.2V		Digital V _{EE} . Internally connected to AV _{EE} (resistance: 4Ω to 6Ω). Bypass with 0.1μF to DGND
12	D0	O	ECL		LSB of data outputs. External pull-down resistor is required.
13	D1				Data outputs. External pull-down resistors are required.
15	D2				
16	D3				
21	D4				
24	D5				
25	D6				
26	D7				MSB of data outputs. External pull-down resistor is required.
1	LINV	I	ECL		Input pin for D0 (LSB) to D6 output polarity inversion (see A/D Output Code Table). Pulled low when left open.
35	MINV	I	ECL		Input pin for D7 (MSB) output polarity inversion (see A/D Output Code Table). Pulled low when left open.
51, 52	V _{IN}	I	V _{RT} to V _{RB}		Analog input pins. These two pins must be connected externally, since they are not internally connected. See Application Note for precautions.

Pad Descriptions (Continued)

PAD NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
46	V_{RB}	I	-2V		Reference voltage (bottom). Typically -2V. Bypass with a 0.1μF and 10μF to AGND.
54	V_{RM}	I	$V_{RB}/2$		Reference voltage mid point. Can be used as a pin for integral linearity compensation.
62	V_{RT}	I	0V		Reference voltage (top) typically 0V.

A/D OUTPUT CODE TABLE

V_{IN} (Note 1)	STEP	MINV 1 LINV 1		0 1		1 0		0 0	
		D7	D0	D7	D0	D7	D0	D7	D0
0V	0	000 00		100 00		011 11		111 11	
		000 00		100 00		011 11		111 11	
	1	000 01		100 01		011 10		111 10	
		⋮		⋮		⋮		⋮	
-1V	127	011 11		111 11		000 00		100 00	
	128	100 00		000 00		111 11		011 11	
		⋮		⋮		⋮		⋮	
	254	111 10		011 10		100 01		000 01	
-2V	255	111 11		011 11		100 00		000 00	
		111 11		011 11		100 00		000 00	

NOTE:

- $V_{RT} = 0V$, $V_{RB} = -2V$

Pad Coordinates

PAD COORDINATE 1

PAD NO.	PAD NAME	X [μm]	Y [μm]
1	LINV	2198.40	4490.40
2		2008.00	4490.40
3		1817.60	4490.40
4		1627.20	4490.40
5		1436.80	4490.40
6		1246.40	4490.40
7		1056.00	4490.40
8	DV _{EE}	865.60	4490.40
9	DGND	675.20	4490.40
10	DGND	388.80	4490.40
11		209.60	4311.20
12	D0	209.60	3730.40
13	D1	209.60	3540.00
14		209.60	3349.60
15	D2	209.60	3159.20
16	D3	209.60	2968.80
17		209.60	2778.40
18		209.60	2629.60
19		209.60	2458.40
20		209.60	2301.60
21	D4	209.60	2111.20
22		209.60	1920.80

PAD NO.	PAD NAME	X [μm]	Y [μm]
23		209.60	1730.40
24	D5	209.60	1540.00
25	D6	209.60	1349.60
26	D7	209.60	1159.20
27		209.60	588.00
28	DGND	209.60	362.40
29	DGND	484.80	215.20
30	DV _{EE}	675.20	215.20
31		865.60	215.20
32		1056.00	215.20
33		1246.40	215.20
34		1436.80	215.20
35	MINV	1627.20	215.20
36		1817.60	215.20
37		2008.00	215.20
38	CLK	2198.40	215.20
39	CLK	2388.80	215.20
40		2579.20	215.20
41		2728.00	215.20
42		2974.40	215.20
43		3164.80	215.20
44		3355.20	215.20

PAD NO.	PAD NAME	X [μm]	Y [μm]
45		3545.60	215.20
46	V _{RB}	3736.00	215.20
47	AV _{EE}	3926.40	215.20
48	AV _{EE}	4075.20	215.20
49		4377.60	215.20
50	AGND	4377.60	1292.00
51	V _{IN}	4377.60	1570.40
52	V _{IN}	4377.60	1720.80
53	AGND	4377.60	1999.20
54	V _{RM}	4377.60	2352.80
55	AGND	4377.60	2698.40
56	V _{IN}	4377.60	2984.80
57	V _{IN}	4377.60	3135.20
58	AGND	4377.60	3413.60
59		4377.60	4490.40
60	AV _{EE}	4075.20	4490.40
61	AV _{EE}	3926.40	4490.40
62	V _{RT}	3736.00	4490.40
63		3545.60	4490.40
64		3164.80	4490.40
65		2728.00	4490.40
66		2579.20	4490.40

Pad Coordinates (Continued)**PAD COORDINATE 2**

PAD NO.	PAD NAME	X [μm]	Y [μm]
1	LINV	2158.40	4450.40
2		1968.00	4450.40
3		1777.60	4450.40
4		1587.20	4450.40
5		1396.80	4450.40
6		1206.40	4450.40
7		1016.00	4450.40
8	DV _{EE}	825.60	4450.40
9	DGND	635.20	4450.40
10	DGND	348.80	4450.40
11		169.60	5271.20
12	D0	169.60	3690.40
13	D1	169.60	3500.00
14		169.60	3309.60
15	D2	169.60	3119.20
16	D3	169.60	2928.80
17		169.60	2738.40
18		169.60	2589.60
19		169.60	2418.40
20		169.60	2261.60
21	D4	169.60	2071.20
22		169.60	1880.80

PAD NO.	PAD NAME	X [μm]	Y [μm]
23		169.60	1690.40
24	D5	169.60	1500.00
25	D6	169.60	1309.60
26	D7	169.60	1119.20
27		169.60	548.00
28	DGND	169.60	322.40
29	DGND	444.80	175.20
30	DV _{EE}	635.20	175.20
31		825.60	175.20
32		1016.00	175.20
33		1206.40	175.20
34		1396.80	175.20
35	MINV	1587.20	175.20
36		1777.60	175.20
37		1968.00	175.20
38	$\overline{\text{CLK}}$	2158.40	175.20
39	CLK	2348.80	175.20
40		2539.20	175.20
41		2688.00	175.20
42		2934.40	175.20
43		3124.80	175.20
44		3315.20	175.20

PAD NO.	PAD NAME	X [μm]	Y [μm]
45		3505.60	175.20
46	V _{RB}	3696.00	175.20
47	AV _{EE}	3886.40	175.20
48	AV _{EE}	4035.20	175.20
49		4337.60	175.20
50	AGND	4337.60	1252.00
51	V _{IN}	4337.60	1530.40
52	V _{IN}	4337.60	1680.80
53	AGND	4337.60	1959.20
54	V _{RM}	4337.60	2312.80
55	AGND	4337.60	2658.40
56	V _{IN}	4337.60	2944.80
57	V _{IN}	4337.60	3095.20
58	AGND	4337.60	3373.60
59		4337.60	4450.40
60	AV _{EE}	4035.20	4450.40
61	AV _{EE}	3886.40	4450.40
62	V _{RT}	3696.00	4450.40
63		3505.60	4450.40
64		3124.80	4450.40
65		2688.00	4450.40
66		2539.20	4450.40

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