Preliminary

275V 40-Channel Row Driver with SCR Outputs

Ordering Information

Device	Package Options		
	80-Lead Ceramic Gullwing	64-Lead 3-Sided Plastic Gullwing	Die
HV506	HV506DG	HV506PG	HV506X

Features

- ❏ Processed with HVDI® technology
- ❏ Symmetric row drive
- ❏ Output voltage up to 275V
- ❏ Source/Sink current 300mA (min.)
- ❏ Shift Register Speed 3MHz
- ❏ Pin-programmable shift direction (DIR)
- ❏ Hi-Rel processing available

General Description

The HV506 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suitable for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays.

When the data reset pin (DR_{IO}) is at logic high, it will reset all the outputs of the internal shift register to zero. At the same time, the output of the shift register will start shifting a logic high from the least significant bit to the most significant bit. The DR_{IO} can be triggered at any time. The DIR pin controls the direction of data through the device. When DIR is at logic high, DR_{IOA} is the input and DR_{IOB} is the output. When DIR is grounded, DR_{IOB} is the input and the DR_{IOA} is the output. See the Output Sequence Operation Table for output sequence. The $\overline{POL}$ and $\overline{OE}$ pins perform the polarity select and output enable function respectively. Data is clocked through the shift register loaded on the low to high transition of the clock. A logic high in the shift register will cause the other corresponding output to swing to V_{DD} if $\overline{POL}$ is high, or to V_{SS} if $\overline{POL}$ is low. All other outputs will be in the High-Z state. If $\overline{OE}$ is at logic high all outputs will be in the High-Z state. An output in the High-Z state may block up to 275V above V_{SS} or 275V below V_{DD}. The D_P/D_N pins are for the positive/negative discharge of the high voltage output HV_{OUT}. Data output buffers are provided for cascading devices.

LV_{DD} requires low current for the HV506 logic section. V_{DD} requires high current for the output section . Typically these two pins are at the same potential. The same current and potential conditions apply to the LV_{SS}, logic, and V_{SS}, output pins. V_{sub} must always be equal or greater than the most positive supply.

Absolute Maximum Ratings

Logic supply voltage, LV_{DD}[1]		-0.5V to +15V
Output supply voltage, V_{DD}[1]		-0.5V to +15V
Substrate bias voltage, V_{sub}		See Note 3
Output voltage, HV_{OUT}		±300V
Logic input levels		-0.5V to V_{DD} +0.5V
Continuous total power dissipation[2]	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Plastic	-40°C to +85°C
	Ceramic	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:

1. All voltages are referenced to V_{SS}.
2. For operation above 25°C ambient derate linearly to maximum operating temperture at 20mW/°C for plasitc and at 19mW/°C for ceramic.
3. V_{sub} must be the most positive with respect to V_{SS}.

Electrical Characteristics

(over recommended operating conditions of V_{DD} = 12V, LV_{DD} = 12V, and T_A = 25°C unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			10	mA	f_{CLK} = 3MHz
I_{DDQ}	Quiescent V_{DD} supply current			100	μA	All V_{IN} = V_{SS} or V_{DD}
V_{OH}	High-level output	HV_{OUT}	V_{DD}-10		V	I_O= -300mA
		Data out	10.8		V	I_O= -100μA
V_{OL}	Low-level output	HV_{OUT}		V_{SS}+10	V	I_O= 300mA
		Data out		1.2	V	I_O= 100μA
I_{IH}	High-level logic input current			1	μA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current			-1	μA	V_{IL} = V_{SS}
I_{OFF}	Output OFF leakage current (High-Z)			10	μA	HV_{OUT} - V_{SS} = 275V, V_{sub} = HV_{OUT}
				10	μA	V_{DD} - HV_{OUT} = 275V, V_{sub} = V_{DD}

Notes:

1. Only one output can be turned on at a time.

SCR Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V_{OH}	High-level output	V_{DD}-10		V	I_O= -300mA
V_{OL}	Low-level output		V_{SS}+10	V	I_O= 300mA
I_L	Latching Current		15	mA	
V_L	Latching Voltage		100	V	
I_H	Holding Current	10		mA	
V_H	Holding Voltage	10		V	
I_{OFF}	Output OFF leakage current (High-Z)		10	μA	HV_{OUT} - V_{SS} = 275V, V_{sub} = HV_{OUT}
			10	μA	V_{DD} - HV_{OUT} = 275V, V_{sub} = V_{DD}

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		3	MHz	
$t_{W\ (H/L)}$	Pulse width - clock high or low	150		ns	
t_{SUD}	Data set-up time before clock rises	50		ns	
t_{HD}	Data hold time after clock rises	50		ns	
t_{SUC}	HV_{OUT} delay from clock rises (Hi-Z to H or L)		1	μs	C_L = 10nF
t_{SUE}	HV_{OUT} delay from $\overline{\text{Output Enable}}$ rises		600	ns	C_L = 10nF
t_{HC}	HV_{OUT} delay from clock rises (H or L to Hi-Z)		2	μs	C_L = 10nF
t_{HE}	HV_{OUT} delay from $\overline{\text{Output Enable}}$ rises		600	ns	C_L = 10nF
t_{DHL}*	Delay time clock to data output falls		250	ns	C_L = 15pF
t_{DLH}*	Delay time clock to data output rises		250	ns	C_L = 15pF
$t_{OFF(SCR)}$	Turn off time of output SCR		4	μs	Time after $I_{OUT} \leq$ 2mA, C_L = 10nF
$t_{OFF(D)}$	Turn off time of output diode		2	μs	Time after $I_{OUT} \leq$ 2mA, C_L = 10nF
t_{POW}	$\overline{\text{POL}}$ pulse width	3		μs	
t_{OEW}	$\overline{\text{Output Enable}}$ pulse width	3		μs	
SR	Slew rate of HV_{OUT}		200	V/μs	

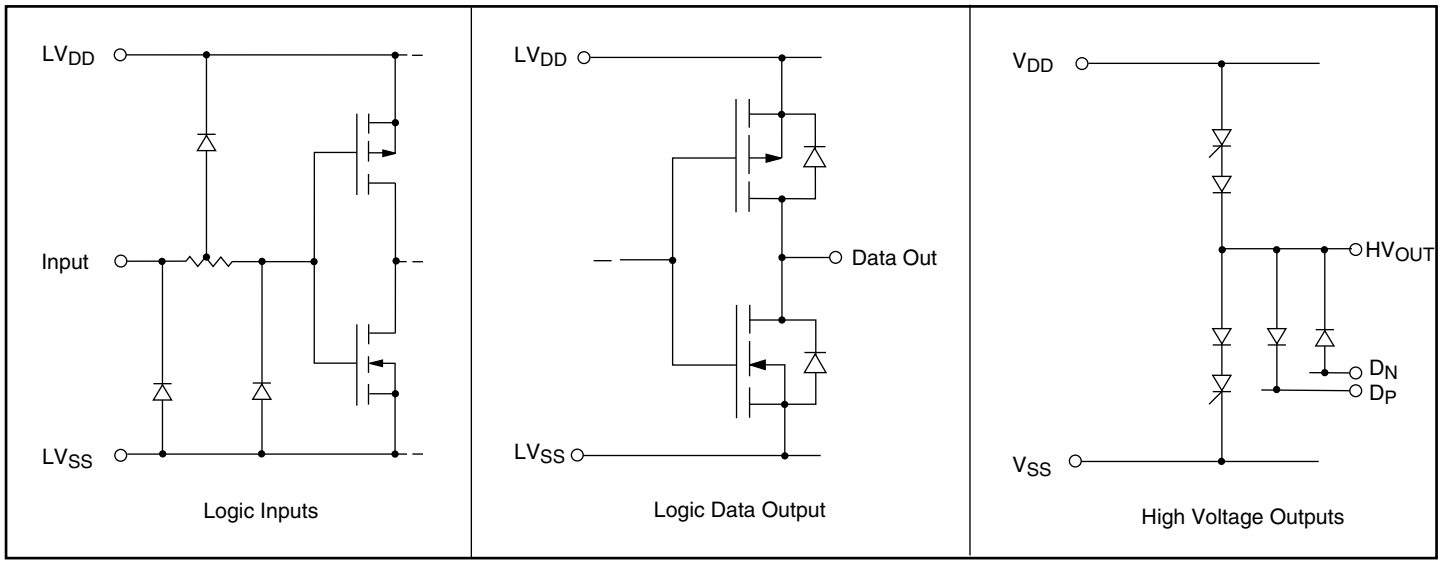
* The delay is measured from the trailing edge of the clock but the data is triggered by the rising edge of the clock. There is an internal delay for the data output which is equal to t_{WH}. Therefore the delay is measured from the trailing edge of the clock.

Recommended Operating Conditions

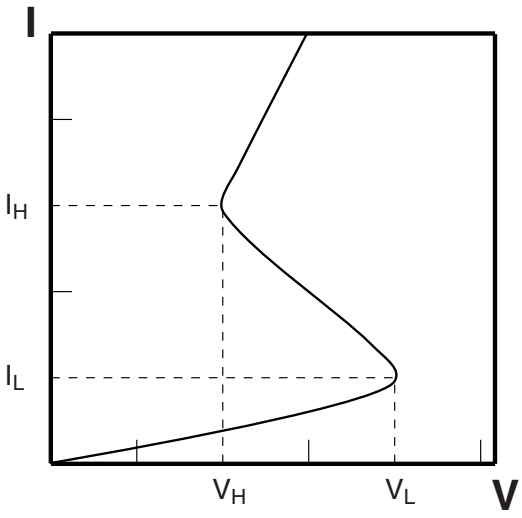
Symbol	Parameter		Min	Max	Units
LV_{DD}	Logic supply voltage		10.8	13.2	V
V_{DD}	Output supply voltage		10.8	13.2	V
V_{IH}	High-level input voltage		$0.8LV_{DD}$	LV_{DD}	V
V_{IL}	Low-level input voltage		0	$0.2LV_{DD}$	V
f_{CLK}	Clock frequency			3	MHz
I_O	High voltage output current			±300	mA
T_A	Operating free-air temperature	Plastic	-40	+85	°C
		Ceramic	-55	+125	°C
I_{OD}	Allowable pulse current through diodes			±500	mA

Notes:
The substrate pin V_{sub} (pin 39) must be biased for proper output breakdown voltage. $V_{sub} \geq V_{DD}$ or HV_{OUT} whichever is higher.
LV_{DD}/V_{DD} are measured with respect to LV_{SS}/V_{SS}.

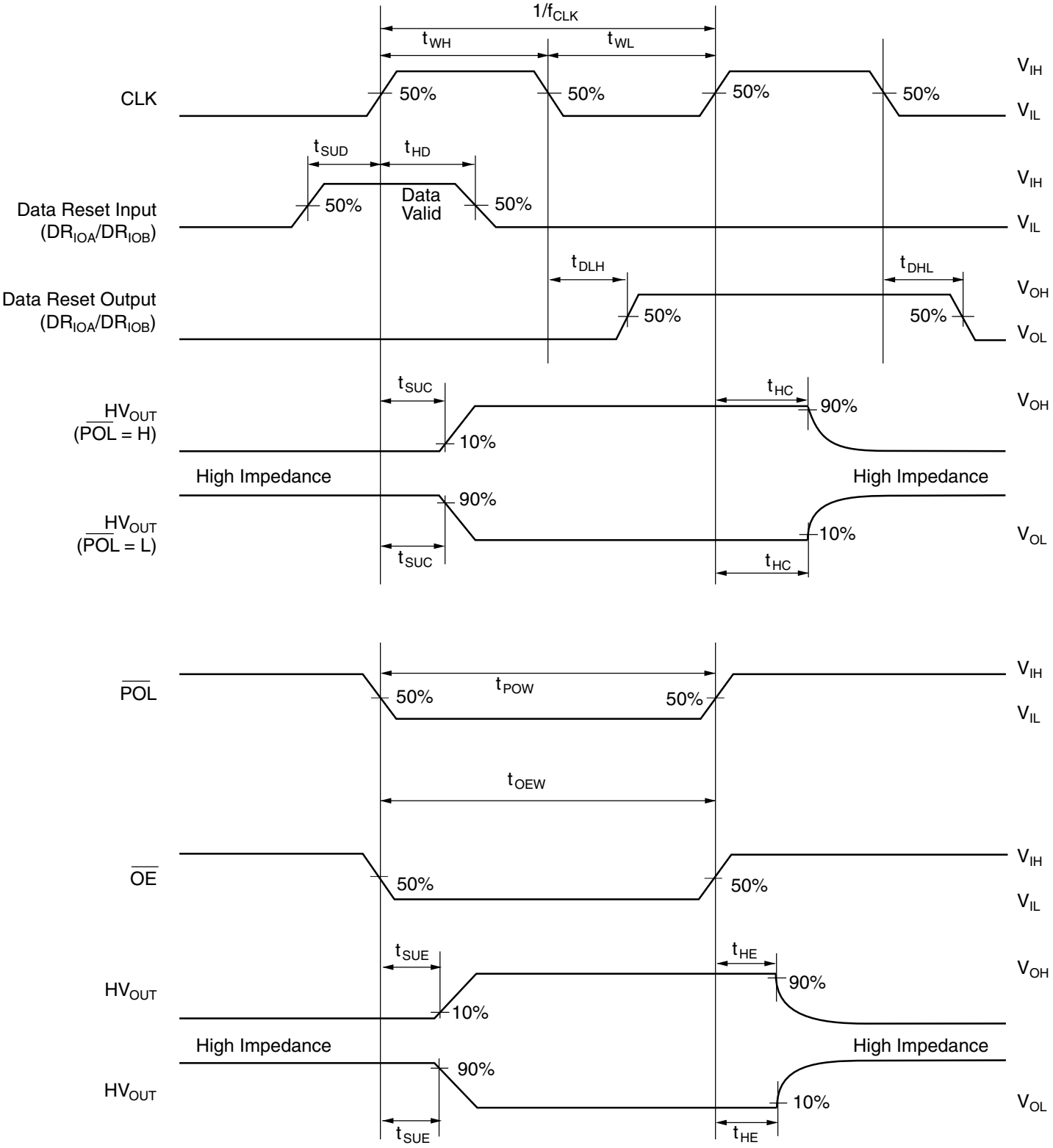
Input and Output Equivalent Circuits



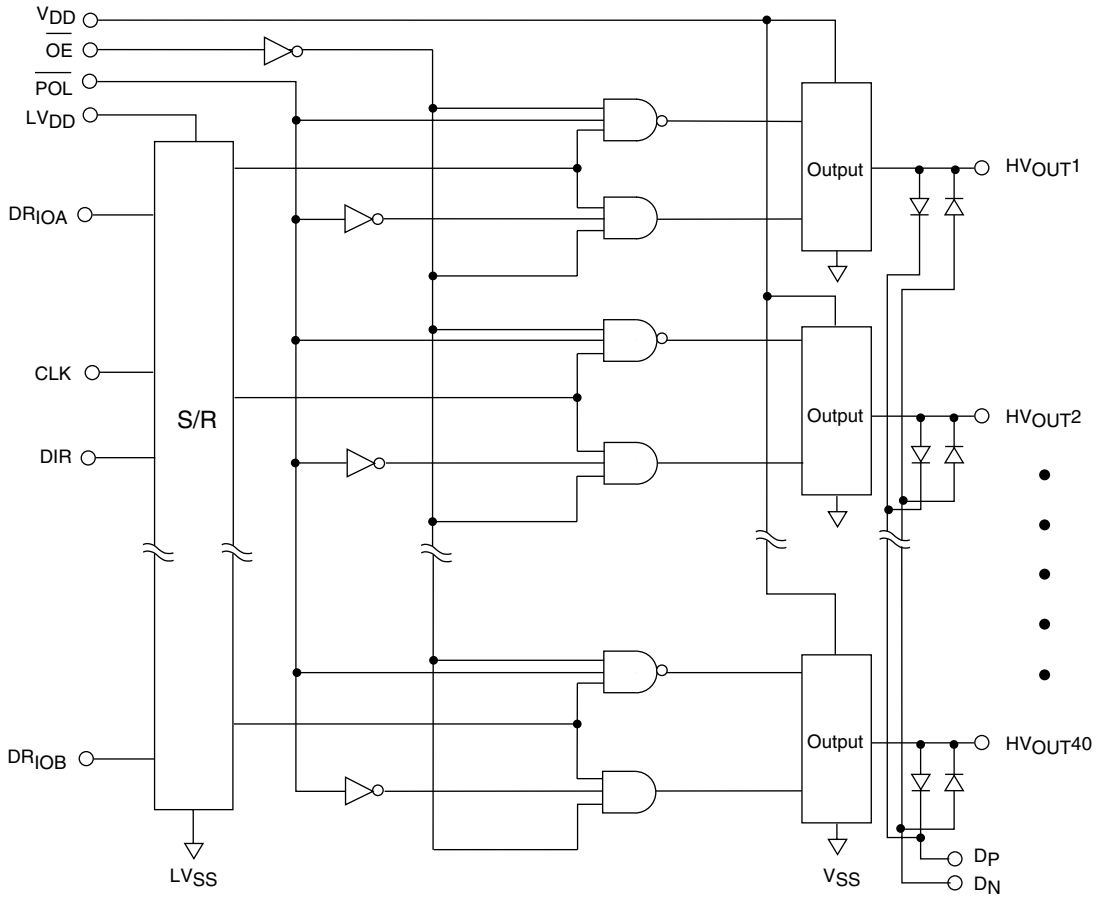
SCR Characteristics



Switching Waveforms



Functional Block Diagram



Function Table

I/O Relations	Inputs					HV Outputs
	CLK	DIR	S/R Data	$\overline{POL}$	$\overline{OE}$	
O/P HIGH	X	X	H	H	L	H
O/P OFF	X	X	L	X	L	HIGH-Z
O/P LOW	X	X	H	L	L	L
O/P OFF	X	X	X	X	H	All O/P HIGH-Z

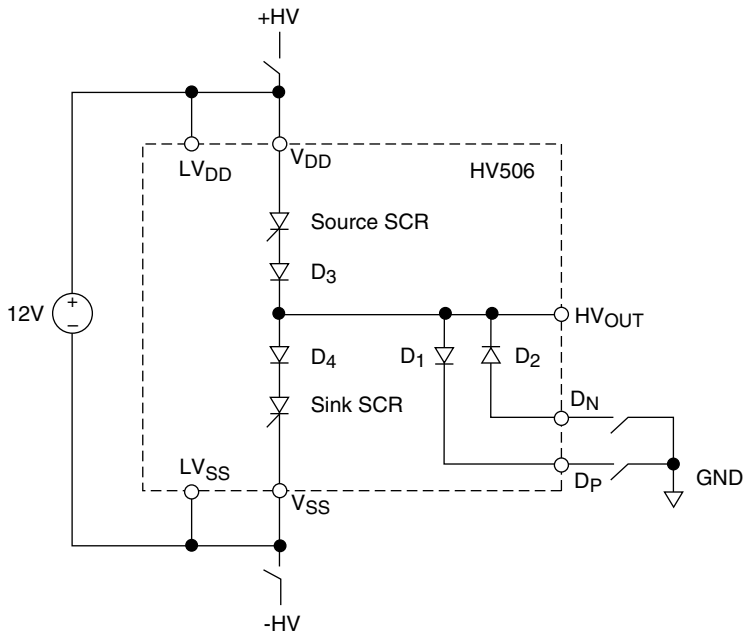
Note:
H = logic high level, L = logic low level, X = irrelevant

Output Sequence Operation Table

DIR	Data Reset In	Data Reset Out	HV_{OUT} # Sequence	Direction[3]
L	DR_{IOB}	DR_{IOA}[1]	40 → 1	
H	DR_{IOA}	DR_{IOB}[2]	1 → 40	

Notes:
1. DR_{IOA} is DR_{IOB} delayed by 40 clock pulses.
2. DR_{IOB} is DR_{IOA} delayed by 40 clock pulses.
3. Reference to chip layout drawing.

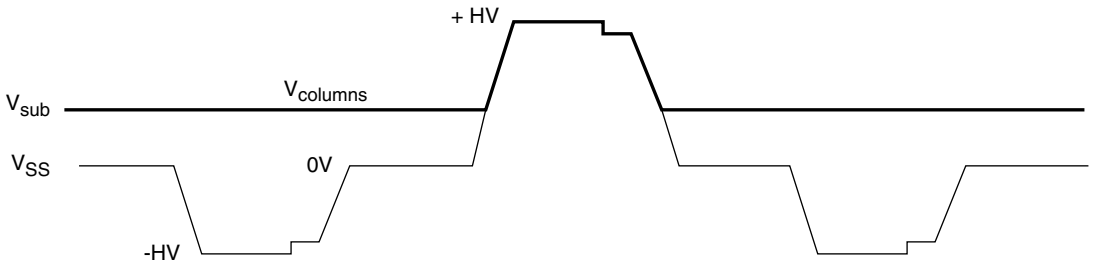
Typical Output Circuit Connections



Note: The voltage potential between LV_{DD}/V_{DD} and LV_{SS}/V_{SS} must not exceed recommended operating conditions of 10.8V - 13.2V (12V typical)

Substrate Bias Operation

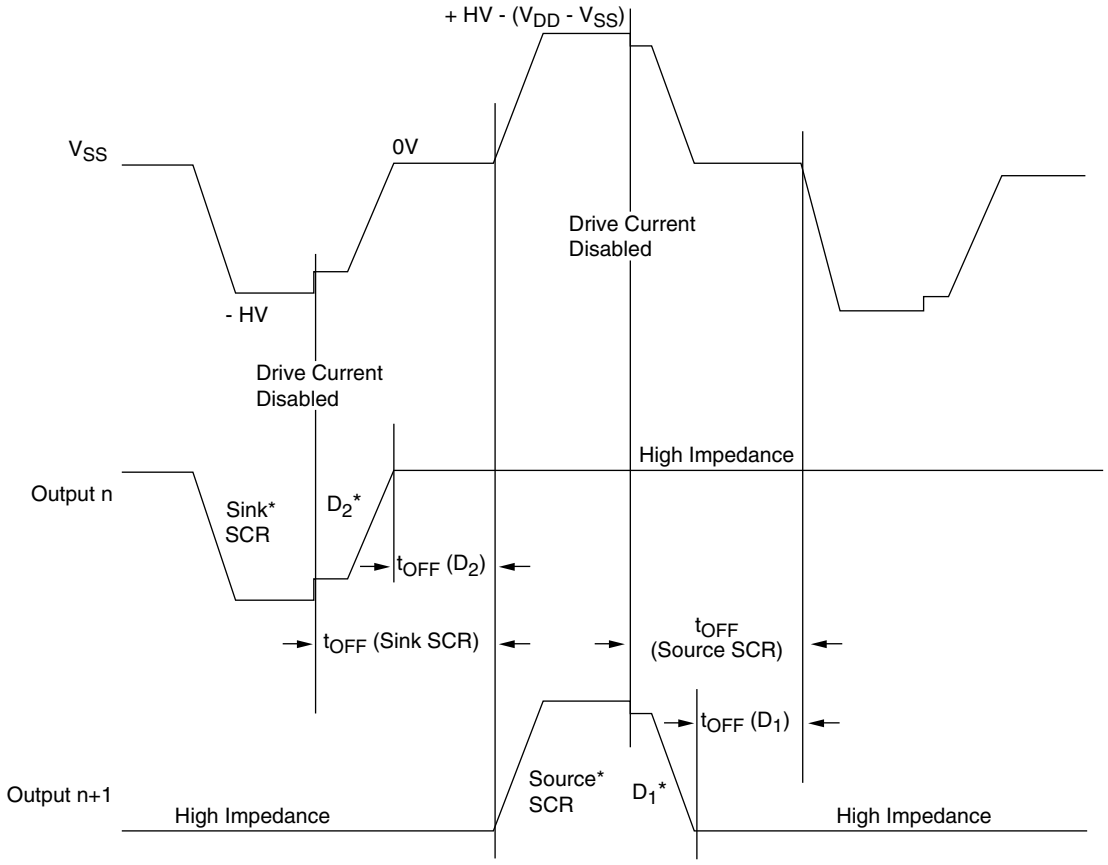
In order to achieve the desired output breakdown voltage, the substrate must be biased to the most positive potential of any circuit node. For this condition, $V_{sub} \geq V_{DD}$ or HV_{OUT} whichever is higher. Refer to Typical Output Circuit Connections for wiring. A typical V_{sub} signal is shown below.



Note: In general, when driving the outputs positive, V_{SUB} = +HV. And when driving outputs negative, V_{SUB} equals most positive voltage; e.g. GND or >0V.

HV Switching Waveforms and Operation

To drive a TFEL row with a negative pulse: The desired sink SCR is enabled and V_{SS} is connected to -HV via a current limited switch. After holding the output at the -HV level, the switch is opened in order to set the sink SCR current to zero. The row is then discharged through a discharge diode when D_2 is switched to GND. The application of a positive pulse to a row operates in a similar manner using the selected source SCR and D_1.



* Notes internal device handling current flow. Refer to Typical Output Circuit Connections for schematic.

Pin Configurations

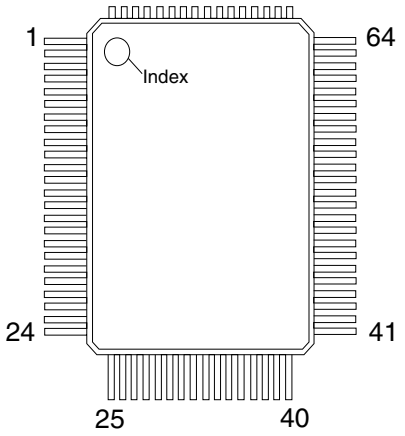
HV506

Option A:

Pin	Function	Pin	Function
1	HV_{OUT} 1	33	$\overline{OE}$
2	HV_{OUT} 2	34	$\overline{POL}$
3	HV_{OUT} 3	35	LV_{DD}
4	HV_{OUT} 4	36	V_{SS}
5	HV_{OUT} 5	37	V_{DD}
6	HV_{OUT} 6	38	LV_{SS}
7	HV_{OUT} 7	39	V_{sub}
8	HV_{OUT} 8	40	N/C
9	HV_{OUT} 9	41	N/C
10	HV_{OUT} 10	42	D_N
11	HV_{OUT} 11	43	D_P
12	HV_{OUT} 12	44	N/C
13	HV_{OUT} 13	45	HV_{OUT} 21
14	HV_{OUT} 14	46	HV_{OUT} 22
15	HV_{OUT} 15	47	HV_{OUT} 23
16	HV_{OUT} 16	48	HV_{OUT} 24
17	HV_{OUT} 17	49	HV_{OUT} 25
18	HV_{OUT} 18	50	HV_{OUT} 26
19	HV_{OUT} 19	51	HV_{OUT} 27
20	HV_{OUT} 20	52	HV_{OUT} 28
21	N/C	53	HV_{OUT} 29
22	D_P	54	HV_{OUT} 30
23	D_N	55	HV_{OUT} 31
24	N/C	56	HV_{OUT} 32
25	N/C	57	HV_{OUT} 33
26	LV_{SS}	58	HV_{OUT} 34
27	V_{DD}	59	HV_{OUT} 35
28	DIR	60	HV_{OUT} 36
29	V_{SS}	61	HV_{OUT} 37
30	CLOCK	62	HV_{OUT} 38
31	DR_{IOA}	63	HV_{OUT} 39
32	DR_{IOB}	64	HV_{OUT} 40

Note: Pins 65–80 are NC.

Package Outline



top view

3-sided Plastic 64-pin Gullwing Package

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