RF Sigma-Delta Fractional-N / IF Integer-N / Low Power Frequency Synthesizer With Integrated RF VCOs

■ Features

- Full CMOS dual-band RF synthesizer
- Full CMOS IF synthesizer
- Integrated VCOs, Loop Filters, Varactors, and Resonators
- Minimal External Components Required
- 2.7V to 3.6V operation
- Low current consumption
- Low Phase Noise
- Selectable or programmable power-save mode
- Small 24 pin LGA (Leadless Grid Array) package

■ Applications

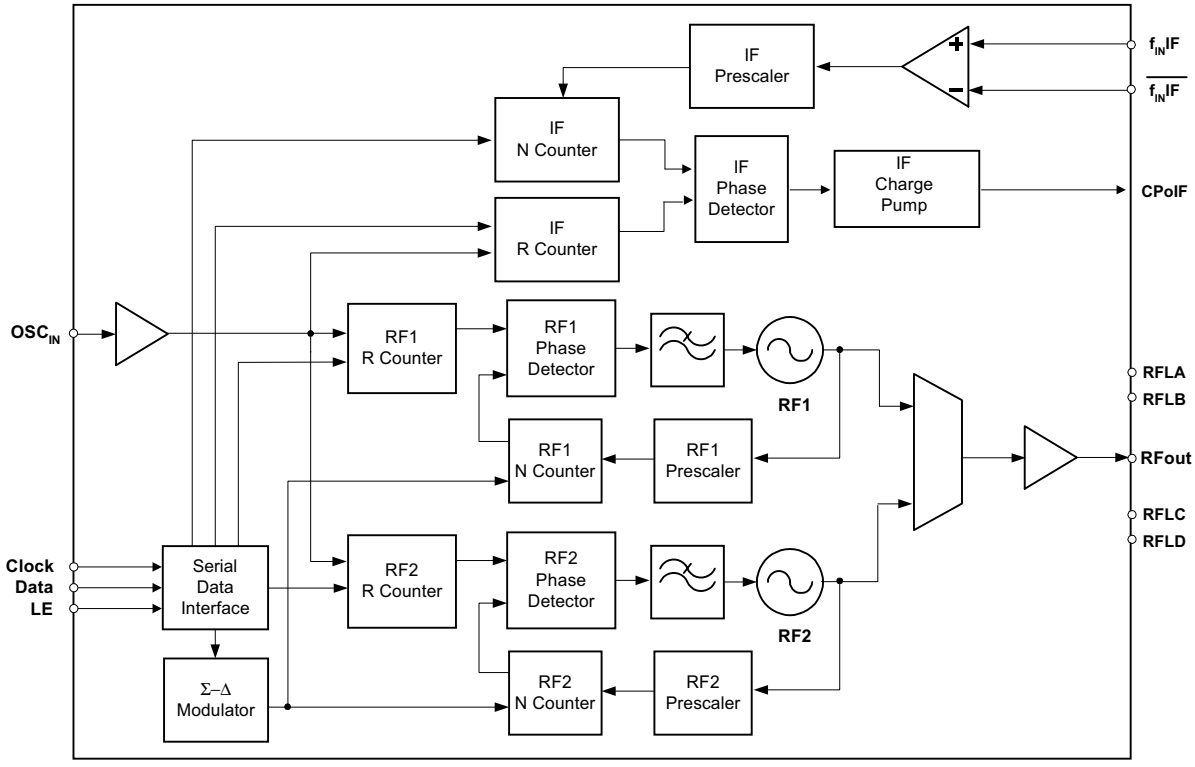
- Dual-band communications
- Cordless telephone systems
- Portable wireless communications
  - GSM, DCS1800, PCS1900 cellular systems
  - AMPS and cellular (900MHz) CDMA
  - PCS (Korean PCS and US PCS) CDMA
- Wireless local area networks (WLANs)
- Cable TV tuners(CATV)
- Other wireless communication systems

■ General Description

The HM6F5221 of full CMOS monolithic, both IF and dual-band RF synthesizer is to be used as a local oscillator for RF and IF of a dual conversion transceiver. It is fabricated using HYNIX semiconductor's mixed-signal/RF CMOS process.

HM6F5221 contains two VCOs, loop filters, regulators, reference and VCO dividers, charge pumps, and phase detectors. HM6F5221 performs Fractional-N frequency for RF synthesis and Integer-N frequency for IF synthesis. Serial data is transferred into the HM6F5221 via three-wire interface (Data, Enable, and Clock).

■ Functional Block Diagram



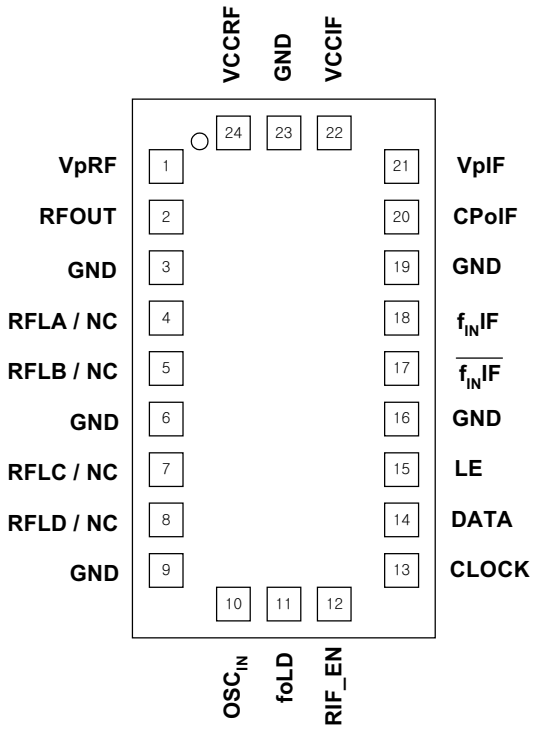
Contents

Section **Page**

Table of Contents

Table **Page**

■ Pin Assignment



Leadless Grid Array Package

■ Pin Descriptions

Pin No. HM6F5221 24-pin LGA Package	PIN NAME	I/O	Description
1	VpRF	-	Power Supply for RF charge pump. Must be ≥ VCCRF.
2	RFOUT	O	VCO output frequency for RF1 or RF2.
3	GND	-	Ground Pin.
4	RFLA / NC	I/O	RF1 center frequency control pin using external inductor connected to RF1 VCO.
5	RFLB / NC	I/O	RF1 center frequency control pin using external inductor connected to RF1 VCO.
6	GND	-	Ground Pin.
7	RFLC / NC	I/O	RF1 center frequency control pin using external inductor connected to RF2 VCO.
8	RFLD / NC	I/O	RF1 center frequency control pin using external inductor connected to RF2 VCO.
9	GND	-	Ground Pin.

■ Pin Descriptions (continued)

Pin No. HM6F5221 24-pin LGA Package	PIN NAME	I/O	Description
10	OSC_{IN}	I	Oscillator input to drive both the IF and RF R counter inputs.
11	foLD	O	Multiplexed output of the RF/IF programmable or reference dividers, and RF/IF lock detect signals.
12	RIF_EN	I	RF/IF PLL Enable (Enable when HIGH, Power down when LOW). Controls both the RF and IF PLL to power down directly. Also set the charge pump output to be in TRI-STATE when LOW. Powers up when HIGH depends on the state of RF_PWDN or IF_PWDN.
13	CLOCK	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 24-bit shift register.
14	DATA	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
15	LE	I	Load enable high impedance CMOS input. When **LE** goes HIGH.
16	GND	.	Ground Pin.
17	finIF/	I	IF Prescaler complementary input. For a single-ended output IF VCO, a bypass capacitor should be placed as close as possible to this pin.
18	finIF	I	IF prescaler input. Small signal input from the VCO.
19	GND	-	Ground Pin.
20	CPoIF	O	Internal IF charge pump output. For connection to a loop filter for driving the input of an external VCO.
21	VpIF	-	Power Supply for IF charge pump. Must be ≥ **VCCIF**.
22	VCCIF	-	Power supply voltage input for IF analog, IF digital, data interface, f**oLD** and oscillator circuits. Input may range from 2.7V to 3.6V. **VCCIF** must equal **VCCRF**. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
23	GND	-	Ground Pin.
24	VCCRF	-	Power supply voltage input for RF analog and RF digital circuits. Input may range from 2.7V to 3.6V. **VCCRF** must equal **VCCIF**. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.

■ Absolute Maximum Ratings

Characteristics	Symbol	Value	Unit
Power Supply Voltage	VCC	-0.3 ~ +4.2	V
	VPP	-0.3 ~ +4.2	V
Voltage on any pin with GND=0 volts	Vi	-0.3 ~ VCC+0.3	V
Storage Temperature Range	T_S	-55 ~ +150	^{O}C
Lead Temperature	T_L	260	^{O}C

CAUTION: Stress above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. Other conditions above those indicated in the operational sections of this specification are not implied.

■ Electrostatic Characteristics

Characteristics	Pin NO.	ESD Level	Unit
Human Body Model	All	T.B.D.	V
Machine Model	All	T.B.D.	V
Charge Device Model	All	T.B.D.	V

CAUTION: This Device is high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should only be done at ESD free workstations.

■ Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VCC	2.7	3.0	3.6	V
Power Supply Voltage Difference	V∆ (VCC-VPP)	-0.3	-	0.3	V
Operating Temperature	T_A	-40 ~ 85			^{o}C

CAUTION: All specification are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 ^{o}C unless otherwise stated.

■ Electrical Characteristics

VCC = 3.0V, -40°C < T_A < 85°C, Except as Specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
V_{CC}	Power Supply Voltage		2.7	3.0	3.6	V
V_{PP}			2.7	3.0	3.6	V
I_{CC}[1]	Total Supply Current	RF1 and IF	-	18	24	mA
	RF1 Mode Supply Current	V_{CC}=2.7V to 3.6V, RF1 @ , f_Φ= 10KHz	-	13	17	mA
	RF2 Mode Supply Current	V_{CC}=2.7V to 3.6V, RF2 @ , f_Φ= 10KHz	-	12	17	mA
	IF Mode Supply Current	V_{CC}=2.7V to 3.6V, IF @ , f_Φ= 10KHz	-	5	7	mA
$I_{CC-PWRDN}$	Power down Current	V_{CC}=3.0V		1	10	µA
Reference Oscillator Inputs						
f_{OSC}	Oscillator Frequency.		6	-	26	MHz
V_{OSC}	Oscillator Sensitivity	OSC_{IN}	0.5	-	VCC +0.3 V	V_{PP}
I_{IHR}	Oscillator Input Current	V_{IH} =V_{CC}=3.6V	-	-	100	µA
I_{ILR}	Oscillator Input Current	V_{IL} =0V, V_{CC}=3.6V	-100	-	-	µA
Digital Inputs[2]						
V_{IH}	High Level Input Voltage	*	0.8 V_{CC}	-	-	V
V_{IL}	Low Level Input Voltage	*	-	-	0.2 V_{CC}	V
I_{IH}	High Level Input Current	V_{IH} =V_{CC}=3.6V*	-1.0	-	1.0	µA
I_{IL}	Low Level Input Current	V_{IL} =0V, V_{CC}=3.6V*	-1.0	-	1.0	µA
Digital Outputs[2]						
V_{OH}	High-Level Output Voltage	I_{OH} = -500 µA	V_{CC}-0.4	-	-	V
V_{OL}	Low-Level Output Voltage	I_{OL} = 500 µA	-	-	0.4	V
Serial Data Control[3]						
t_{CK}	Clock Cycle Time	See Data Input Timing	40	-	-	ns
t_r	Clock Rise Time	See Data Input Timing	-	-	50	ns
t_f	Clock Fall Time	See Data Input Timing	-	-	50	ns
t_{CS}	Data Setup Time to Clock	See Data Input Timing	5	-	-	ns
t_{CH}	Data Hold Time to Clock	See Data Input Timing	0	-	-	ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	10	-	-	ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	10	-	-	ns
t_{ES}	Clock to Load Enable Setup Time	See Data Input Timing	10	-	-	ns
t_{EH}	Clock to Load Enable Hold Time	See Data Input Timing	12	-	-	ns
t_{ED}	Load Enable to Clock Delay Time	See Data Input Timing	12	-	-	ns
t_{EW}	Load Enable Pulse Width	See Data Input Timing	50	-	-	ns

Notes :

1. RF1= 1.55GHz, RF2 = 1.2GHz, IF = 540MHz
2. For signal Clock, Data, LE, RIF_EN, FoLD. Does not include f_{IN}RF, f_{IN}IF and OSC_{IN}.
3. All timing is referenced to the 50% level of the waveform, unless otherwise noted.

■ Electrical Characteristics (Continued)

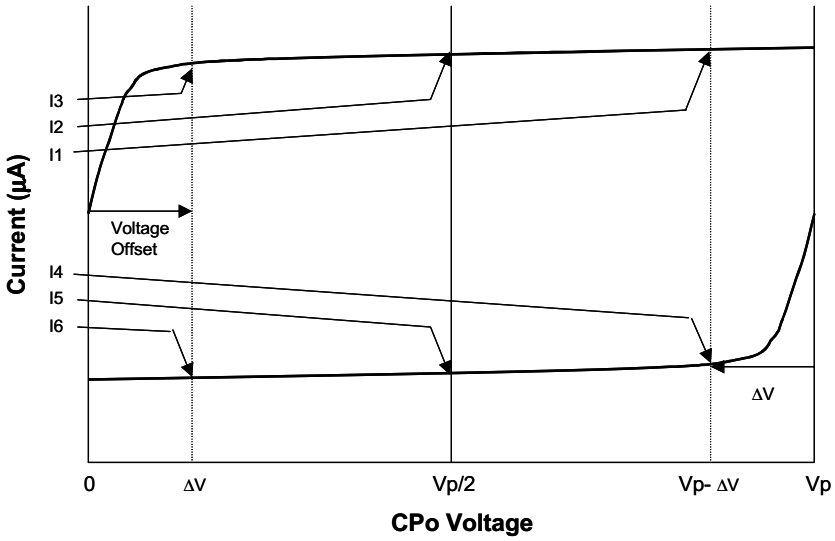
Symbol	Parameter[1]	Conditions	Min	Typ	Max	Units
RF Synthesizer Characteristics						
f_Φ	Internal Phase Detector Frequency	$f_\Phi = f_{OSC} / R$	6	-	26	MHz
f_{CEN}	RF1 VCO Center Frequency	RF1 Active	1530	-	1780	MHz
f_{CEN}	RF2 VCO Center Frequency	RF2 Active	954	-	1230	MHz
f_{CEN}	RF1 VCO Pushing	Open Loop				MHz/V
	RF2 VCO Pushing					MHz/V
	RF1 VCO Pulling	VSWR = 2:1 All Phases Open Loop		T.B.D		MHz_{PP}
	RF2 VCO Pulling					MHz_{PP}
	RF1 Phase Noise	1.25 MHz offset RFOUT =				DBc/Hz
	RF2 Phase Noise	60 KHz offset RFOUT =				DBc/Hz
		900 KHz offset RFOUT =				DBc/Hz
	RF1 Harmonic Suppression	Second Harmonic				dBc
	RF2 Harmonic Suppression					dBc
	RFOUT Power Level	Z_L = 50 Ω, RF1 Active				dBm
		Z_L = 50 Ω, RF2 Active				dBm
	RF1 Output Reference Spurs	Offset =				dBc
	RF2 Output Reference Spurs	Offset =				dBc

Note : 1. RF1 = 1.55GHz, RF2 = 1.2GHz, and IF = 540MHz for all parameters unless otherwise noted.

■ Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IF Charge Pump						
$I_{CPo\text{-}source\ IF}$	IF Charge Pump Output Current (See the Table.4)	$V_{Cpo} = V_p/2$, IF_CP = 0	-	-100	-	µA
$I_{CPo\text{-}sink\ IF}$		$V_{Cpo} = V_p/2$, IF_CP = 0	-	100	-	µA
$I_{CPo\text{-}source\ IF}$		$V_{Cpo} = V_p/2$, IF_CP = 1	-	-800	-	µA
$I_{CPo\text{-}sink\ IF}$		$V_{Cpo} = V_p/2$, IF_CP = 1		800		µA
$I_{CPo\text{-}TRI}$	Charge Pump TRI_STATE Current	$0.5 \le V_{CPo} \le V_p\text{-}0.5$ $-40°C \le T_A \le +85°C$	-2.5	-	2.5	nA
I_{CPo} vs. V_{CPo}	CP Current vs. Voltage Variation	$0.5 \le T_A \le V_p\text{-}0.5$ $T_A = 25°C$, RF I_{CPo}		5	10	%
I_{CPo} vs. Temp.	CP Current vs. Temperature	$V_{CPo} = V_p/2$, RF I_{CPo} $-40°C \le T_A \le +85°C$		8		%

■ Charge Pump Current Specification Definitions



I1 = CP sink current at $V_{CPo} = V_p - \Delta V$
I2 = CP sink current at $V_{CPo} = V_p/2$
I3 = CP sink current at $V_{CPo} = \Delta V$
I4 = CP source current at $V_{CPo} = V_p - \Delta V$
I5 = CP source current at $V_{CPo} = V_p/2$
I6 = CP source current at $V_{CPo} = \Delta V$

ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to VCC and ground. Typical values are between 0.5V and 1.0V

Notes

I_{CPo} vs. V_{CPo} = [1/2 * {|I1|-|I3|}] / [1/2 * {|I1|+|I3|}] * 100% and [1/2 * {|I4|-|I6|}] / [1/2 * {|I4|+|I6|}] * 100%

$I_{CPo\text{-}sink}$ vs. $I_{CPo\text{-}source}$ = [|I2|-|I5|] / [1/2 * {|I2| + |I5|}] * 100%

I_{CPo} vs. T_A = [| I2@temp | - | I2@25°C |] / | I2@25°C | * 100% and [| I5@temp | - | I5@25°C |] / | I5@25°C | * 100%

■ Functional Description

POWER ON RESET

The HM6F5221 generates a power on reset operation at power up.

REFERENCE OSCILLATOR INPUTS

The Reference oscillator frequency for RF and IF PLL is provided by an external reference through the OSC_{IN} pin. The OSC_{IN} block can operate up to 40MHz with an input sensitivity of 0.5 Vpp. It drives both the IF and the RF R counters in common input signal path. When an external TCXO is connected to the OSC_{IN} input pin, the TCXO drives both IF R counter and RF R counter.

REFERENCE DIVIDER

The RF and IF R Counters are clocked through the Oscillator block either separately or in common. The maximum frequency is 40MHz. RF R counter is 2 bits CMOS counters with a divide range from 1 to 3*(See the Table.7)* IF R counter is 15 bits CMOS counter with a divide range from 2 to 32767*(See the Table.3).*

PROGRAMMABLE DIVIDER

The RF and IF N Counters are clocked by the small signal finRF and finIF input pins respectively. The RF N counter consists of 5-bit programmable counter(B counter) and 4-bit swallow counter(A counter*)(See the Table.15 and the Table.16 and the Table.17).* The IF N counter consists of 12-bit programmable counter(B counter) and 6-bit swallow counter (A counter*)(See the Table.11 and the Table.12)*.

PRESCALER

The fully CMOS RF prescaler consists of a differential input buffer and CML frequency divider, while the fully CMOS IF prescaler consists of a differential input buffer and TSPC frequency divider. The input buffer amplifies an input signal from an internal VCO to the required level set by sensitivity requirements. The output of the RF amplifier delivers a differential signal to the RF divider with the correct DC level, while the IF amplifier a single-ended signal to the IF divider. Buffers is single-ended driven. The single-ended operation is preferred in typical applications.

The RF prescaler provides 8/9 or 12/13 prescaler ratios to allow the multi-modulus operation, while the IF circuitry contains 32/33 or 64/65 dual-modulus prescaler. The prescaler clocks the subsequent CMOS flip-flop chain comprising the fully programmable A and B counters*(See the Table.18 and the Table.13).*

FRACTIONAL COMPENSATION

(Σ–Δ modulator)

The RF part of HM6F5221 adopts the Σ–Δ modulator as core of the fractional counter that makes it possible to obtain divide ratio N to be a fractional number between two contiguous integers. The Σ–Δ modulator effectively randomizes the quantization noise generated from digitizing process and results in extreme suppression of in-band noise power by pushing it out to out-of-band as in conventional Σ–Δ data converter. This technique eliminates the need for compensation current injection into the loop filter and improves fractional spurious performance, suitable for high-tier applications.

For proper Σ–Δ modulator operation, the user should be kept in mind that

1. A fractional number should be set in the range from 0 to K-1 in step 1/K
2. The clock frequency (OSC_{IN}) that is higher than 10 MHz is recommended for better performance. But power consumption can be increase.

Note that the clock frequency much lower than 10MHz can deteriorate the fractional noise performance.
(See the Table.6 and the Table.15)

SERIAL INTERFACE

The programmable functions are accessed through the serial interface. The interface is made of 3 functions : clock, data, and latch enable(LE). Serial data for the

various counters is clocked in from data on the rising edge of clock, into the 24-bit shift register. Data is entered MSB first. The last two bits decode the internal register address. On the rising edge of LE, data stored in the shift register is loaded into one of the 4 appropriate latches (selected by address bits). A complete programming description is included in the following sections.

POWER CONTROL

Each PLL is individually power controlled by device enable pin or serial interface power down bits. The enable pins override the power down bits. The RIF_EN pin controls both the RF PLL and the IF PLL. When the pin is high, the power down bits determine the state of power control*(See the Table.5 and Table.9 and the Table.20).* Activation of any PLL power down mode results in the disabling of the respective N counter and de-biasing of its respective fin input (to a high impedance state). The R counter functionality also becomes disabled when power down bit is activated. The oscillator input block also powers down. Power down forces the respective charge pump and phase detector logic to a TRI-STATE condition. A power down counter reset function resets both N and R counters. Upon powering up the N counter resumes counting in close alignment with R counter (the maximum error is one prescaler cycle). The serial interface remains active and capable of loading and latching in data during all of power down modes.

PFD and CP

The RF/IF phase detector, composed of PFD and CP, outputs an average proportional to the phase difference of between outputs of N and R counter. This average is converted to the control voltage of VCO by external loop filter. The slope of the PFD is programmable using RF_R[16](RF_PFD_POL) and IF_R[17](IF_PFD_POL) depending on whether RF/IF VCO has positive slope or negative slope *(See the Table.4 for IF and the Table.8 for RF).* Also, the RF charge pump output current gain is set to either 1x or 2x using RF_R[17] (RF_CP_GAIN) and the IF charge pump output gain is set to either 1x or 2x using IF_R[18] (IF_CP_GAIN) slope *(See the Table.4 for IF and the Table.8 for RF).*

■ Programming Description

INPUT DATA REGISTER

The HM6F5221 can be programmed via the serial bus interface. The interface is made of 3 functional signals: **Clock**, **Data**, and load enable(**LE**). Serial data is moved into the 24-bit shift register on the rising edge of the clock. These data enters MSB first. When **LE** goes HIGH, data in the shift register is moved into one of the 4 latches(by the 2-bit control).

MSB ◀——— data flow(MSB first) **LSB**

DATA[23:2]	CTL[1:0]

Table.1 Control Bit Map (CTL[1:0])

CONTROL BITS		DATA LOCATION
C[1]	C[0]	
0	0	IF_R Register
0	1	IF_N Register
1	0	RF_R Register
1	1	RF_N Register

Table.2 Data Bit Map (DATA[23:2])

Register Name	REGISTER BIT LOCATION MSB → LSB																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF_R	FoLD		*X*	IF_PWDN		IF_CP		IF_R_DIV (15bit)															0	0
IF_N	IFSW	PRE	*VNT*			IF_B_DIV (12bit)											IF_A_DIV(6bit)						0	1
RF_R	FoLD		RF_PWDN		*X*		RF_CP		*X*	RF_R_DIV(2bit)		FRAC_K_DIV(11bit)											1	0
RF_N	RFSW	PRE	RF_B_DIV(5bit)					RF_A_DIV(4bit)				FRAC_F_DIV(11bit)											1	1

Note: *VNT(vendor test bits*) and *X* (dummy bit) are reserved.
They should be set to be zero (LOW) for normal usage.

■ Programming Description (Continued)

PROGRAMMABLE REFERENCE DIVIDERS

IF_R REGISTER

If the Control Bits(C[1:0]) are 00, data is moved from the 24-bit shift register into the IF_R register which sets the IF reference counter. Serial data format is shown in the table below.

MSB **IF_R[23:0]** **LSB**

FoLD [1:0]		X	IF_PWDN [1:0]		IF_CP [1:0]		IF_R_DIV [14:0]		C[1]	C[0]
23	22	21	20	19	18	17	16	2	1	0

Program Code → | ← Division Ratio of the IF R Counter → | Control Bits

Table.3 Binary 15-Bit Programmable IF R Divider Ratio (R Counter) (IF_R[16] –IF_R[2])

Division Ratio	IF_R [16]	IF_R [15]	IF_R [14]	IF_R [13]	IF_R [12]	IF_R [11]	IF_R [10]	IF_R [9]	IF_R [8]	IF_R [7]	IF_R [6]	IF_R [5]	IF_R [4]	IF_R [3]	IF_R [2]
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes : Division ratio: 3 to 32767 (The divide ratios less than 3 are prohibited)
Data shifted in MSB first.

Table.4 IF Charge Pump and Phase Frequency Control - (IF_CP) (IF_R[18:17])

IF_CP_GAIN	IF_PFD_POL

Acronym	Data Bits	Low(0)	High(1)	Comments
IF_CP_GAIN	IF_R[18]	1X	2X	IF Charge Pump Current Gain
IF_PFD_POL	IF_R[17]	Negative	Positive	IF Phase Detector Polarity

Table.5 IF Power Down and Power Down Mode - (IF_PWDN) (IF_R[20:19])

PWRDN_IF	PWRDN_MODE_IF

Acronym	Data Bits	Low(0)	High(1)	Comments
PWRDN_IF	IF_R[20]	Power Up	Power Down	IF Power Down
PWRDN_MODE_IF	IF_R[19]	Asynchronous power down	Synchronous power down	IF Power Down Mode Select

■ Programming Description (Continued)

Fout / Lock Detect Programming Bits - (FoLD)

See the RF_R register section for more detail.

RF_R REGISTER

If the Control Bits(C[1:0]) are 10, data is moved from the 24-bit shift register into the RF_R register which sets the RF reference (RF R counter; 2-bit) / fractional counter (K counter; 11-bit). Serial data format is shown below.

MSB **RF_R[23:0]** **LSB**

FoLD [1:0]		RF_PWDN [1:0]		*X*		RF_CP [1:0]		*X*	RF_R_DIV [1:0]		FRAC_K_DIV [10:0]		C[1]	C[0]
23	22	21	20	19	18	17	16	15	14	13	12	2	1	0

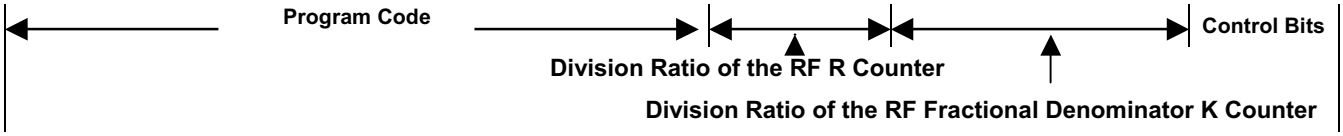


Table.6 Binary 11-Bit Programmable Fractional Denominator K Divider Ratio (K Counter) (RF_R[12:2])

Division Ratio	RF_R [12]	RF_R [11]	RF_R [10]	RF_R [9]	RF_R [8]	RF_R [7]	RF_R [6]	RF_R [5]	RF_R [4]	RF_R [3]	RF_R [2]
1	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Notes : Division ratio: 1 to 2047
Data shifted in MSB first.

Table.7 Binary 2-Bit Programmable RF R Divider Ratio (RF R Counter) (RF_R[14:13])

Division Ratio	RF_R [14]	RF_R [13]
1	0	1
2	1	0
3	1	1

Notice : We recommend that RF R divider ratio is 2. In this ratio, HM6F5201 have best optimized performance in power, fractional compensation and lock time.

■ Programming Description (Continued)

Table.8 RF Charge Pump and Phase Frequency Detector Control - (RF_CP) (RF_R[17:16])

RF_CP_GAIN	RF_PFD_POL

Acronym	Data Bits	Low(0)	High(1)	Comments
RF_CP_GAIN	RF_R[17]	1X	2X	RF Charge Pump Current Gain
RF_PFD_POL	RF_R[16]	Negative	Positive	RF Phase Detector Polarity

Table.9 RF Power Down and Power Down Mode - (RF_PWDN) (RF_R[21:20])

PWRDN_RF	PWRDN_MODE_RF

Acronym	Data Bits	Low(0)	High(1)	Comments
PWRDN_RF	RF_R[21]	Power Up	Power Down	RF Power Down
PWRDN_MODE_RF	RF_R[20]	Asynchronous power down	Synchronous power down	RF Power Down Mode Select

Table.10 Fout / Lock Detect Programming Truth Table - (FoLD) (IF_R[23:22] / RF_R[23:22])

RF_R[22] (RF LD)	IF_R[22] (IF LD)	RF_R[23] (RF Fo)	IF_R[23] (IF Fo)	FoLD Output State
0	0	0	0	Disabled
0	1	0	0	IF Lock Detect
1	0	0	0	RF Lock Detect
1	1	0	0	RF/IF Lock Detect
X	0	0	1	IF Reference Divider Output
X	0	1	0	RF Reference Divider Output
X	1	0	1	IF Programmable Divider Output
X	1	1	0	RF Programmable Divider Output
0	0	1	1	Disabled
0	1	1	1	IF Counter Reset
1	0	1	1	RF Counter Reset
1	1	1	1	RF and IF Counter Reset

X = Don't care condition

Notes :

When FoLD output is disabled, it is actively pulled to low logic state.

Lock detect output provided to indicate when the VCO frequency is in "LOCK". When the loop is locked and a lock detect mode is selected, the pins output is high with narrow pulses LOW. In RF/IF detect mode a locked condition is indicated when RF and IF are both locked.

■ Programming Description (Continued)

PROGRAMMABLE DIVIDER

IF_N REGISTERS

If the Control Bits(C[1:0]) are 01, data is transferred from the 24-bit shift register into the IF_N register which sets the IF programmable counter. IF N counter consists of swallow counter(A counter: 6-bit), main counter(B counter; 12-bit). Serial data format is shown below.

MSB **IF_N[23:0]** **LSB**

IFSW	PRE	VNT [1:0]		IF_B_DIV [11:0]		IF_A_DIV [5:0]		C[1]	C[0]
23	22	21	20	19	8	4	2	1	0

Program Code — **Division Ratio of the IF N Counter** — **Control Bits**

Table.11 Binary 6-Bit Programmable Swallow Counter Division Ratio (IF A Counter) (IF_N[7:2])

Division Ratio	IF_N [7]	IF_N [6]	IF_N [5]	IF_N [4]	IF_N [3]	IF_N [2]
0	0	0	0	0	0	0
1	0	0	0	0	0	1
•	•	•	•	•	•	•
63	1	1	1	1	1	1

Division ratio : 0 to 63 B > A

Table.12 Binary 12-Bit Programmable IF Main Counter Division Ratio (IF B Counter) (IF_N[19:8])

Division Ratio	IF_N [19]	IF_N [18]	IF_N [17]	IF_N [16]	IF_N [15]	IF_N [14]	IF_N [13]	IF_N [12]	IF_N [11]	IF_N [10]	IF_N [9]	IF_N [8]
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
5	0	0	0	0	0	0	0	0	0	1	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

Notes : Division ratio: 3 to 4095 (The division ratio less than 3 are prohibited)

Vendor Test Bits - (VNT) (IF_N[21:20])

Vendor test bits are for verification of some functions and characteristics. In normal usage, they should be set to LOW.

■ Programming Description (Continued)

Table.13 IF Prescaler Select - (PRE) (IF_N[22])

Acronym	Data Bits	Low(0)	High(1)	Comments
PRE	IF_N[22]	32/33	64/65	IF Prescaler Modulus Select

Notes : PRE (prescaler select) is used to set IF prescaler. The HM6F5221 contains two dual modulus prescaler for IF mode. It uses the 16/17 or 32/33 dual modulus prescaler mode to internally operate at 680 MHz ~ 1.1 GHz.

Table.14 IF Frequency Divider Select - (IFSW) (IF_N[23])

Acronym	Data Bits	Low(0)	High(1)	Comments
IFSW	IF_N[23]	Divide by 2	Divide by 4	IF Frequency Divider Ratio Select

Notes : IFSW (IF frequency divider select switch) is used to set IF output frequency divider ratio. You can select the divider ratio in order to use different communication systems.

RF_N REGISTER

If the Control Bits(C[1:0]) are 11, data is moved from the 24-bit shift register into the RF_N register, which sets the RF programmable counter. RF N counter consists of swallow counter(A counter: 4-bit), main counter(B counter; 5-bit) and RF fractional counter (F counter; 11-bit). Serial data format is shown below.

MSB **RF_N[23:0]** **LSB**

RFSW	PRE	RF_B_DIV [4:0]		RF_A_DIV [3:0]		FRAC_F_DIV [10:0]		C[1]	C[0]
23	22	21	17	16	13	12	2	1	0

Division Ratio of the RF N Counter — **Control Bits**

Division Ratio of the RF Fractional Numerator F Counter

Table.15 Binary 11-Bit Programmable Fractional Numerator F Divider Ratio (F Counter) (RF_N[12:2])

Division Ratio	RF_N [12]	RF_N [11]	RF_N [10]	RF_N [9]	RF_N [8]	RF_N [7]	RF_N [6]	RF_N [5]	RF_N [4]	RF_N [3]	RF_N [2]
1	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Notes : Division ratio: 1 to 2047

It is not allowed that Fractional F divider ratio is 0. Because values of F divider ratio is used as numerator.

■ Programming Description (Continued)

Table.16 Binary 4-Bit Programmable Swallow Counter Division Ratio (RF A Counter) (RF_N[16:13])

When RF prescaler has 12/13 divide ratio

Division Ratio	RF_N [16]	RF_N [15]	RF_N [14]	RF_N [13]
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
•	•	•	•	•
11	1	1	1	1

When RF prescaler has 8/9 divide ratio

Division Ratio	RF_N [16]	RF_N [15]	RF_N [14]	RF_N [13]
0	X	0	0	0
1	X	0	0	1
•	•	•	•	•
7	X	1	1	1
X	X	X	X	X

Notes : Division ratio : 0 to 11 B > A

Table.17 Binary 5-Bit Programmable RF Main Counter Division Ratio (RF B Counter) (RF_N[21:17])

Division Ratio	RF_N [21]	RF_N [20]	RF_N [19]	RF_N [18]	RF_N [17]
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
•	•	•	•	•	•
31	1	1	1	1	1

Notes : Division ratio: 3 to 31 (The division ratio less than 3 are prohibited)

Table.18 RF Prescaler Select - (PRE) (RF_N[22])

Acronym	Data Bits	Low(0)	High(1)	Comments
PRE	RF_N[22]	8/9	12/13	RF Prescaler Modulus Select

Notes : PRE (prescaler select) is used to set RF prescaler. The HM6F5221 contains two dual modulus prescaler. It uses the 8/9 or 12/13 dual modulus prescaler mode to operate at 500 MHz ~ 2.5 GHz.
In 8/9 dual modulus prescaler mode, HM6F5221 can operate up to 2.5GHz. But we recommend that you select RF prescaler mode following rule.

Table.19 RF Frequency Band Select - (RFSW) (RF_N[23])

Acronym	Data Bits	Low(0)	High(1)	Comments
RFSW	RF_N[23]	RF1 Out	RF2 Out	RF frequency band select

Notes : RFSW (RF mux control bit) is used to set RF output frequency band. You can select the one of two bands order to use different communication systems.

■ Program Mode Control

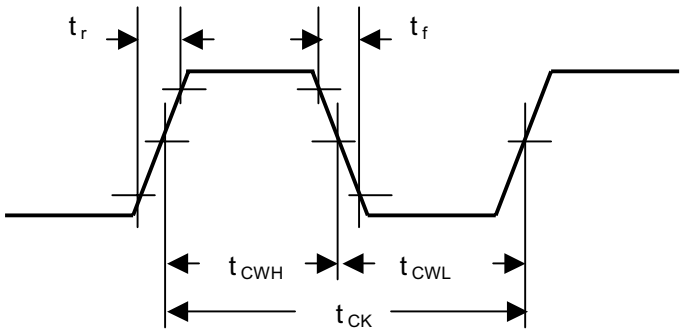
REFERENCE OSCILLATOR INPUT and POWER DOWN CONTROL

Table.20 Reference Oscillator Input and Power Down Control

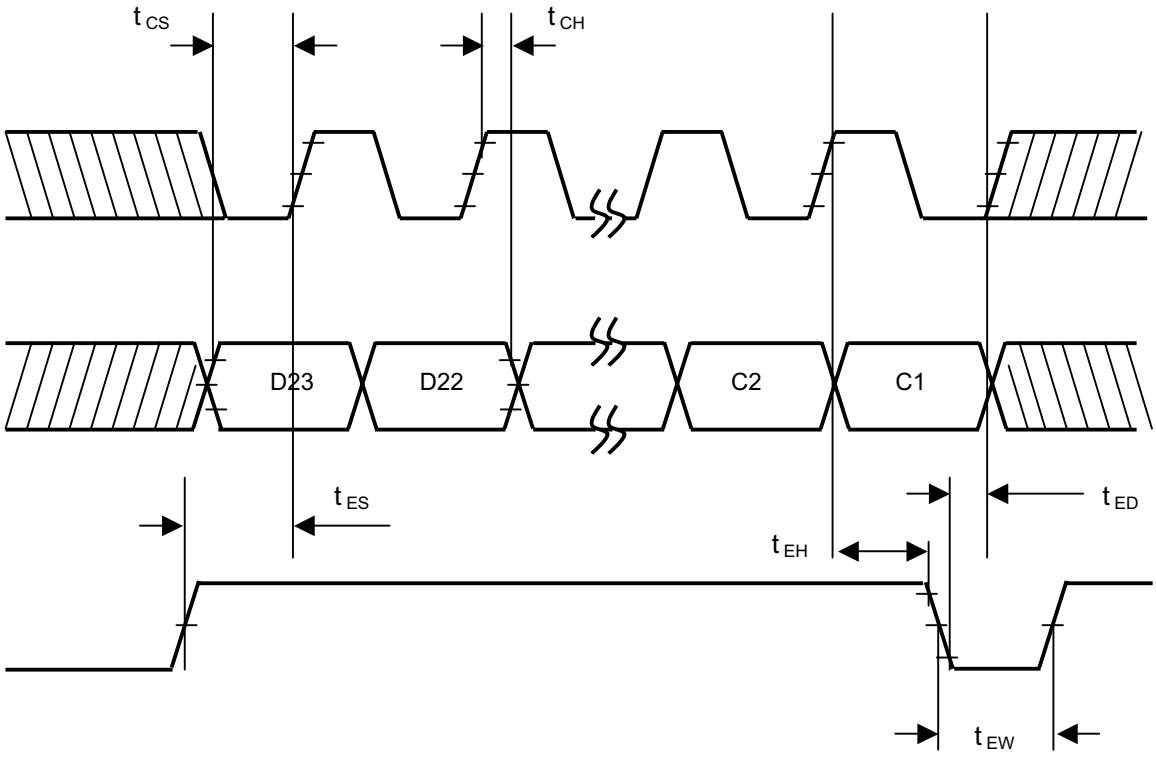
PWRDN_IF	PWRDN_RF	IF	RF
IF_R[18]	RF_R[21]		
0	0	OSC_{IN}	OSC_{IN}
0	1	OSC_{IN}	LOW (Power down)
1	0	LOW (Power down)	OSC_{IN}
1	1	LOW (Power down)	LOW (Power down)

■ Application Example

■ Serial Data Input Timing



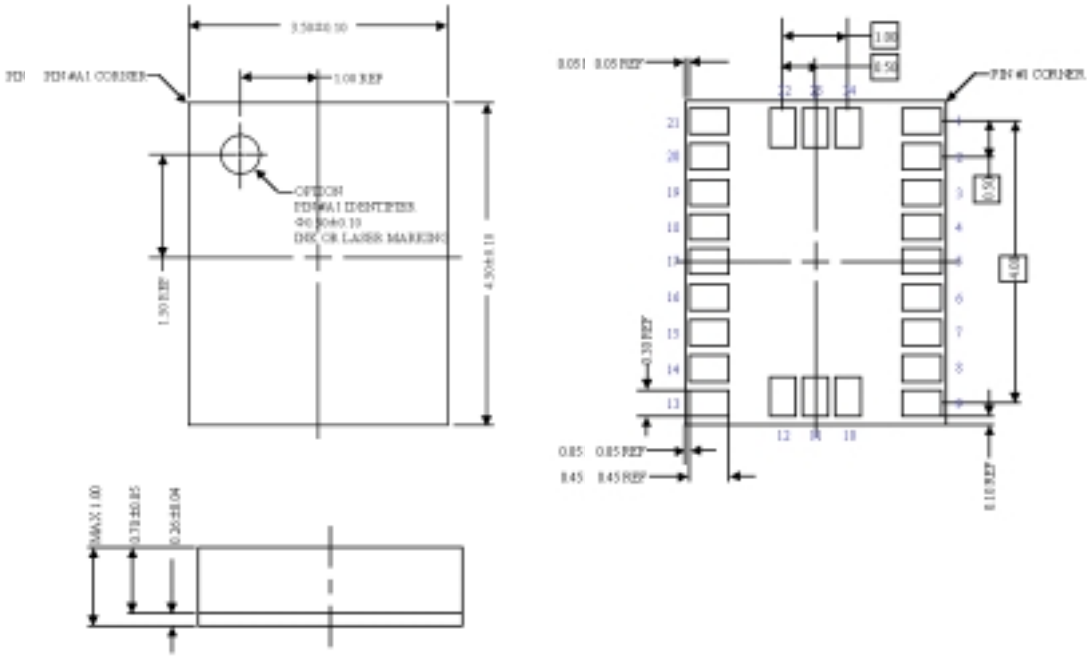
CLOCK Timing Diagram



Serial Data Timing Diagram

■ Package Outline

Physical Dimensions (unit : ㎜)



Leadless Grid Array Package