HD155101BF

RF Single-chip Linear IC for GSM and EGSM Systems

HITACHI

ADE-207-256A (Z)
2nd Edition
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Description

The HD155101BF was developed for GSM and EGSM cellular systems, and integrates most of the functions of a transceiver. The HD155101BF incorporates the bias circuit for a RF LNA, a 1st mixer, 1st-IF amplifier, 2nd mixer, AGC amplifier and an IQ quadrature demodulator for the receiver, and an IQ quadrature modulator and offset PLL for the transmitter. Also, on chip are the dividers for the 1st & 2nd local oscillator signals and 90˚ phase splitter. Moreover the HD155101BF includes control circuits to implement power saving modes. These functions can operate down to 2.7 V and are housed in a 48-pin LQFP SMD package.

Hence the HD155101BF can form a small size transceiver handset for GSM and EGSM by adding a PLL frequency synthesizer IC, a power amplifier and some external components. See page 7 “Configuration”.

The HD155101BF is fabricated using a 0.6 µm double-polysilicon Bi-CMOS process.

Functions

Receiver (RX)

- Low Noise Amplifier (LNA) bias circuit
- 1st mixer
- IF amplifier
- 2nd mixer
- Automatic gain control amplifier (AGC)
- IQ demodulator with 90° phase splitter

Transmitter (TX)

- IQ modulator with 90° phase splitter
- Offset PLL
  - — Down converter
  - — Phase comparator
  - — TX VCO driver

HD155101BF

Others

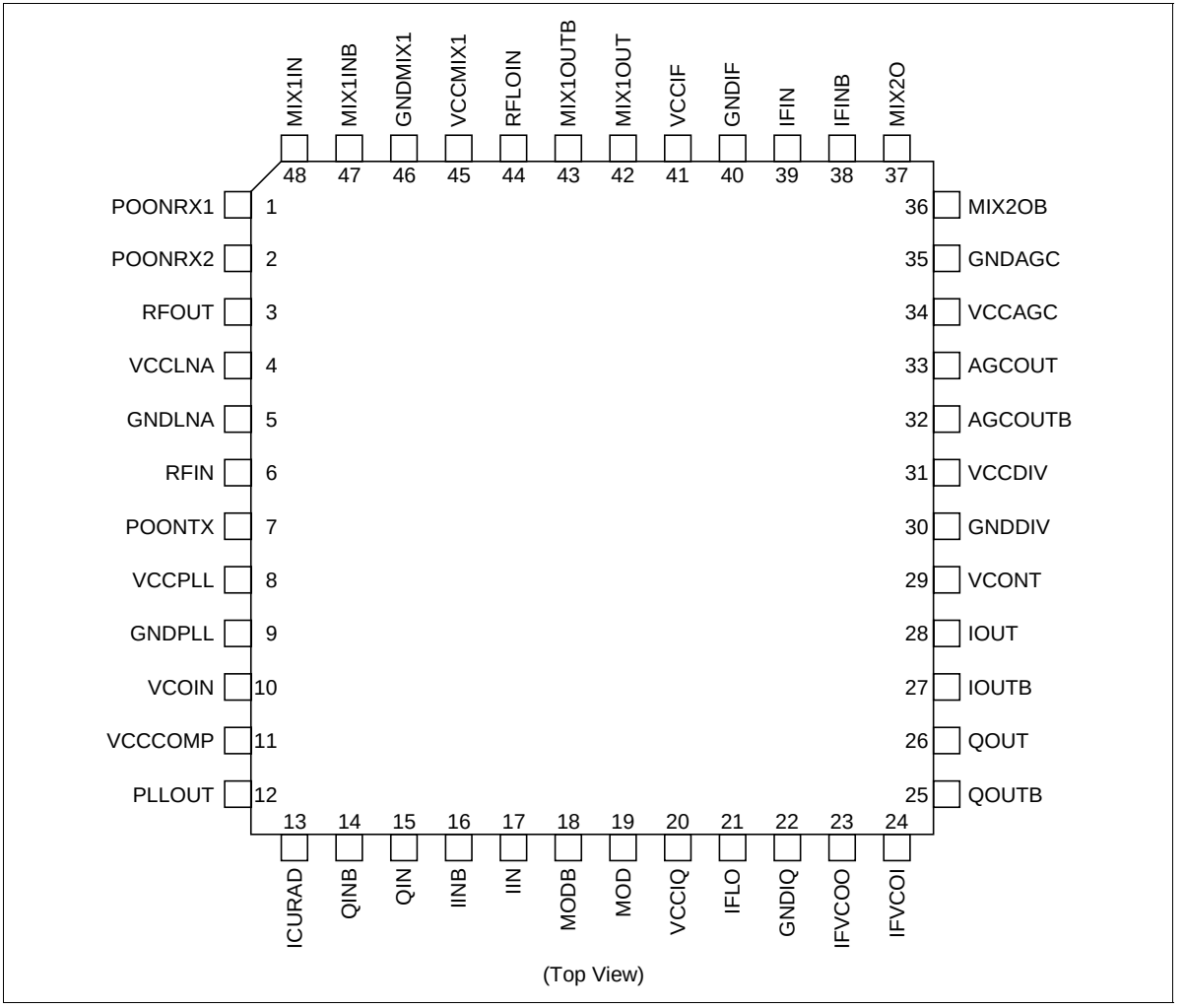
- IF dividers
- Power saving circuit
- IFVCO

Features

- Highly integrated RF processing for hand-portables
- Wide operating frequency
  RX:
  — RF: 925 to 960 MHz
  — 1st IF: 130 to 300 MHz
  — 2nd IF: 26 to 60 MHz
  TX:
  — RF: 880 to 915 MHz
  — IF: 156 to 360 MHz
- Offset PLL architecture reduces TX spurious
- Low current consumption (Vcc = 3 V)
  RX mode: 42.5 mA Typ (including IFVCO current (2.5 mA Typ)) + LNA transistor current (5.6 mA Typ)
  TX mode: 38.0 mA Typ (including IFVCO current (2.5 mA Typ))
  Idle mode: 1 μA Typ
- Operating supply voltage:
  — Phase comparator and TX VCO driver circuits: 2.7 to 5.25 V
  — Other blocks: 2.7 to 3.6 V
- Operating temperature range: –20 to +85°C
- 48 pin SMD Low Profile Quad Flat Package (LQFP): FP-48

Pin Arrangement

The HD155101BF is housed in a 48-pin LQFP SMD package to which is suitable for applications where space is limited. “Pin Functions” shows the arrangement and roles assigned for each pin of the HD155101BF.



(Top View)

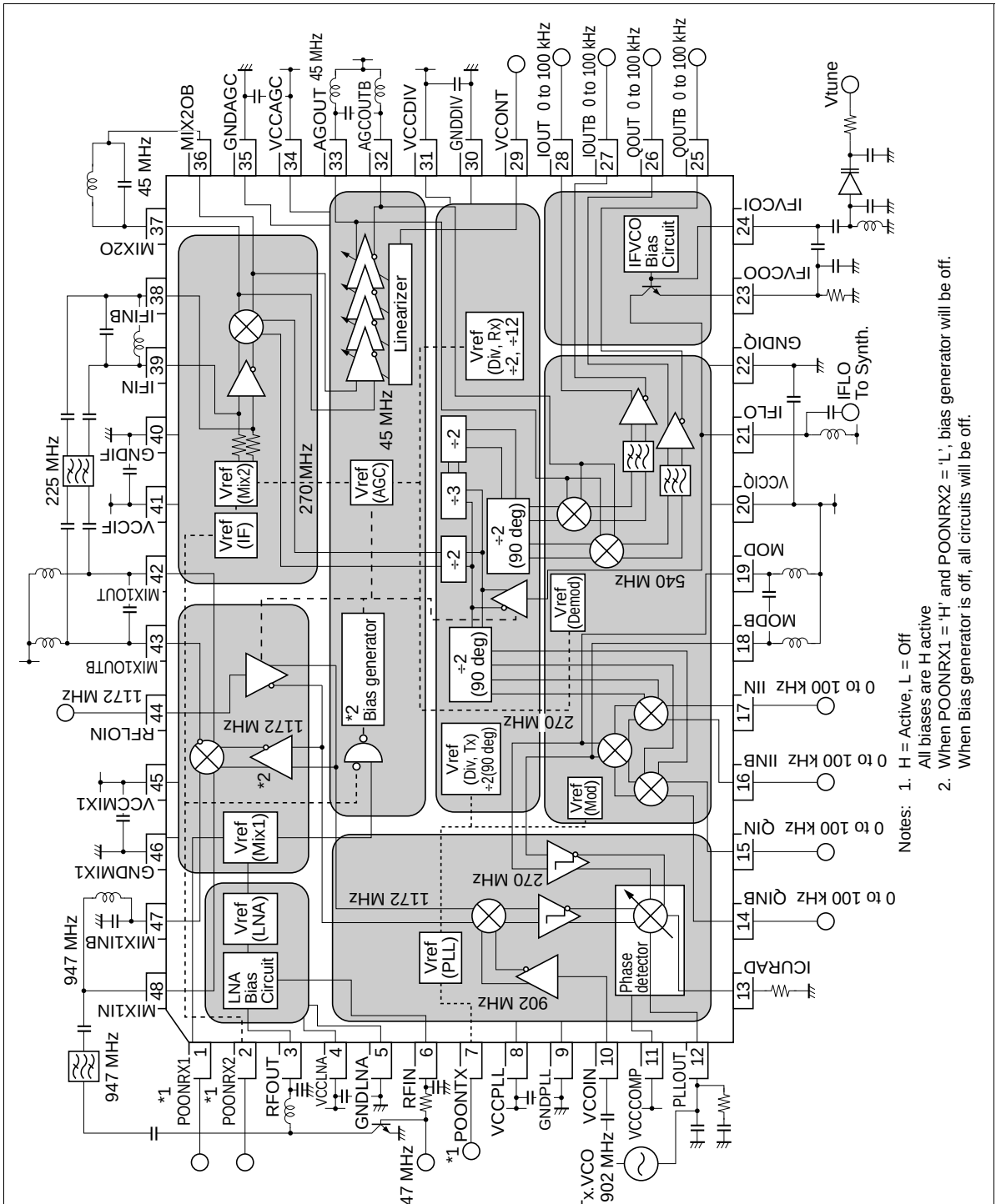
Pin Functions

Pin No.	Symbol	Input/ Output	Meaning of symbol	Function
1	POONRX1	Input	POwer ON for RX1	If 'H', LNA and MIX1 are active. Other receiver blocks don't care.
2	POONRX2	Input	POwer ON for RX2	LNA and MIX1 don't care. If 'H', Other receiver blocks are active.
3	RFOUT	Output	RF signal OUTput	Open collector type output of LNA. The collector of LNA transistor.
4	VCCLNA	Vcc	VCC of LNA block	Power supply of LNA
5	GNDLNA	Gnd	GND of LNA block	Ground of LNA
6	RFIN	Input	RF signal INput	Input of LNA. The base of LNA transistor
7	POONTX	Input	POwer ON for TX	If 'H', the blocks for transmitter are active. The reciver blocks don't care.
8	VCCPLL	Vcc	VCC of OPLL block	Power supply for offset PLL except phase comparator
9	GNDPLL	Gnd	GND of OPLL block	Ground of offset PLL
10	VCOIN	Input	VCO signal INput	Input of Tx. VCO signal
11	VCCCOMP	Vcc	VCC of phase COMParator	Power supply for just phase comparator of offset PLL
12	PLLOUT	Output	OPLL OUTput	Current output to control and modulate Tx. VCO This pin should be connected external loop filter.
13	ICURAD	Input	I CURrent ADjust	This pin should be connected an external R to determine charge pump current of phase comparator
14	QINB	Input	Q signal INput Bar	Q negative signal input of IQ quadrature modulator
15	QIN	Input	Q signal INput	Q positive signal input of IQ quadrature modulator
16	IINB	Input	I signal INput Bar	I negative signal input of IQ quadrature modulator
17	IIN	Input	I signal INput	I positive signal input of IQ quadrature modulator
18	MODB	Output	MODulator output Bar	Negative output of IQ quadrature modulator
19	MOD	Output	MODulator output	Positive output of IQ quadrature modulator
20	VCCIQ	Vcc	VCC of IQ block	Power supply of IQ block
21	IFLO	Input/ Output	IF LOcal signal input/output	IF local signal input to be fed to divider
22	GNDIQ	Gnd	GND of IQ block	Ground of IQ block
23	IFVCOO	Output	IFVCO Output	Emitter of IFVCO transistor
24	IFVCOI	Input	IFVCO Input	Base of IFVCO transistor

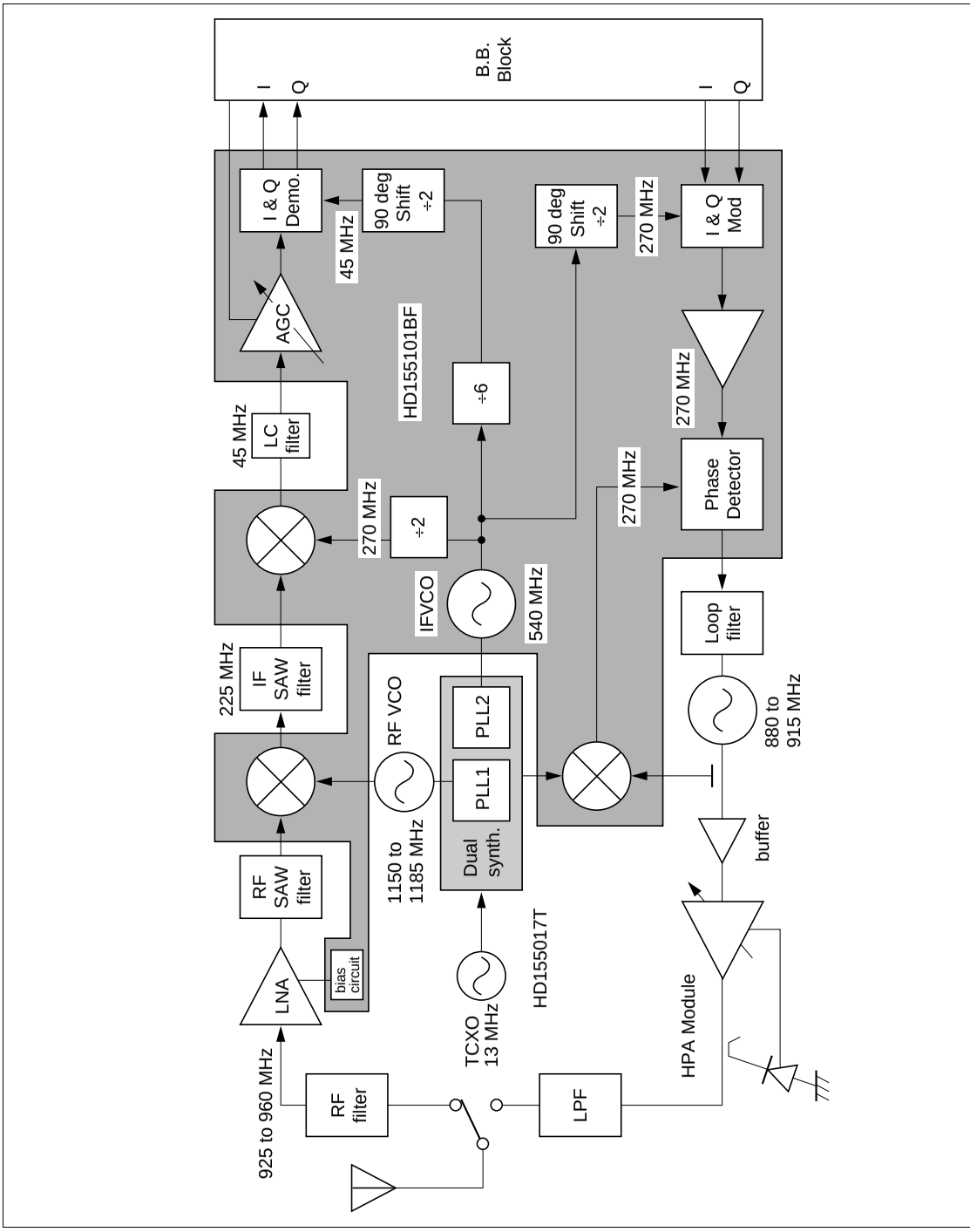
Pin Function (cont)

Pin No.	Symbol	Input/ Output	Meaning of symbol	Function
25	QOUTB	Output	Q signal OUTput Bar	Q negative signal output of IQ quadrature demodulator
26	QOUT	Output	Q signal OUTput	Q positive signal output of IQ quadrature demodulator
27	IOUTB	Output	I signal OUTput Bar	I negative signal output of IQ quadrature demodulator
28	IOUT	Output	I signal OUTput	I positive signal output of IQ quadrature demodulator
29	VCONT	Input	Voltage of AGC CONTrol	The DC voltage input to control the power gain of AGC
30	GNDDIV	Gnd	GND of DIVider block	Ground of divider to make IF local signals
31	VCCDIV	Vcc	VCC of DIVider block	Power supply of divider to make IF local signals
32	AGCOUTB	Output	AGC OUTput Bar	AGC negative signal output to be fed to IQ quadrature demodulator
33	AGCOUT	Output	AGC OUTput	AGC positive signal output to be fed to IQ quadrature demodulator
34	VCCAGC	Vcc	VCC of AGC block	Power supply of AGC
35	GNDAGC	Gnd	GND of AGC block	Ground of AGC
36	MIX2OB	Output	MIX2 Output Bar	2nd mixer (MIX2) negative signal output to be fed to AGC
37	MIX2O	Output	MIX2 Output	2nd mixer (MIX2) positive signal output to be fed to AGC
38	IFINB	Input	1stIF signal INput Bar	IFAMP negative signal input for 1st IF signal
39	IFIN	Input	1stIF signal INput	IFAMP positive signal input for 1st IF signal
40	GNDIF	Gnd	GND of IFMIX2 block	Ground of IFAMP and 2nd mixer (MIX2)
41	VCCIF	Vcc	VCC of IFMIX2 block	Power supply of IFAMP and 2nd mixer (MIX2)
42	MIX1OUT	Output	MIX1 Output	1st mixer (MIX1) positive signal output
43	MIX1OUTB	Output	MIX1 Output Bar	1st mixer (MIX1) negative signal output
44	RFLOIN	Input	RF LOcal signal INput	RF 1st local signal input to be fed to 1st mixer (MIX1) and the down converter of offset PLL
45	VCCMIX1	Vcc	VCC of MIX1 block	Power supply of 1st mixer (MIX1)
46	GNDMIX1	Gnd	GND of MIX1 block	Ground of 1st mixer (MIX1)
47	MIX1INB	Input	MIX1 Input Bar	1st mixer (MIX1) negative signal input
48	MIX1IN	Input	MIX1 Input	1st mixer (MIX1) positive signal input

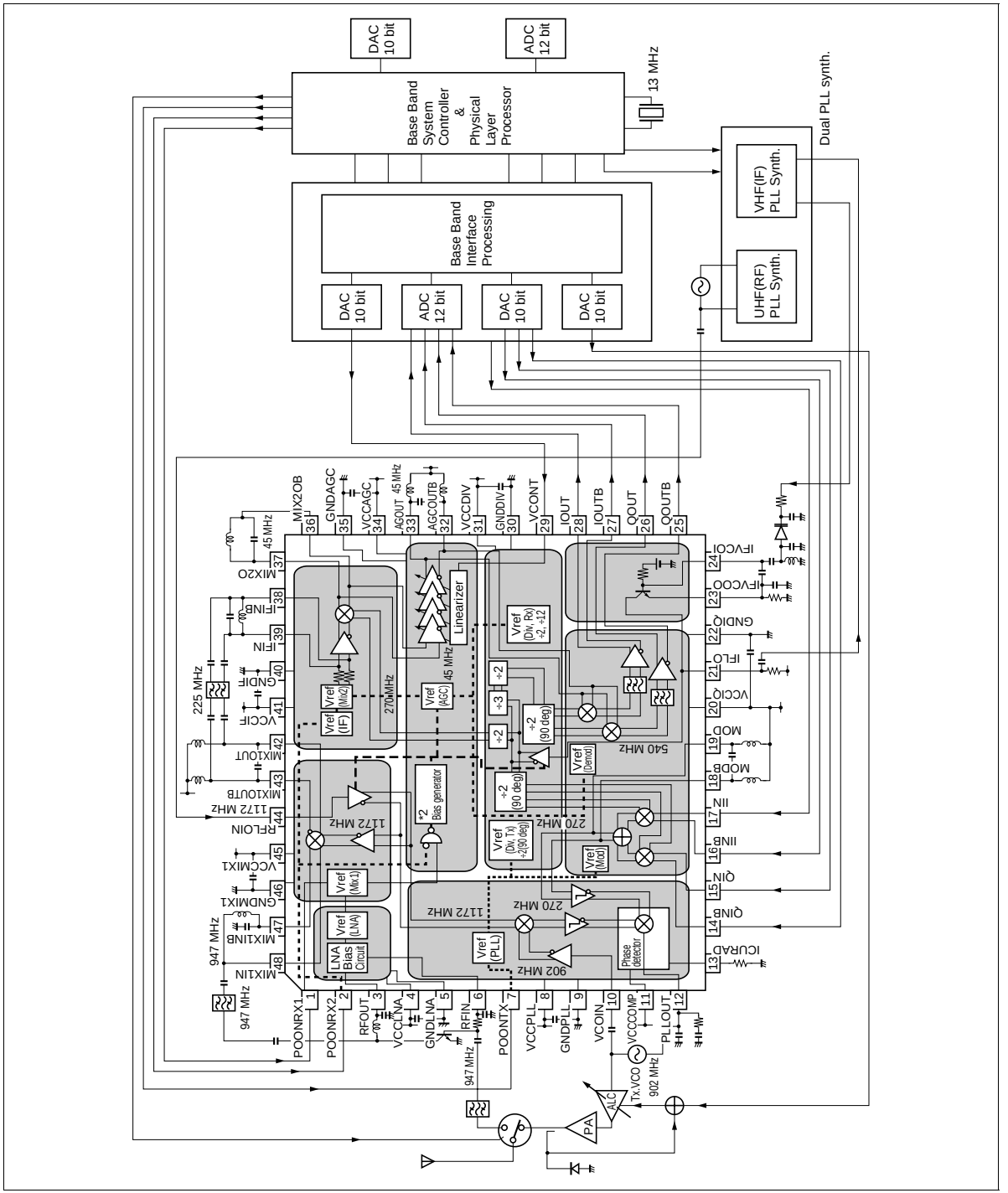
Block Diagram



Configuration



A GSM Application Example



Functional Operation

The HD155101BF has been designed from system stand point and incorporated a large number of the circuit blocks necessary in the design of a digital cellular handset.

Receiver Operation

The HD155101BF incorporates a LNA bias circuit for an external RF transistor, whose NF and power gain can be better selected.

This circuit amplifies the RF signal after selection by the antenna filter before the signal enters the first mixer section. The RF signal is combined with a high side local oscillator (LO) signal to generate a wanted first IF signal in the 130 to 300 MHz range. The 1st mixer circuit uses a double-balanced Gilbert cell architecture, which has open collector differential outputs. If, at 225 MHz, a 800 Ω LC load is connected to the mixer's outputs then a SSB NF of 9.0 dB with a gain of 7.0 dB is realizable. The corresponding input compression point is –11 dBm, which allows the device to be used within a GSM and EGSM system.

A filter is used after the 1st mixer to provide image rejection and the conditioned signal is then passed through an intermediate amplifier, before being down converted to a second IF in the range of 26 to 60 MHz.

The second mixer can generate a 45 MHz 2nd IF, if a 270 MHz 2nd LO signal is used. The 2nd LO is obtained by dividing the IFLO signal by 2. The 2nd mixer also uses the Gilbert cell architecture, but with internal resistive differential outputs of 300 Ω. IF amplifier and second mixer has a SSB NF of 5.6 dB, a power gain of 12 dB and an input compression point of –25 dBm. In order to improve the blocking characteristics of the device an external LC resonator across the differential outputs of the second mixer is recommended.

The signal is then passed to the AGC circuit, which has a dynamic range of more than 80 dB (–42 dB to +55 dB Typ) and is controlled by a DC voltage, which is generated by the microprocessor. This DC control range is from 0.15 V to 2.3 V. The AGC, which is designed for the GSM system, provides a linearity of ±1.0 dB in any 20 dB window. The outputs of the AGC are 2 kΩ differential and are connected the external supply via inductors.

The signal is then down converted by a demodulator to I and Q. Internal divider circuits convert the IFLO signal to the same frequency as the 2nd IF before passing this local signal through a phase splitter / shifter in order to generate the in phase and quadrature IQ components. The phase accuracy of the IQ demodulator is < ±1° and the amplitude mismatch is < ±0.5 dB. In order to accommodate different baseband interfaces the HD155101BF IQ differential outputs have a voltage swing of 2.4 Vp-p and a DC offset of < ±60 mV. Within each output stage a 2nd order Butterworth filter (fc = 210 kHz), is used to improve the blocking performance of the device.

In order to allow flexibility in circuit implementation the HD155101BF can configured to use either a single-ended or balanced external circuitry and components.

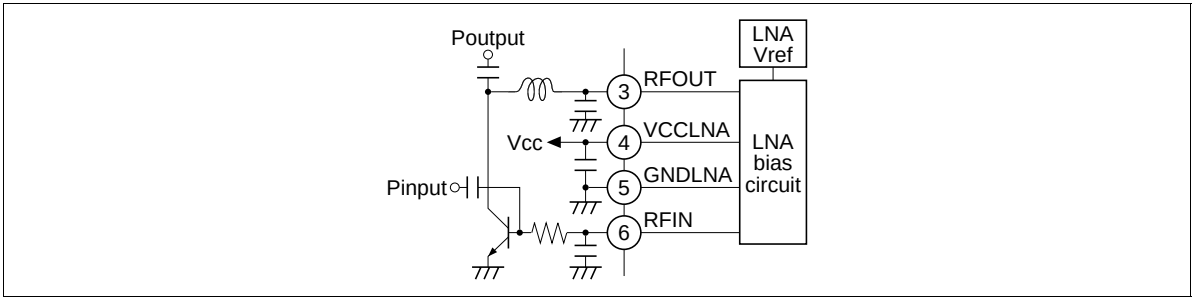


Figure 1 LNA Bias Circuit

Transmitter Operation

The transmitter chain converts differential IQ baseband signals to a suitable format for transmission by a power amplifier.

The common mode DC voltage range of the modulator inputs is 0.8 to 1.2 V and they have 2.4 Vp-p Max differential swing. The modulator circuit uses double-balanced mixers for the I and Q paths. The LO signals are generated by dividing the IFLO signal by 2 and then passing them through a phase splitter / shifter. The IF signals generated are then summed and produce a single modulated IF signal which is amplified and fed into the offset PLL block. Carrier suppression due to the mixer circuit is better than 31 dBc. However, if the common mode DC voltage of the I and Q inputs is adjusted, carrier suppression can be improved better than 40 dBc easily. In addition, upper side-band suppression is better than 35 dBc.

Within the offset PLL block there is a down converter, a phase comparator and a VCO driver. The down converter mixes the 1st LO signal and the TX VCO to create a reference LO signal for use in the offset PLL circuit. The phase comparator and the VCO driver generate an error current, which is proportional to the phase difference between the reference IF and the modulated IF signals. This current is used in a 2nd order loop filter to generate a voltage, which in turn modulates the TX VCO. In order to optimize the PLL loop gain, the error current value can be modified by changing the value of an external resistor - ICURAD. In order to accommodate a range of TX VCO, the offset PLL circuit has been designed to operate with a supply voltage of up to 5.25 V.

Operating Modes

The HD155101BF has the necessary control circuitry to implement the necessary states within the GSM system. Also provided is a power save mode which reduces the current consumption of the device by powering down unnecessary function blocks. Three pins are assigned for mode control, POONRX1, POONRX2 and POONTX. Table 1 shows the relationship between the pins and the required operating mode. Control of these pins are by the system controller.

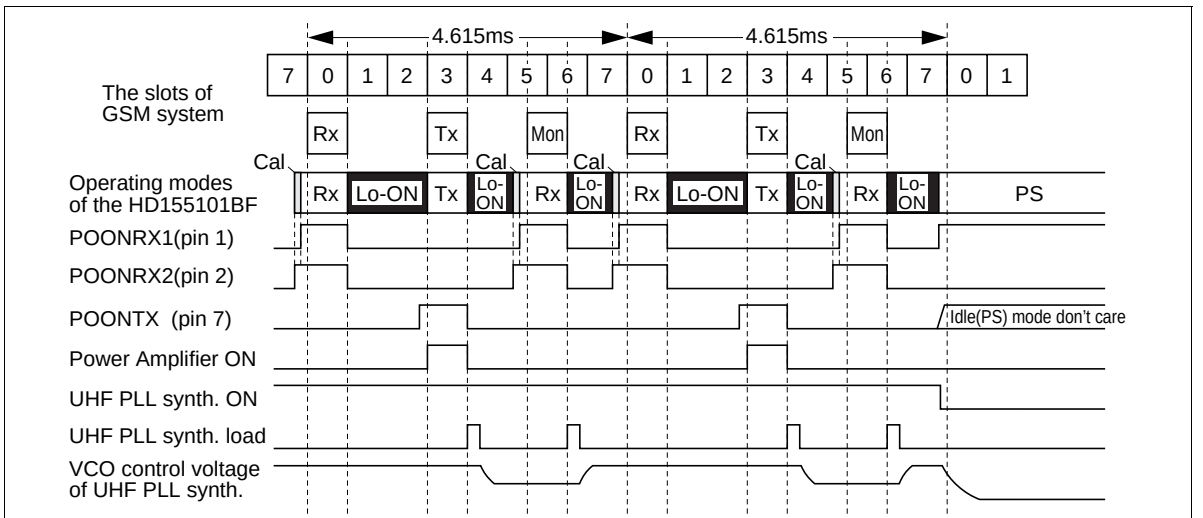
As per GSM requirements the TX and RX sections are not on at the same time. For the receiver there is a calibration mode for which the LNA bias circuit and 1st mixer are switched off. During this period the gain of the AGC can be adjusted. Also the DC offsets of the IQ demodulator are measured and subsequently canceled.

In order to change between the RX and TX modes a state called “warm-up” is used to ensure that the LO

Power saving is implemented through use of the idle mode. All function blocks of the HD155101BF are switched off until such time as the system controller commends the device to power up again.

Table 1 Operating Modes with Power Saving

		Receive (Rx)	Calibrate (Cal)	Warm-up (Lo-ON)	Transmit (Tx)	Idle (PS)
Mode	POONRX1 (pin 1)	H	L	L	L	H
switch	POONRX2 (pin 2)	H	H	L	L	L
	POONTX (pin 7)	L	L	L	H	Don't care
HD155101BF	LNA bias	ON	OFF	OFF	OFF	OFF
circuit status	1st mixer	ON	OFF	OFF	OFF	OFF
	IF AMP	ON	ON	OFF	OFF	OFF
	2nd mixer	ON	ON	OFF	OFF	OFF
	AGC	ON	ON	OFF	OFF	OFF
	IO demodulator	ON	ON	OFF	OFF	OFF
	Divider (Rx.)	ON	ON	OFF	OFF	OFF
	Divider (Tx.)	OFF	OFF	OFF	ON	OFF
	IO modulator	OFF	OFF	OFF	ON	OFF
	Offset PLL	OFF	OFF	OFF	ON	OFF
	RF 1st local buffer	ON	ON	ON	ON	OFF
	IF local buffer	ON	ON	ON	ON	OFF
	IFVCO	ON	ON	ON	ON	OFF
	Total current	42.5 mA Typ	32 mA Typ	10.5 mA Typ	38 mA Typ	1 µA Typ



IFVCO Operation

The HD155101BF incorporates an IFVCO circuit. The IFVCO circuit consists of an IFVCO transistor and a bias circuit for it, whose current are 2.0 mA and 0.5 mA respectively. If an internal IFVCO is used, treat pin 23 (IFVCOO), pin 24 (IFVCOI) and pin 21 (IFLO) as shown figure 3-(a).

Using an external IFVCO, pin 23 (IFVCOO) and pin 24 (IFVCOI) cannot be connected any pattern and component, and any component to feed direct current must be also removed from pin 21 (IFLO).

If pin 23 (IFVCOO), pin 24 (IFVCOI) and pin 21 (IFLO) are treated as shown figure 3-(b), current consumption will decrease 2.0 mA.

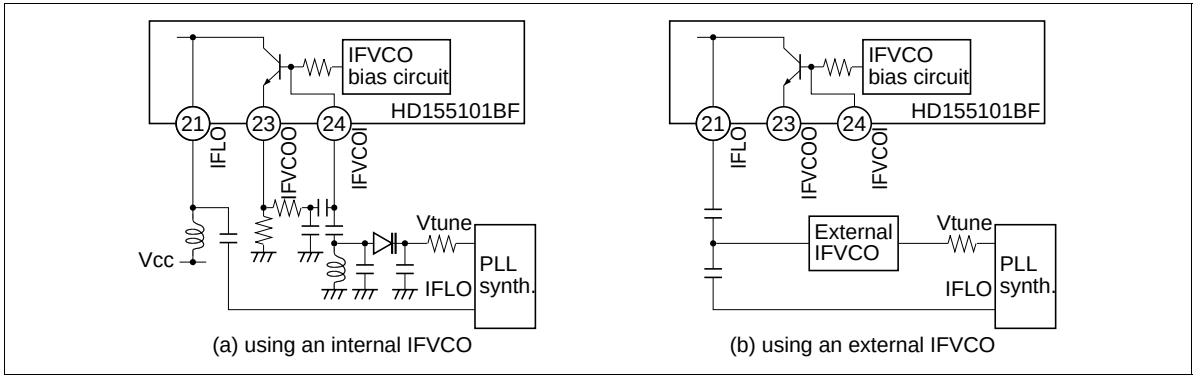


Figure 3 Control Diagram for Operating Mode Selection

Absolute Maximum Ratings

Any stresses in excess of the absolute maximum ratings can cause permanent damage to the HD155101BF.

Item	Symbol	Rating	Unit
Power supply voltage (VCC)	VCC	–0.3 to +4.0	V
Power supply voltage (VCCCOMP)	VCCCOMP	VCC to +5.5	V
Pin voltage	V_T	–0.3 to VCC + 0.3 (6.0 Max)	V
Maximum power dissipation	P_T	400	mW
Operating temperature	Topr	–20 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Electrical Characteristics (Ta = 25°C)

Specifications

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable pins	Note
Power supply voltage (1)	V_{CC}	2.7	3.0	3.6	V		4, 8, 20, 31, 34, 41, 45	
Power supply voltage (2)	V_{CCCOMP}	2.7	3.0	5.25	V		11	
Power supply current (Rx.)	$I_{CC(Rx.)}$	—	42.5	60.0	mA	V_{CC} = 3.0V V_{CCCOMP} = 3.0V	4, 8, 20, 31, 34, 41, 45, 11	
Power supply current (Tx.)	$I_{CC(Tx.)}$	—	38.0	55.0	mA	V_{CC} = 3.0V V_{CCCOMP} = 3.0V	4, 8, 20, 31, 34, 41, 45, 11	
Power supply current (Lo-ON)	$I_{CC(Lo-ON)}$	—	10.5	15.0	mA	V_{CC} = 3.0V V_{CCCOMP} = 3.0V	4, 8, 20, 31, 34, 41, 45, 11	
Power saving mode supply current	$I_{CC(PS)}$	—	1.0	10.0	µA	V_{CC} = 3.0V V_{CCCOMP} = 3.0V	4, 8, 20, 31, 34, 41, 45, 11	
Power up time (Rx.)	$t\ up_{(Rx.)}$	—	1.5	(5.0)	µsec	V_{CC} = 3.0V V_{CCCOMP} = 3.0V		from PS mode
Power up time (Tx.)	$t\ up_{(Tx.)}$	—	0.2	(0.5)	µsec	V_{CC} = 3.0V V_{CCCOMP} = 3.0V		from PS mode
Power on control voltage range (Rx1, Rx2, Tx)	$Vthon_{RX1}$ $Vthon_{RX2}$ $Vthon_{TX}$	2.3	—	—	V	V_{CC} = 3.0V	1 2 7	
Power off control voltage range (RX1, Rx2, Tx)	$Vthoff_{RX1}$ $Vthoff_{RX2}$ $Vthoff_{TX}$	—	—	0.8	V	V_{CC} = 3.0V	1 2 7	
I/Q common-mode output voltage	V_{IOcom}/ V_{QOcom}	1.1	1.3	1.5	V	V_{CC} = 3.0V	25, 26 27, 28	
I/Q differential output swing	V_{IOsw}/ V_{QOsw}	2.4	3.0	—	Vp-p	V_{CC} = 3.0V $V_{IOUT} - V_{IOUTB}$ $V_{QOUT} - V_{QOUTB}$	25, 26 27, 28	
I/Q output offset voltage	$V_{IOoffset}$/ $V_{QOoffset}$	–60	0	+60	mV	V_{CC} = 3.0V $V_{IOUTDC} - V_{IOUTBDC}$ $V_{QOUTDC} - V_{QOUTBDC}$	25, 26 27, 28	
I/Q common-mode input voltage	V_{IIcom}/ V_{QIcom}	(0.8)	1.0	(1.2)	V	V_{CC} = 3.0V	14, 15 16, 17	
I/Q differential input swing	V_{IIsw}/ V_{QIsw}	—	2.0	(2.4)	Vp-p	V_{CC} = 3.0V $V_{IIN} - V_{IINB}$ $V_{QIN} - V_{QINB}$	14, 15 16, 17	

Note: ( ) : These data are actual spread, not guaranteed.

Block Specifications

- Specifications of LNA

Item	Min	Typ	Max	Unit	Test Conditions
Frequency (RF)	925	940	960	MHz	
Power gain	—	18.0	—	dB	RF = 940MHz , Pin = –50dBm
Noise figure	—	1.75	—	dB	RF = 940MHz
i/p IP3	—	–1.0	—	dBm	RF1 = 940.8MHz, RF2 = 941.6MHz
o/p IP3	—	16	—	dBm	RF1 = 940.8MHz, RF2 = 941.6MHz
i/p CP	—	–11.5	—	dBm	RF = 940MHz
o/p CP	—	5.5	—	dBm	RF = 940MHz
Load Z	—	50	—	Ω	50Ω Typ
i/p Z	—	50	—	Ω	50Ω Typ
i/p VSWR	—	1.5	—		RF = 940MHz, 50Ω
o/p VSWR	—	1.5	—		RF = 940MHz, 50Ω
I_{CC} @LNA Trs.	4.7	5.6	6.8	mA	Only Trs. current

Note: These AC characteristics are shown for reference only and do not form part of the HD155101BF component specification.

- Specifications of Mixer 1 (Output Load = 400Ω + 400Ω balanced)

Item	Min	Typ	Max	Unit	Test Conditions
Frequency (RF)	925	940	960	MHz	
Frequency (LO)	1055	1165	1260	MHz	
Frequency (IF)	(130)	225	(300)	MHz	
Conversion gain	4.5	7.0	9.0	dB	RF = 940MHz/Pin = –50dBm, LO = 1165MHz/Pin = –10dBm, IF = 225MHz
Noise figure	(6.0)	9.0	(12.0)	dB	RF = 940MHz, LO = 1165MHz/Pin = –10dBm, IF = 225MHz
i/p IP3	—	–1.0	—	dBm	RF1 = 940.8MHz, RF2 = 941.6MHz, LO = 1165MHz/Pin = –10dBm
o/p IP3	—	6.0	—	dBm	RF1 = 940.8MHz, RF2 = 941.6MHz, LO = 1165MHz/Pin = –10dBm
i/p CP	–13.5	–11.0	(–8.0)	dBm	RF = 940MHz, LO = 1165MHz/Pin = –10dBm, IF = 225MHz
o/p CP	(–9.5)	–5.0	(–0.5)	dBm	RF = 940MHz, LO = 1165MHz/Pin = –10dBm, IF = 225MHz
RF i/p VSWR	—	1.5	(2.0)		RF = 940MHz, 50Ω
LO i/p VSWR	—	1.5	(2.0)		RF = 1165MHz, 50Ω
IF o/p VSWR	—	1.5	(2.0)		RF = 225MHz, 800Ω (400Ω + 400Ω Balanced)

- Specifications of IFAmp + Mixer 2

Item	Min	Typ	Max	Unit	Test Conditions
Input frequency (IF1)	(130)	225	(300)	MHz	
Frequency (LO2)	(156)	270	(360)	MHz	LO2 = IFLO/2
Output frequency (IF2)	(26)	45	(60)	MHz	
Conversion gain	9.0	12.0	14.5	dB	IF1 = 225MHz/Pin = –40dBm, IFLO = 540MHz/Pin = –10dBm, IF2 = 45MHz
Noise figure	(4.5)	5.6	(7.0)	dB	IF1 = 225MHz, IFLO = 540MHz/Pin = –10dBm, IF2 = 45MHz
i/p IP3	—	–16.0	—	dBm	IF11 = 225.8MHz, IF2 = 226.6MHz, IFLO = 540MHz/Pin = –10dBm
o/p IP3	—	–4.0	—	dBm	IF11 = 225.8MHz, IF2 = 226.6MHz, IFLO = 540MHz/Pin = –10dBm
i/p CP	–27.5	–25.0	(–23.0)	dBm	IF1 = 225MHz, IFLO = 540MHz/Pin = –10dBm, IF2 = 45MHz
o/p CP	(–18.0)	–14.0	(–11.0)	dBm	IF1 = 225MHz, IFLO = 540MHz/Pin = –10dBm, IF2 = 45MHz
Isolation	(55)	60	—	dB	Between mixer 1 outputs and IFAmp inputs

Note: ( ) : These data are actual spread, not guaranteed.

- Specifications of AGC

Item	Min	Typ	Max	Unit	Test Conditions
Input frequency	(26)	45	(60)	MHz	
Control voltage range	0.15	—	2.3	V	
Gain range	89	98	107	dB	Gain 1 – Gain 3
Gain linearity	(–1.0)	—	(1.0)	dB	in any 20dB window
Gain 1	45	55	65	dB	Vcont = 2.3V
Gain 2	13	23	33	dB	Vcont = 1.5V
Gain 3	–55	–40	–35	dB	Vcont = 0.15V
i/p CP 1	(–64)	–59	—	dBm	Gain = 50dB
i/p CP 2	(–34)	–29	—	dBm	Gain = 10dB
i/p CP 3	(–22)	–17	—	dBm	Gain = –30dB

Note: ( ) : These data are actual spread, not guaranteed.

- Specifications of IQ Demodulator

Item	Min	Typ	Max	Unit	Test Conditions
Power gain	–0.5	1.4	3.5	dB	IF2 = 45MHz, Pin = –25dBm, Rout = 10kΩ, IFLO = 540MHz, Pin = –10dBm
i/p CP	(–17.5)	–16.0	(–14.0)	dBm	IF2 = 45MHz, Baseband = 67.7kHz, IFLO = 540MHz, Pin = –10dBm
o/p CP	(–19.0)	–15.6	(–12.0)	dBm	IF2 = 45MHz, Baseband = 67.7kHz, IFLO = 540MHz, Pin = –10dBm
IQ phase accuracy	–1.0	0	1.0	deg.	Baseband = 67.7kHz
IQ amplitude mismatch	(–0.5)	0.1	(0.5)	dB	Baseband = 67.7kHz
Output DC offset voltage	–60	0	60	mV	|IOUT – IOUTB| and |QOUT – QOUTB|
IQ differential output swing	2.4	3.0	—	Vp-p	Baseband = 67.7kHz |IOUT – IOUTB| and |QOUT – QOUTB|
I/Q common mode output voltage	1.1	1.3	1.5	V	V_{CC} = 3.0V

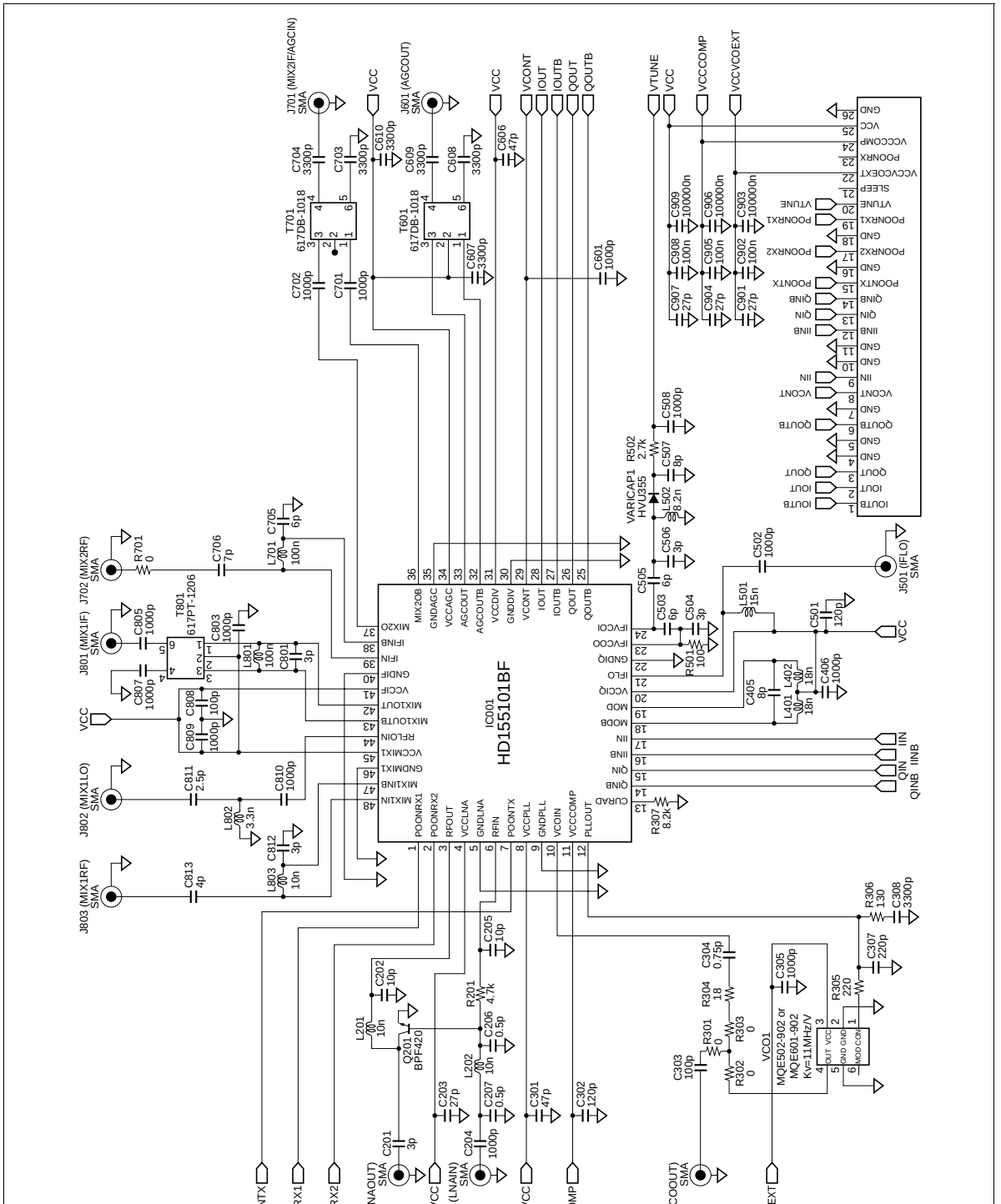
Note: ( ) : These data are actual spread, not guaranteed.

- Specifications of IQ Modulator and Offset PLL
  (RFLO and IFLO signals are supplied by Signal Generator)

Item	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions** (Loop bandwidth = 1.4MHz)
Frequency (RF)	880	902	915	MHz	
Frequency (LO)	1055	1172	1260	MHz	
Frequency (IF)	(120)	135	(180)	MHz	
Power up time	—	0.3	(0.5)	µsec	from PS mode
Lock up time	—	20	(80)	µsec	from PS mode to 915MHz
Carrier suppression ratio	31	40	—	dBc	All '1' GMSK (Baseband = 67.7kHz)
Upper side-band suppression ratio	35	45	—	dBc	I/Q differential input swing = 2.0Vp-p I/Q common mode input voltage = 1.0V
Phase accuracy	—	0.94	(2.5)	deg. rms	200kHz Bandwidth
(PN9, GMSK)	—	2.27	(6.0)	deg. peak	200kHz Bandwidth
Modulation spurious	—	–36.5	(–33.0)	dBc	200kHz offset / 30kHz Bandwidth
(PN9, GMSK)	—	–70.0	(–63.0)	dBc	400kHz offset / 30kHz Bandwidth
	—	–74.0	(–63.0)	dBc	600kHz to 1.8MHz offset / 30kHz Bandwidth
	—	–77.0	(–66.0)	dBc	1.8MHz to 3MHz offset / 100kHz Bandwidth
	—	–80.5	(–68.0)	dBc	3MHz to 6MHz offset / 100kHz Bandwidth
	—	–82.0	(–74.0)	dBc	6MHz upwards offset / 100kHz Bandwidth
Tx noise in RX band	—	–157	(–151)	dBc/Hz	925MHz to 935MHz (10MHz up from Tx band)
(Tx power = 0dBc = 30dBm)	—	–165	(–163)	dBc/Hz	935MHz to 960MHz (20MHz up from Tx band)
Isolation of the 1st local input to TXVCO input	(40)	43	—	dB	
IQ differential input swing	—	2.0	(2.4)	Vp-p	|IIN – IINB| and |QIN – QINB|
I/Q common mode input voltage	(0.8)	1.0	(1.2)	V	

Note: ( ) : These data are actual spread, not guaranteed.

Test Circuit



Measurement Results

LNA Measurement Results (for reference only)

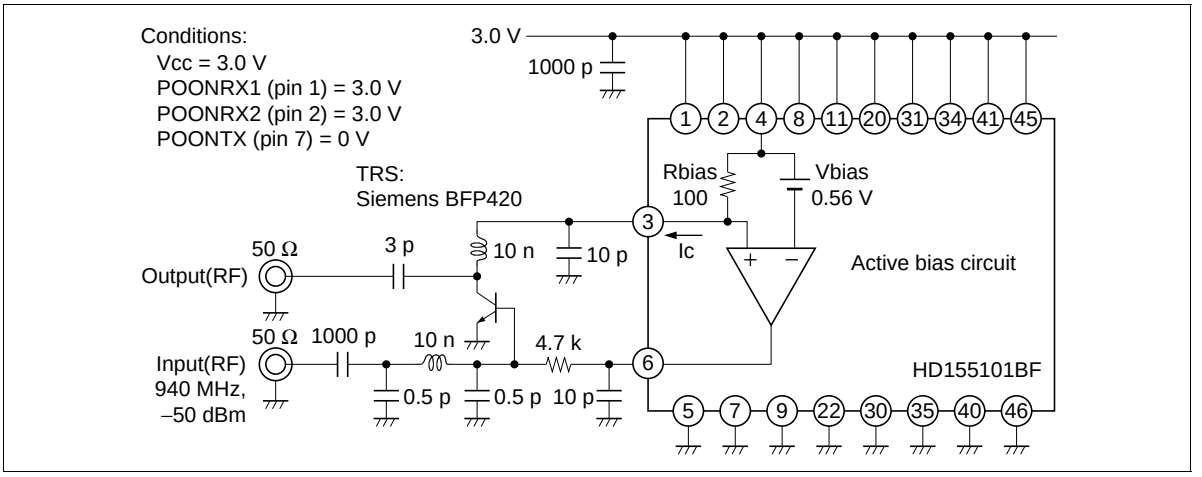


Figure 4 Evaluation Circuit for LNA

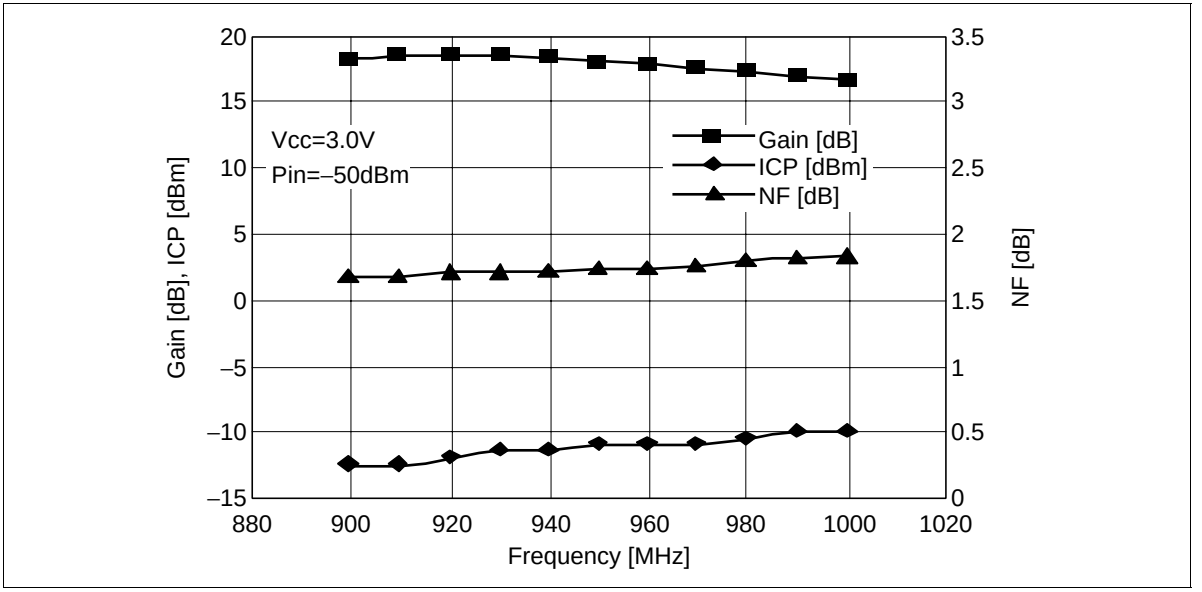


Figure 5 Gain, NF, ICP vs. Frequency

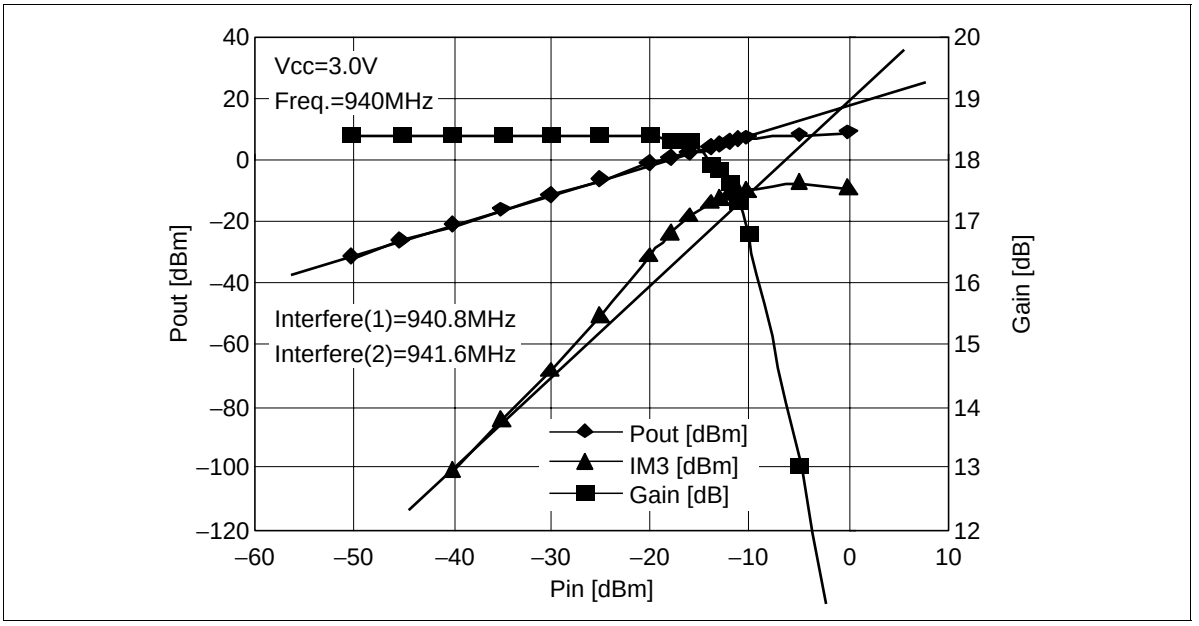


Figure 6 Gain, Pout vs. Pin

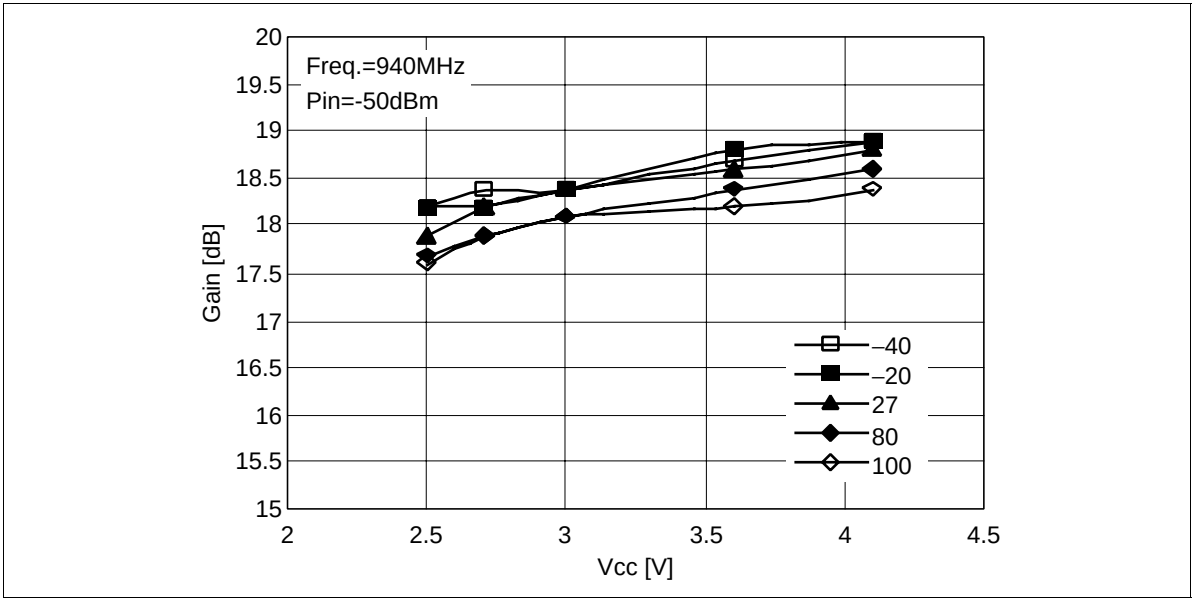


Figure 7 Gain vs. Supply Voltage

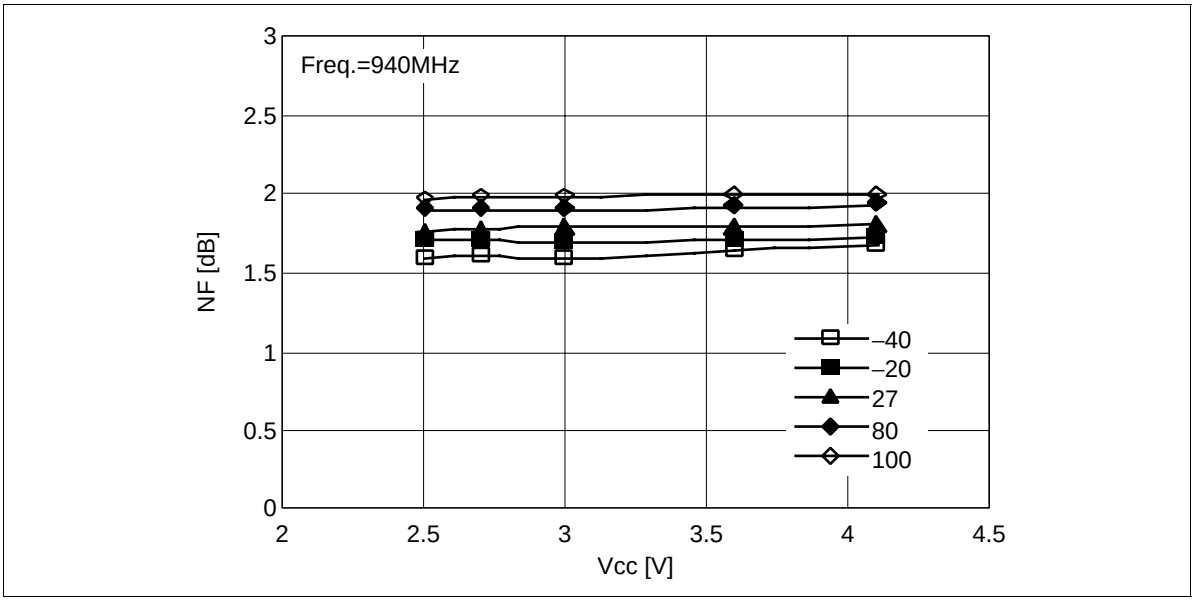


Figure 8 NF vs. Supply Voltage

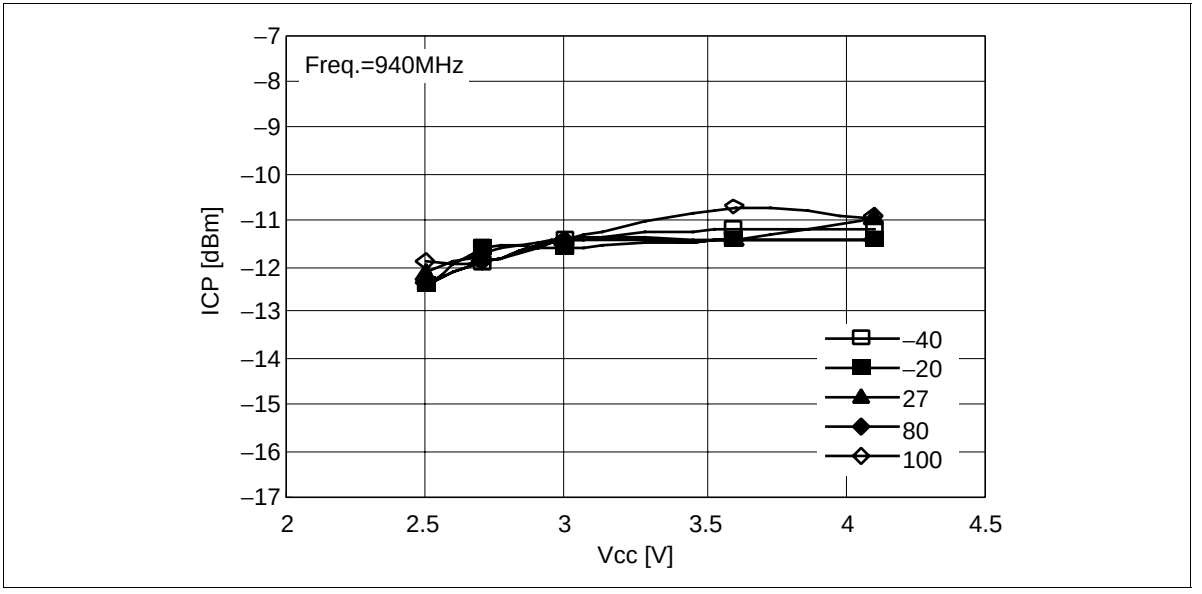


Figure 9 ICP vs. Supply Voltage

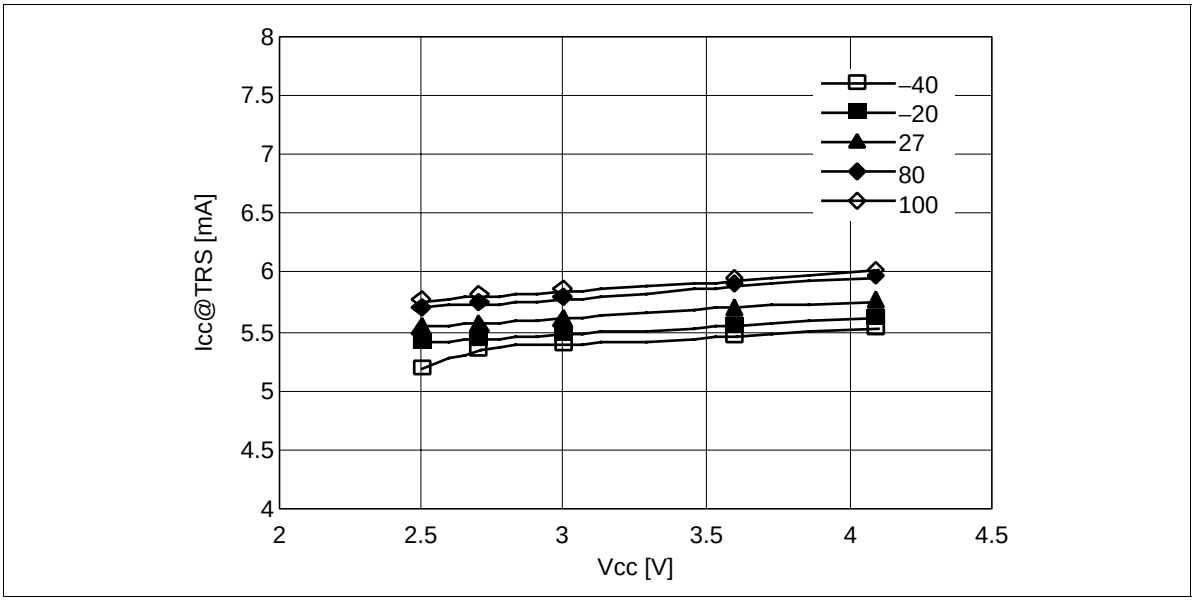


Figure 10 LNA Transistor Current vs. Supply Voltage

1st Mixer Measurement Results

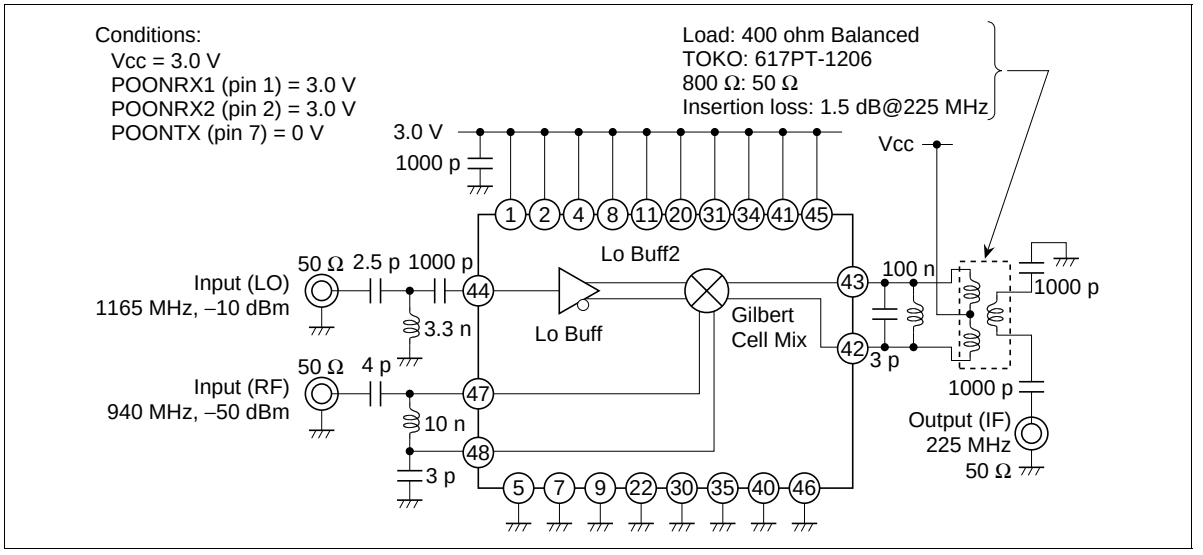


Figure 11 Evaluation Circuit for 1st Mixer

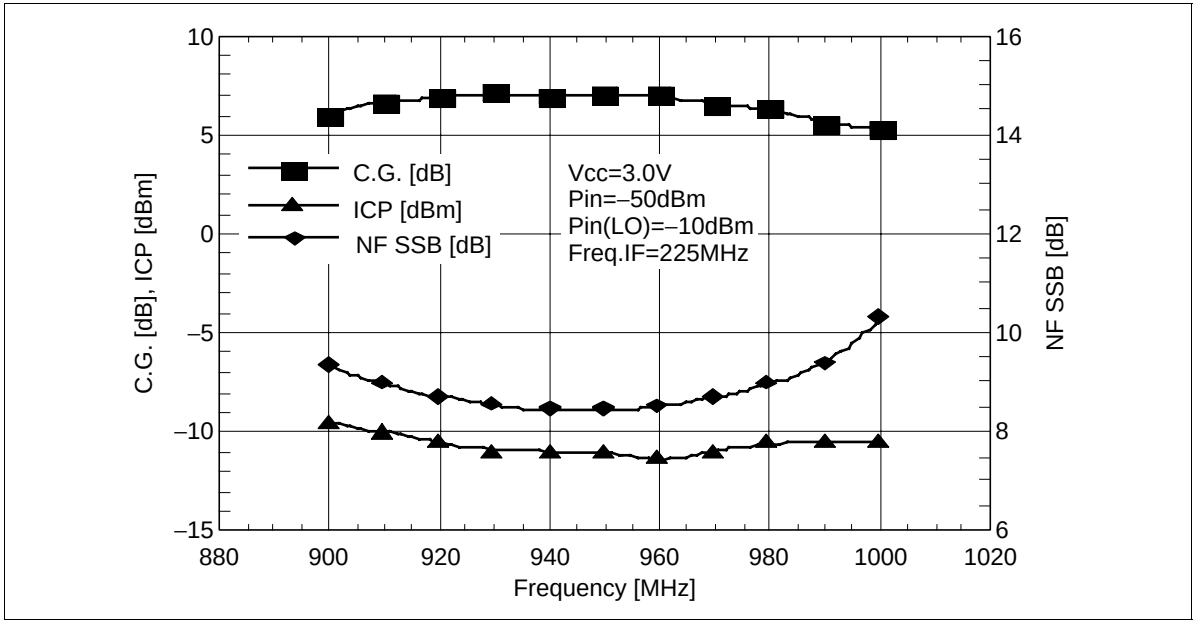


Figure 12 Gain, NF, ICP vs. Frequency

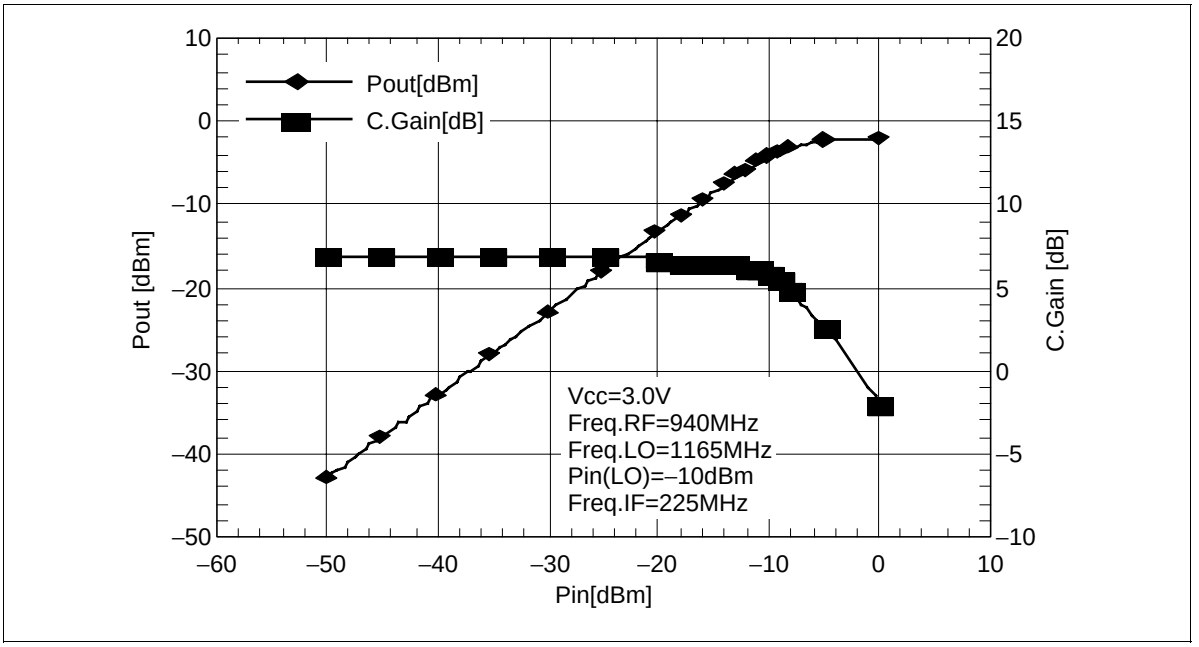


Figure 13 Input-Output Characteristics

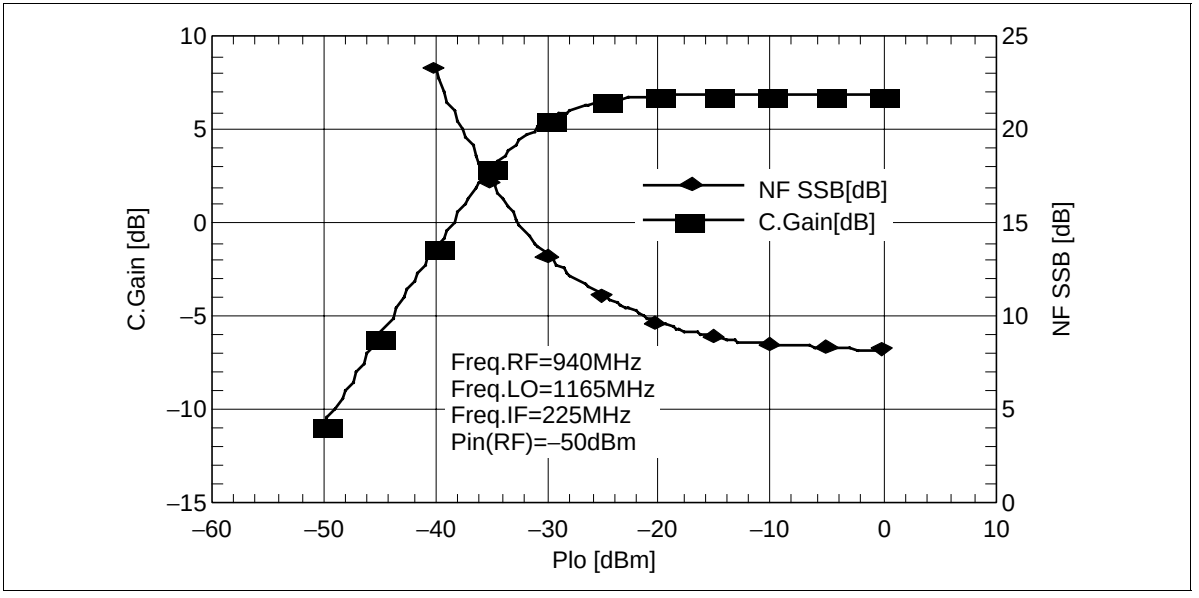


Figure 14 CG, NF vs. Local Input Power

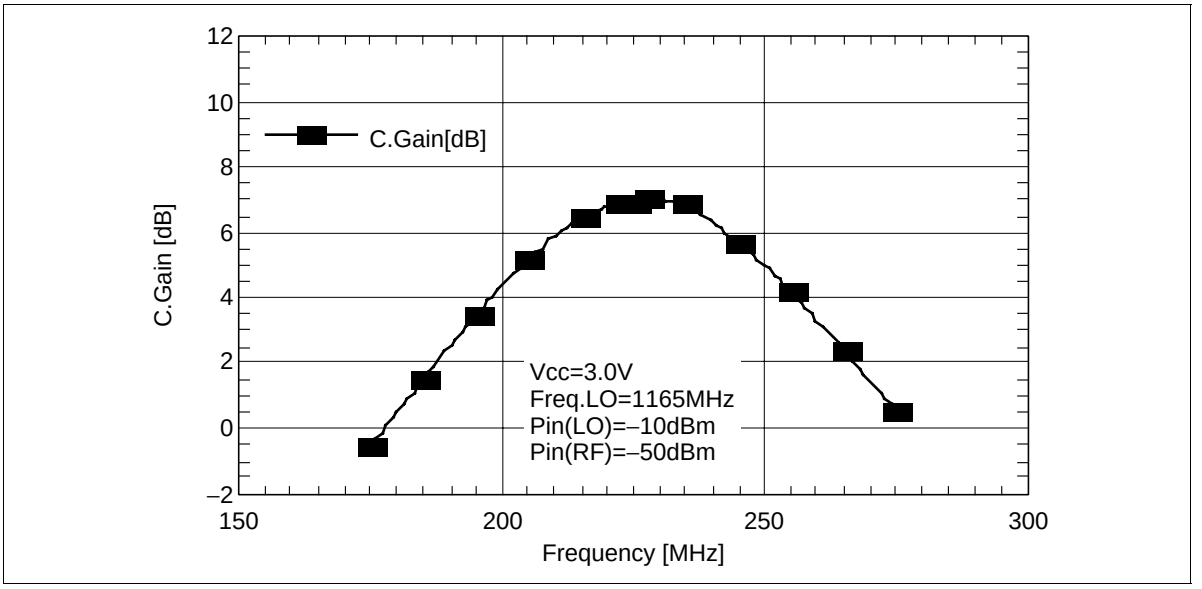


Figure 15 Output Frequency Characteristics

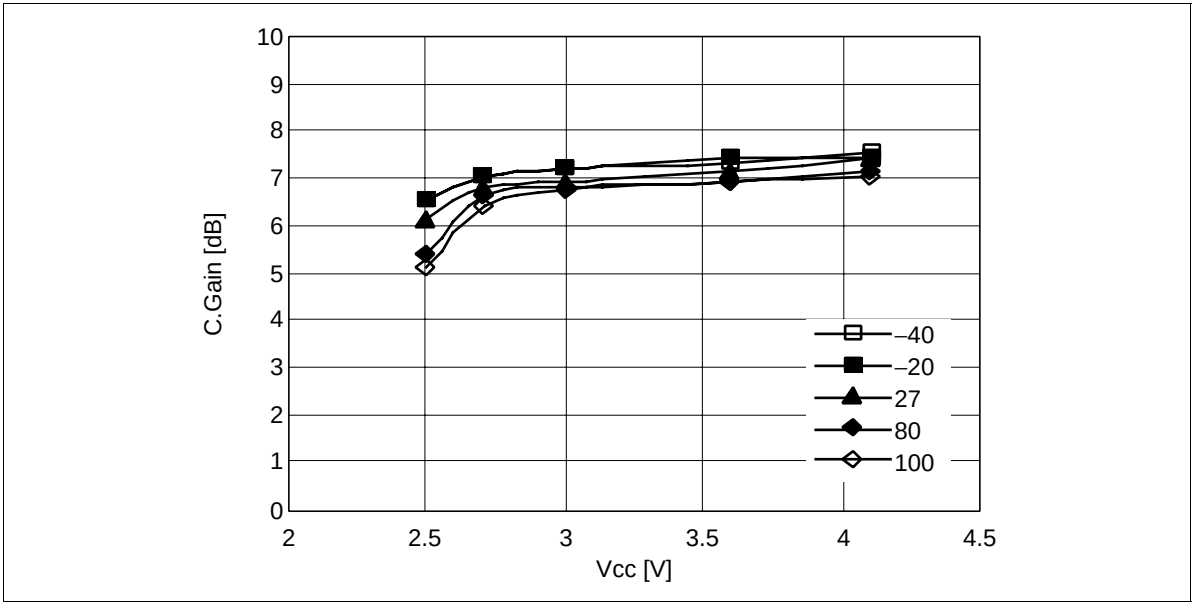


Figure 16 Gain vs. Supply Voltage

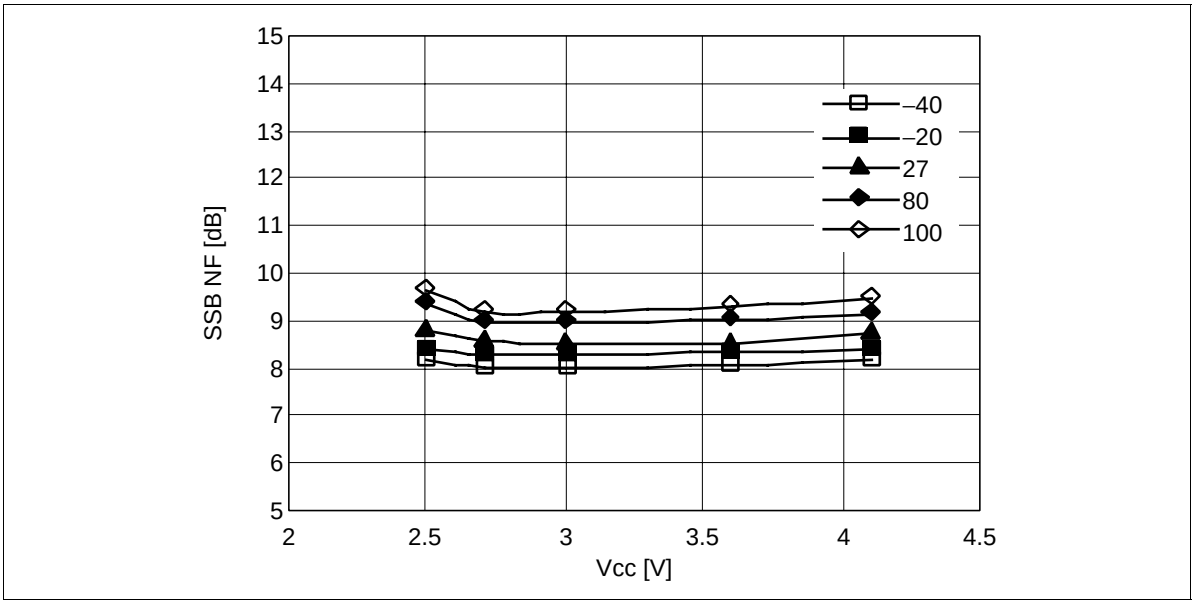


Figure 17 NF(SSB) vs. Supply Voltage

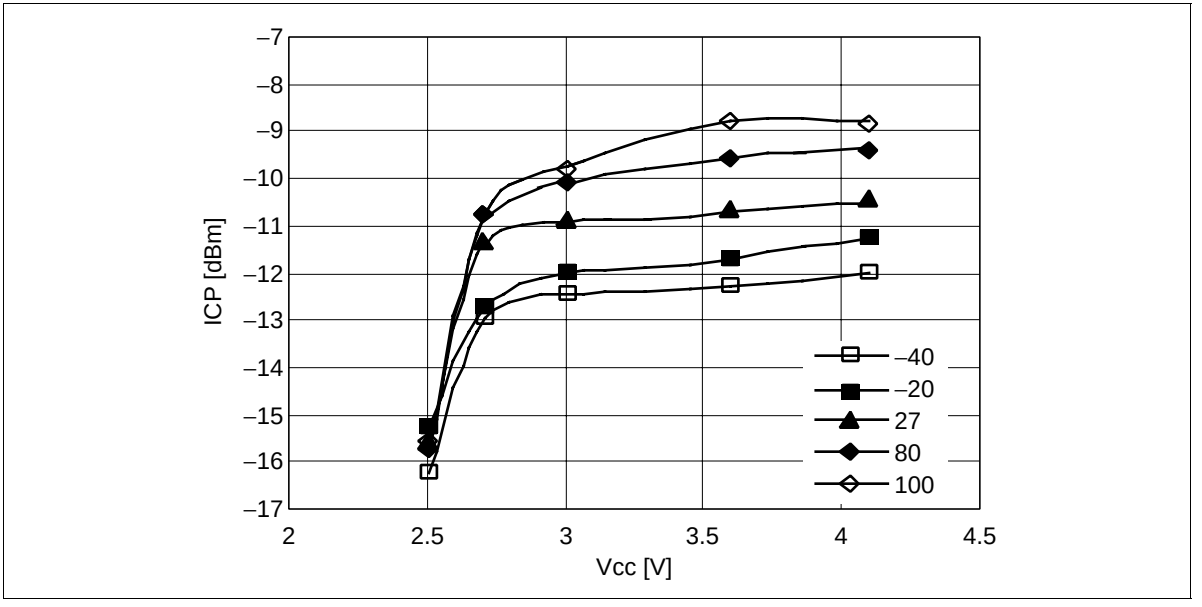


Figure 18 ICP vs. Supply Voltage

IF AMP + 2nd Mixer Measurement Results

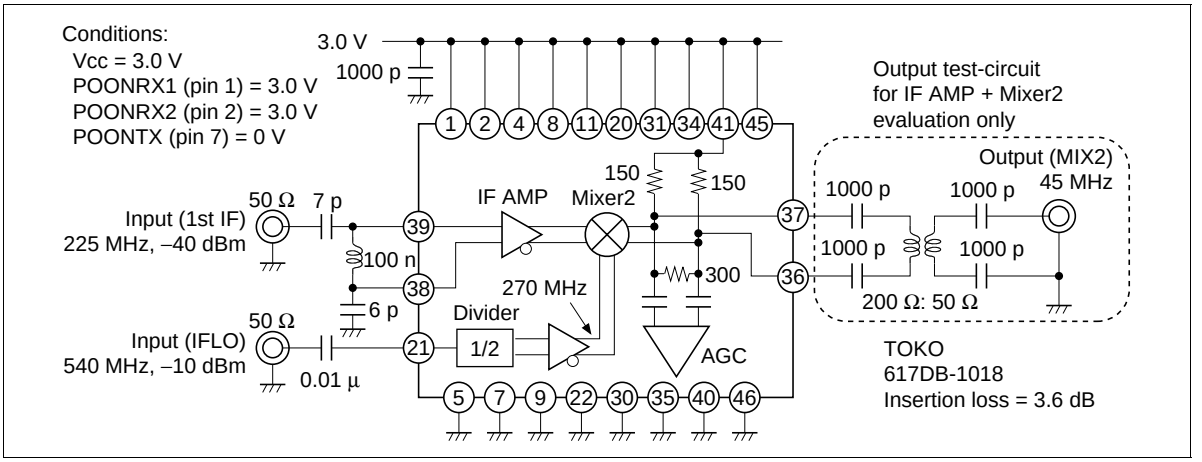


Figure 19 Evaluation Circuit for IF AMP + 2nd Mixer

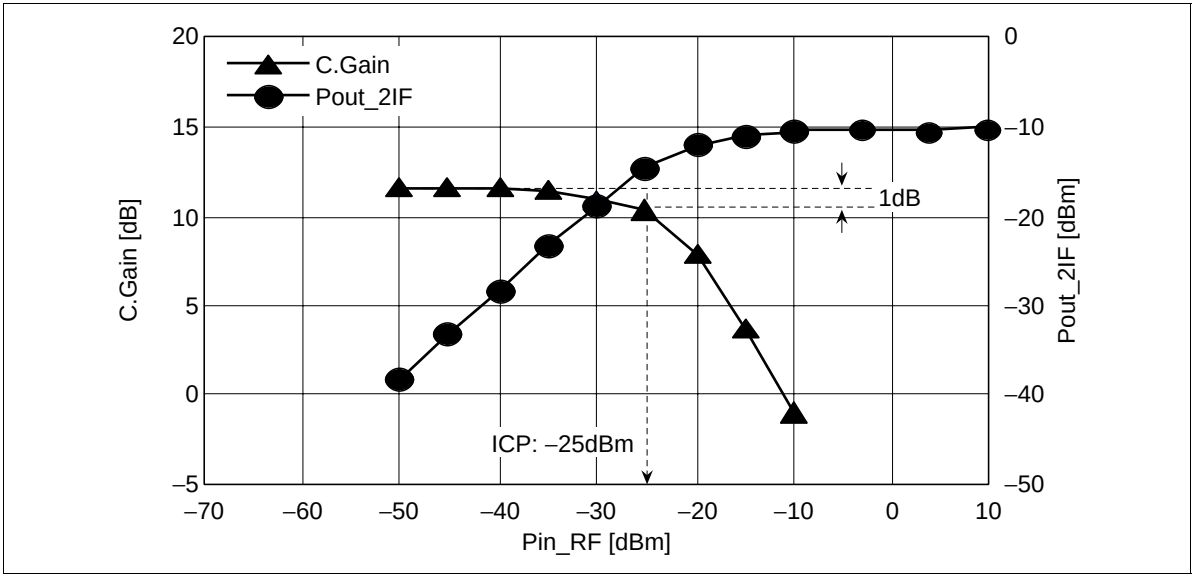


Figure 20 Input-Output Characteristics, 1dB-Compression Point

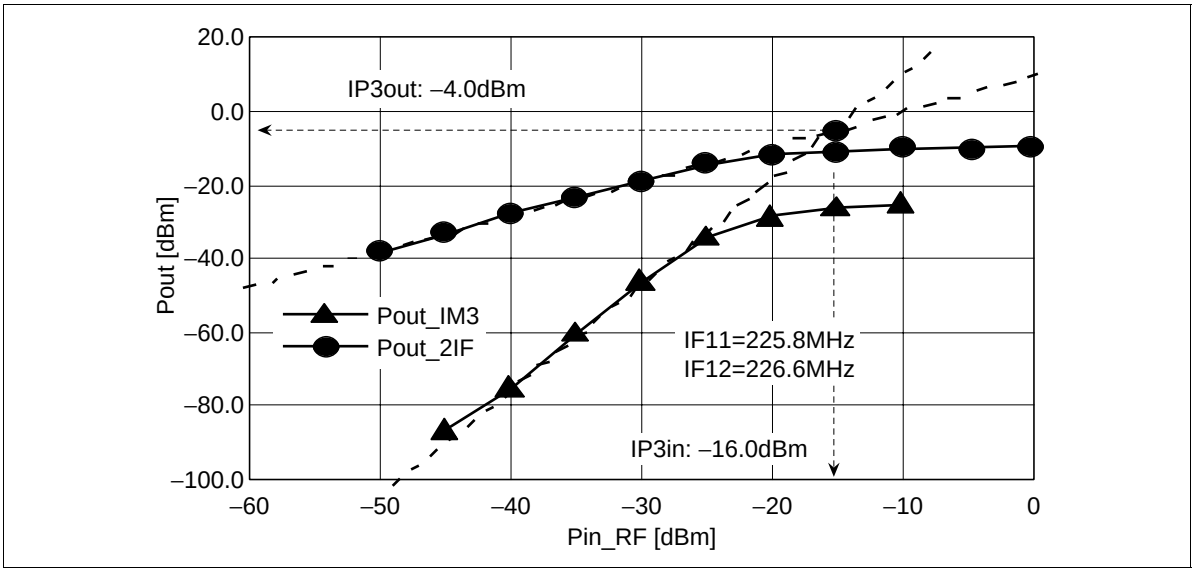


Figure 21 Intermodulation 3rd Characteristics

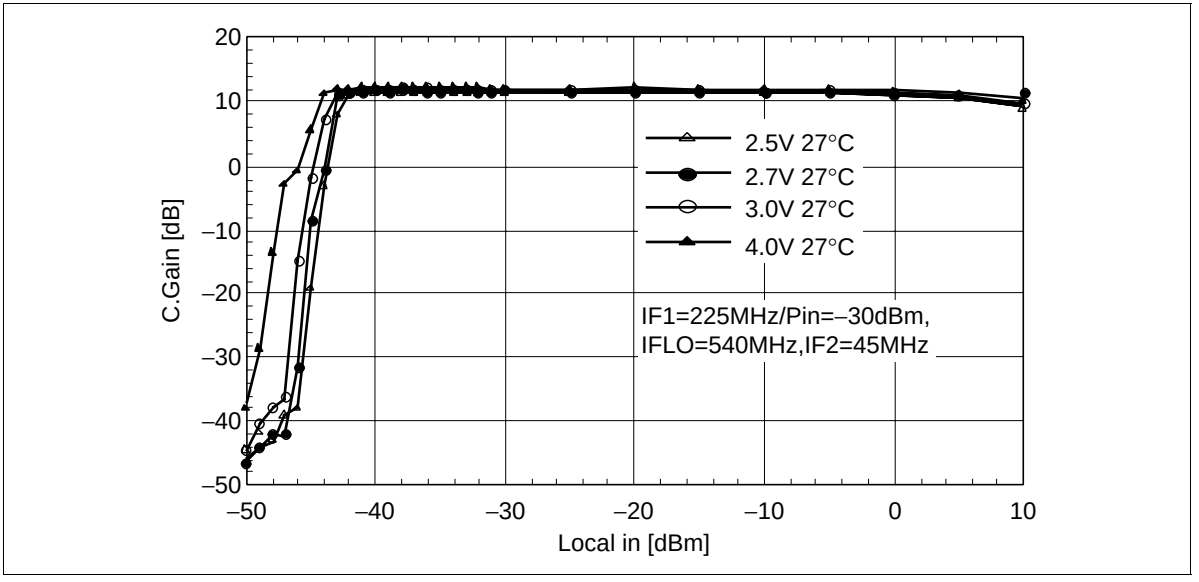


Figure 22 C.Gain vs. Local in Power

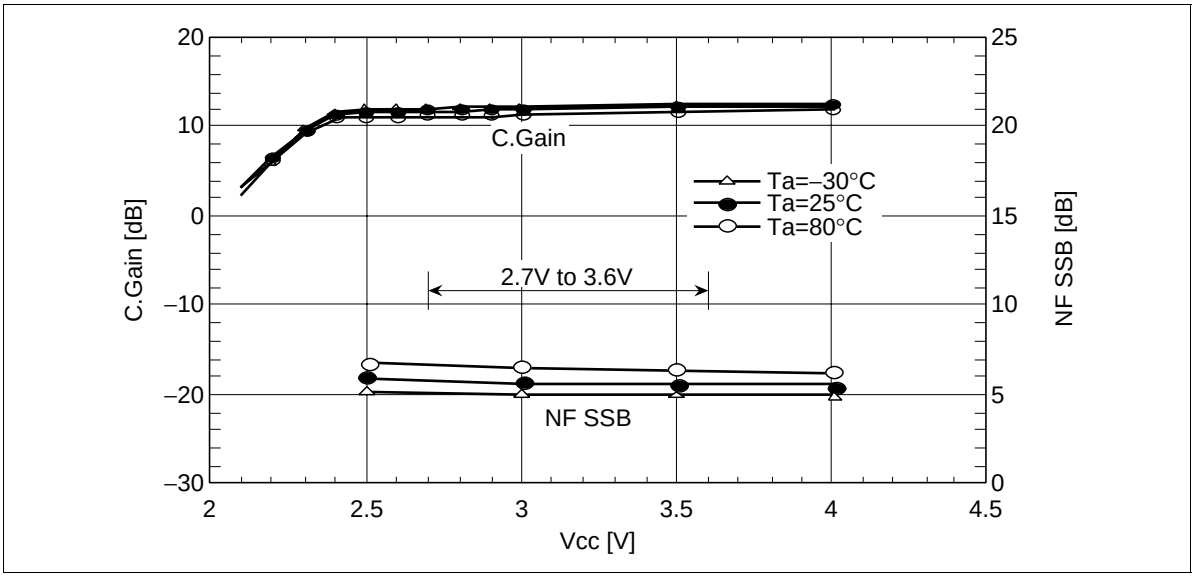


Figure 23 C.Gain, NF SSB vs. Supply Voltage

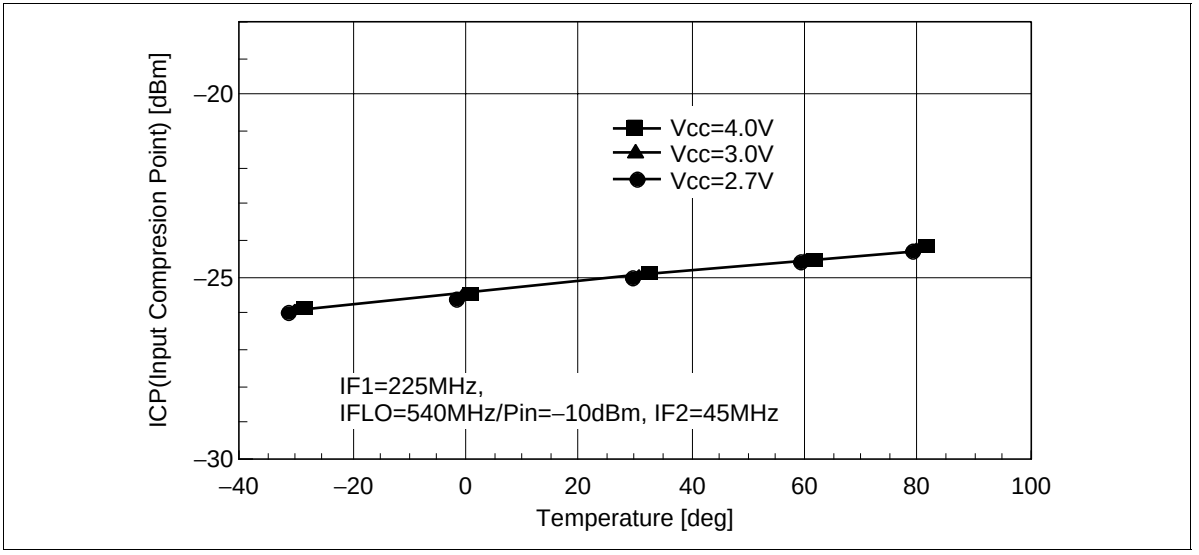


Figure 24 ICP vs. Temperature

AGC Measurement Results

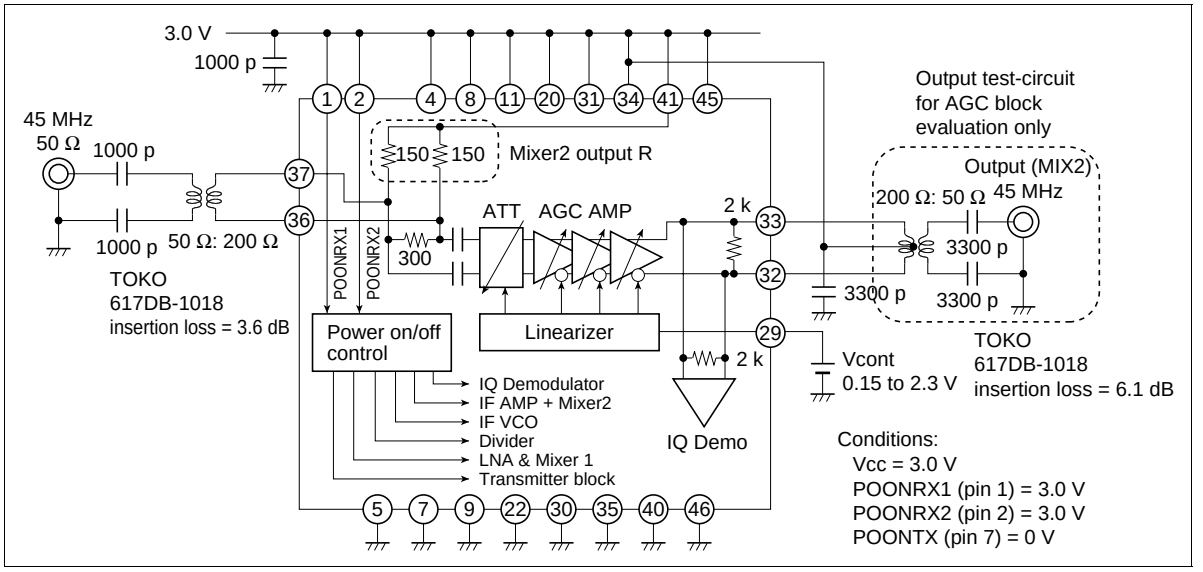


Figure 25 Evaluation Circuit for the AGC & Power On Control Blocks

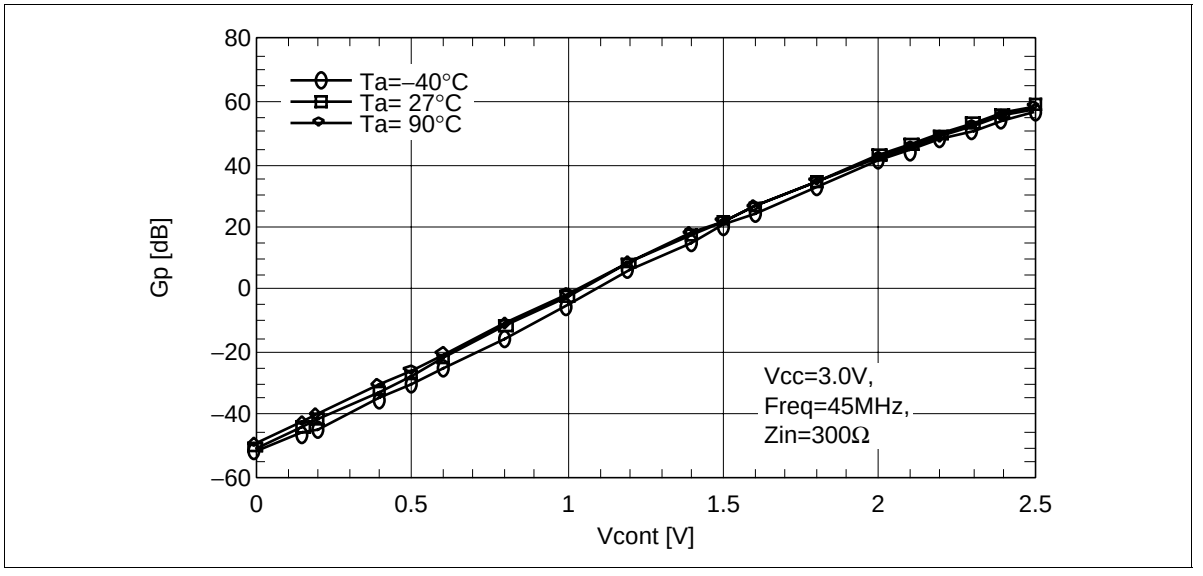


Figure 26 Power Gain vs. Vcont Voltage

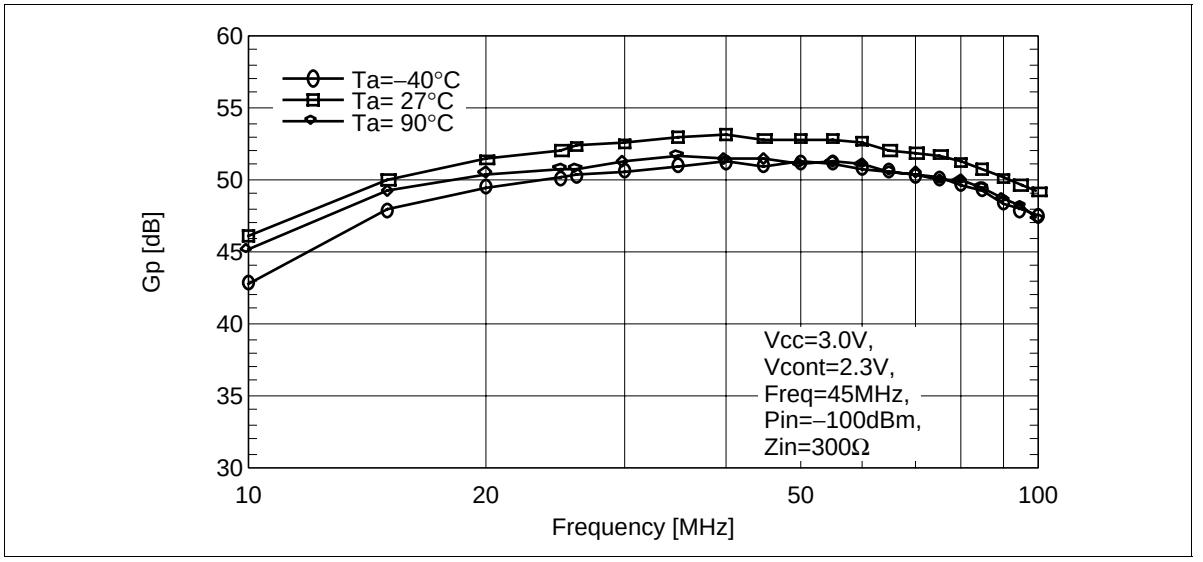


Figure 27 Power Gain vs. Frequency

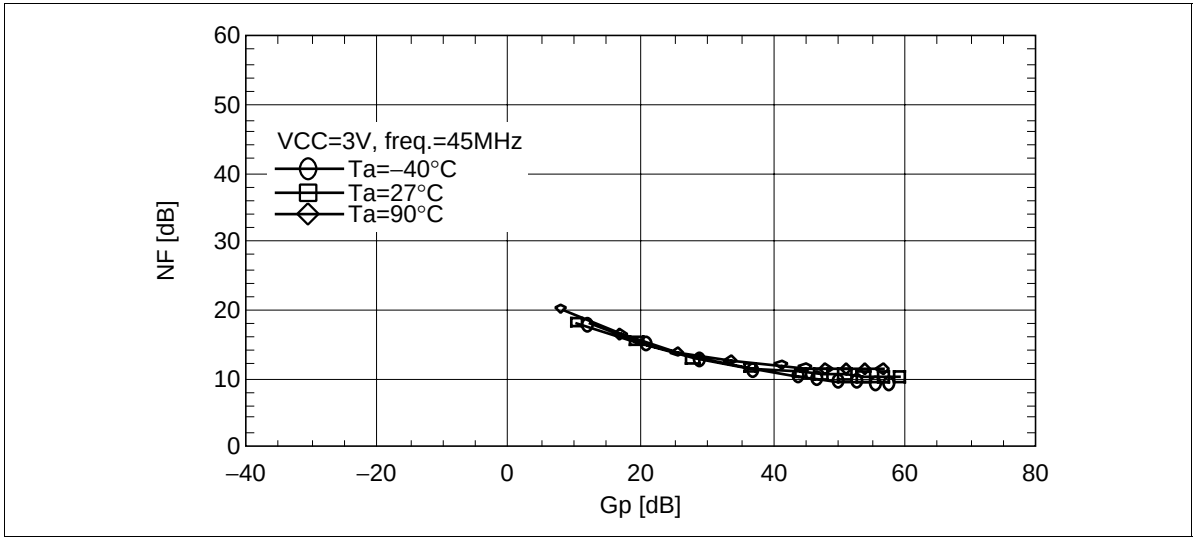


Figure 28 Noise Figure(NF) vs. Power Gain(Gp)

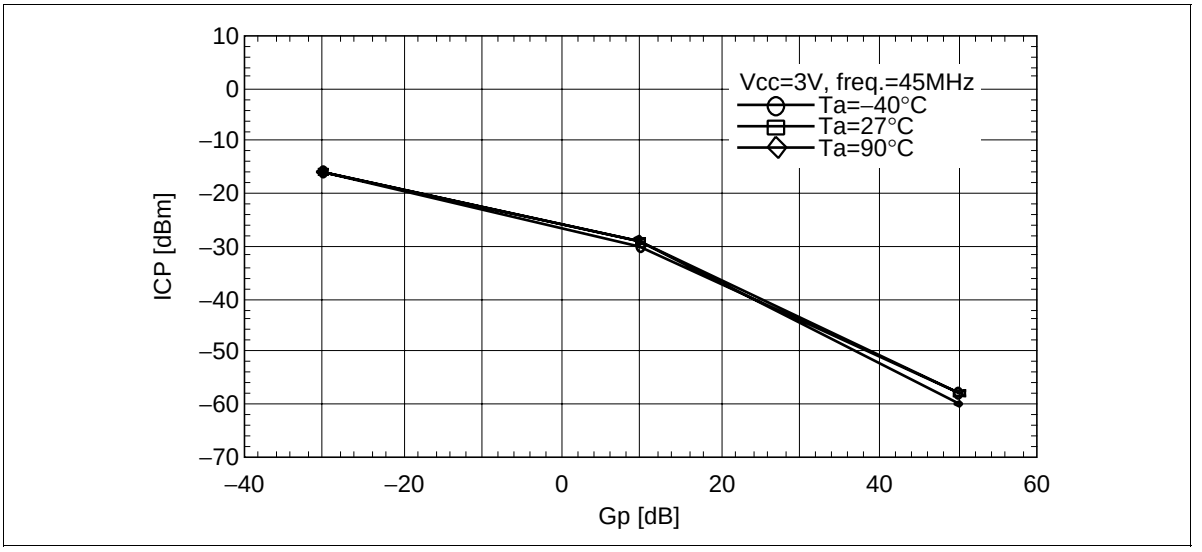


Figure 29 Input Compression Point(ICP) vs. Power Gain(Gp)

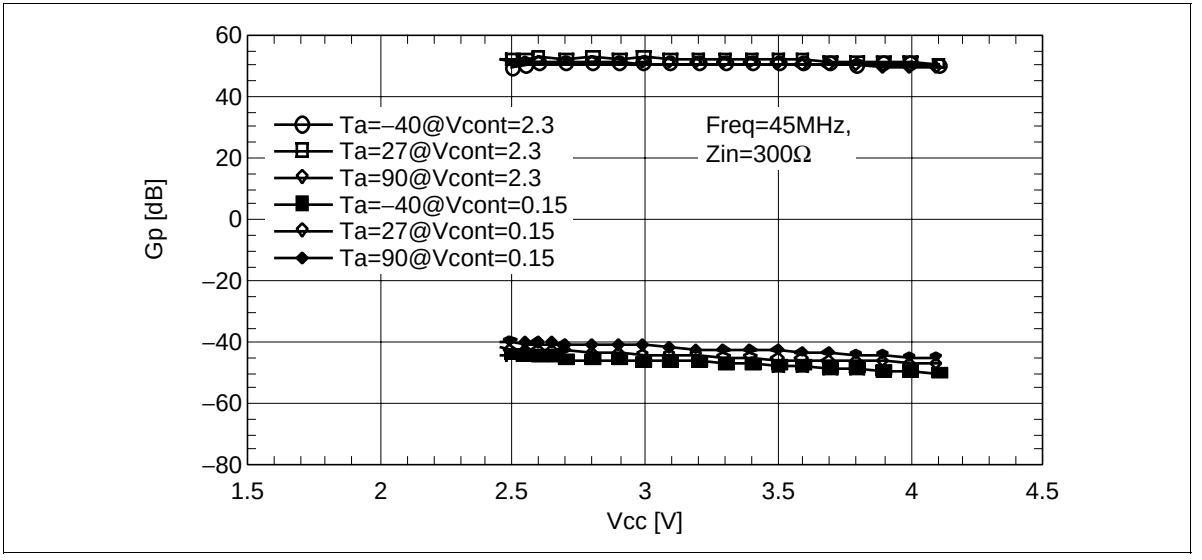


Figure 30 Power Gain(Gp) vs. Supply Voltage(Vcc)

IQ Demodulator Measurement Results

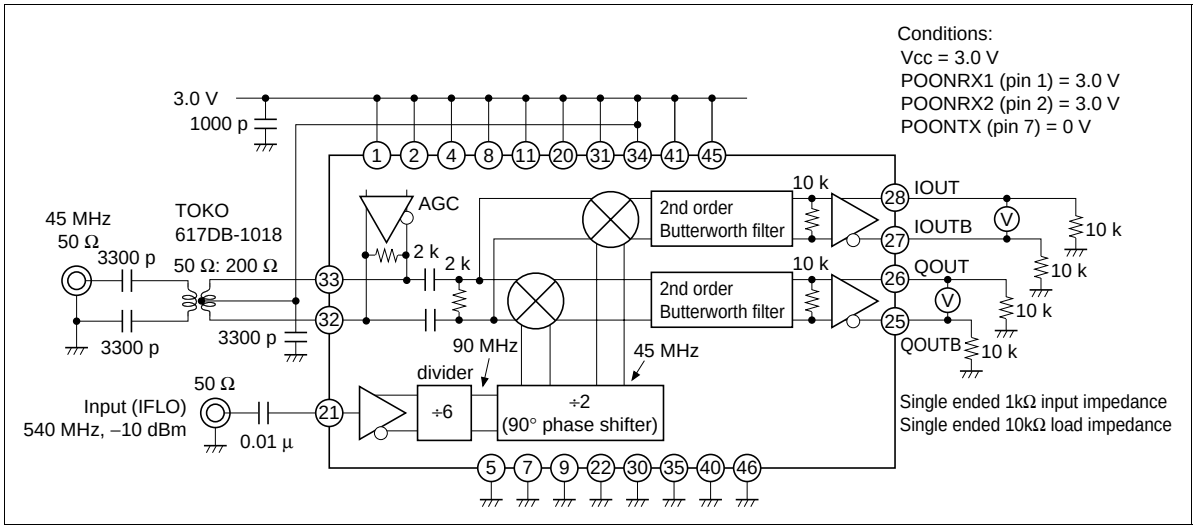


Figure 31 Evaluation Circuit for the I&Q Demodulator Block

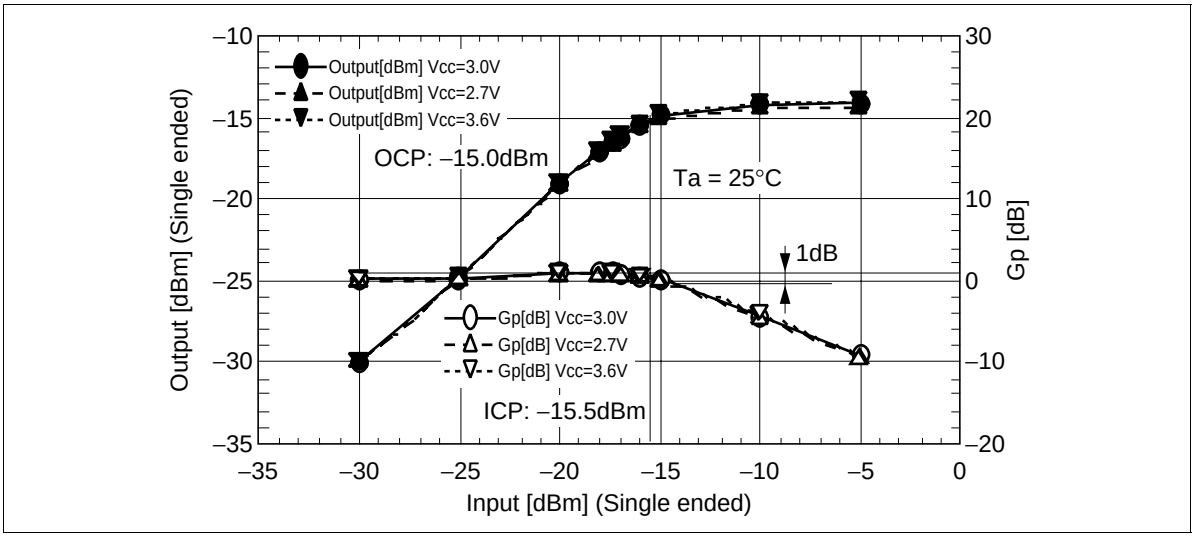


Figure 32 Input-Output Characteristics

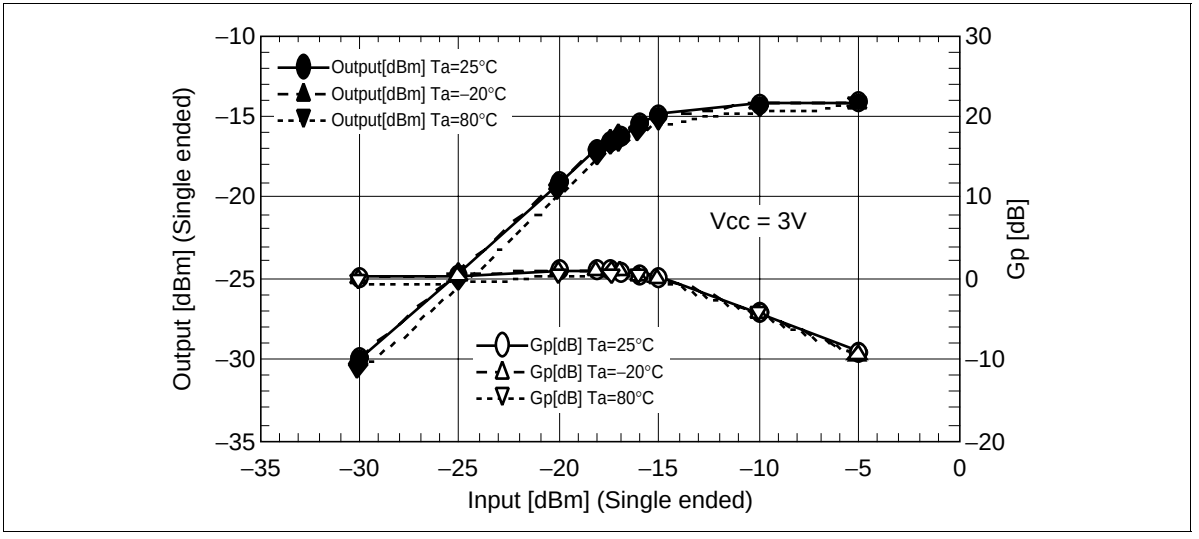


Figure 33 Input-Output Characteristics

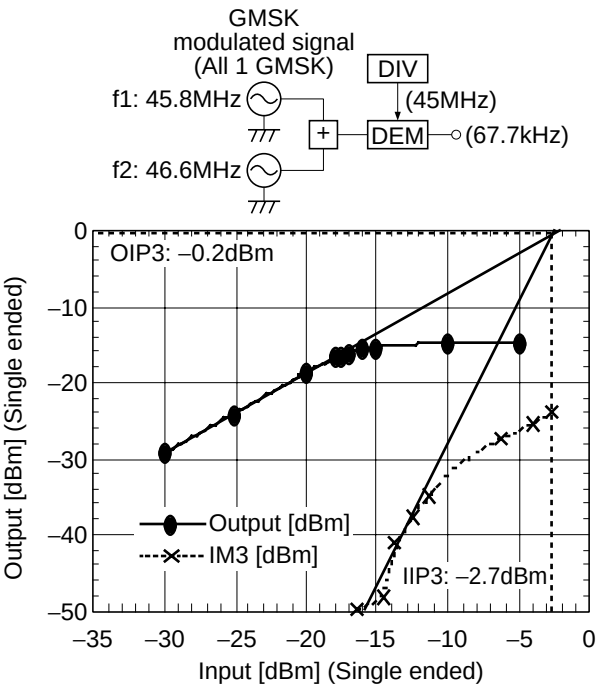
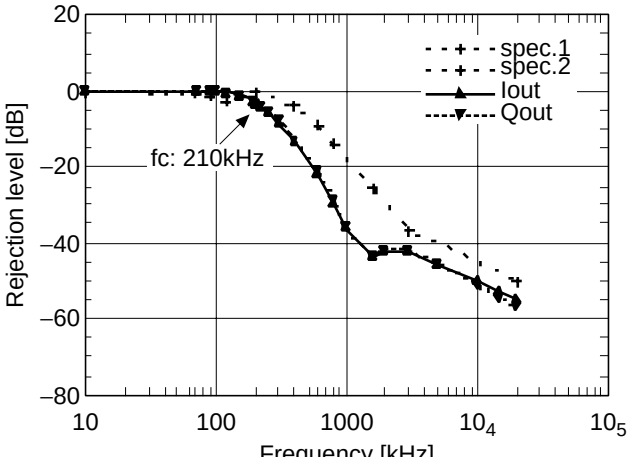
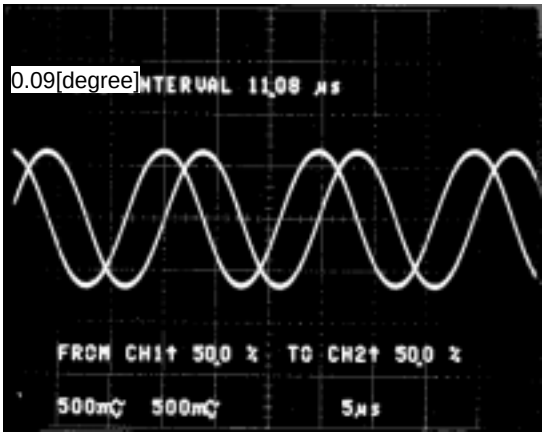


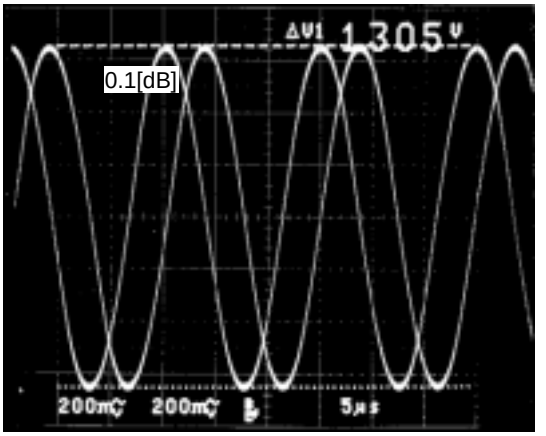
Figure 34 Inter Modulation 3rd Characteristics

Rejection	spec.(Min)	Iout	Qout
@200k	–0.3dB	–2.6dB	–2.4dB
@400k	–4.0dB	–11.5dB	–11.2dB
@600k	–9.4dB	–21.3dB	–21.1dB
@800k	–14.0dB	–29.0dB	–28.7dB
@1600k	–25.9dB	–43.3dB	–43.0dB
@3000k	–36.8dB	–42.2dB	–42.0dB
@20000k	–50.0dB	–54.7dB	–56.1dB

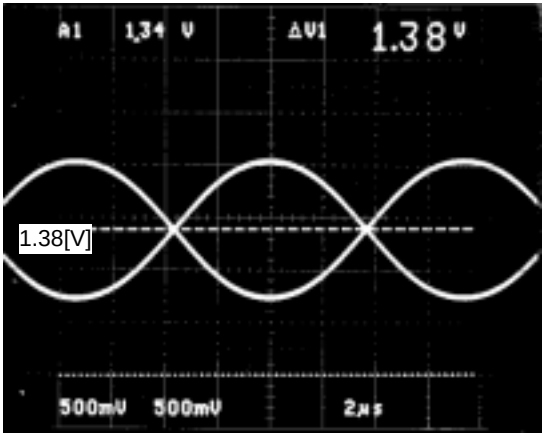




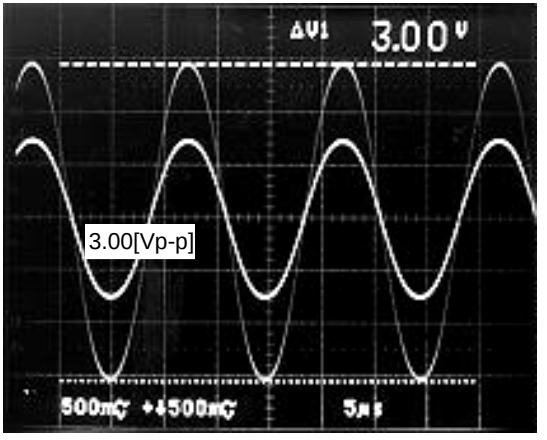
a) I&Q Phase Accuracy



b) I&Q Amplitude Mismatch



c) Common Mode Voltage



d) Differential Output Swing

Figure 36 Demodulator Output Waveforms (67.7 kHz) at Vcc = 3.0 V, Ta = 25°C

Transmitter Measurement Results

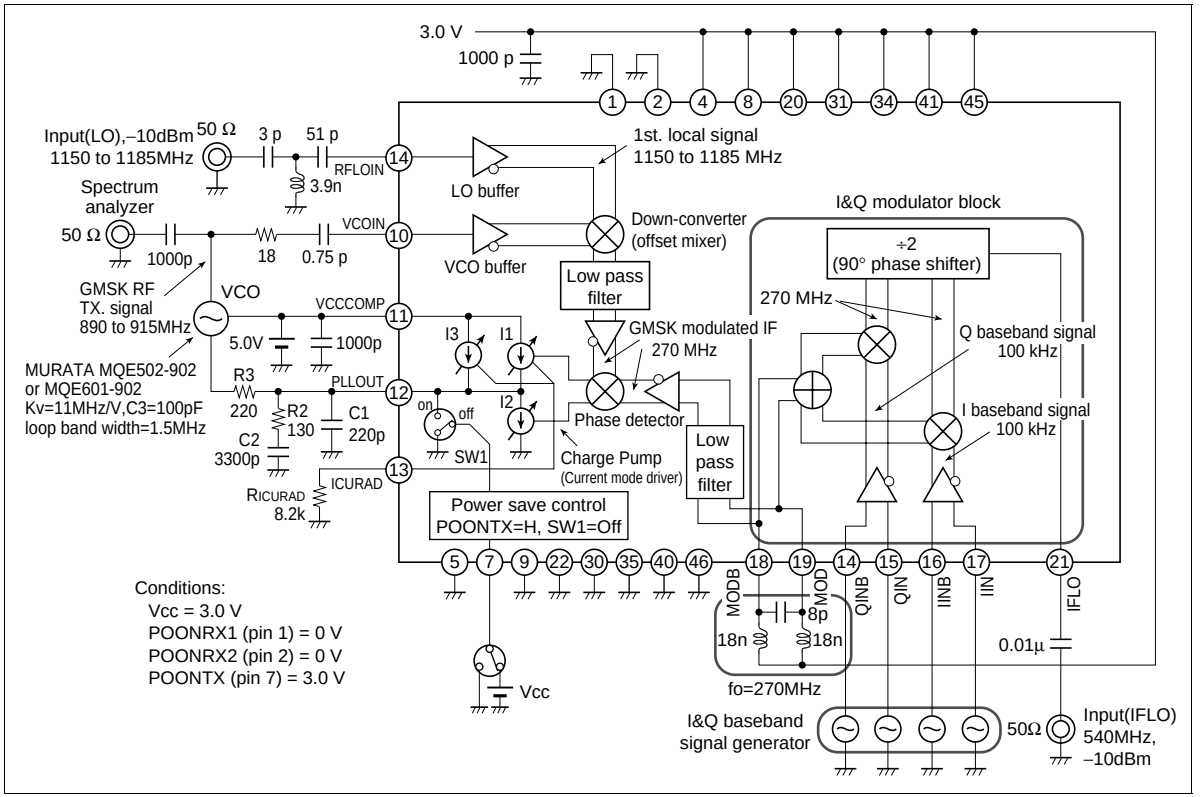
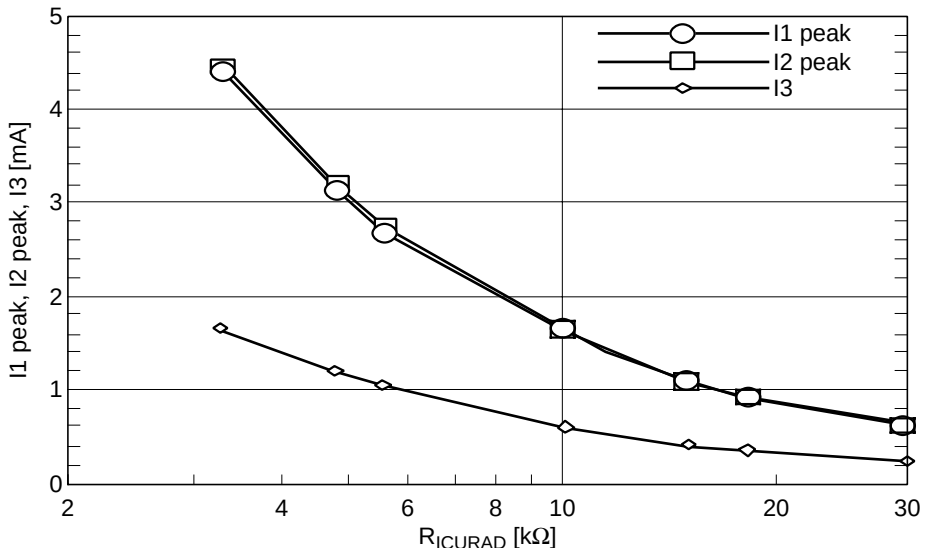


Figure 37 Evaluation Circuit for the Upconverter (I&Q Modulator and Offset PLL Block)



Phase accuracy and lock up time characteristics depend on the OPLL loop bandwidth. The following table shows measurement result of each characteristic, when the OPLL loop bandwidth is changed.

Table 2 Measurement Results of Transmitter Characteristics vs. OPLL Loop Bandwidth Dependence (R_{ICURAD} = 8.2 kΩ, IFLO generated by signal generator)

	Conditions					
Item	**Condition1**	**Condition 2**	**Condition 3**	**Condition 4**	**Condition 5**	**Unit**
VCO & Phase detector	VCO: MURATA MQE502-902 or MQE601-902, C3 = 100 pF in VCO, R_{ICURAD} = 8.2 kΩ, $k_{vr} = 2\pi \times 11 \times 10^6$(rad/Vsec), $k_{dr} = (2.83 \times 10^{-3}) / \pi$ (A/rad)					
Loop bandwidth (measured)	0.8	1.1	1.3	1.5	1.6	MHz
C1	680	390	300	220	180	pF
C2	10.0	6.8	4.7	3.3	2.7	nF
C3	100	100	100	100	100	pF
R2	68	100	110	130	130	Ω
R3	390	330	270	220	200	Ω

Item		**Spec.**	**Measured1**	**Measured2**	**Measured3**	**Measured4**	**Measured5**	**Unit**
200 kHz offset		≤ –33	–37.23	–37.09	–37.60	–37.70	–37.86	dBc
400 kHz offset		≤ –63	–67.41	–67.95	–68.49	–68.94	–69.23	dBc
600 kHz to 1.8 MHz offset		≤ –63	–72.86	–72.85	–73.09	–73.48	–73.26	dBc
1.8 MHz to 3 MHz offset		≤ –66	–79.65	–76.96	–76.45	–75.70	–74.96	dBc
3 MHz to 6 MHz offset		≤ –68	–82.11	–81.11	–80.83	–79.18	–79.58	dBc
6 MHz upwards offset		≤ –74	–82.77	–82.67	–82.59	–81.98	–82.38	dBc
Carrier suppression		≥ 31	47.35	48.44	47.54	46.71	48.36	dBc
Side band suppression		≥ 35	39.10	39.47	39.89	39.89	40.33	dBc
Phase accuracy	PN9	≤ 2.5	1.53	1.16	1.02	0.89	0.84	deg. rms
	PN9	≤ 6.0	3.30	2.90	2.81	2.72	2.64	deg. peak
	All ‘1’	≤ 2.5	0.99	0.95	0.93	0.93	0.89	deg. rms
	All ‘1’	≤ 6.0	2.26	2.33	2.33	2.31	2.04	deg. peak
Lock up time		≤ 80	58.1	41.1	29.4	19.1	17.2	μsec
Tx noise in	925 MHz		–163.3	–158.6	–157.0	–155.1	–154.9	dBc/Hz
Rx band	935 MHz		–166.4	–165.6	–165.4	–164.1	–163.3	dBc/Hz
VCO noise only	925 MHz		–165.2 (0 dBc = –0.5 dBm, noise –165.7 dBm/Hz)					dBc/Hz
	935 MHz		–166.4 (0 dBc = –0.5 dBm, noise –166.9 dBm/Hz)					dBc/Hz

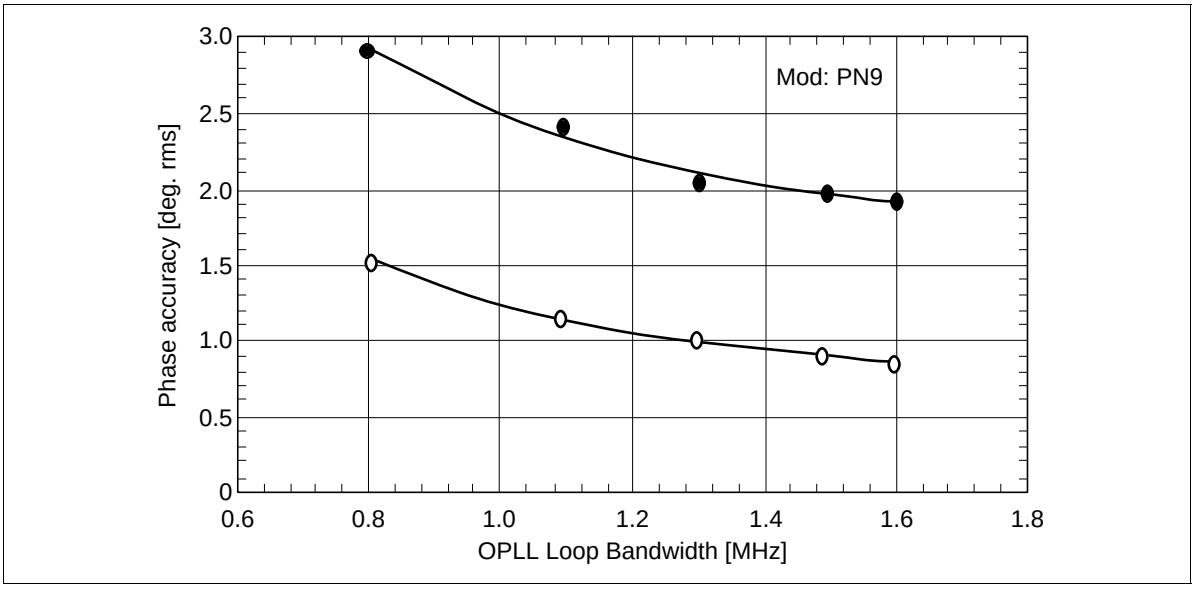


Figure 39 Phase Accuracy vs. OPLL Loop Bandwidth

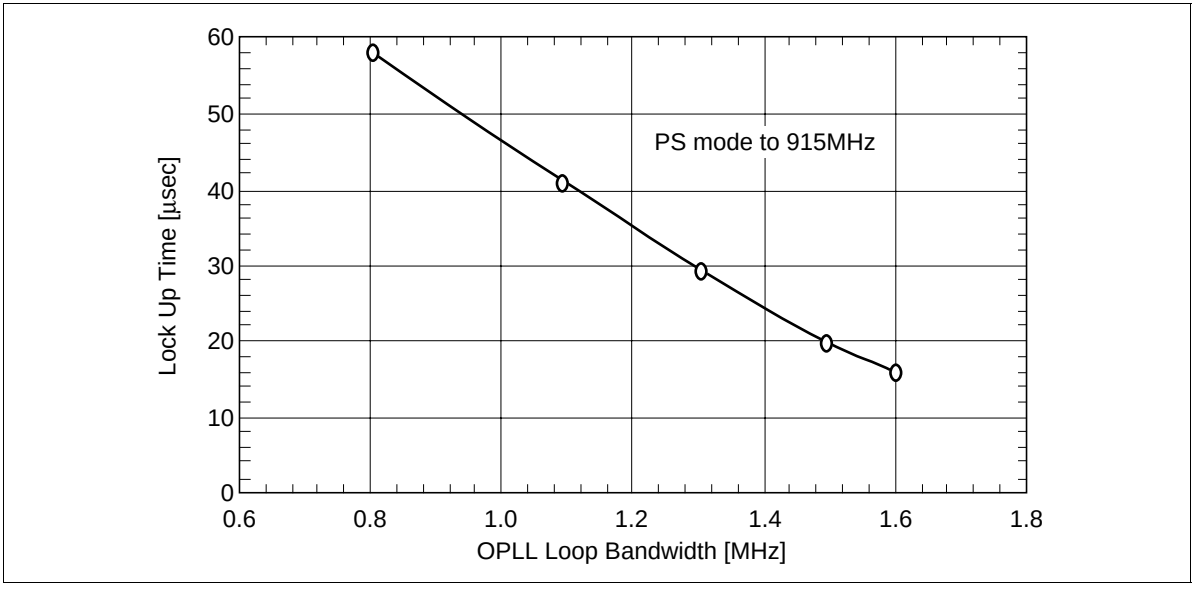


Figure 40 Lock Up Time vs. OPLL Loop Bandwidth

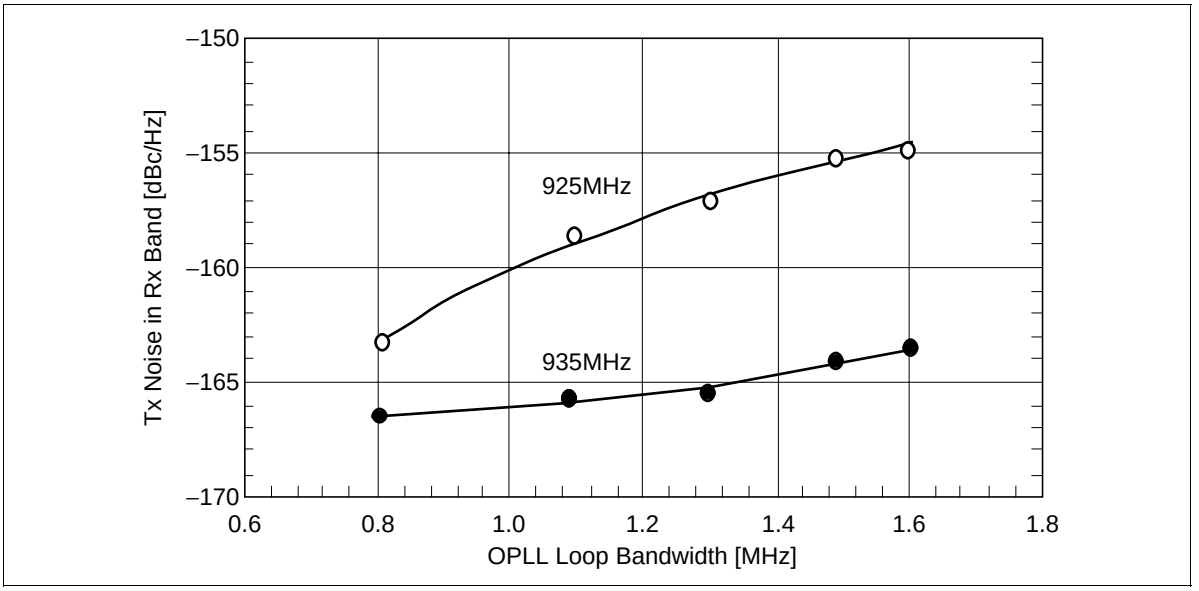


Figure 41 Tx Noise in Rx Band vs. OPLL Loop Bandwidth

Transmitter Measurement Results (1) (R_{ICURAD} = 8.2 kΩ and IFLO generated by signal generator**)**

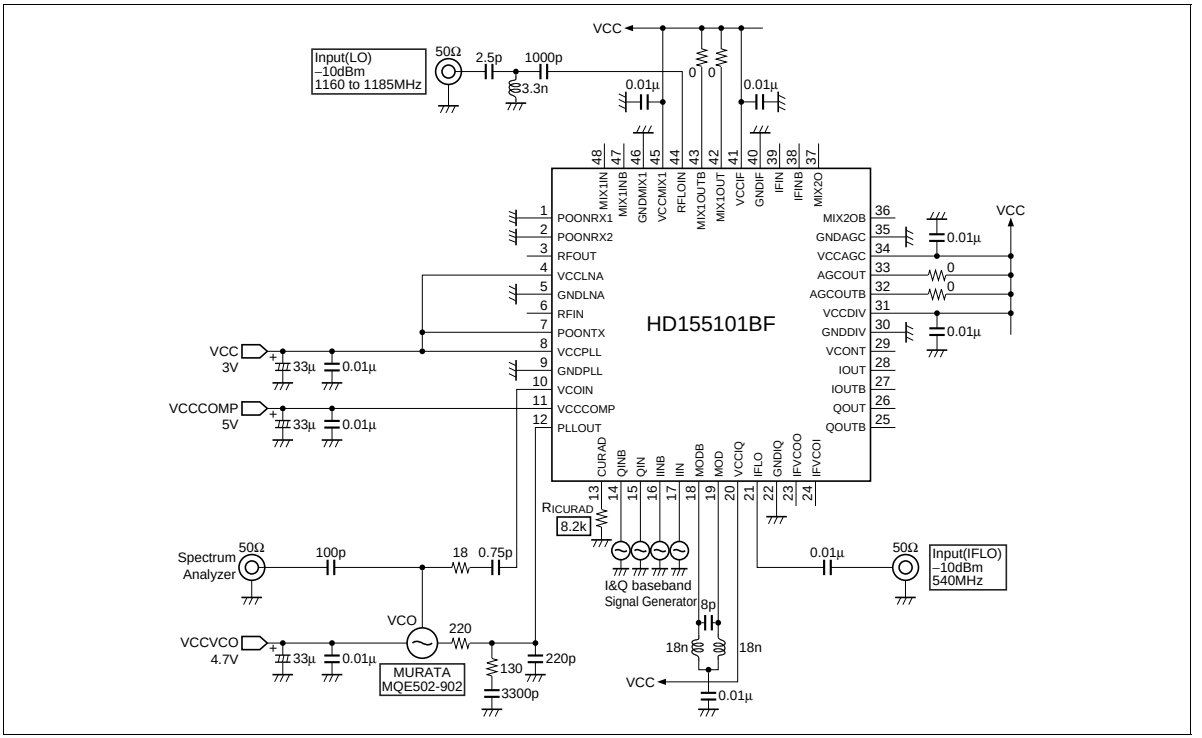
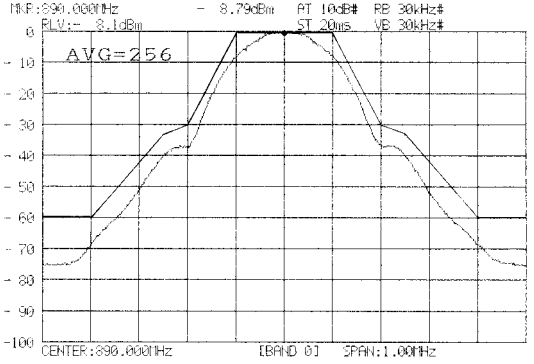


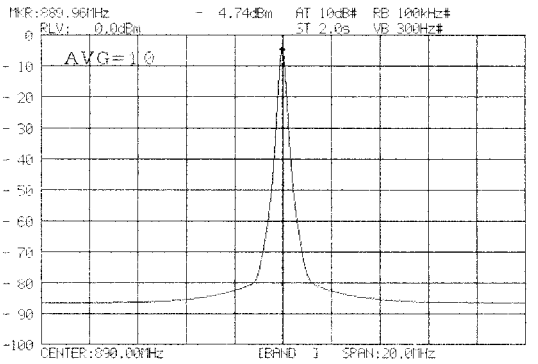
Figure 42 Evaluation Circuit Using Signal Generator for the I&Q Modulator and Offset PLL

Table 3 Measurement Results Using SG (R_{ICURAD} = 8.2 kΩ, IFLO generated by signal generator)

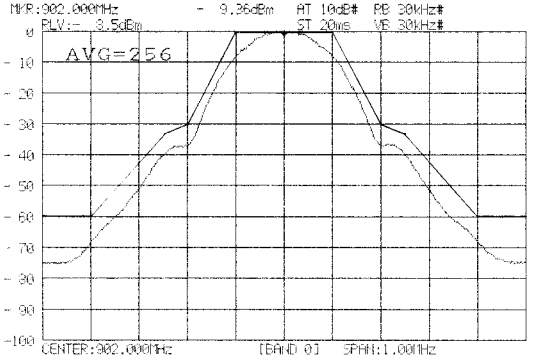
Item		Spec.	Measured1	Measured2	Measured3	Unit
Measured frequency			890	902	915	MHz
200 kHz offset		≤ –33	–36.36	–36.16	–36.60	dBc
400 kHz offset		≤ –63	–68.22	–67.30	–67.02	dBc
600 kHz to 1.8 MHz offset		≤ –63	–74.84	–74.88	–74.69	dBc
1.8 MHz to 3 MHz offset		≤ –66	–77.48	–77.30	–77.10	dBc
3 MHz to 6 MHz offset		≤ –68	–79.73	–79.47	–79.16	dBc
6 MHz upwards offset		≤ –74	–81.63	–80.67	–80.94	dBc
Carrier suppression		≥ 31	46.24	46.11	45.98	dBc
Side band suppression		≥ 35	38.81	38.86	38.84	dBc
Phase accuracy	PN9	≤ 2.5	1.05	1.05	1.05	deg. rms
	PN9	≤ 6.0	2.76	2.61	2.59	deg. peak
	All ‘1’	≤ 2.5	1.00	1.02	1.01	deg. rms
	All ‘1’	≤ 6.0	2.19	2.33	2.13	deg. peak



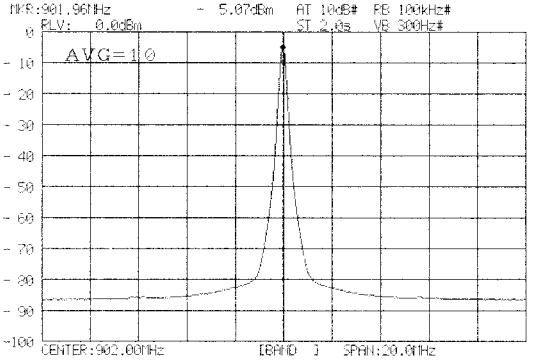
a-1. Spectrum1 (890MHz, PN9)



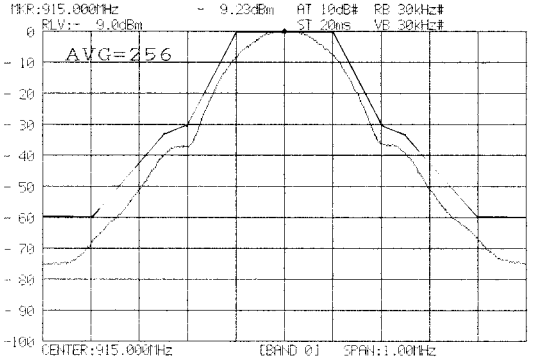
a-2. Spectrum2 (890MHz, PN9)



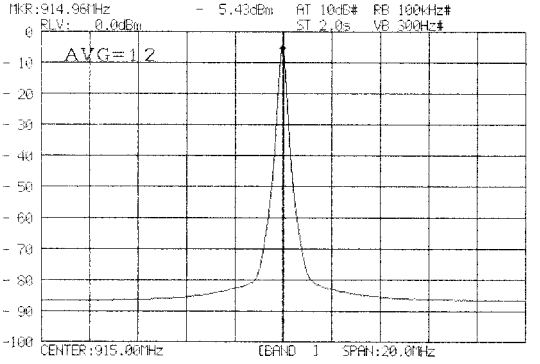
b-1. Spectrum1 (902MHz, PN9)



b-2. Spectrum2 (902MHz, PN9)

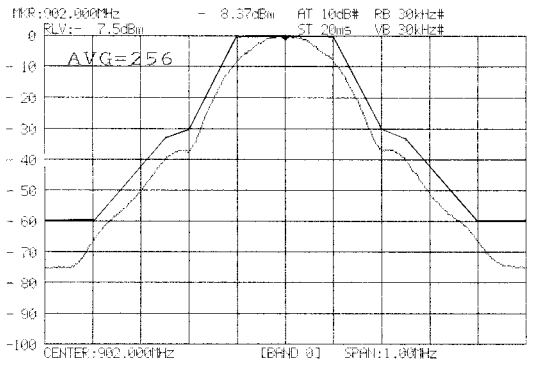


c-1. Spectrum1 (915MHz, PN9)

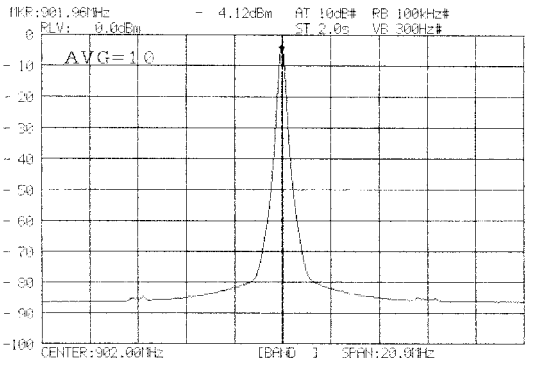


c-2. Spectrum2 (915MHz, PN9)

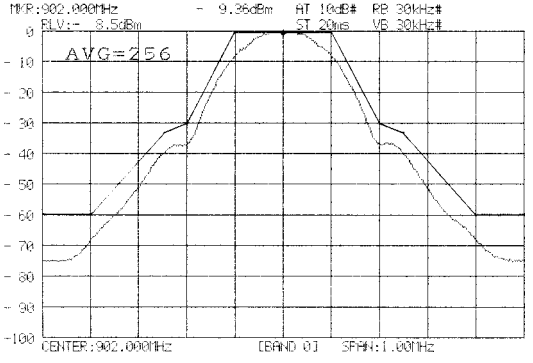
Figure 43 GMSK Modulated Transmitter Output Spectrum (890 MHz, 902 MHz, 915 MHz)



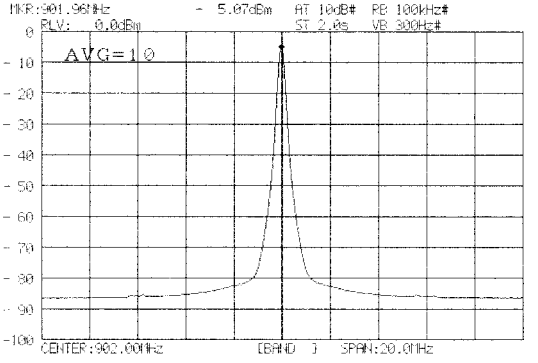
T=–40°C 902MHz, PN9



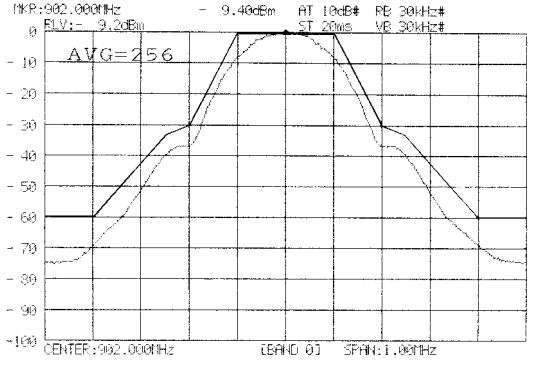
T=–40°C 902MHz, PN9



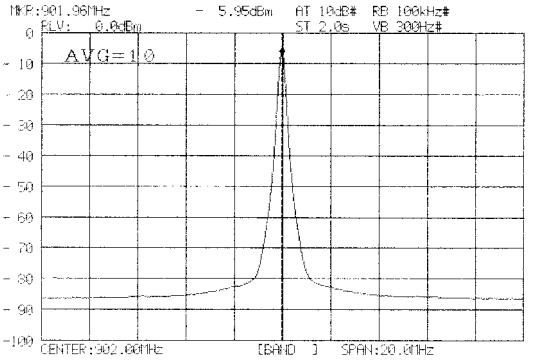
T=27°C 902MHz, PN9



T=27°C 902MHz, PN9



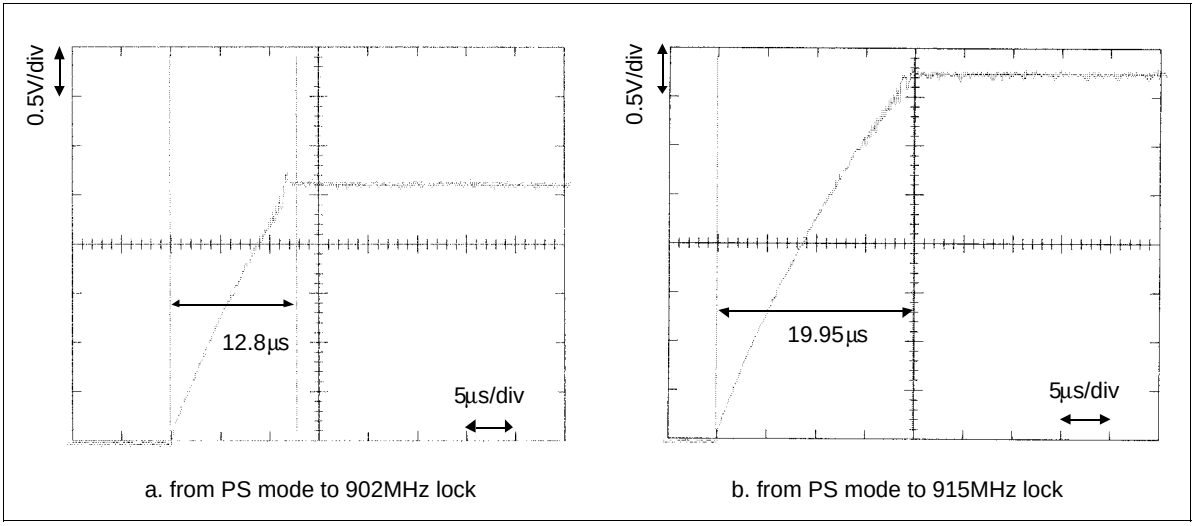
T=100°C 902MHz, PN9



T=100°C 902MHz, PN9

Figure 44 GMSK Modulated Transmitter Output Spectrum vs. Temperature

The Acquisition response of OPLL using 8.2 kΩ icurad is shown below. The control voltage of the VCO was observed by the digital storage oscilloscope.



a. from PS mode to 902MHz lock

b. from PS mode to 915MHz lock

Figure 45 Acquisition Time (Lock Up Time)

Transmitter Measurement Results (2) (R_{ICURAD} = 8.2 kΩ and IFLO using an internal IFVCO**)**

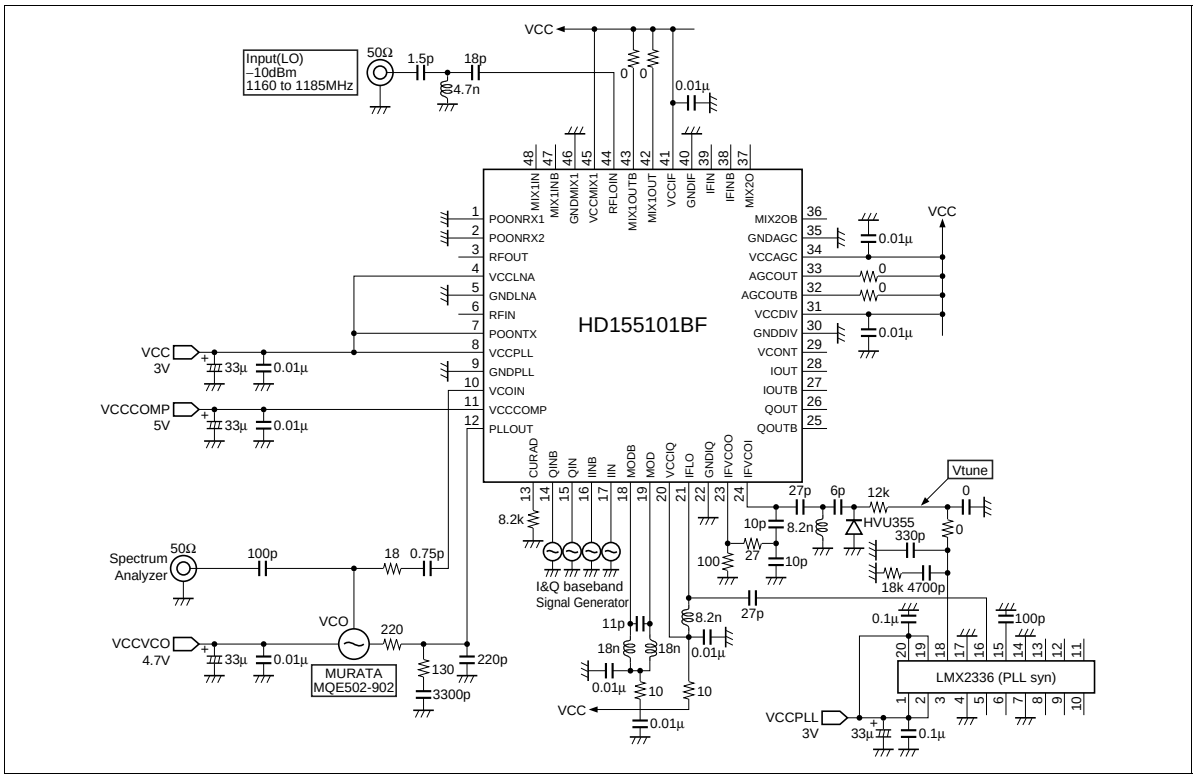
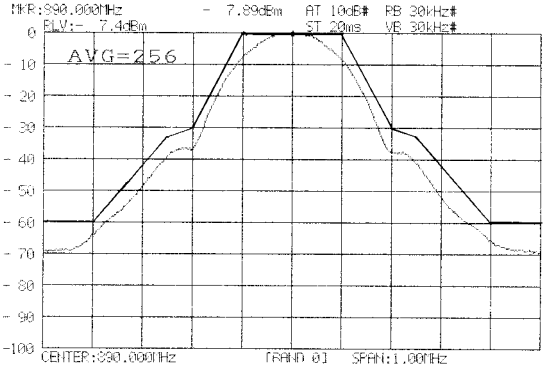


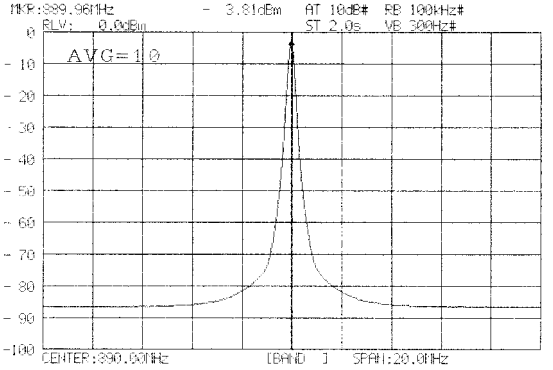
Figure 46 Evaluation Circuit Using Internal IFVCO for the I&Q Modulator and Offset PLL

Table 4 Measurement Results Using an Internal IFVCO (R_{ICURAD} = 8.2 kΩ)

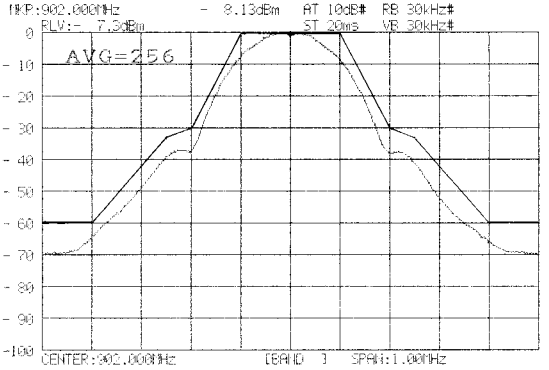
Item		Spec. (GSM Spec.)	Measured1	Measured2	Measured3	Unit
Measured frequency			890	902	915	MHz
200 kHz offset		≤ –33 (–30)	–35.64	–36.24	–36.93	dBc
400 kHz offset		≤ –63 (–60)	–63.63	–64.09	–64.09	dBc
600 kHz to 1.8 MHz offset		≤ –63 (–60)	–69.85	–69.95	–70.47	dBc
1.8 MHz to 3 MHz offset		≤ –66 (–63)	–76.89	–76.50	–76.04	dBc
3 MHz to 6 MHz offset		≤ –68 (–65)	–81.06	–80.67	–80.38	dBc
6 MHz upwards offset		≤ –74 (–71)	–82.67	–82.40	–82.34	dBc
Carrier suppression		≥ 31	41.87	42.50	42.42	dBc
Side band suppression		≥ 35	43.59	44.35	43.25	dBc
Phase accuracy	PN9	≤ 2.5 (5)	2.43	2.09	2.01	deg. rms
	PN9	≤ 6.0 (20)	6.56	6.06	6.41	deg. peak
	All ‘1’	≤ 2.5	0.95	0.93	0.96	deg. rms



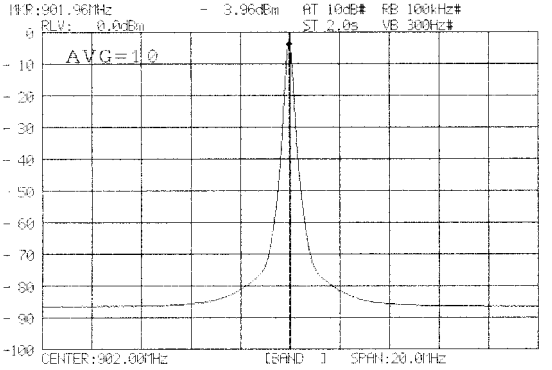
a-1. Spectrum1 (890MHz, PN9)



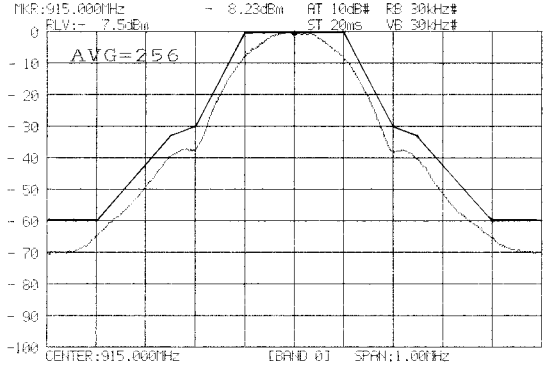
a-2. Spectrum2 (890MHz, PN9)



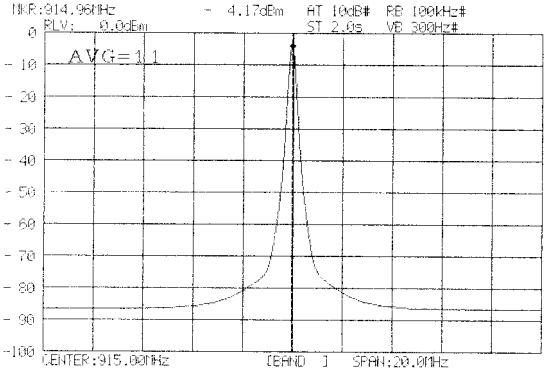
b-1. Spectrum1 (902MHz, PN9)



b-2. Spectrum2 (902MHz, PN9)



c-1. Spectrum1 (915MHz, PN9)



c-2. Spectrum2 (915MHz, PN9)

Figure 47 GMSK Modulated Transmitter Output Spectrum Using an Iternal IFVCO

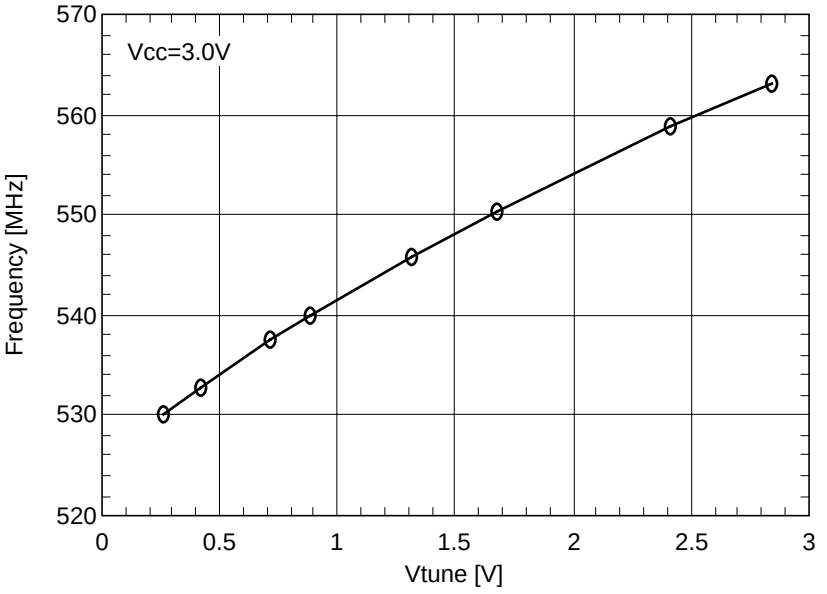


Figure 48 IFVCO Oscillation Frequency vs. Vtune Voltage

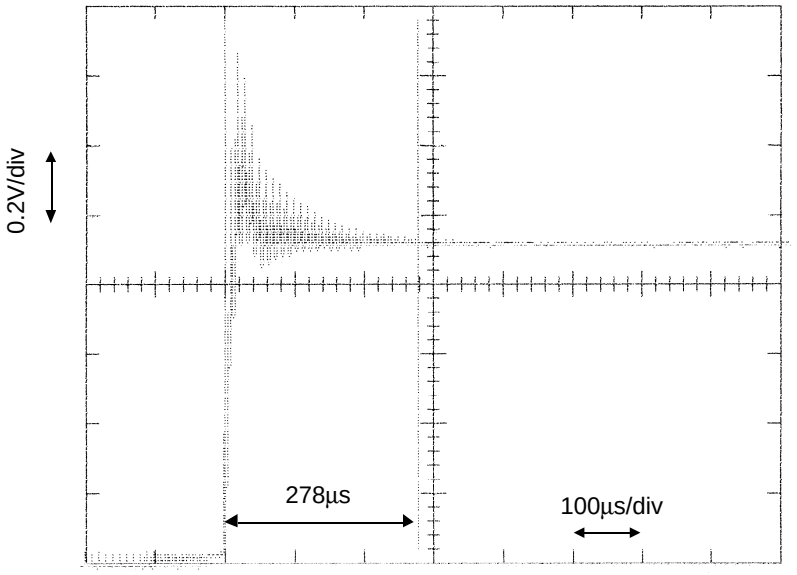
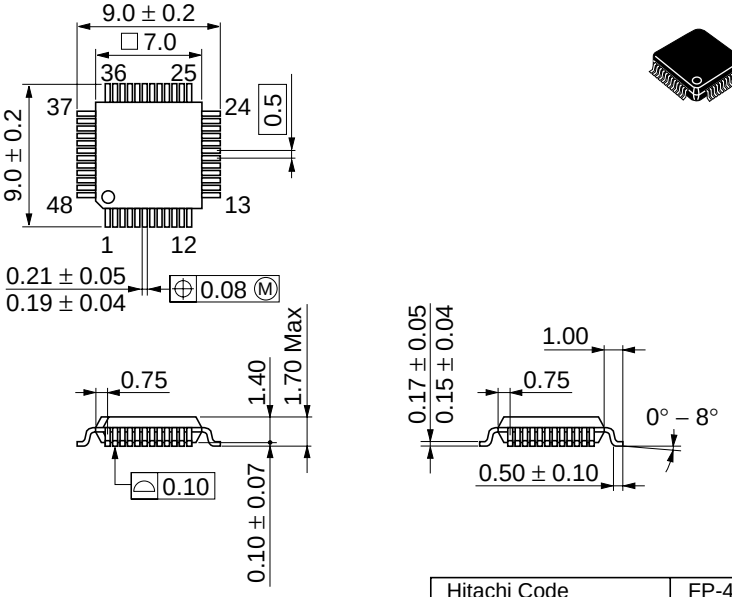


Figure 49 IFVCO Lock Up Time (from PS mode to 540 MHz)

Package Dimesions

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-48
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.2 g

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