H16550S — Universal Asynchronous Receiver/ Transmitter with FIFOs

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CAST, Inc.

11 Stonewall Court
Woodcliff Lakes
New Jersey 07677 USA
Phone: +1-201-391-8300
Fax: +1-201-391-8694
E-Mail: info@cast-inc.com
URL: www.cast-inc.com

Features

- Available under terms of the SignOnce IP License
- Capable of running all existing 16450 and 16550a Fully Synchronous-design software
- In FIFO mode, the transmitter and receiver are each buffered with 16 byte FIFOs to reduce the number of interrupts presented to the CPU
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Programmable baud generator divides any input clock by 1 to (2^{16} - 1) and generates the 16 x clock
- Modem control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully programmable serial interface

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core documentation
Design File Formats	EDIF Netlist; VHDL Source RTL (available at extra cost)
Constraints File	h16550s.ucf
Verification	VHDL testbench, test vectors
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
ModelSim v5.3	
Support	
Support provided by CAST, Inc.	

Applications

The core is suitable for implementing serial interfaces in a wide range of applications, including:

- Serial or modem computer interface
- Serial interface within modems and other devices

Table 1: Core Implementation Data

Supported Family	Device Tested	CLB Slices[2]	Clock IOBs[1]	IOBs[1]	Performance (MHz)	Xilinx Tools
Virtex	XCV50-6	319	1	38	56	ISE 4.1.01i
Virtex-E	XCV50E-8	385	1	38	81	ISE 4.1.01i
Virtex-II	XC2V80-5	293	N/A	39	87	ISE 4.1.01i
Spartan-II	XC2S30-6	319	1	38	63	ISE 4.1.01i
Spartan-IIE	XC2S50E-7	319	1	38	66	ISE 4.1.01i

Notes:
1. Assuming all core I/Os are routed off-chip
2. Optimized for speed

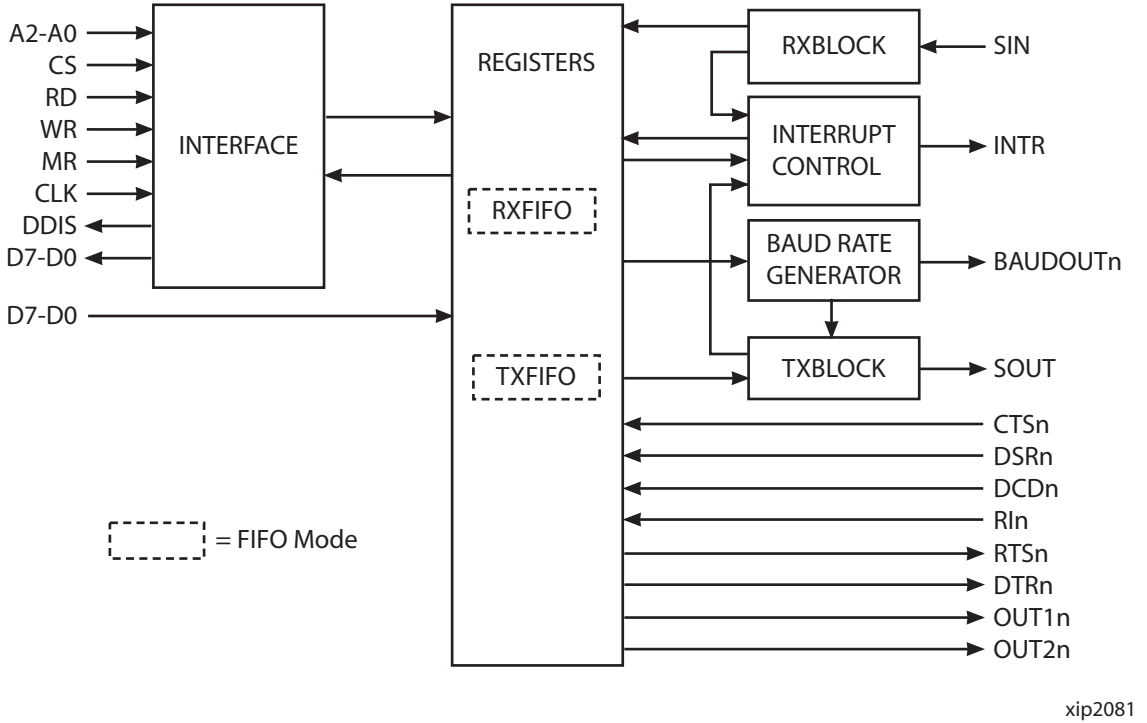

Figure 1: The H16550S Core

General Description

The H16550S is a standard UART providing 100% software compatibility with the popular Texas Instruments 16550 device. It performs serial-to-parallel conversion on data originating from modems or other serial devices, and performs parallel-to-serial conversion on data from a CPU to these devices.

The H16550S can be run in either 16450-compatible character mode or in 16550-compatible FIFO mode, where an internal FIFO relieves the CPU of excessive software overhead.

Developed for easy reuse in Xilinx FPGA applications, the H16550S is available optimized for several device families with competitive utilization and performance characteristics.

Functional Description

As shown above and explained below, the H16550S includes six major blocks: Interface, Registers, RXBlock, Interrupt Control, Baud Rate Generator, and TXBlock.

Interface

The Interface block handles the communications with the processor (or parallel) side of the system. All writing and reading of internal registers is accomplished through this block.

Registers

The Registers block holds all of the device's internal registers. See the Register Description table for details on existing registers and their addresses. Some information comes from the other blocks, but this is all gathered together in the Registers block and made available to all blocks.

RXBlock

This is the receiver block. It handles the receiving of the incoming serial word. It is programmable to recognize data widths such as 5, 6, 7 or 8 bits, various parity settings such as even, odd or no parity, and different stop bits of 1, 1½ and 2 bits. It checks for errors in the input data stream such as overrun errors, frame errors, parity errors and break errors. If the incoming word has no problems, it is placed either in the Receiver Holding register or in the Receiver FIFO, depending on the mode programmed.

Interrupt Control

The Interrupt Control block sends an interrupt signal back to the processor, depending on the state of the FIFO and its received and transmitted data. Various levels of interrupt

can be read from the Interrupt Identification register, which gives the level of interrupt. Interrupts are sent in response to the condition of empty transmission or receiving buffers (or FIFOs), an error in the receiving of a character, or other conditions requiring the attention of the processor.

Baud Rate Generator

This block takes the input clock, CLK, and divides it by a programmed value (from 1 to $2^{16} - 1$). This divided clock is then divided by 16 to create the transmission clock called the Baudout clock.

TXBlock

The Transmit block handles the transmission of data written to the Transmission Holding register (or transmit FIFO). It adds required start, parity, and stop bits to the data being transmitted so that the receiving device can do the proper error handling and receiving.

Core Modifications

The widths of the address and/or data fields (of the extended and pure mode of operation) can be customized.

Core Assumptions

The H16550S core is modeled after the Texas Instruments 16550. The following points differentiate the H16550S from the Texas Instruments device. A wrapper is required to create a core with the same functions. A sample wrapper is included.

- No provision is made for a crystal. The CLK input is designed to accept a standard digital input.
- The RCLK input in the Asynchronous version is replaced by CLK with rclk_enb which has the same frequency as BAUDOUTn.
- The bidirectional Data Bus has been split into an input and an output component. To use the core with a bi-directional Data Bus, the DDIS signal can be used as the controlling signal for the tri-state drivers.
- RD2, WR2, CS1 and CS2 have been eliminated. A single signal takes their place. These are RD, WR and CS.
- The ADSN signal has been removed. The H16550S functions as if the ADSN signal is held low. The included wrapper can be used to add the ADSN functionality latching the address and data buses.
- The main clock input CLK must be active from power-up.
- The Baudrate Generator is reset to the 0001h value upon activation of the MR signal. Programming the BRG to 0000h is an illegal value. The minimum value for the BRG is 0001h. Until the BRG is programmed, no output is generated.
- The Output Data Bus always shows the value of the last register read.

Verification Methods

The H16550S UART core's functionality has been extensively tested with a testbench and a large number of test patterns.

Pin Description

The signal names of the CAST H16550S core are shown in Table 2.

Table 2: Core Signal Pinout

Signal	Signal Direction	Polarity	Description
MR	Input	High	Master Reset
CLK	Input	-	Master clock
RD	Input	High	Read control
WR	Input	High	Write control
CS	Input	High	Chip Select
DIN[7:0]	Input	-	Data Input Bus
CTSn	Input	Low	Clear-to -Send
DSRn	Input	Low	Data Set Ready
DCDn	Input	Low	Data Carrier Detect
SIN	Input	-	Serial Input Data
RIn	Input	Low	Ring Indicator
A[2:0]	Input	-	Register Select
DOUT[7:0]	Output	-	Data Output Bus
SOUT	Output	-	Serial Output Data
DDIS	Output	High	Driver Disable
RTSn	Output	Low	Request-to-Send
DTRn	Output	Low	Data Terminal Ready
OUT1n	Output	Low	Output 1
OUT2n	Output	Low	Output 2
INTR	Output	High	Interrupt pending
BAUDOUTn	Output	Low	Baud Out
RXRDY	Output	Low	Receiver Ready to Receive Transmissions
TXRDY	Output	Low	Transmitter Ready to Transmit Data

Ordering Information

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Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For AllianceCORE-specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
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