Radiation Hardened Dual-D Flip-Flop with Set and Reset

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HCS74T is a Radiation Hardened Positive Edge Triggered Flip-Flop with set and reset.

The HCS74T utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HCS74T are contained in SMD 5962-95782. For more information, visit our website at: **www.intersil.com/**

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/

Ordering Information

ORDERING INFORMATION	PART NUMBER	TEMP. RANGE (^{O}C)
5962R9578201TCC	HCS74DTR	-55 to 125
5962R9578201TXC	HCS74KTR	-55 to 125

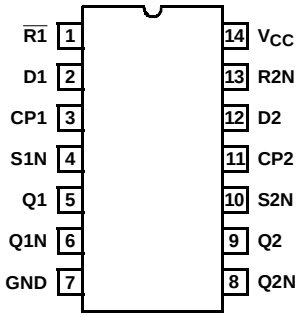
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

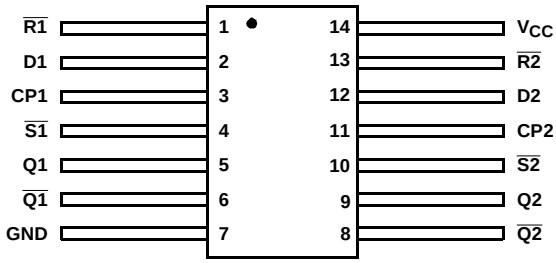
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - Latch-Up Free Under Any Conditions, SOS Process
  - SEP Effective LET No Upsets: >100 MEV-cm^2/mg
  - Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- 3 Micron Radiation Hardened SOS CMOS
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - V_{IL} = 30% of V_{CC} Max
  - V_{IH} = 70% of V_{CC} Min
- Input Current Levels Ii ≤ 5µA at V_{OL}, V_{OH}

Pinouts

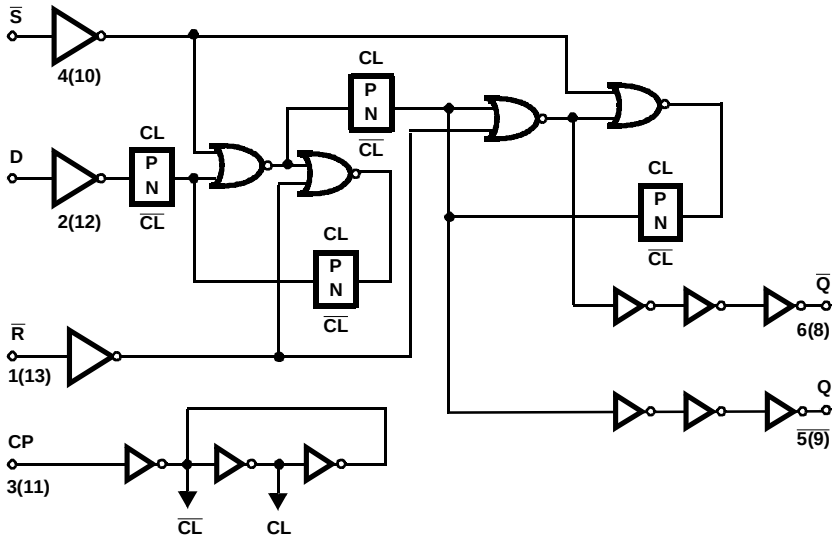
HCS74T (SBDIP), CDIP2-T14
TOP VIEW



HCS74T (FLATPACK), CDFP3-F14
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	⟋	H	H	L
H	H	⟋	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

NOTE: L = Logic Level Low, H = Logic Level High, X = Don't Care
⟋ = Transition from Low to High Level

Q0 = The level of Q before the indicated input conditions were established.

† This configuration is non-stable, that is, it will not persist when set and reset inputs return to their inactive (High) level.

Die Characteristics

DIE DIMENSIONS:

(2261µm x 2235µm x 533µm ±51µm)

89 x 88 x 21mils ±2mil

METALLIZATION:

Type: Al Si

Thickness: 11kÅ ±1kÅ

SUBSTRATE POTENTIAL:

Unbiased (Silicon on Sapphire)

BACKSIDE FINISH:

Sapphire

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 13kÅ ±2.6kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

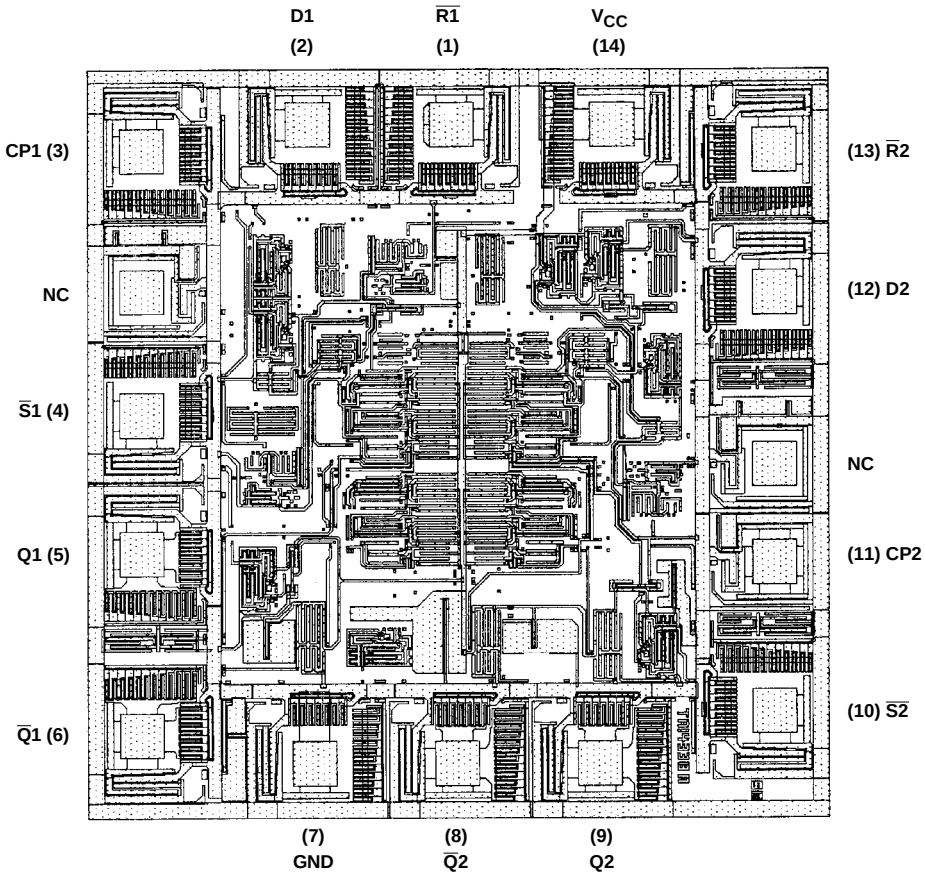
192

PROCESS:

CMOS SOS

Metallization Mask Layout

HCS74T



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.