HardCopy

Devices for APEX 20K Conversion

September 2001, ver. 1.0 Data Sheet

Introduction

HardCopy™ devices enable high-density APEX™ 20K device technology to be used in high-volume applications where significant cost reduction is desired. HardCopy devices are physically and functionally compatible with APEX 20KE and APEX 20KC devices. They combine the time-to-market advantage, performance, and flexibility of APEX 20K devices with the ability to move to high-volume, low-cost devices for production. The conversion process from an APEX 20K device to a HardCopy device is fully automated, with customer involvement limited to providing a few Quartus® II software-generated output files.

Features...

Preliminary Information

- HardCopy devices are manufactured using an 0.18-µm CMOS six-layer-metal fabrication process
  - Preserves functionality of a configured APEX 20KE or APEX 20KC device
  - Pin-compatible with APEX 20KE and APEX 20KC devices
  - Meets or exceeds timing of configured APEX 20KE and APEX 20KC devices
  - Optional emulation of original programmable logic device (PLD) programming sequence
  - High-performance, low-power device
  - MultiCore™ architecture integrating embedded memory and look-up table (LUT) logic used for register-intensive functions
  - Embedded system blocks (ESBs) used to implement memory functions, including first-in first-out (FIFO) buffers, dual-port RAM, and content-addressable memory (CAM)
  - Customization performed through metallization layers
- High-density architecture
  - 400,000 to 1.5 million typical gates (see Table 1)
  - Up to 51,840 logic elements (LEs)
  - Up to 442,368 RAM bits that can be used without reducing available logic

Table 1. HardCopy Device Features *Note (1)*

Feature	HC20K400	HC20K600	HC20K1000	HC20K1500
Maximum system gates	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	400,000	600,000	1,000,000	1,500,000
LEs	16,640	24,320	38,400	51,840
ESBs	104	152	160	216
Maximum RAM bits	212,992	311,296	327,680	442,368
Phase-locked loops (PLLs)	4	4	4	4
Maximum macrocells	1,664	2,432	2,560	3,456
Maximum user I/O pins	488	588	708	808

***Note to** Table 1:*

(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

…and more Features

- Low-power operation
  - 1.8-V supply voltage (see Table 2)
  - MultiVolt™ I/O support for 1.8-V, 2.5-V, and 3.3-V interfaces
  - ESBs offering power-saving mode
- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication and division
  - ClockShift™ feature providing clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR, synchronous dynamic RAM (SDRAM), and ZBT static RAM (SRAM)
  - 16 input and 16 output LVDS channels
  - Fast t_{CO} and t_{SU} times for complex logic
  - MultiVolt I/O support for 1.8-V, 2.5-V, and 3.3-V interfaces
  - Individual tri-state output enable control for each pin
  - Output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including LVDS, LVPECL, PCI-X, AGP, CTT, SSTL-3 and SSTL-2, GTL+, and HSTL Class I
  - Supports hot-socketing operation

Table 2. HardCopy Device Supply Voltages	
Feature	**Voltage**
Internal supply voltage (V_{CCINT})	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	1.8 V, 2.5 V, 3.3 V, 5.0 V *(1)*

***Note to** Table 2:*
(1) HardCopy devices can be 5.0-V tolerant by using an external resistor.

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- HardCopy device implementation features
  - Customized interconnect for each design
  - HardCopy devices preserve APEX device MegaLAB™ structure, LEs, ESBs, IOE, PLLs, and LVDS circuitry
  - Up to four metal layers customizable for customer designs
  - Completely automated proprietary design conversion flow
    - Testability analysis and fix
    - Automatic test pattern generation (ATPG)
    - Automatic place and route
    - Static timing analysis
    - Static functional verification
    - Physical verification

Tables 3 through 6 show the HardCopy device ball-grid array (BGA) and FineLine BGA™ package options, I/O counts, and sizes.

Table 3. HardCopy Device BGA Package Options & I/O Count *Note (1)*	
Device	**652-Pin BGA**
HC20K400	488
HC20K600	488
HC20K1000	488
HC20K1500	488

Table 4. HardCopy Device FineLine BGA Package Options & I/O Count *Note (1)*		
Device	**672-Pin**	**1,020-Pin**
HC20K400	488	–
HC20K600	508	588
HC20K1000	508	708
HC20K1500	–	808

Note to Tables 3 and 4:
(1) I/O counts include dedicated input and clock pins.

Table 5. HardCopy Device BGA Package Sizes

Feature	652-Pin BGA
Pitch (mm)	1.27
Area (mm^2)	2,025
Length × width (mm × mm)	45.0 × 45.0

Table 6. HardCopy Device FineLine BGA Package Sizes

Feature	672-Pin	1,020-Pin
Pitch (mm)	1.00	1.00
Area (mm^2)	729	1,089
Length × width (mm × mm)	27 × 27	33 × 33

General Description

HardCopy devices extend the flexibility of high-density PLDs to a cost-effective, high-volume production solution. The conversion process from an Altera® PLD to a HardCopy device offers seamless migration of a high-density system-on-a-programmable-chip (SOPC) design to a low-cost alternative device with minimal risk. Using HardCopy devices, Altera's SOPC solutions can be leveraged from prototype to production, while reducing costs and speeding time-to-market.

A significant benefit of HardCopy devices is that customers do not need to be involved in the device conversion process. Unlike application-specific integrated circuit (ASIC) development, the HardCopy design flow does not require generation of test benches, test vectors, or timing and functional simulation. The HardCopy conversion process only requires the Quartus II software-generated output files from a fully functional APEX 20KE or APEX 20KC device. Altera performs the conversion and delivers functional prototypes in as few as seven weeks.

A risk-free alternative to ASICs, HardCopy devices are customizable, full-featured devices created by Altera's proprietary design conversion methodology. They are based on Altera's industry-leading high-density device architecture and use an area-efficient sea-of-logic-elements (SOLE) core.

HardCopy devices retain all the same features as the APEX 20KE and APEX 20KC devices, which combine the strength of LUT-based and product-term-based devices in conjunction with the same embedded memory structures. All routing resources that were programmable in the APEX device family are replaced by custom interconnect, resulting in a considerable die size reduction and subsequent cost saving.

The SRAM configuration cells of the original PLD are replaced in HardCopy devices by metal elements, which define the function of each logic element (LE), embedded memory, and I/O cell in the device. These resources are connected to each other using the same metallization layers. Once a HardCopy device has been manufactured, the functionality of the device is fixed and no programming is possible. Altera performs the conversion of the original PLD design to an equivalent HardCopy device using a proprietary design conversion flow.

The conversion of a PLD to a HardCopy device begins with a user design that has been implemented in an APEX 20KE or APEX 20KC device. Table 7 shows the device equivalence for HardCopy and APEX devices.

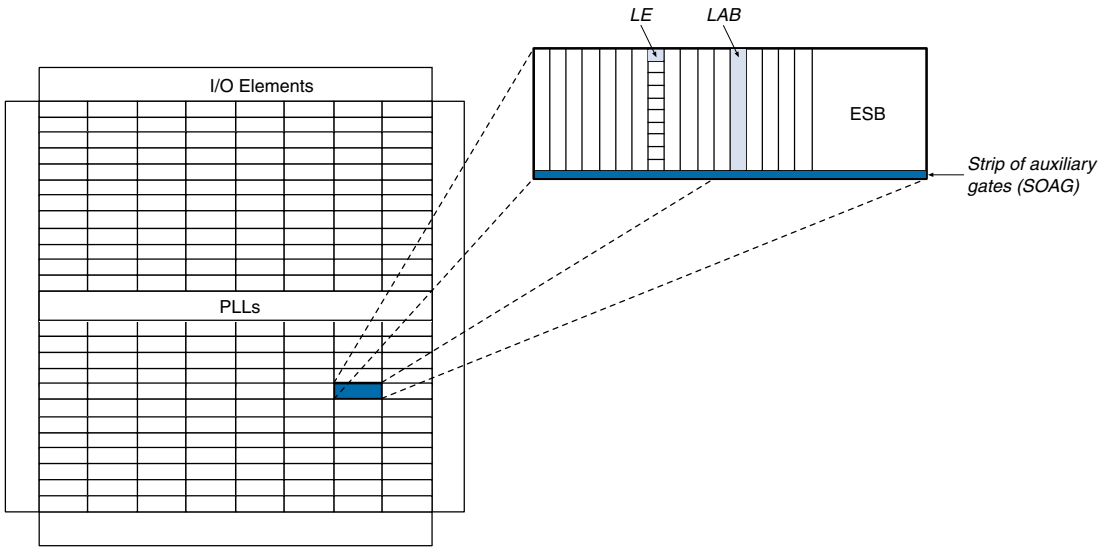
Table 7. HardCopy & APEX Device Equivalence

HardCopy 20K Device	APEX 20KE Device	APEX 20KC Device
HC20K1500	EP20K1500E	EP20K1500C
HC20K1000	EP20K1000E	EP20K1000C
HC20K600	EP20K600E	EP20K600C
HC20K400	EP20K400E	EP20K400C

To ensure HardCopy device performance and functionality, the APEX design must be completely debugged before committing the design to HardCopy device conversion.

HardCopy device implementation begins with extracting the Quartus II software-generated SRAM Object File (**.sof**) and converting its connectivity information into a structural Verilog netlist. This netlist is then placed and routed in a similar fashion to a gate array. There are no dedicated routing channels. The router can exploit all available metal layers (up to four) and route over LE cells and other functional blocks. Altera's proprietary architecture and design methodology will guarantee virtually 100% routing of any APEX 20KE or APEX 20KC design compiled and fitted successfully using the Quartus II software. Place and route is timing-driven and will comply with the timing constraints of the original PLD design as specified in the Quartus II software. Figure 1 shows a diagram of the HardCopy device architecture.

Figure 1. HardCopy Device Architecture



The strip of auxiliary gates (SOAG) is an Altera proprietary feature designed into the HardCopy device and is used during the HardCopy implementation process. The SOAG structures can be configured into several different types of functions through the use of metallization. For example, high fanout signals require adequate buffering, so buffers are built out of SOAG cells for this purpose.

HardCopy devices include the same advanced features as the APEX 20KE and APEX 20KC devices, such as enhanced I/O standard support, content-addressable memory (CAM), additional global clocks, and enhanced ClockLock circuitry. Table 8 lists the features included in HardCopy devices.

Table 8. HardCopy Device Features

Feature	HardCopy Devices
MultiCore system integration	Full support
Hot-socketing support	Full support
32-/64-bit, 33-MHz PCI	Full compliance
32-/64-bit, 66-MHz PCI	Full compliance
MultiVolt I/O	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected bank by bank 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction *m*/(*n* × *v)* clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift circuitry LVDS support Up to four PLLs ClockShift, clock phase adjustment
Dedicated clock and input pins	Eight
I/O standard support	1.8-V, 2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI and PCI-X 3.3-V AGP CTT GTL+ LVCMOS LVTTL True-LVDS™ and LVPECL data pins LVDS and LVPECL clock pins HSTL Class I PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	CAM Dual-port RAM FIFO RAM ROM

All HardCopy devices are tested using ATPG vectors prior to shipment. For fully synchronous designs near 100%, fault coverage can be achieved through the built-in full-scan architecture. ATPG vectors allow the designer to focus on simulation and design verification.

Because the configuration of HardCopy devices is built-in during manufacture, they cannot be configured in-system. However, if the APEX 20KE or APEC 20KC device configuration sequence must be emulated, the HardCopy device has this capability.

All of the device features of APEX 20KE and APEX 20KC devices are available in HardCopy devices. For detailed description of these device features, refer to the *APEX 20K Programmable Logic Device Family Data Sheet* and the *APEX 20KC Programmable Logic Device Family Data Sheet*.

Differences Between HardCopy & APEX Devices

Several differences must be considered before a design is ready for implementation in HardCopy technology:

- The HardCopy device is only customizable at the time it is manufactured. Make sure that the original APEX device has undergone thorough testing in the end-system before deciding to proceed with conversion to a HardCopy device because no changes can be made to the HardCopy device after it has been manufactured.
- ESBs that are configured as RAM or CAM will power-up un-initialized in the HardCopy device. In the PLD it is possible to configure, or "pre-load," the ESB memory as part of the configuration sequence, then overwrite it when the device is in normal functional mode. This pre-loaded memory feature of the PLD is not available in HardCopy devices. If a design contains RAM or CAM with assumed data values at power-up, then the HardCopy device will not operate as expected. If a design uses this feature, then it should be re-compiled without the memory pre-load. ESBs configured as ROM are fully supported.
- The JTAG boundary scan order in the HardCopy device is different compared to the APEX device. A HardCopy BSDL file that describes the re-ordered boundary scan chain should be used.

The BSDL files for HardCopy devices are different from the corresponding APEX 20KE or APEX 20KC devices. Download the correct HardCopy BSDL file from Altera's web site at **http://www.altera.com**.

- The advanced 0.18-µm aluminum metal process is used to support both APEX 20KE and APEX 20KC devices. The performance improvement achieved by the die size reduction and metal interconnect optimization more than offsets the need for copper in this case. Altera guarantees that a target HardCopy device will provide the same or better performance as in the corresponding APEX 20KC device.

Configuration Options

The three different configuration options available for the HardCopy device are: Instant On, 50 ms Delay, and Configuration Sequence Emulation. Each mode is described below.

- In Instant On mode, the HardCopy device is available for use shortly after the device receives power. The on-chip power-on-reset circuit will set or reset all registers. The CONF_DONE output will be tri-stated once the power-on reset (POR) has elapsed. No configuration device or configuration input signals are necessary.
- In 50 ms Delay mode, the HardCopy device will perform in a similar fashion to the Instant On mode, except that there will be an additional delay of 50 ms (nominal), during which time the device will be held in reset stage. The CONF_DONE output is pulled low during this time and then tri-stated after the 50 ms have elapsed. No configuration devices or configuration input signals are necessary for this option.
- In Configuration Sequence Emulation mode, the HardCopy device undergoes an emulation of a full configuration sequence as if configured by an external processor or an EPC device. In this mode, the CONF_DONE signal is tri-stated after the correct number of clock cycles. This mode may be useful where there is some dependency on the configuration sequence (e.g., multi-device configuration or processor initialization). In this mode, the device expects to see all configuration control and data input signals.

Speed Grades

Because HardCopy devices are customized, no speed grading is performed. All HardCopy devices will meet the timing requirements of the original PLD of the fastest speed grade. Generally, the HardCopy device will have a higher f_{MAX} than the corresponding PLD, but the speed increase will vary on a design-by-design basis.

Quartus II-Generated Output Files

The HardCopy conversion process requires several Quartus II software-generated files. These key output files are listed and briefly explained below.

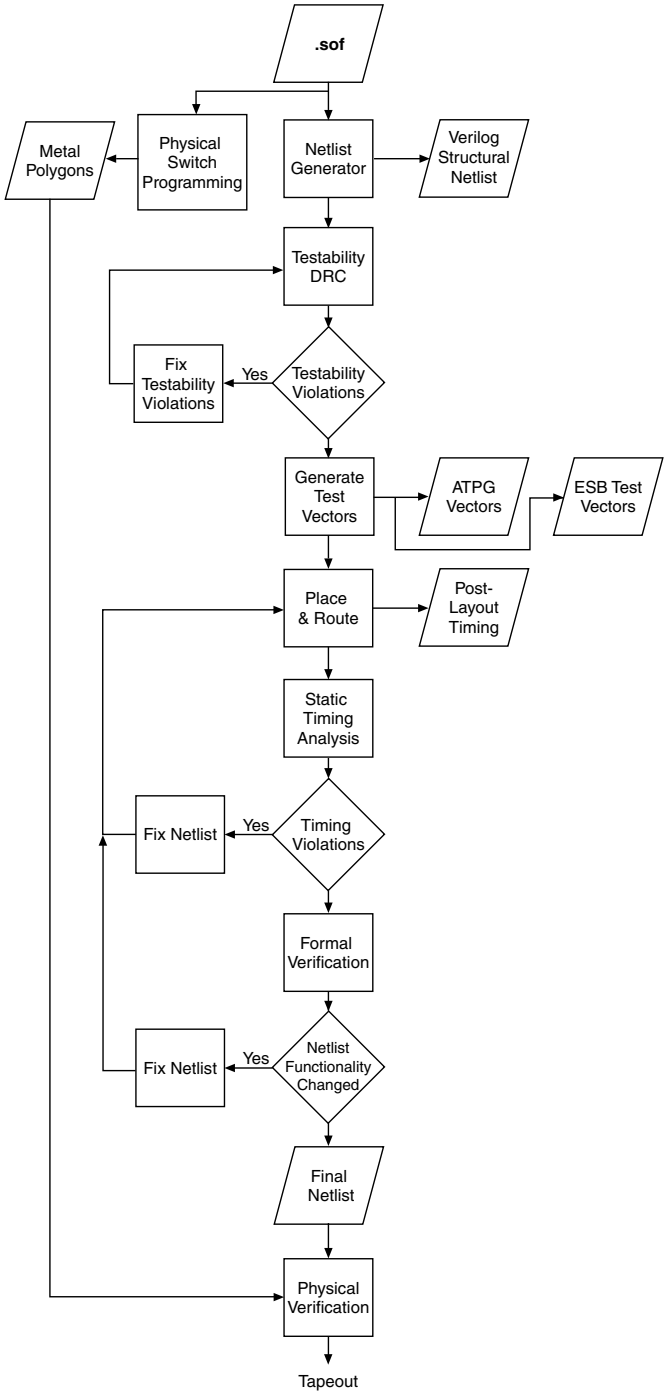
- The SRAM Object File (**.sof**) contains all of the necessary information needed to configure a PLD
- The Compiler Report File (**.csf.rpt**) is parsed to extract useful information about the design
- The Verilog atom-based netlist file (**.vo**) is used to check the HardCopy netlist
- The pin out information file (**.pin**) contains user signal names and I/O configuration information
- The Delay Information File (**.sdo**) is used to check the original PLD timing
- A completed HardCopy timing requirements file describes all necessary timing information on the design. A template of this text file is available for download from the Altera web site at **http://www.altera.com**.

The conversion process consists of several steps. First, a netlist is constructed from the SOF. Then, the netlist is checked to ensure that the built-in scan test structures will operate correctly. The netlist is then fed into a place-and-route engine, and the design interconnect is generated. Static timing analysis ensures that all timing constraints are met, and static functional verification techniques are employed to ensure correct device conversion. After successfully completing these stages, physical verification of the device takes place, and the metal mask layers are taped out to fabricate the HardCopy device.

Conversion Flow

Design conversion for HardCopy devices occurs in several steps, which are outlined in this section and shown in Figure 2. The conversion uses both proprietary and third-party EDA tools.

Figure 2. HardCopy Conversion Flow Diagram



Netlist Generation

Using an Altera proprietary conversion tool, the SOF is converted into a Verilog structural netlist. This netlist describes how each structural element (IOE, LE, ESB, PLL, and LVDS circuitry) in the design is configured and how each structural element is connected to other structural elements. The information that describes the structural element configuration is converted into a physical coordinate format so that metal elements can be implemented on top of the pre-defined HardCopy base array.

Testability Audit

Once the Verilog netlist is available, an audit is performed for testability violations. This audit ensures that all the built-in scan chain structures will work reliably during the testing of HardCopy devices. Certain circuit structures such as gated clocks, gated resets, oscillators, one shots, or any other type of asynchronous circuit structures will make the performance of scan chain structures unreliable. Thus, during this testability audit all such circuit structures are detected and disabled when the device is put into test mode.

Placement

The netlist is read into a place-and-route tool which then optimizes the placement of every LE and ESB that is used in the design. The optimization is based on the netlist connectivity in addition to the timing constraints of the design. The placement of all IOEs is fixed. After placement is complete, scan chain ordering information is generated so that the scan paths can be connected.

Test Vector Generation

ESB test vectors ensure that all memory bits function correctly. ATPG vectors test all LE and IOE logic. These vectors ensure that a high stuck-at-fault coverage is achieved. The target fault coverage figure for all HardCopy devices is at least 95%.

Once the testability audit is completed successfully and the scan chains have been re-ordered, ESB and ATPG test vectors can be generated. Once test vector generation is complete, they are simulated to verify correct operation.

Routing

Routing can commence in parallel with the test vector generation. Routing involves generating the physical interconnect between every element in the design. At this stage, physical design rule violations are fixed. For example, nodes with large fan-outs need to be buffered, otherwise the transition time of these signals will be too slow and the power consumption of the device will increase. The SOAG structures are used for this purpose. All other types of physical design rule violations are also fixed during this stage, such as antenna violations.

Extracted Delay Calculation

Once the routing is complete, interconnect parasitic capacitance and resistance information is generated. This is converted into a Standard Delay Format File (**.sdf**) with a delay calculation tool. Timing for minimum delays is generated in addition to maximum delays.

Static Timing Analysis & Timing Closure

The timing of the design is checked and corrected after place and route using the post-layout generated SDF. Setup time violations are corrected in two ways. First, extra buffers, which are created using SOAG resources, can be inserted to speed up slow signals. Second, if buffer insertion does not completely fix the setup violation, the placement can be re-optimized.

Setup time violations are rare in HardCopy devices because the die size is considerably smaller than the equivalent APEX 20KE or APEX 20KC device. Statistically, the interconnect loading and distance is much smaller in HardCopy devices, so the device will operate at a higher clock frequency. Hold-time violations are fixed by inserting delay elements into fast data paths. The delay elements are also built out of SOAG resources.

Once all timing violation corrections have been implemented in the netlist, the placement and routing is updated to reflect the changes. This process is iterated until all timing violations are removed. Typically only a single iteration is required after the initial place and route. Finally, static functional verification is tested after this stage to double-check the netlist integrity.

Formal Verification

After any change to the netlist, its integrity must be verified through static functional verification (or formal verification) techniques and involves showing that two versions of a design are functionally identical when certain constraints are applied. For example, the netlist after test fixes must be logically equivalent to the netlist before test fixes when the test mode is disabled. This technique does not rely on any customer-supplied functional simulation vectors.

Physical Verification

Before manufacturing the metal customization layers, the physical programming information must be verified. This stage involves cross-checking for physical design rule violations in the layout database, and also checking that the circuit was physically implemented correctly. These processes are commonly known as running design rule check (DRC) and layout versus schematic (LVS) verification.

Manufacturing

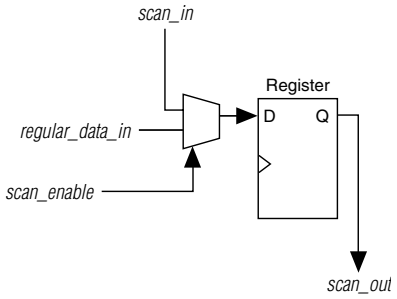
Metallization masks are created to manufacture HardCopy devices. After manufacturing, the parts are tested using the test vectors that were developed as part of the implementation process.

Testing

HardCopy devices are fully tested as part of the manufacturing process. No user-specific simulation vectors are required for this purpose, as every HardCopy device utilizes full scan path technology. This means that every node inside the chip is both controllable and observable through one or more of the package pins of the device. The scan paths, or "scan chains," are exercised through ATPG. This ensures a high-confidence level that all manufacturing defects are detected.

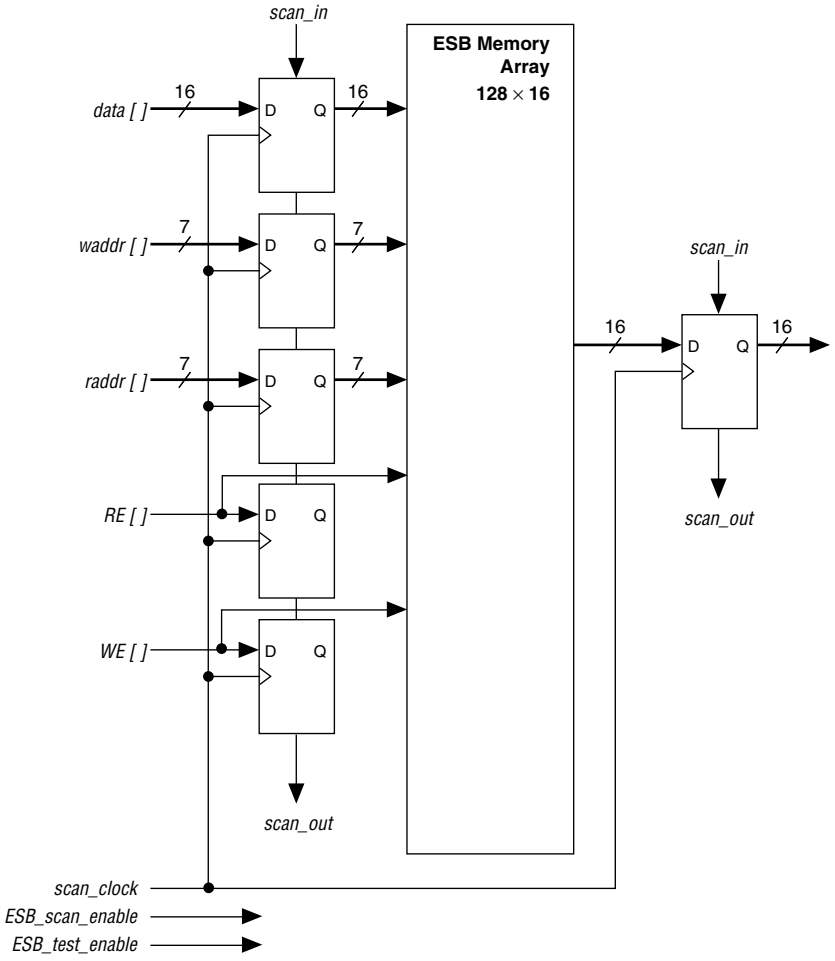
Every register in the HardCopy device belongs to a scan chain. Scan chains are test features that exist in ASICs to ensure that access to all internal nodes of a design is possible. With scan chains, defective parts can be screened out during the manufacturing process. Scan chain registers are constructed by combining the original PLD register with a 2-to-1 multiplexer. In normal user mode, the multiplexer is transparent to the user. In scan mode, the registers in the device are connected into a long shift register so that ATPG vectors can be scanned into and out of the device. Several independent scan chains exist in the HardCopy device. Figure 3 shows a diagram of a scan register.

Figure 3. HardCopy Scan Chain Circuitry



In addition to the scan circuitry, which is designed to test all LEs and IOEs, every ESB contains dedicated test circuitry so that all bits inside the memory array are tested for correct operation. Access to the ESB memory is also facilitated through scan chains. The ESB also offers an ESB test mode in which the ESB is reconfigured into a 128 × 16 RAM block. In this mode, data is scanned into the ESB I/O registers and written into the ESB memory. For ESBs configured as product-term logic or ROM, the write enable signal will have no effect on the ESB memory array data. When the test mode is disabled (default), the ESB reverts to the desired user functionality. Figure 4 shows the ESB test mode configuration.

Figure 4. ESB Test Mode Configuration



PLLs are tested through the use of built-in self test (BIST) circuitry and test point additions. All test circuitry is disabled once the device is installed into the end user system so that the device then behaves in the expected normal functional mode.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All HardCopy devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. HardCopy devices support the JTAG instructions shown in Table 9.

The BSDL files for HardCopy devices are different from the corresponding APEX 20KE or APEX 20KC parts. Download the correct HardCopy BSDL file from Altera's web site at **http://www.altera.com**.

Table 9. HardCopy JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	SAMPLE/PRELOAD allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. It is also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO

The HardCopy device instruction register length is 10 bits; the USERCODE register length is 32 bits. Tables 10 and 11 show the boundary-scan register length and device IDCODE information for HardCopy devices.

Table 10. HardCopy Boundary-Scan Register Length

Device	Boundary-Scan Register Length
HC20K400	1,506
HC20K600	1,806
HC20K1000	2,190
HC20K1500	2,502

Table 11. 32-Bit HardCopy Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
HC20K400	0000	1000 0100 0000 0000	000 0110 1110	1
HC20K600	0000	1000 0110 0000 0000	000 0110 1110	1
HC20K1000	0000	1001 0000 0000 0000	000 0110 1110	1
HC20K1500	0000	1001 0101 0000 0000	000 0110 1110	1

***Notes to** Table 11:*
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 5 shows the timing requirements for the JTAG signals.

Figure 5. HardCopy JTAG Waveforms

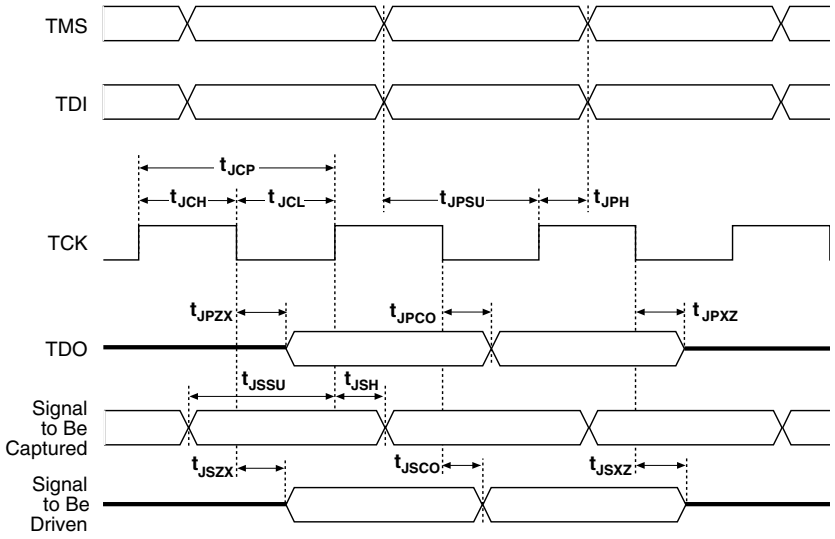


Table 12 shows the JTAG timing parameters and values for HardCopy devices.

Table 12. HardCopy JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

For more information on using JTAG BST circuitry in Altera devices, see *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices).*

Operating Conditions

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V HardCopy devices.

Table 13. HardCopy Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	2.5	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	BGA packages, under bias		135	° C

Table 14. HardCopy Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(2)*, *(5)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time (10% to 90%)			40	ns
t_F	Input fall time (90% to 10%)			40	ns

Table 15. HardCopy Device DC Operating Conditions *Notes (6), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level LVTTL, CMOS, or 3.3-V PCI input voltage		1.7, 0.5 × V_{CCIO} *(8)*		4.1	V
V_{IL}	Low-level LVTTL, CMOS, or 3.3-V PCI input voltage		–0.5		0.8, 0.3 × V_{CCIO} *(8)*	V
V_{OH}	3.3-V high-level LVTTL output voltage	I_{OH} = –12 mA DC, V_{CCIO} = 3.00 V *(9)*	2.4			V
	3.3-V high-level LVCMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(9)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(9)*	1.7			V
V_{OL}	3.3-V low-level LVTTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*			0.4	V
	3.3-V low-level LVCMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(10)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(10)*			0.1 × V_{CCIO}	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(10)*			0.7	V
I_I	Input pin leakage current *(11)*	V_I = 4.1 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current *(11)*	V_O = 4.1 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration emulation	V_{CCIO} = 3.0 V *(12)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(12)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(12)*	60		150	kΩ

Table 16. HardCopy Device Capacitance *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to** Tables 13 **through** 16**:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –0.5 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins (including dedicated inputs, clock, I/O, and JTAG pins) may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V, or 3.3 V.
(7) These values are specified under the HardCopy device recommended operating conditions, shown in Table 14 on page 20.
(8) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the V_{IH}, V_{IL}, V_{OH}, V_{OL}, and I_I parameters when V_{CCIO} = 1.8 V.
(9) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(10) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(11) This value is specified for normal device operation. The value may vary during power-up.
(12) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(13) Capacitance is sample-tested only.

Tables 17 through 32 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only; HardCopy devices may exceed these specifications.

Table 17. LVTTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –12 mA, V_{CCIO} = 3.0 V *(1)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 12 mA, V_{CCIO} = 3.0 V *(2)*		0.4	V

Table 18. LVCMOS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Power supply voltage range		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	V_{CCIO} = 3.0 V I_{OH} = –0.1 mA *(1)*	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0 V I_{OL} = 0.1 mA *(2)*		0.2	V

Table 19. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA *(1)*	2.1		V
		I_{OH} = –1 mA *(1)*	2.0		V
		I_{OH} = –2 mA *(1)*	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA *(2)*		0.2	V
		I_{OL} = 1 mA *(2)*		0.4	V
		I_{OL} = 2 mA *(2)*		0.7	V

Table 20. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.7	1.9	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage			0.35 × V_{CCIO}	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(1)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*		0.45	V

Table 21. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.5		$0.3 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 22. 3.3-V PCI-X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.5		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
I_{IL}	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10.0		10.0	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1500 µA			$0.1 \times V_{CCIO}$	V
L_{PIN}	Pin Inductance				15.0	nH

Table 23. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		450	mV
Δ V_{OD}	Change in VOD between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
Δ V_{OS}	Change in VOS between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to APEX devices)		90	100	110	Ω

Table 24. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 36 mA *(2)*			0.65	V

Table 25. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –7.6 mA *(1)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 7.6 mA *(2)*			V_{TT} – 0.57	V

Table 26. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA *(2)*			V_{TT} – 0.76	V

Table 27. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			V_{TT} – 0.6	V

Table 28. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(1)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(2)*			V_{TT} – 0.8	V

Table 29. HSTL Class I I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.71	1.8	1.89	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		0.68	0.75	0.90	V
V_{IH}	High-level input voltage		V_{REF} + 0.1		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			0.4	V

Table 30. LVPECL Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output Supply Voltage	3.135	3.3	3.465	V
V_{IH}	Low-level input voltage	1,300		1,700	mV
V_{IL}	High-level input voltage	2,100		2,600	mV
V_{OH}	Low-level output voltage	1,450		1,650	mV
V_{OL}	High-level output voltage	2,275		2,420	mV
V_{ID}	Input voltage differential	400	600	950	mV
V_{OD}	Output voltage differential	625	800	950	mV
t_r, t_f	Rise and fall time (20 to 80%)	85		325	ps
t_{DSKEW}	Differential skew			25	ps
t_O	Output load		150		Ω
R_L	Receiver differential input resistor		100		Ω

Table 31. 3.3-V AGP I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OUT} = –500\ \mu A$	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	$I_{OUT} = 1500\ \mu A$			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Table 32. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF} *(3)*	Termination and reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$			V
V_{IL}	Low-level input voltage				$V_{REF} – 0.2$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	$I_{OH} = –8$ mA *(1)*	$V_{REF} + 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA *(2)*			$V_{REF} – 0.4$	V
I_O	Output leakage current (when output is high Z)	$GND \le V_{OUT} \le V_{CCIO}$	–10		10	µA

Notes to** Tables 17 **through** 32**:

(1) The I_{OH} parameter refers to high-level output current.
(2) The I_{OL} parameter refers to low-level output current. This parameter applies to open-drain pins as well as output pins.
(3) V_{REF} specifies center point of switching range.

Figure 6 shows the output drive characteristics of HardCopy devices.

Figure 6. Output Drive Characteristics of HardCopy Devices

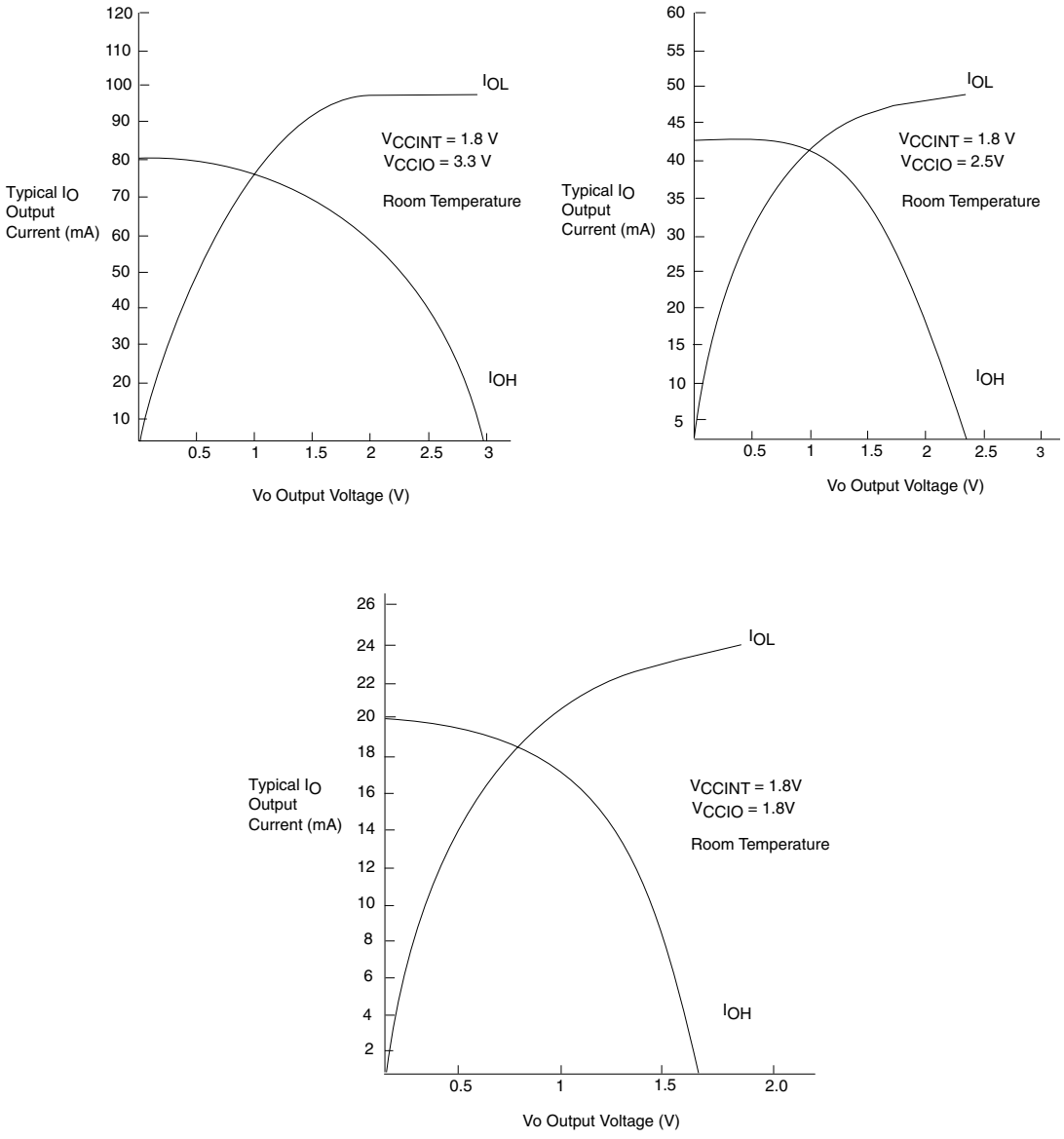
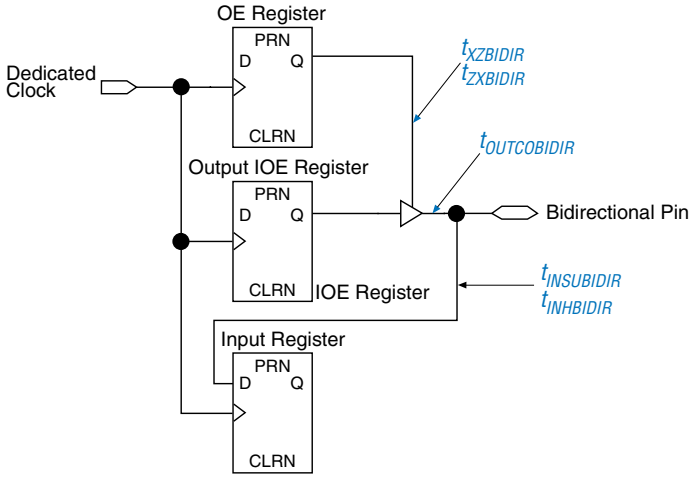


Figure 7 shows the timing model for bidirectional I/O pin timing.

Figure 7. Synchronous Bidirectional Pin External Timing



Tables 33 and 34 describe HardCopy device external timing parameters.

Table 33. HardCopy Device External Timing Parameters *Note (1)*

Symbol	Clock Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 35 pF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 35 pF

Table 34. HardCopy Device External Bidirectional Timing Parameters *Note (1)*		
Symbol	**Parameter**	**Condition**
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at LAB-adjacent input register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at LAB-adjacent input register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
$t_{XZBIDIR}$	Synchronous output enable register to output buffer disable delay	C1 = 35 pF
$t_{ZXBIDIR}$	Synchronous output enable register to output buffer enable delay	C1 = 35 pF
$t_{INSUBIDIRPLL}$	Setup time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{INHBIDIRPLL}$	Hold time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{OUTCOBIDIRPLL}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE register	C1 = 35 pF
$t_{XZBIDIRPLL}$	Synchronous output enable register to output buffer disable delay with PLL	C1 = 35 pF
$t_{ZXBIDIRPLL}$	Synchronous output enable register to output buffer enable delay with PLL	C1 = 35 pF

Note to** Tables 33 **and** 34**:
(1) These timing parameters are sample-tested only.

Tables 35 and 36 show the external timing parameters for HC20K1500 devices.

Table 35. HC20K1500 External Timing Parameters			
Symbol	**Min**	**Max**	**Unit**
t_{INSU}	2.0		ns
t_{INH}	0.0		ns
t_{OUTCO}	2.0	5.0	ns
$t_{INSUPLL}$	3.3		ns
t_{INHPLL}	0.0		ns
$t_{OUTCOPLL}$	0.5	2.1	ns

Table 36. HC20K1500 External Bidirectional Timing Parameters

Symbol	Min	Max	Unit
$t_{INSUBIDIR}$	1.9		ns
$t_{INHBIDIR}$	0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.0	ns
$t_{XZBIDIR}$		7.1	ns
$t_{ZXBIDIR}$		7.1	ns
$t_{INSUBIDIRPLL}$	3.9		ns
$t_{INHBIDIRPLL}$	0.0		ns
$t_{OUTCOBIDIRPLL}$	0.5	2.1	ns
$t_{XZBIDIRPLL}$		4.2	ns
$t_{ZXBIDIRPLL}$		4.2	ns

Note to** Tables 35 **and** 36**:

(1) Timing information is preliminary. Final timing information will be available in a future version of this data sheet.

Notes:

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