Using the HI1276 Evaluation Board

Application Note | September 1993 | AN9332

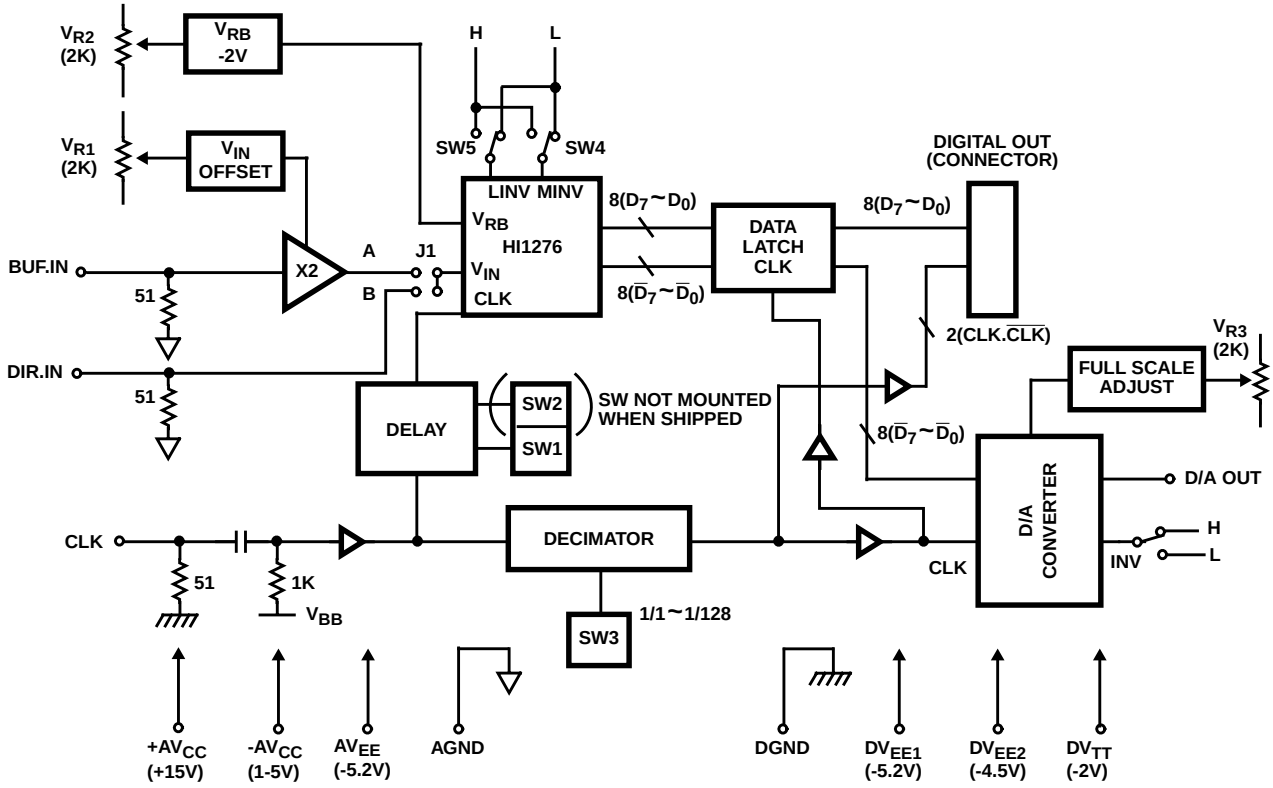
Description

The HI1276 evaluation board is a tool for customers to evaluate the performance of the HI1276AIL, an 8-bit, 500MSPS, high-speed A/D converter. In addition to features such as a reference voltage generator, this evaluation board is equipped with input voltage offset capability, a clock decimator, output data latches, a 10-bit high-speed DAC, and a 20-pin cable connector for digital outputs. This evaluation board is designed to facilitate evaluation of the HI1276AIL.

Features

- 8-Bit Resolution
- Maximum Conversion Rate 500MSPS
- Supply Voltages . . . . . .-5.2V, -4.5V, -2.0V, +15V, -15V
- Clock Level Converter . . . Sine Wave to ECL Level Signal
- Reference Voltage Adjustment Circuit for A/D Converter
- Built-In Clock Frequency Decimation Circuit . . . 1/1 to 1/128

Block Diagram



SUPPLY CURRENT

ITEM	MIN	TYP	MAX	UNIT
A_{VEE} + D_{VEE1} (-5.2V)	-	0.6	0.9	A
D_{VEE2} (-4.5V)	-	1.0	1.5	A
DVTT (-2.0V)	-	0.75	1.2	A
$-AV_{CC}$ (-15.0V)	-	60	100	mA
$+AV_{CC}$ (+15.0V)	-	50	100	mA

ANALOG INPUT

ITEM	MIN	TYP	MAX	UNIT
Input Voltage (BUF. IN) (Note 1)	-0.5	-	+0.5	V
Input Voltage (DIR. IN) (Note 1)	-2.0	-	0	V
Input Impedance	-	50	-	Ω

NOTE: For the analog input method, see Section 3 of “Adjustment Methods and Notes on Operation”.

CLOCK INPUT (CLK)

ITEM	MIN.	TYP	MAX	UNIT
Input Voltage (Peak to Peak)	-	1.0	-	V_{P-P}
Input Impedance	-	50	-	Ω

OUTPUT CODE TABLE

	MINV (SW5)	0	0	1	1
	LINV (SW4)	0	1	0	1
V_{IN}	0V	111 • • • 11	100 • • • 00	011 • • • 11	000 • • • 00
	•	111 • • • 10	100 • • • 01	011 • • • 10	000 • • • 01
	•	•	•	•	•
	•	•	•	•	•
	•	•	•	•	•
	•	100 • • • 00	111 • • • 11	000 • • • 00	011 • • • 11
	•	011 • • • 11	000 • • • 00	111 • • • 11	100 • • • 00
	•	•	•	•	•
	•	•	•	•	•
	•	•	•	•	•
	•	000 • • • 010	011 • • • 10	100 • • • 01	111 • • • 10
	-2V	000 • • • 00	011 • • • 11	100 • • • 00	111 • • • 11

1: ECL High Level
0: ECL Low Level

Adjustment Methods and Notes on Operation

1. V_{IN} offset (V_{R1}) - Centers the BUF. IN signal range (0V center assumed) within the A/D converter input range.
2. A/D Full Scale (V_{R2}) - Adjusts the A/D converter V_{RB} voltage (-2V typical).
3. J1 jumper wire selects the analog input pins BUF. IN or DIR. IN. (See Block Diagram.)

ANALOG INPUT METHOD	A	B	OFFSET
When Using BUF. IN	Shorted	Open	Adjusted by V_{R1}
When Using DC-Coupled DIR. IN Input	Open	Shorted	Input Offset Signal
When Using AC-Coupled DIR. IN Input	1kΩ	0.1µF	Adjusted by V_{R1}

4. D/A full scale (V_{R3}) - Adjusts the D/A output full scale voltage (-1V typ.).
5. SW1 and SW2 - Selection switches to adjust the clock delay. These switches enable the clock delay to be stepped to any one of 23 settings through binary input. Binary input from 00001 to 00110 increments the clock delay at approximately 125ps intervals. Binary input from 00111 to 10111 increments the clock delay at approximately 190ps intervals. The switches are designed such that, when SW1 is normally set to 1010 or A in hexadecimal, and SW2 is either set to L or not mounted, good timing margin can be achieved at any clock frequency.
6. SW3 (Decimation) - The switch to select clock frequency decimation. Selection settings are as follows:

NO.	DECIMATION RATE
0	1/1
1	1/2
2	1/4
3	1/8
4	1/16
5	1/32
6	1/64
7	1/128

7. SW4 - The switch for MINV High/Low
8. SW5 - The switch for LINV High/Low
9. SW6 (D/A INV) - The switch for D/A converter output inversion
10. Pins P4 to P33 facilitate probe GND connection. As shown in the Figure 2, the distance between the probe point and the GND is 300 mils, and there is 1.2mm throughhole for each probe point.The signal and GND locations are designed for use with a Tektronix GND tip (part number 013-1185-00).
11. D/A converter (IC11) input data (waveform probe pins P24 to P31) are the complementary signals of the decimated A/D converter outputs. These are inverted again in the D/A converter so that the polarity of the reproduced waveform matches the analog input to the A/D.
12. When observing the reproduced waveform (DA OUT output), set the decimator so that the clock frequency of the D/A converter (IC11: HI20201JCB) is less than 100MHz.
13. The part number of the digital output connector is KEL 8830E-020-170S. A corresponding connector and cable assembly is JUNKOSHA KB0020MCG50B1.
14. The buffer used on the evaluation board will give the best available performance. However, it is an expensive part and requires ±15V supplies. The circuit in Figure 3 is a much lower cost solution. It will have a bandwidth of about 250MHz with a slightly degraded SNR performance at higher input frequencies. It will provide a gain of approximately -2 and V_{OFFSET} can be driven from the same offset circuit used on the evaluation board.

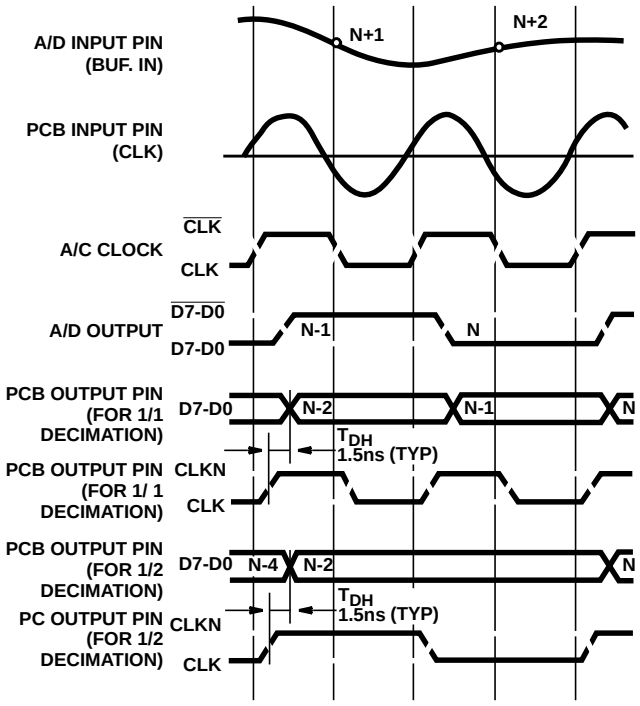


FIGURE 1.

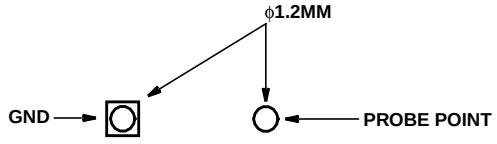


FIGURE 2.

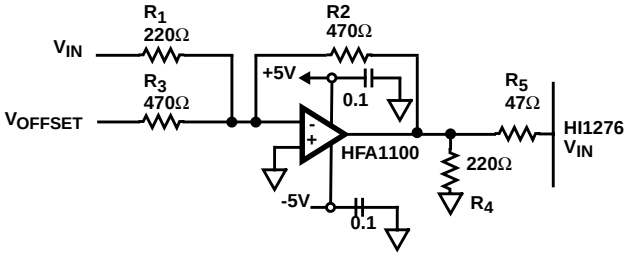


FIGURE 3. INVERTING BUFFER

Typical Performance Curves

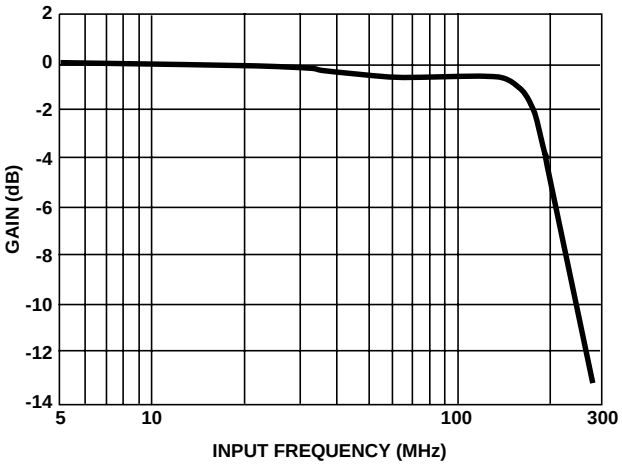


FIGURE 4. GAIN vs INPUT FREQUENCY

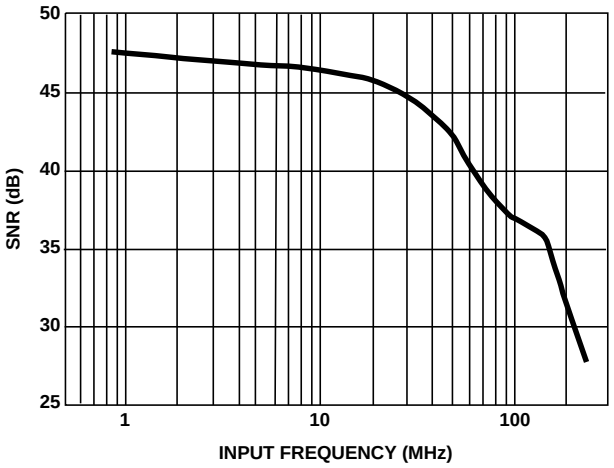


FIGURE 5. SNR vs INPUT FREQUENCY

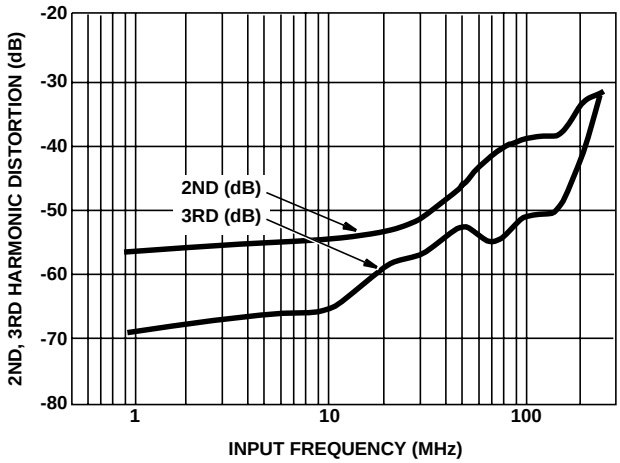
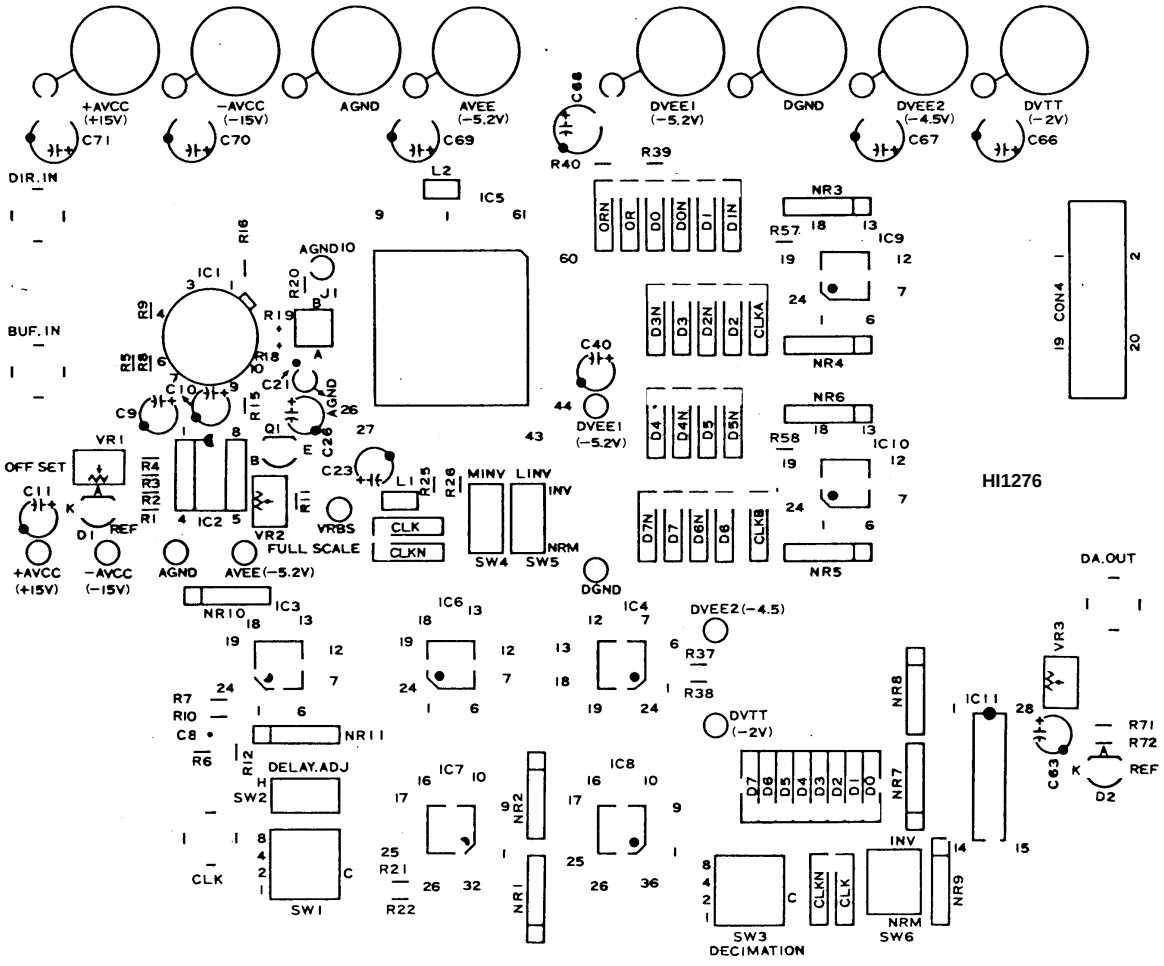


FIGURE 6. 2ND, 3RD HARMONIC DISTORTION vs INPUT FREQUENCY

Parts Layout

COMPONENT PLANE



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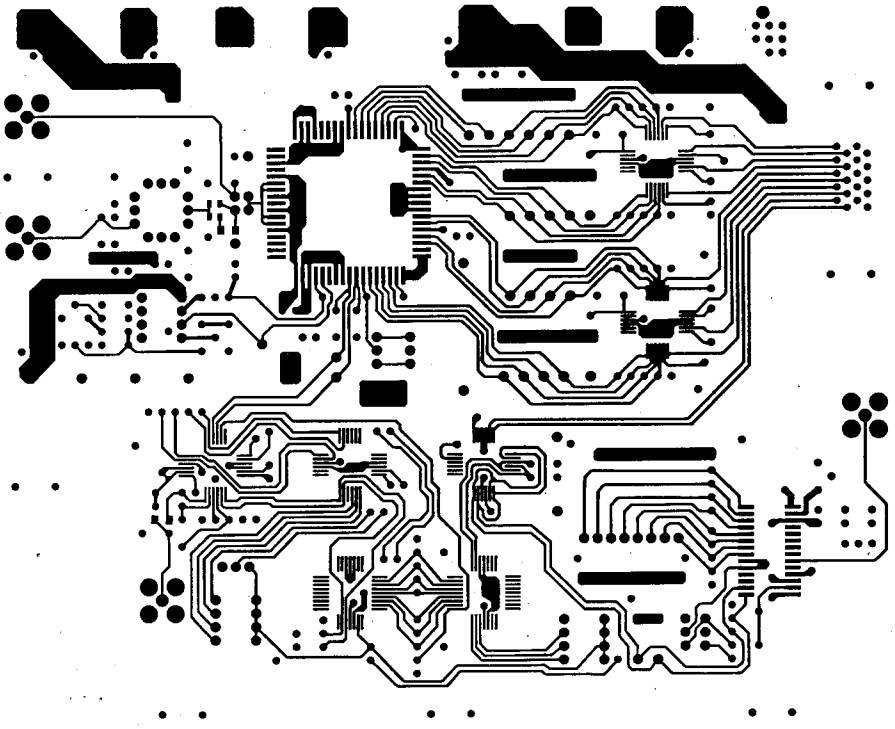
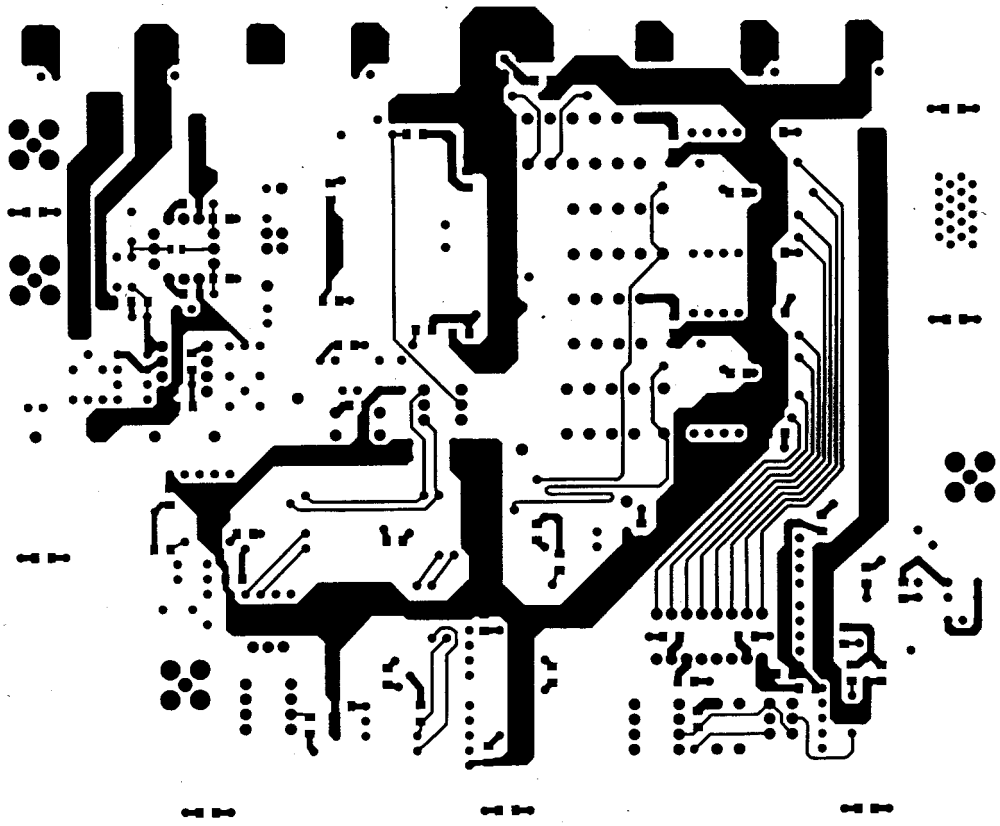
Print Pattern

COMPONENT PLANE

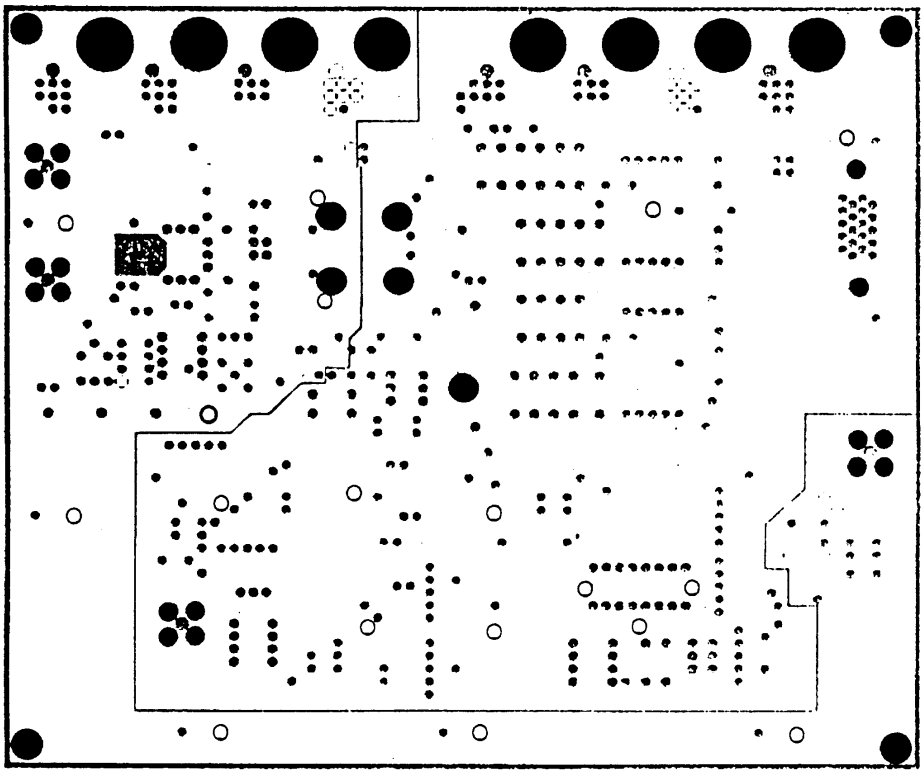


SOLDER PLANE

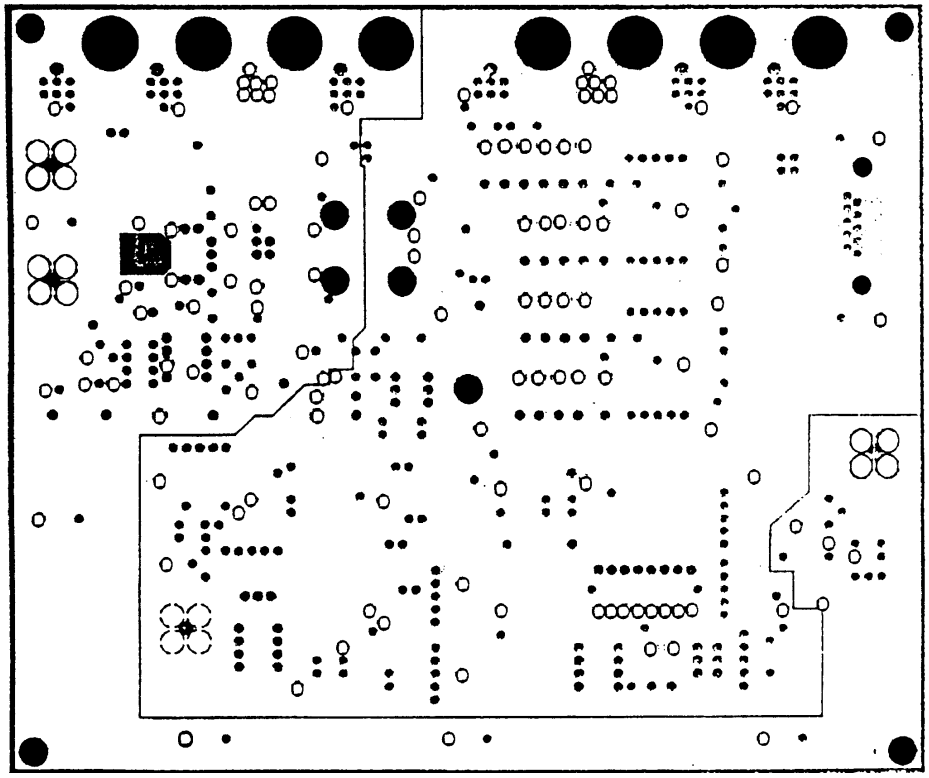


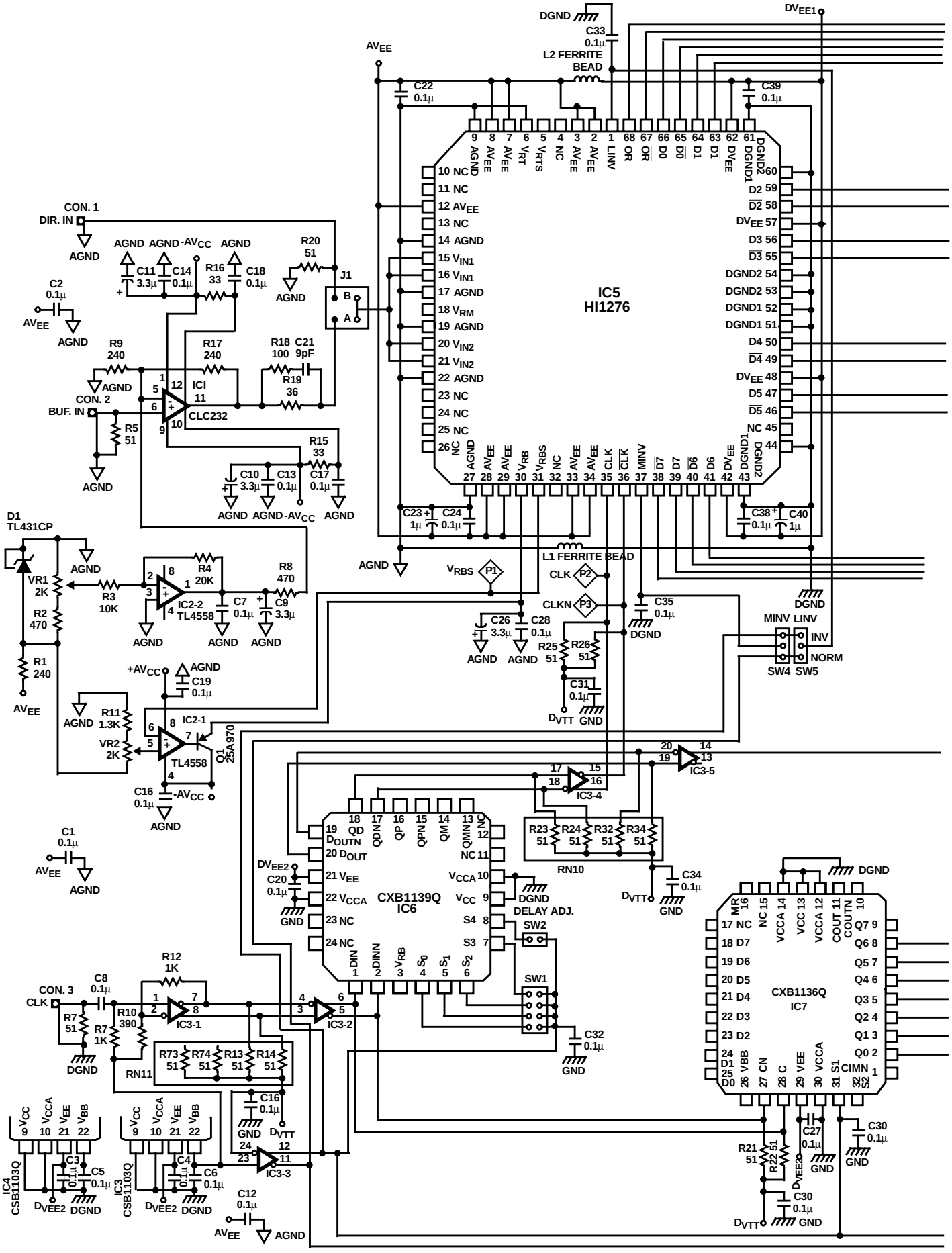
Print Pattern (Continued)

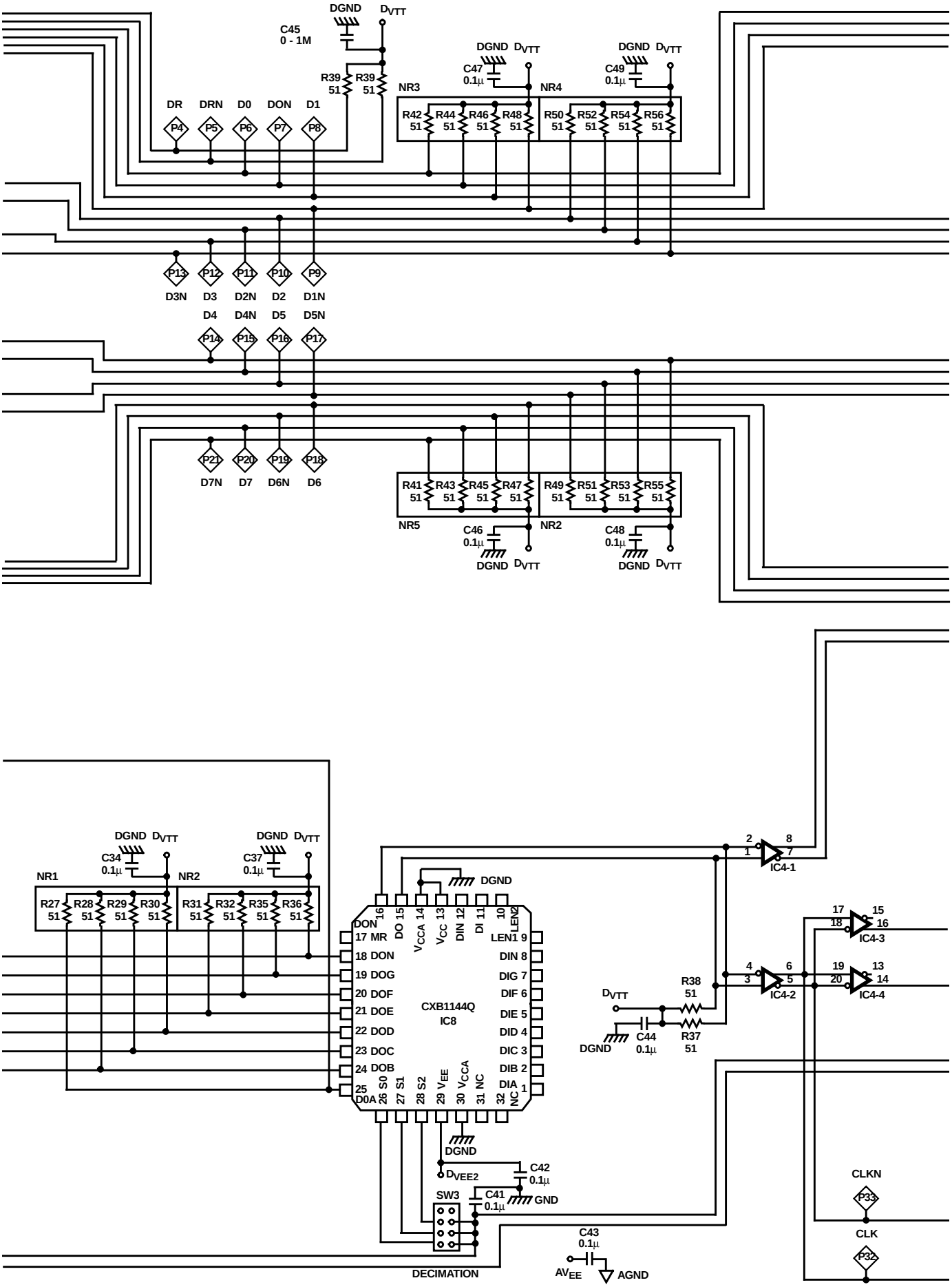
GND PLANE (INNER LAYER)

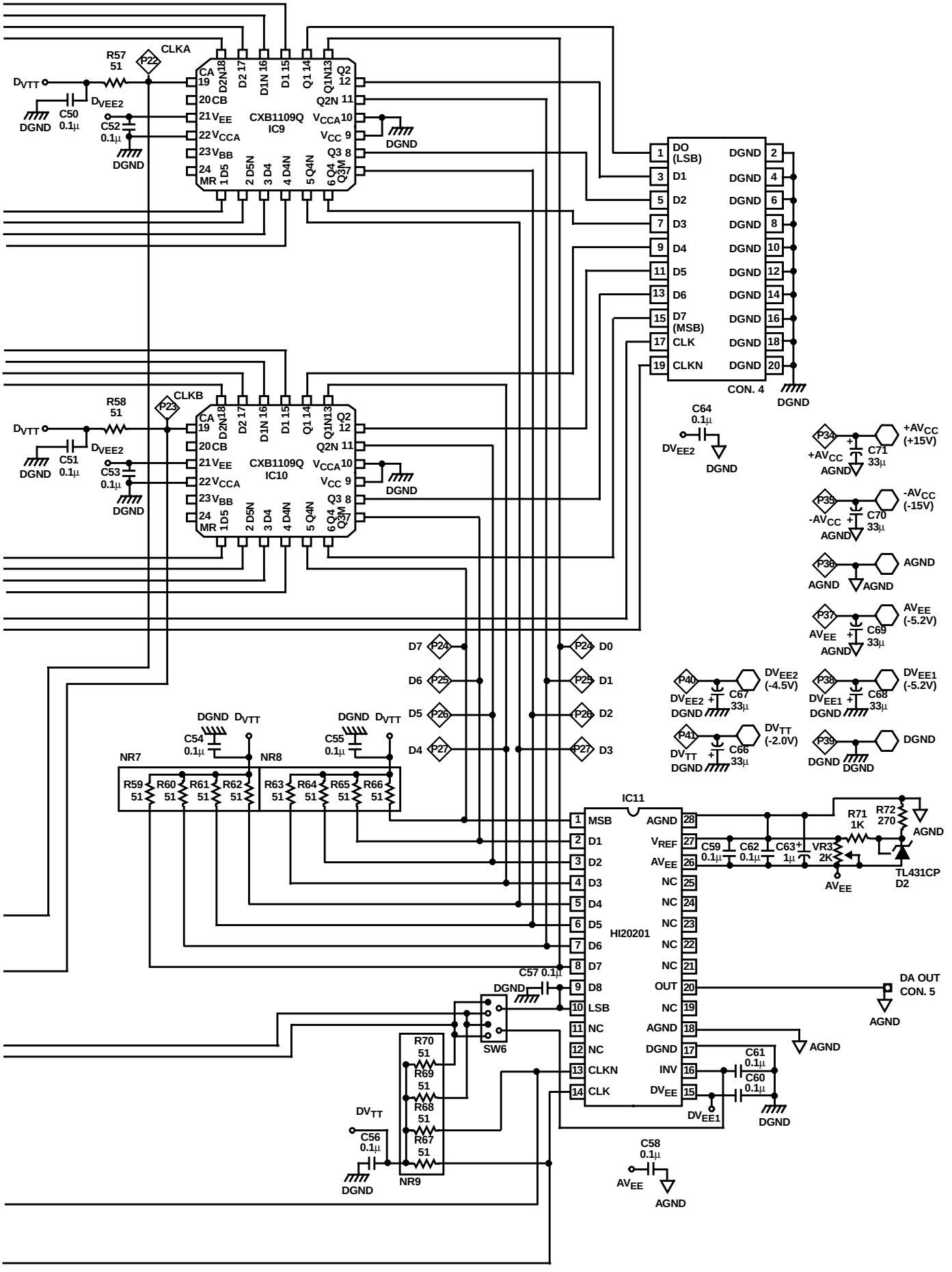


V_{EE} LAYER (INNER LAYER)




IC5
HI1276
IC6
CXB1139Q
IC7
CXB1136Q
IC4
CSB1103Q
IC3
CSB1103Q
CLC232
TL4558
TL431CP
25A970
CON. 1
DIR. IN
CON. 2
BUF. IN
CON. 3
CLK
J1
L2 FERRITE BEAD
L1 FERRITE BEAD
DELAY ADJ.
SW1
SW2
SW4
SW5
RN10
RN11
AGND
DGND
AVEE
DVEE1
DVEE2
DVTT
GND
-AVCC
+AVCC
VRBS
CLK
CLKN
MINV
LINV
INV
NORM


DGND
DVTT
C45
0 - 1M
R39
51
R39
51
DR
DRN
D0
DON
D1
P4
P5
P6
P7
P8
NR3
NR4
C47
0.1µ
C49
0.1µ
R42 R44 R46 R48
R50 R52 R54 R56
51
P13
P12
P11
P10
P9
D3N
D3
D2N
D2
D1N
D4
D4N
D5
D5N
P14
P15
P16
P17
P21
P20
P19
P18
D7N
D7
D6N
D6
R41 R43 R45 R47
R49 R51 R53 R55
NR5
NR2
C46
0.1µ
C48
0.1µ
NR1
C34
0.1µ
C37
0.1µ
R27 R28 R29 R30
R31 R32 R35 R36
CXB1144Q
IC8
DON
MR
DOG
DOF
DOE
DOD
DOC
DOB
D0A
S0
S1
S2
VEE
VCCA
NC
DIA
DIB
DIC
DID
DIE
DIF
DIG
DIN
LEN1
LEN2
DO
VCCA
VCC
DI
IC4-1
IC4-2
IC4-3
IC4-4
R38
51
R37
51
C44
0.1µ
C42
0.1µ
C41
0.1µ
SW3
GND
DVEE2
C43
0.1µ
AVEE
AGND
DECIMATION
CLKN
CLK
P33
P32


CLKA
CLKB
CXB1109Q
IC9
IC10
IC11
HI20201
CON. 4
DA OUT
CON. 5
TL431CP
D2
SW6
NR7
NR8
NR9
DGND
AGND
DVTT
DVEE2
DVEE1
AVEE
+AVCC
-AVCC
+AVCC (+15V)
-AVCC (-15V)
AVEE (-5.2V)
DVEE2 (-4.5V)
DVEE1 (-5.2V)
DVTT (-2.0V)
R57 51
R58 51
R59 51
R60 51
R61 51
R62 51
R63 51
R64 51
R65 51
R66 51
R67 51
R68 51
R69 51
R70 51
R71 1K
R72 270
C50 0.1µ
C51 0.1µ
C52 0.1µ
C53 0.1µ
C54 0.1µ
C55 0.1µ
C56 0.1µ
C57 0.1µ
C58 0.1µ
C59 0.1µ
C60 0.1µ
C61 0.1µ
C62 0.1µ
C63 1µ
C64 0.1µ
C67 33µ
C68 33µ
C69 33µ
C70 33µ
C71 33µ
VR3 2K
D7
D6
D5
D4
D0
D1
D2
D3
MSB
LSB
CLK
CLKN
INV
OUT
VREF