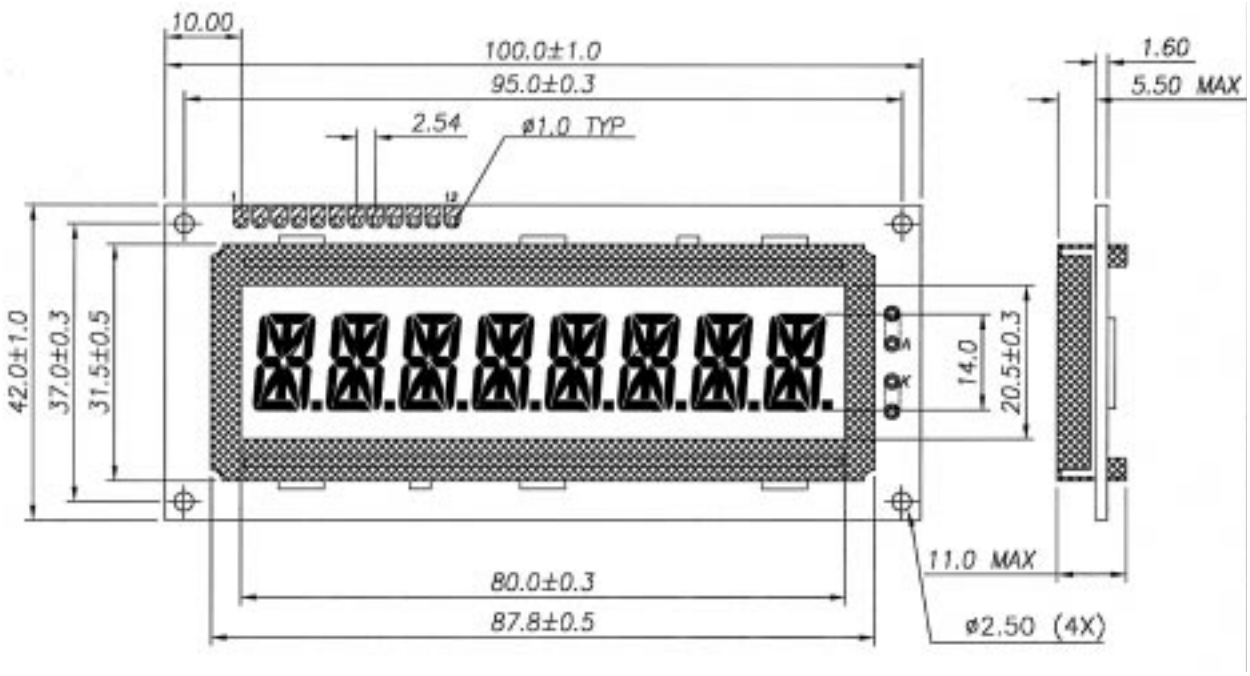
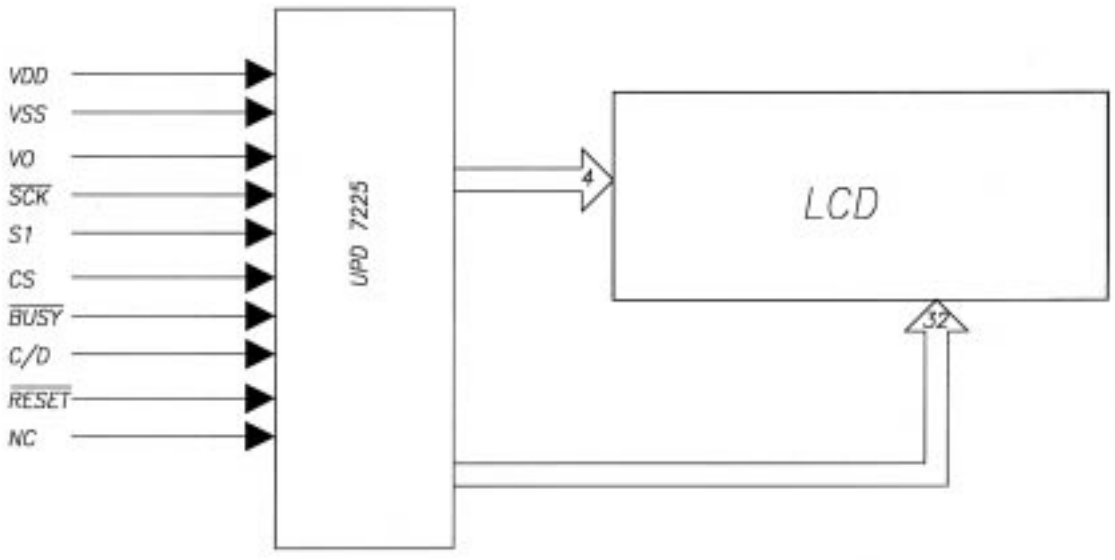
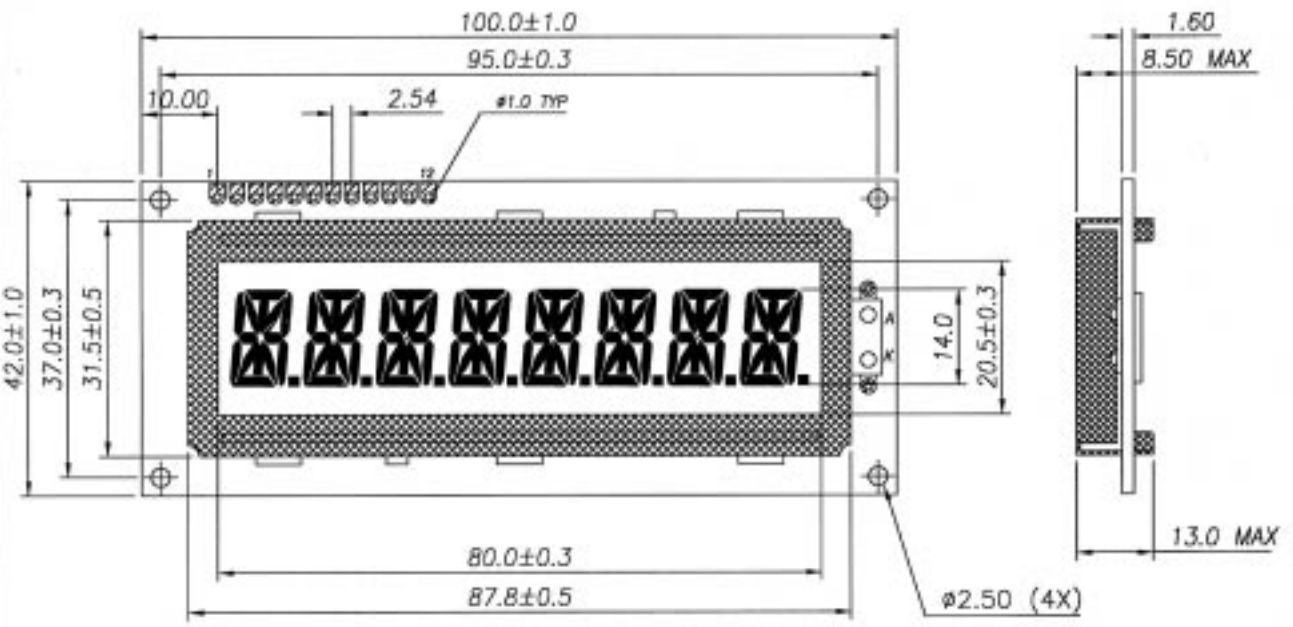
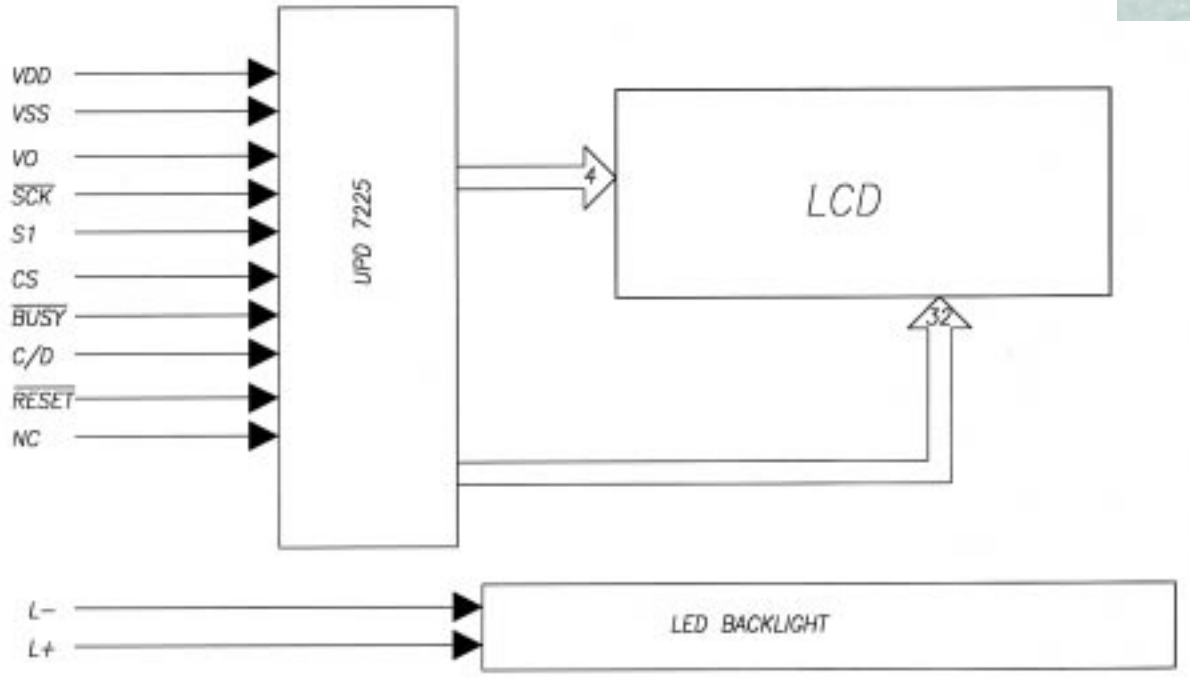


57 Block Diagram





Block Diagram



DECODED DISPLAY RAM DATA

14 - Segment Alphanumeric Data Decoder Character Set

Display byte (HEX)	Char	Display RAM address n+3	n+2	n+1	n
C0		A	7	C	0
C1		2	7	6	4
C2		8	7	8	5
C3		0	1	E	0
C4		8	7	8	1
C5		2	1	E	4
C6		2	1	6	4
C7		0	5	E	4
C8		2	6	6	4
C9		8	1	8	1
CA		0	6	C	0
CB		2	0	6	A
CC		0	0	E	0
CD		1	6	6	2
CE		1	1	6	8
CF		0	7	E	0

Display byte (HEX)	Char	Display RAM address n+3	n+2	n+1	n
D0		2	3	6	4
D1		0	7	E	8
D2		2	3	6	C
D3		1	5	8	4
D4		8	1	0	1
D5		0	6	E	0
D6		4	0	6	2
D7		4	6	6	8
D8		5	0	0	A
D9		9	0	0	2
DA		4	1	8	2
DB		Invalid			
DC		1	0	0	8
DD		Invalid			
DE		Invalid			
DF		Invalid			

DECODED DISPLAY RAM DATA

14 - Segment Alphanumeric Data Decoder Character Set

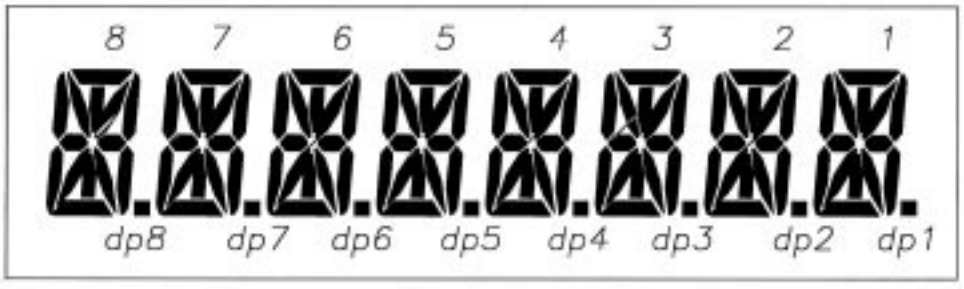
Display byte (HEX)	Char	Display RAM address n+3	n+2	n+1	n
A0		0	0	0	0
A1		Invalid			
A2		Invalid			
A3		Invalid			
A4		Invalid			
A5		Invalid			
A6		Invalid			
A7		0	0	0	2
A8		0	0	0	A
A9		5	0	0	0
AA		F	0	0	F
AB		A	0	0	5
AC		Invalid			
AD		2	0	0	4
AE		Invalid			
AF		4	0	0	2

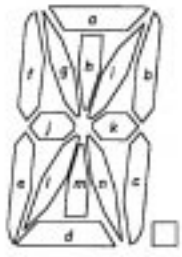
Display byte (HEX)	Char	Display RAM address n+3	n+2	n+1	n
B0		4	7	E	2
B1		0	6	0	0
B2		2	3	C	4
B3		2	7	8	4
B4		2	6	2	4
B5		2	5	A	4
B6		2	5	E	4
B7		0	7	0	0
B8		2	7	E	4
B9		2	7	A	4
BA		Invalid			
BB		Invalid			
BC		4	0	8	2
BD		2	0	8	4
BE		1	0	8	8
BF		Invalid			

INSTRUCTION SET

Command	Description	Instruction code D7 D6 D5 D4 D3 D2 D1 D0	HEX
1. MODE SET	Initialize the μPD7225 1) LCD Drive Configuration 2) LCD Bias Voltage Configuration 3) LCD Frame Frequency	0 1 0 0 0 0 1 0	42
2. UNSYNCHRONOUS DATA TRANSFER	Synchronize Display RAM data transfer to Display latch with CS	0 0 1 1 0 0 0 0	30
3. SYNCHRONOUS DATA TRANSFER	Synchronize display RAM data transfer to DISPLAY latch with LCD Drive Cycle	0 0 1 1 0 0 0 1	31
4. INTERRUPT DATA TRANSFER	Interrupt Display RAM data transfer to Display Latch	0 0 1 1 1 0 0 0	38
5. LOAD DATA POINTER	Load Data Pointer with 5 bits of immediate Data	1 1 1 D4 D3 D2 D1 D0	E0~EF
6. CLEAR DISPLAY RAM	Clear the Display RAM and reset the Data Pointer	0 0 1 0 0 0 0 0	20
7. WRITE DISPLAY RAM	Write 4 bits of immediate Data to the Display RAM Location addressed by the Data Pointer: Increment Data Pointer	1 1 0 1 D3 D2 D1 D0	D0~DF
8. AND DISPLAY RAM	Perform a Logical AND between the Display RAM data addressed by the Data Pointer and 4 bits of immediate Data: Write result to same Display RAM Location. Increment Data Pointer.	1 0 0 1 D3 D2 D1 D0	90~9F
9. OR DISPLAY RAM	Perform a Logical OR between the Display RAM data addressed by the Data Pointer and 4 bits of immediate Data: Write result to same Display RAM Location. Increment Data Pointer	1 0 1 1 D3 D2 D1 D0	B0~BF
10. ENABLE SEGMENT DECODER	Start use of the Segment Decoder	0 0 0 1 0 1 0 1	15
11. DISABLE SEGMENT DECODER	Stop use of the Segment Decoder	0 0 0 1 0 1 0 0	14
12. ENABLE DISPLAY	Turn on the LCD	0 0 0 1 0 0 0 1	11
13. DISABLE DISPLAY	Turn off the LCD	0 0 0 1 0 0 0 0	10
14. CLEAR BLINKING RAM	Clear the Blink RAM and reset the Data Pointer	0 0 0 0 0 0 0 0	0
15. WRITE BLINKING RAM	Write 4 bits of immediate Data to the blinking RAM Location addressed by the Data Pointer: Increment Data Pointer	1 1 0 0 D3 D2 D1 D0	C0~CF
16. AND BLINKING RAM	Perform a Logical AND between Blinking RAM data addressed to by the Data Pointer and 4 bits if immediate Data: Write result to the same Blinking RAM location: Increment Data Pointer	1 0 0 0 D3 D2 D1 D0	80~8F
17. OR BLINKING RAM	Perform a Logical OR between Blinking RAM data addressed by the Data Pointer and 4 bits if immediate Data: Write result to the same Blinking RAM location: Increment Data Pointer	1 0 1 0 D3 D2 D1 D0	A0~AF
18. ENABLE BLINKING	Start Segment Blinking at the Frequency Specified by 1 bit of Immediate Data	0 0 0 1 1 0 1 D0	1A~1B
19. DISABLE BLINKING	Stop Segment Blinking	0 0 0 1 1 0 0 0	18

DISPLAY PATTERN





BIT	Display RAM addressed 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	1h	X	1a	1g	2h	X	2a	2g	3h	X	3a	3g	4h	X	4a	4g	5h	X	5a	5g	6h	X	6a	6g	7h	X	7a	7g	8h	X	8a	8g
1	1i	1f	1b	1j	2i	2f	2b	2j	3i	3f	3b	3j	4i	4f	4b	4j	5i	5f	5b	5j	6i	6f	6b	6j	7i	7f	7b	7j	8i	8f	8b	8j
2	1k	1e	1c	1l	2k	2e	2c	2l	3k	3e	3c	3l	4k	4e	4c	4l	5k	5e	5c	5l	6k	6e	6c	6l	7k	7e	7c	7l	8k	8e	8c	8l
3	1n	1d	dp	1m	2n	2d	dp2	2m	3n	3d	dp3	3m	4n	4d	dp4	4m	5n	5d	dp5	5m	6n	6d	6d	6m	7n	7d	dp7	7m	8n	8d	dp8	8m

Note: X=1 or 0

HMU9509-LY

Digital Module

DESCRIPTION

HMU9509 is an 8-character, 14-segment intelligent module designed to communicate with microprocessor through an 8-bit serial interface.

FEATURES

- Low power consumption CMOS technology
- Compact design and easy panel mounting
- Built-in 14 segment ASCII alphanumeric decoder
- Two 32x4 static RAM for display data and blinking data storage
- An intelligent quadruplex driver display module
- Positive or negative mode option
- 14.00mm (0.55inch) alphanumeric Character height
- +5V single power supply
- Highly reliable and uniform LED backlight
- Serial data input

ELECTRICAL CHARACTERISTICS (Ta=+25°C, VDD=5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		3	5	5.5	V
Current consumption	I_{DD}			200		μA
Input high voltage	V_{IH}		0.7 VDD		VDD	V
Input low voltage	V_{IL}		0		0.3VDD	V
Output high voltage	V_{DH}	Output current =-10μA	VDD -0.5			V
Output low voltage	V_{DH}	Output current =-100μA			0.5	V
Power supply for LCD drive	V_{DD}-V_O	Ta=0°C		4.7		V
		Ta=25°C		4.5		V
		Ta=50°C		4		V
LED forward voltage	V_{LED}	L+ IF=80mA	4.5	5	5.5	V
Peak spectrum	λ	IF=80mA		565		nm
SCK cycle	t CYK		900			ns
SCK high pulse width	t WHK		400			ns
SCK low pulse width	t WLK		400			ns
SI set-up time to SLK	t ISK		100			ns
SI hold time after to SCK	t IHK		1200			ns
C/D set-up time to 8th. SCK	t DSK		9			μS
CD hold time after 8th. SCK	t DHK		1			μS
CS hold time after 8th. CLK	t CHK		1			μS
CS pulse width low	t CWL		40			μS
CS pulse width high	t CWH		40			μS

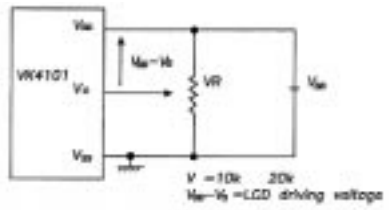
OPERATING SPECIFICATION

Operating Temperature	-10°C to +70°C
Storage Temperature	-30°C to +85°C
Operating Relative Humidity	90%max

DEFINITION OF TERMINALS

PIN ON.	SYMBOL	FUNCTION
1	VDD	Ground Terminal
2	VSS	Supply Terminal
3	VO	LCD driving voltage
4	SCK	Serial clock input
5	SI	Serial input
6	CS	Chip select input
7	BUSY	Busy output
8	C/D	Command/Data select
9	RESET	Reset input
10	NC	No connection
11	L-	Terminal for backlighting
12	L+	with limiting resistor

POWER SUPPLY



TIMING DIAGRAM