11/90

HD61202 (Dot matrix liquid crystal graphic display column driver)

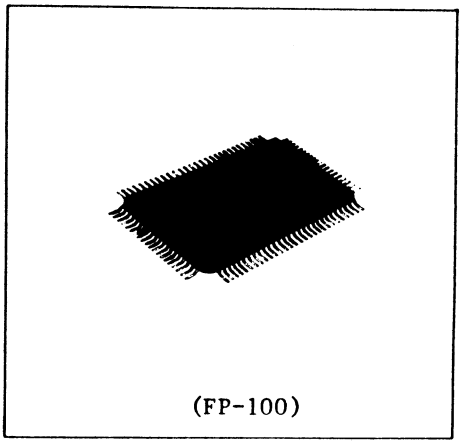
HD61202 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro-computer in the internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to ON/OFF of each dot of liquid crystal display to provide more flexible display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic display with many dots.

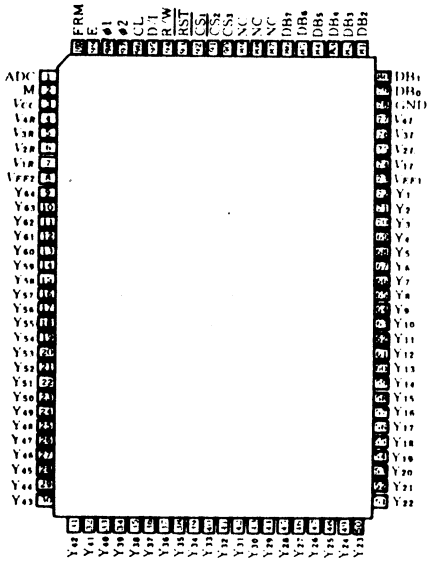
The HD61202 which is produced in the CMOS process, can accomplish a portable battery drive equipment by combining a CMOS micro-computer, utilizing the liquid crystal display's lower power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration by combining the row (common) driver HD61203.



(FP-100)

PIN ARRANGEMENT



(Top View)

FEATURES

- Dot matrix liquid crystal graphic display column driver incorporating display RAM.
- RAM data direct display by internal display RAM
  RAM bit data "1" ..... ON
  RAM bit data "0" ..... OFF
- Internal display RAM address counter preset, increment
- Display RAM capacity ..... 512 bytes (4096 bits)
- 8-bit parallel interface

ELECTRONIC ASSEMBLY GMBH
LOCHHAMER SCHLAG 17 · D-82166 GRÄFELFING
TELEFON 089/8541991 · TELEFAX 089/8541721

- Internal liquid crystal display driver circuit 64
- Display duty

  Drives liquid crystal panels with 1/32 ∿ 1/64 duty multiplexing.
- Wide range of instruction function

  Display Data Read/Write, Display ON/OFF, Set address, Set Display Start line, Read Status
- Lower power dissipation.....during display 2mW max
- Power supply Vcc_____5V ± 10%
- Liquid crystal display driving voltage___8V ∿ 15.5V
- CMOS process
- 100 - pin flat plastic package (FP-100)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V	2
	V_{EE1} V_{EE2}	V_{CC} -17.0 ∿ V_{CC} +0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} -0.3 ∿ V_{CC} +0.3	V	4
Terminal voltage (2)	V_{T2}	-0.3 ∿ V_{CC} +0.3	V	2, 5
Operating temperature	Topr	-20 ∿ +75	°C	
Storage temperature	Tstg	-55 ∿ +125	°C	

(Note 1) LSI's may be destroyed for ever, if being used beyond the absolute maximum ratings.
In ordinary operation, it is desirable to use them observing the recommended operation conditions.
Using beyond these conditions may cause malfunction and poor reliability.

(Note 2) All voltage values are referred to GND=0V.

(Note 3) Apply the same supply voltage to V_{EE} 1 and V_{EE2}.

(Note 4) Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R and V4R.
Maintain
Vcc≥V1L=V1R≥V3L=V3R≥V4L=V4R≥V2L=V2R≥VEE

(Note 5) Applies to M, FRM, CL, $\overline{RST}$, ADC, ϕ1, ϕ2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0∿7.

ELECTRICAL CHARACTERISTICS

(GND=0V, VCC=4.5 ∿ 5.5V, Vcc-VEE=8∿15.5V , Ta=-20∿+75°C)

Item	Symbol	Test condition	Limit			Unit	Note
			Min.	Typ.	Max.		
Input "High" voltage	V_{IHC}		0.7×Vcc	-	Vcc	V	1
	V_{IHT}		2.0	-	Vcc	V	2
Input "Low" voltage	V_{ILC}		0	-	0.3×Vcc	V	1
	V_{ILT}		0	-	0.8	V	2
Output "High" voltage	V_{OH}	IOH=-205μA	2.4	-	-	V	3
Output "Low" voltage	V_{OL}	IOL=1.6mA	-	-	0.4	V	3
Input leakage current	I_{IL}	Vin=GND∿Vcc	-1.0	-	+1.0	μA	4
Three state (OFF) input current	I_{TSL}	Vin=GND∿Vcc	-5.0	-	+5.0	μA	5
Liquid crystal supply leakage current	I_{LSL}	Vin=VEE∿Vcc	-2.0	-	+2.0	μA	6
Driver ON resistance	R_{ON}	Vcc-VEE=15V $\pm I_{LOAD}$=0.1mA	-	-	7.5	kΩ	
Dissipation current	Icc(1)	During display	-	-	100	μA	7
	Icc(2)	During access access cycle= 1MHz	-	-	500	μA	7

(Note 1) Applies to M, FRM, CL, $\overline{RST}$, φ1 and φ2.

(Note 2) Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I and DB0 ∿ 7.

(Note 3) Applies to DB0 ∿ 7.

(Note 4) Applies to terminals except for DB0 ∿ 7.

(Note 5) Applies to DB0 ∿ 7 at high impedance.

(Note 6) Applies to V1L ∿ V4L and V1R ∿ V4R.

(Note 7) Specified when liquid crystal display is in 1/64 duty.

Operation frequency f_{CLK}=250 kHz (φ1 and φ2 frequency)

Frame frequency f_M = 70 Hz (FRM frequency)

Specified in the state of

Output terminal ----- not loaded

Input level --------- V_{IH}=Vcc(V)

V_{IL}=GND (V)

Measured at Vcc terminal

● INTERFACE AC CHARACTERISTICS

MPU Interface

(GND=0V, Vcc=4.5 ∿ 5.5V, Ta=-20∿+75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	1, 2
E high level width	P_{WEH}	450	-	-	ns	1, 2
E low level width	P_{WEL}	450	-	-	ns	1, 2
E rise time	tr	-	-	25	ns	1, 2
E fall time	tf	-	-	25	ns	1, 2
Address setup time	t_{AS}	140	-	-	ns	1, 2
Address hold time	t_{AH}	10	-	-	ns	1, 2
Data setup time	t_{DSW}	200	-	-	ns	1
Data delay time	t_{DDR}	-	-	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	-	-	ns	1
Data hold time (Read)	t_{DHR}	20	-	-	ns	2

(Note 1)

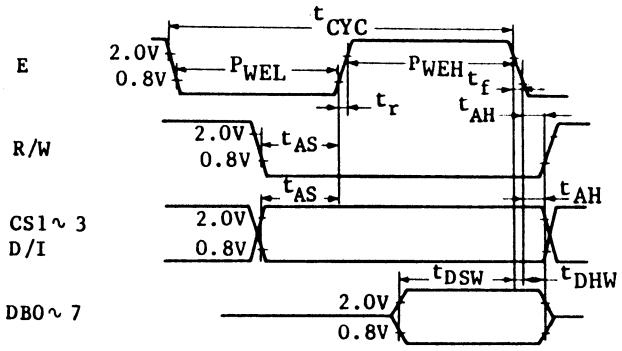


Fig. 1 CPU Write Timing

(Note 2)

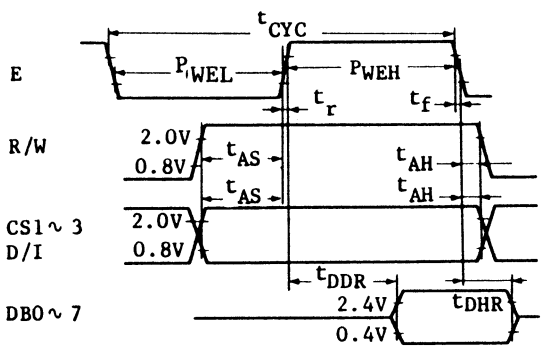
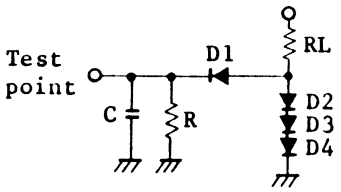


Fig. 2 CPU Read Timing

(Note 3) DB0 ∿ 7 : load circuit



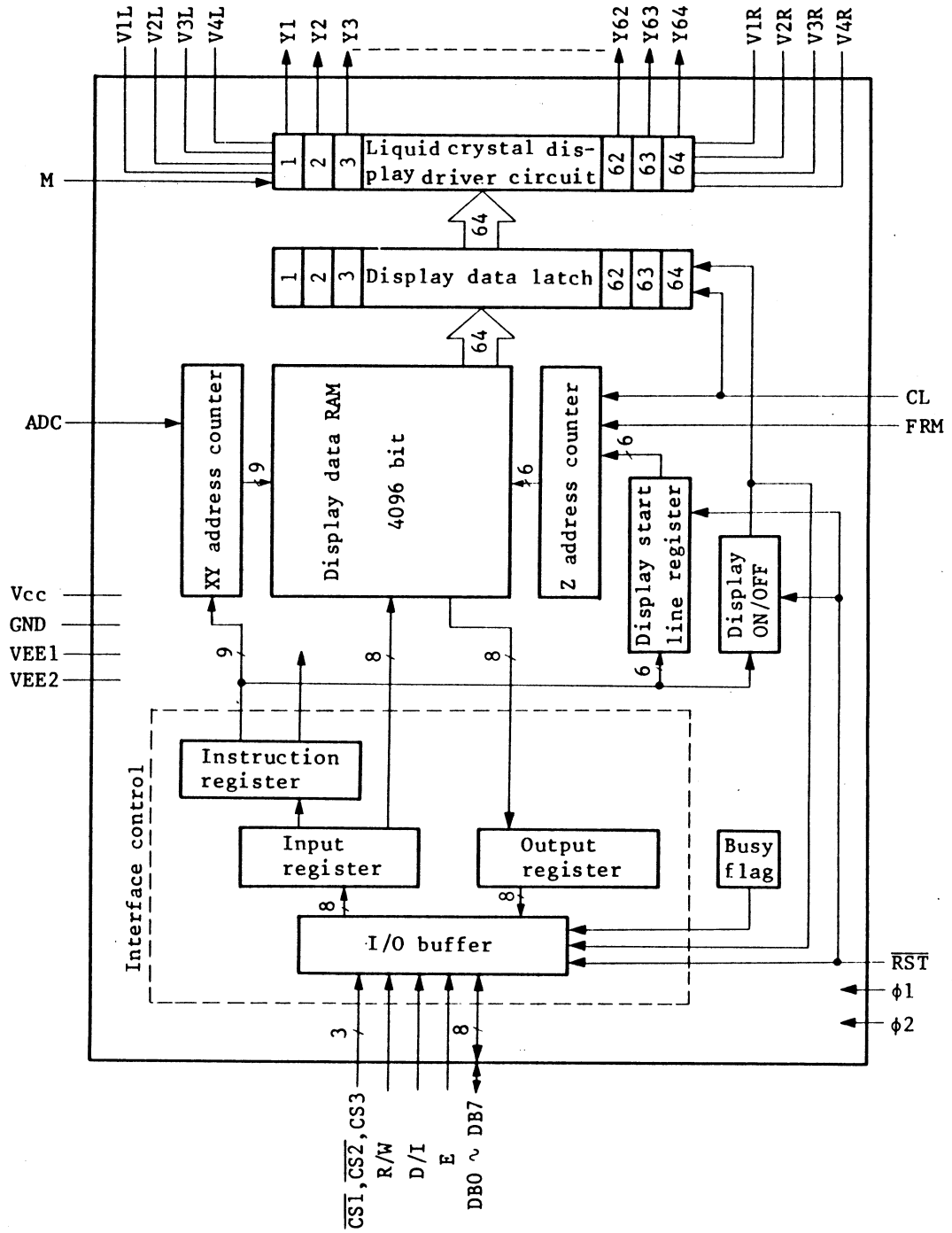
RL=2.4KΩ

R =11KΩ

C =130pF (including jig capacity)

Diodes D1 to D4 are all 1S2074Ⓗ

■ BLOCK DIAGRAM



TERMINAL FUNCTIONS

Terminal name	Number of terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is GND = 0V V_{CC} = 5V ± 10%
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the next conditions. Terminal name: $\overline{CS1}$ = 'L', $\overline{CS2}$ = 'L', $\overline{CS3}$ = 'H' Condition: 'L' 'L' 'H'
E	1	I	MPU	Enable At write(R/W=L) : Data of DB0 to DB7 is latched at the fall of E. At read(R/W=H) : Data appears at DB0 to DB7 while E is in "High" level.
R/W	1	I	MPU	Read/Write R/W=H : Data appears at DB0 to DB7 and can be read by the CPU When E=H, $\overline{CS1}$, $\overline{CS2}$=L and CS3=H. R/W=L : DB0 to DB7 can accept at fall of E when $\overline{CS1}$, $\overline{CS2}$=L and CS3=H.
D/I	1	I	MPU	Data/Instruction D/I=H : Indicates that the data of DB0 to DB7 is display data. D/I=L : Indicates that the data of DB0 to DB7 is display control data.
ADC	1	I	V_{CC}/GND	Address control signal determine the relation between Y address of display RAM and terminals from which the data is output. ADC=H : Y1-$0, Y64-$63 ADC=L : Y64-$0, Y1-$63
DB0∿DB7	8	I/O	MPU	Data bus, three-state I/O common terminal

FUNCTION OF EACH BLOCK

● Interface Control

(1) I/O buffer

Data is transferred through 8 data buses (DB0 ∿ DB7).

DB7 .... MSB (Most Significant Bit)

DB0 .... LSB (Least Significant Bit)

Data can neither be input nor output unless CS1 to CS3 are in the active mode. Therefore, when CS1 to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC, namely, the internal state is maintained and no instruction excute. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively by CS1 to CS3.

(2) Register

Both input register and output register are provided to interface to MPU of which the speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals.

Table 1. Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

① Input register

Input register is used to store data temporarily before writing it into display data RAM.

The data from MPU is written into input register, then into display data RAM automatically by internal operation.

When CS1 to CS3 are in the active mode and D/I and R/W select the input register as shown in Table 1, data is latched at the fall of E signal.

② Output register

Output register is used to store data temporarily which is read from display data RAM. To read out the data from output register, CS1 to CS3 should be in the active mode and both D/I and R/W should be 1. With READ instruction, data stored in the output register is output while E is "H" level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1.
The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

Therefore, the data of the specified address can not be output with READ instruction soon after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Fig. 5 shows the CPU read timing.

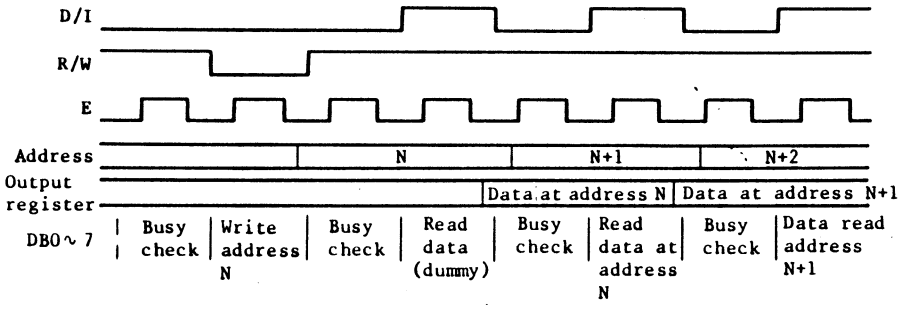
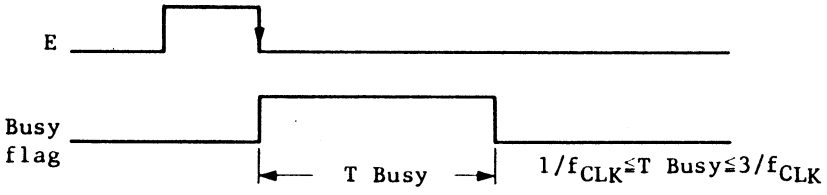


Fig. 5 CPU Read Timing

● Busy Flag

"1" of busy flag indicates that HD61202 is on the move and any instructions except Status Read instruction can not be accepted. The value of the busy flag is read out on DB7 by the Status Read instruction. Make sure that the busy flag is reset ("0") before the issue of instruction.



f_{CLK} is $\phi 1$, $\phi 2$ frequency

- Display ON/OFF Flip Flop

Display ON/OFF flip flop selects one of two states, ON state and OFF state of segments Y1 to Y64. In ON state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in OFF state independent of the data in RAM. It is controlled by display ON/OFF instruction '0' of $\overline{RST}$ signal sets the segments in OFF state. The status of the flip flop is output to DB5 by Status Read instruction. Display ON/OFF instruction does not influence data in RAM. To control display data latch by this flip flop, CL signal (display synchronous signal) should be input correctly.

- Display Start Line Register

The register specifies a line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.

6-bit display start line information is written into this register by display start line set instruction, with 'H' level of FRM signal instructing to start the display, the information in this register is transferred to Z address counter which controls the display address, and the Z address counter is preset.

- X, Y Address Counter

This is a 9-bit counter which designates addresses of internal display data RAM. X address counter of upper 3 bits and Y address counter of lower 6 bits should be set each address by respective instruction.

(1) X address counter

Ordinary register with no count functions. An address is set in by instructions.

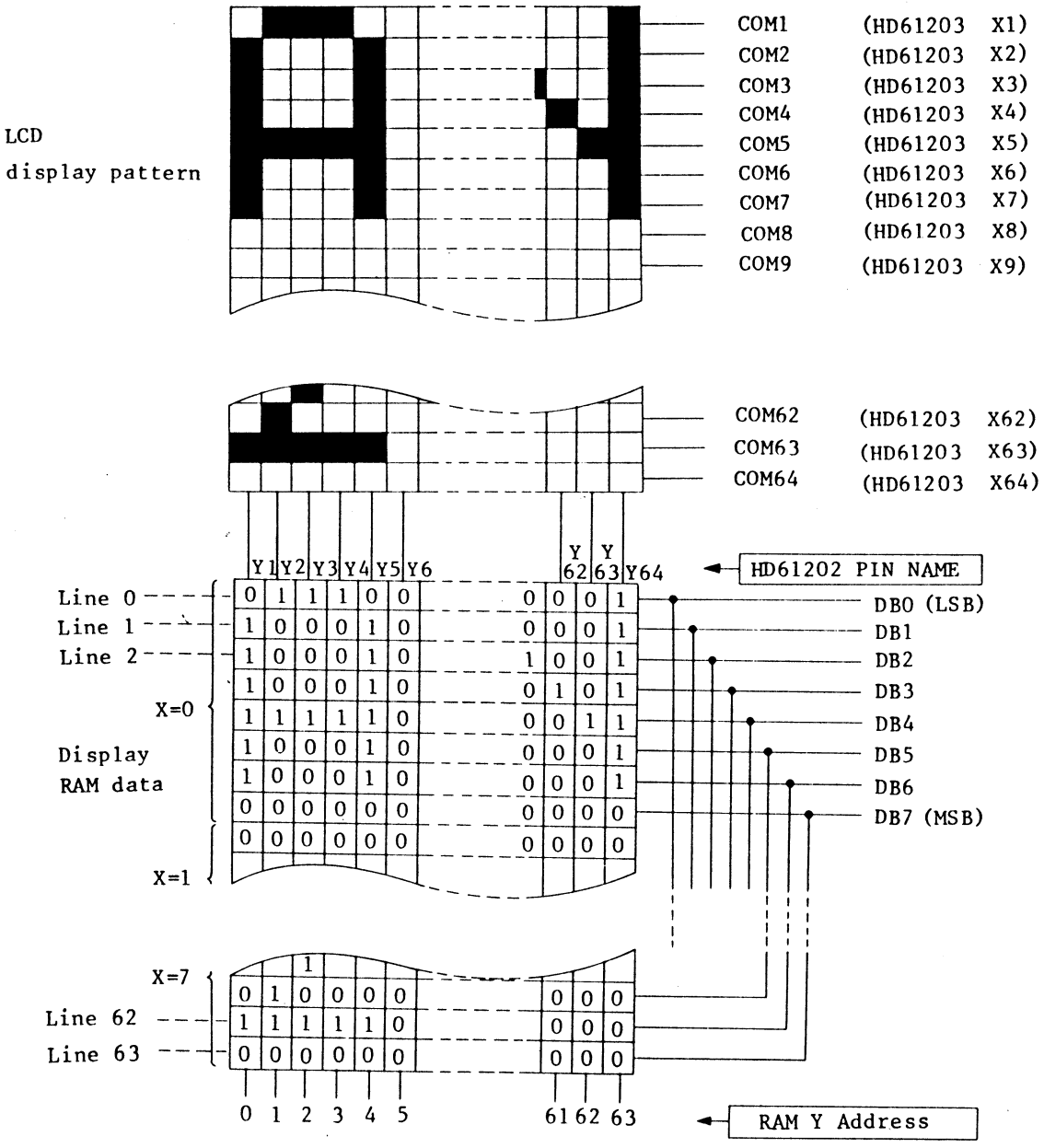
(2) Y address counter

An address is set in by instruction and it is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

- Display Data RAM

Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light ON (data=1) and light OFF (data=0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment PINs can be reversed by ADC signal.
As ADC signal controls Y address counter, a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Fig. 6 shows the relations between Y address of RAM and segment pins in the cases of ADC=1 and ADC=0. (display start line=0, 1/64 duty).



(a) ADC="1" (Connected to Vcc)

Fig. 6 Relation between RAM Data and Display

Table 2. Instructions

Instructions	Code										Functions	
	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1 Display ON/OFF	0	0	0	0	1	1	1	1	1	1/0	Controls the ON/OFF of display. RAM data and internal status are not affected. 1:ON, 0:OFF.	
2 Display start line	0	0	1	1	display start line (0∿63)						Specifies a RAM line displayed at the top of the screen.	
3 Set page (X address)	0	0	1	0	1	1	1	Page (0∿7)			Sets the page (X address) of RAM at the page (X address) register.	
4 Set Address	0	0	0	1	Y address (0∿63)						Sets the Y address at the Y address counter	
5 Status Read	1	0	Busy	0	ON/OFF	RESET	0	0	0	0	Reads the status. RESET 1: reset 0:normal ON/OFF 1: display OFF 0:display ON Busy 1: on the internal operation 0: Ready	
6 Write deisplay data	0	1	Write Data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
7 Read display data	1	1	Read Data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Note 1) Busy time varies with the frequency (f_{CLK}) of $\phi 1$, and $\phi 2$.

$$(1/f_{CLK} \leqq T_{BUSY} \leqq 3/f_{CLK})$$

- Detailed Explanation

(1) Display ON/OFF

	R/W	D/I	DB7							DB0
Code	0	0	0	0	1	1	1	1	1	D

← high-order-bit low-order-bit →

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen width D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

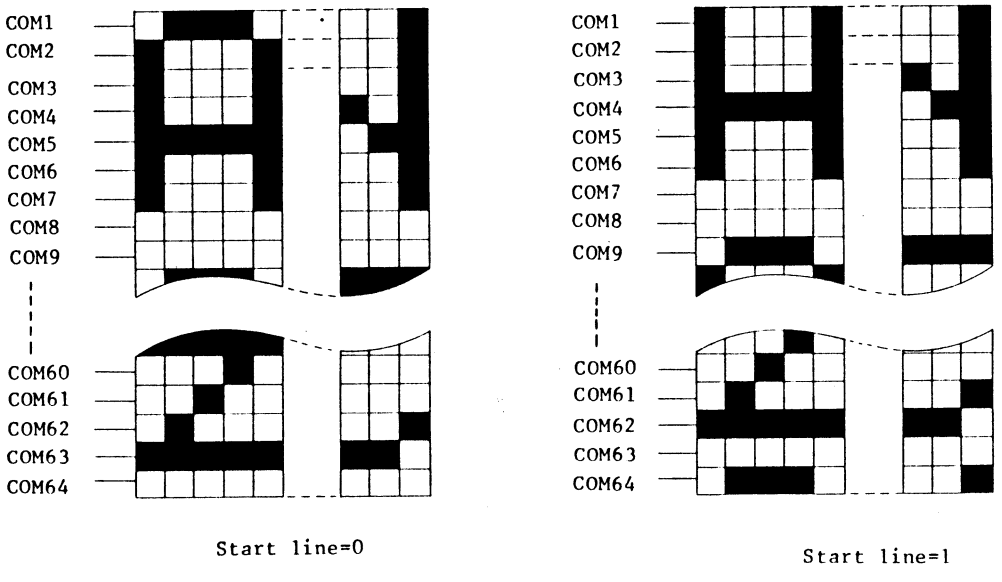
(2) Display start line

	R/W	D/I	DB7							DB0
Code	0	0	1	1	A	A	A	A	A	A

← high-order-bit low-order-bit →

Z address AAAAAA (binary) of the display data RAM is set at the display start line register and displayed at the top of the screen. Fig. 7 are the examples of display (1/64 duty) when the start line=0 ∿ 3. When the display duty is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

Fig. 7 Relation Between Start Line and Display



(3) Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order-bit low-order-bit →

X address AAA (binary) of the display data RAM is set at the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set.

(4) Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order-bit low-order-bit →

Y address AAAAAA (binary) of the display data RAM is set at the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

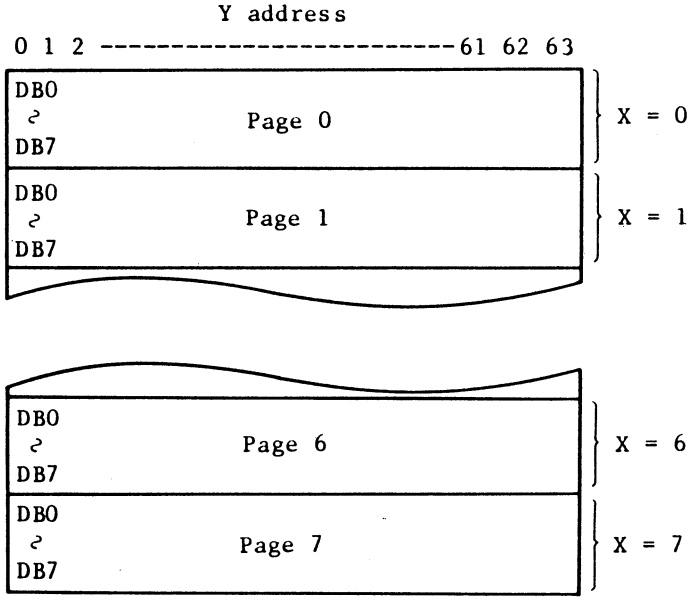


Fig. 8 Address Configuration of Display Data RAM

(5) Status Read

	R/W	D/I	DB7							DB0
Code	1	0	BUSY	0	ON/ OFF	RESET	0	0	0	0

◄— high-order-bit — low-order-bit - ►

BUSY: When BUSY is 1, the LSI is in internal operation. No instructions are accepted while BUSY is 1, so you should make sure that BUSY is 0 before writing the next instruction.

ON/OFF: This bit shows the liquid crystal display conditions - ON condition or OFF condition.
When ON/OFF is 1, the display is in OFF condition.
When ON/OFF is 0, the display is in ON condition.

RESET: RESET=1 shows that the system is being initialized. In this condition, any instructions except Status Read instruction cannot be accepted.
RESET=0 shows that initializing has finished and the system is in the usual operation.

(6) Write Display Data

	R/W	D/I	DB7							DB0
Code	0	1	D	D	D	D	D	D	D	D

◄- high-order-bit — low-order-bit ►

Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

(7) Read Display Data

	R/W	D/I	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D

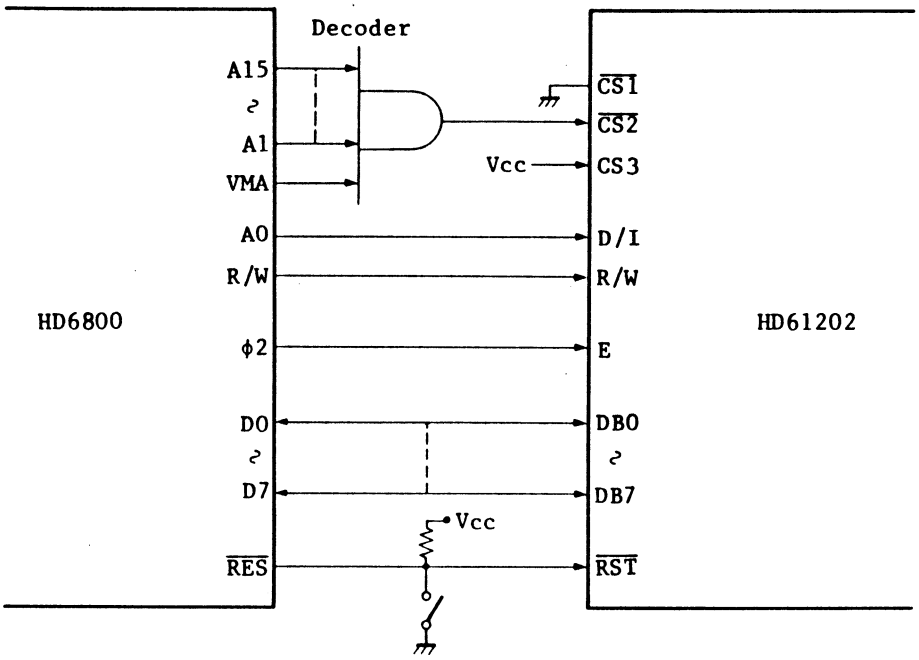
◄- high-order-bit — low-order-bit —►

Read out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary soon after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

Interface with CPU

a) Example of connection with HD6800



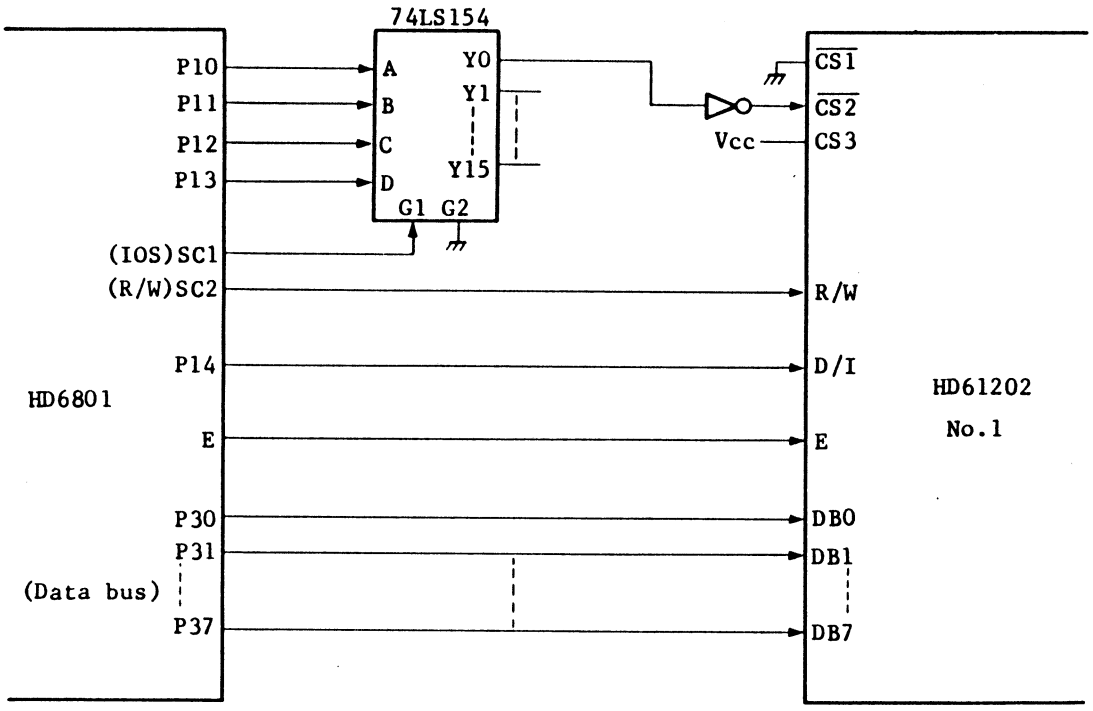
The example of connection with HD6800 series

In this decoder, addresses of HD61202 in the address area of HD6800 are:

Read/Write of the display data	$FFFF
Write of display instruction	$FFFE
Read out of status	$FFFE

Therefore, you can control HD61202 by reading/writing the data at these addresses.

b) Example of connection with HD6801



- Set HD6801 in Mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus.
- 74LS154 is 4 to 16 decoder and generate chip select signal to make specified HD61202 active after decoding 4 bits of P10 to P13.
- Therefore, after making the operation possible by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61202. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to the each manual.