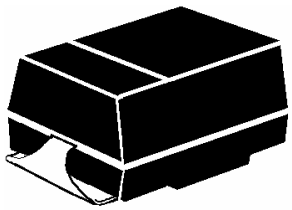
Microsemi
SCOTTSDALE DIVISION

LOW CAPACITANCE TRANSIENT ABSORPTION ZENER™

DESCRIPTION

The SAC series is a low capacitance transient voltage suppressor (TVS) in a modified DO-214AA package rated at 500 Watts, providing board-level protection for data or signal lines. The low capacitance of 50 pF minimizes the amount of signal loss or deformation up through 70 MHz. If bi-directional protection is needed, two devices in anti-parallel configuration are required as shown in Figure 4. The 500 watt rating described in Figures 1 and 3 provides lightning protection per IEC61000-4-5 (Levels 1 and 2) as well as ESD and EFT protection per IEC61000-4-2 and IEC61000-4-4 respectively. This economical molded surface mount package also has very low thermal resistance due to its unique axial subassembly.

APPEARANCE



DO-214AA
See package notes

IMPORTANT: For the most current data, consult *MICROSEMI's* website: http://www.microsemi.com

FEATURES

- 500 Watts Peak Pulse Power
- Low Capacitance
- Small Size
- Economical Series
- UL94V-0 Flammability Classification
- Robust axial subassembly in DO-214AA style package

APPLICATIONS / BENEFITS

- Low Capacitance for data-line protection to 70 MHz
- Low Level Lightning Protection per IEC61000-4-5 and as described for surge ratings herein
- ESD and EFT protection per IEC61000-4-2 and IEC61000-4-4 respectively

MAXIMUM RATINGS

- Peak Pulse Power Dissipation at 25°C: 500 Watts @ 10/1000 μs.
- Steady State Power Dissipation at T_L = +75°C: 2.5 Watts.
- Clamping Speed (0 volts to $V_{(BR)}$ Min.) less than 5 nanoseconds.
- Operating and Storage Temperature: -65°C to +150°C.

MECHANICAL AND PACKAGING

- **CASE:** Void Free Transfer Molded Thermosetting Plastic (see DO-214AA dimensions and notes)
- **FINISH:** All External Surfaces Are Corrosion Resistant and Leads Solderable
- **POLARITY:** Cathode (TVS) Marked with Band.
- **MARKING:** Part number without HSMBJ prefix (ie. SAC5.0)
- **WEIGHT:** 0.1 Grams (Approx.)

ELECTRICAL CHARACTERISTICS @ 25°C

MICROSEMI PART NUMBER (prefix all with HSMBJ…)	REVERSE STAND-OFF VOLTAGE (Note 1) V_{WM} Volts	BREAKDOWN VOLTAGE @ $I_{(BR)}$ 1.0mA $V_{(BR)}$ Volts Min.	MAXIMUM STANDBY CURRENT @V_{WM} I_D μA	MAXIMUM CLAMPING VOLTAGE I_P = 5.0A* V_C Volts	MAXIMUM PEAK PULSE CURRENT* RATING I_{PP} Amps	CAPACITANCE @ O Volts pF	WORKING INVERSE BLOCKING VOLTAGE V_{WIB} Volts	INVERSE BLOCKING LEAKAGE CURRENT @ V_{WIB} I_{IB} mA	PEAK INVERSE BLOCKING VOLTAGE V_{PIB} Volts
SAC5.0	5.0	7.60	300	10.0	44	50	75	1	100
SAC6.0	6.0	7.90	300	11.2	41	50	75	1	100
SAC7.0	7.0	8.33	300	12.6	38	50	75	1	100
SAC8.0	8.0	8.89	100	13.4	36	50	75	1	100
SAC8.5	8.5	9.44	50	14.0	34	50	75	1	100
SAC10	10	11.10	5.0	16.3	29	50	75	1	100
SAC12	12	13.30	5.0	19.0	25	50	75	1	100
SAC15	15	16.70	5.0	23.6	20	50	75	1	100
SAC18	18	20.00	5.0	28.8	15	50	75	1	100
SAC22	22	24.40	5.0	35.4	14	50	75	1	100
SAC26	26	28.90	5.0	42.3	11.1	50	75	1	100
SAC36	36	40.0	5.0	60.0	8.6	50	75	1	100
SAC45	45	50.00	5.0	77.0	6.8	50	150	1	200
SAC50	50	55.50	5.0	88.0	5.8	50	150	1	200

*See Figure 3

Clamping Factor: Typically 1.4 @ full rated power, 1.20 @ 50% rated power. The ratio of the numerical value of V_C to $V_{(BR)}$.

Microsemi
Scottsdale Division
8700 E. Thomas Rd. PO Box 1390, Scottsdale, AZ 85252 USA, (480) 941-6300, Fax: (480) 947-1503

Microsemi
SCOTTSDALE DIVISION

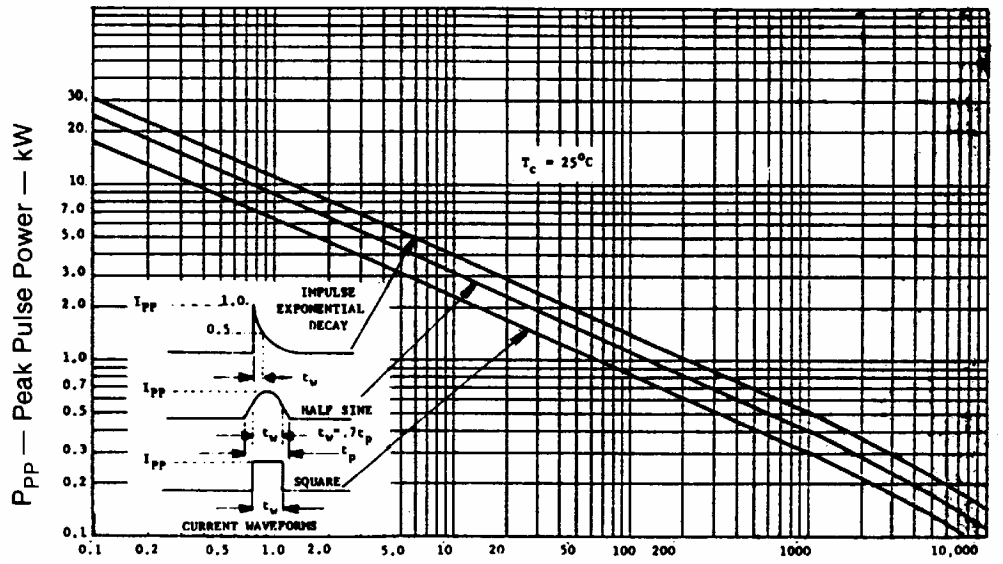
LOW CAPACITANCE TRANSIENT ABSORPTION ZENER™

Note 1: A transient voltage suppressor is normally selected according to voltage (V_{WM}), which should be equal to or greater than the dc or continuous peak operating voltage level.

Note 2: When pulse testing, test in TVS avalanche direction. Do not pulse in "forward" direction.

Note 3: For unidirectional applications, it is recommended that an additional low capacitance diode or rectifier be used in parallel with the TVS. This added parallel diode will be facing the same polarity direction as the TVS and opposite that of the internal low capacitance diode in Figure 4. This will prevent a reverse transient from damaging the internal low capacitance diode. The added diode or rectifier should also have a higher reverse voltage rating than the TVS clamping voltage V_C. Diode or rectifier ratings in excess of 100 volts with low capacitance will provide this added protective function. If using two SAC devices in anti-parallel for bi-directional applications, this protective feature is satisfied. The bi-directional TVS configuration in Figure 4 will result in twice the capacitance of a single SAC device.

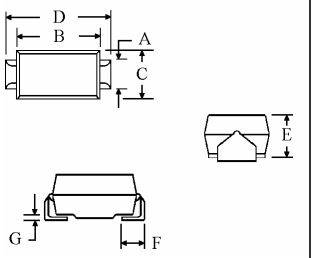
OUTLINE AND CIRCUIT



t_w – Pulse Width µs

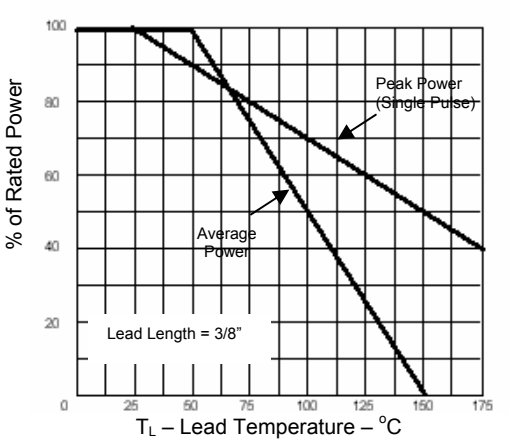
FIGURE 1

PACKAGE DIMENSIONS



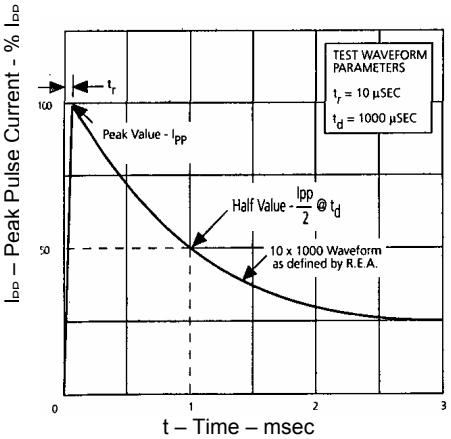
DIM	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.073	.087	1.85	2.21
B	.160	.180	4.06	4.57
C	.130	.155	3.30	3.94
D	.205	.220	5.21	5.59
E	.075	.130	1.91	3.30
F	.030	.060	.76	1.52
G	.006	.016	.15	.41

NOTE: Dimension E exceeds the JEDEC outline in height as shown



T_L – Lead Temperature – °C

FIGURE 2



t – Time – msec

FIGURE 3

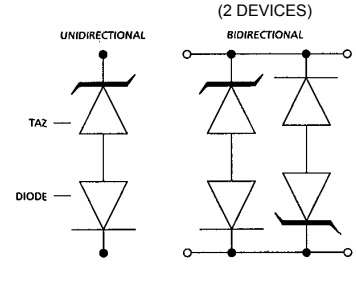


FIGURE 4

Microsemi
Scottsdale Division
8700 E. Thomas Rd. PO Box 1390, Scottsdale, AZ 85252 USA, (480) 941-6300, Fax: (480) 947-1503