FAIRCHILD SEMICONDUCTOR®

# HGTG5N120CND, HGTP5N120CND, HGT1S5N120CNDS

**Data Sheet** **December 2001**

## 25A, 1200V, NPT Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

The HGTG5N120CND, HGTP5N120CND and HGT1S5N120CNDS are **N**on-**P**unch **T**hrough (NPT) IGBT designs. They are new members of the MOS gated high voltage switching IGBT family. IGBTs combine the best features of MOSFETs and bipolar transistors. This device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The IGBT used is developmental type TA49309. The diode used in anti-parallel is developmental typeTA49058.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

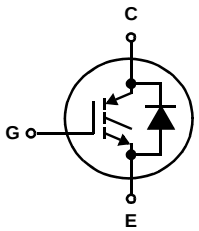
Formerly Developmental Type TA49307.

## Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| HGTG5N120CND | TO-247 | 5N120CND |
| HGTP5N120CND | TO-220AB | 5N120CND |
| HGT1S5N120CNDS | TO-263AB | 5N120CND |

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in Tape and Reel, i.e., HGT1S5N120CNDS9A.

## Symbol

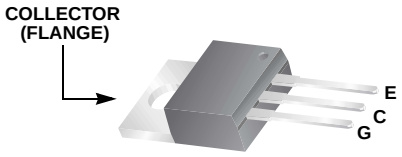



## Features

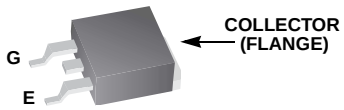
- 25A, 1200V, $T_C = 25^oC$
- 1200V Switching SOA Capability
- Typical Fall Time. . . . . 350ns at $T_J = 150^oC$
- Short Circuit Rating
- Low Conduction Loss
- *Temperature Compensating* SABER™ Model
  *Thermal Impedance* SPICE Model
  www.fairchildsemi.com
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

## Packaging

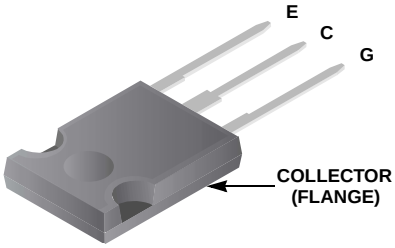
**JEDEC TO-220AB ALTERNATE VERSION**




**JEDEC TO-263AB**




**JEDEC STYLE TO-247**




**FAIRCHILD SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 4,364,073 | 4,417,385 | 4,430,792 | 4,443,931 | 4,466,176 | 4,516,143 | 4,532,534 | 4,587,713 |
| 4,598,461 | 4,605,948 | 4,620,211 | 4,631,564 | 4,639,754 | 4,639,762 | 4,641,162 | 4,644,637 |
| 4,682,195 | 4,684,413 | 4,694,313 | 4,717,679 | 4,743,952 | 4,783,690 | 4,794,432 | 4,801,986 |
| 4,803,533 | 4,809,045 | 4,809,047 | 4,810,665 | 4,823,176 | 4,837,606 | 4,860,080 | 4,883,767 |
| 4,888,627 | 4,890,143 | 4,901,127 | 4,904,609 | 4,933,740 | 4,963,951 | 4,969,027 | |

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## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | HGTG5N120CND HGTP5N120CND HGT1S5N120CNDS | UNITS |
|---|---|---|---|
| Collector to Emitter Voltage | $BV_{CES}$ | 1200 | V |
| Collector Current Continuous | | | |
| At $T_C = 25^oC$ | $I_{C25}$ | 25 | A |
| At $T_C = 110^oC$ | $I_{C110}$ | 12 | A |
| Collector Current Pulsed (Note 1) | $I_{CM}$ | 40 | A |
| Gate to Emitter Voltage Continuous | $V_{GES}$ | ±20 | V |
| Gate to Emitter Voltage Pulsed | $V_{GEM}$ | ±30 | V |
| Switching Safe Operating Area at $T_J = 150^oC$, Figure 2 | SSOA | 30A at 1200V | |
| Power Dissipation Total at $T_C = 25^oC$ | $P_D$ | 167 | W |
| Power Dissipation Derating $T_C > 25^oC$ | | 1.33 | $W/^oC$ |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{STG}$ | -55 to 150 | $^oC$ |
| Maximum Lead Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from case for 10s | $T_L$ | 300 | $^oC$ |
| Package Body for 10s, see Tech Brief 334 | $T_{pkg}$ | 260 | $^oC$ |
| Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$ | $t_{SC}$ | 8 | µs |
| Short Circuit Withstand Time (Note 2) at $V_{GE} = 12V$ | $t_{SC}$ | 15 | µs |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 840V$, $T_J = 125^oC$, $R_G = 25\Omega$.

## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Collector to Emitter Breakdown Voltage | $BV_{CES}$ | $I_C = 250\mu A$, $V_{GE} = 0V$ | | 1200 | - | - | V |
| Collector to Emitter Leakage Current | $I_{CES}$ | $V_{CE} = 1200V$ | $T_C = 25^oC$ | - | - | 250 | µA |
| | | | $T_C = 125^oC$ | - | 100 | - | µA |
| | | | $T_C = 150^oC$ | - | - | 2 | mA |
| Collector to Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C = 5.5A$, $V_{GE} = 15V$ | $T_C = 25^oC$ | - | 2.1 | 2.4 | V |
| | | | $T_C = 150^oC$ | - | 2.9 | 3.5 | V |
| Gate to Emitter Threshold Voltage | $V_{GE(TH)}$ | $I_C = 45\mu A$, $V_{CE} = V_{GE}$ | | 6.0 | 7.0 | - | V |
| Gate to Emitter Leakage Current | $I_{GES}$ | $V_{GE} = \pm 20V$ | | - | - | ±250 | nA |
| Switching SOA | SSOA | $T_J = 150^oC$, $R_G = 25\Omega$, $V_{GE} = 15V$, $L = 200\mu H$, $V_{CE(PK)} = 1200V$ | | 25 | - | - | A |
| Gate to Emitter Plateau Voltage | $V_{GEP}$ | $I_C = 5.5A$, $V_{CE} = 600V$ | | - | 10.6 | - | V |
| On-State Gate Charge | $Q_{G(ON)}$ | $I_C = 5.5A$, $V_{CE} = 600V$ | $V_{GE} = 15V$ | - | 45 | 55 | nC |
| | | | $V_{GE} = 20V$ | - | 60 | 75 | nC |
| Current Turn-On Delay Time | $t_{d(ON)I}$ | IGBT and Diode at $T_J = 25^oC$ $I_{CE} = 5.5A$ $V_{CE} = 960V$ $V_{GE} = 15V$ $R_G = 25\Omega$ $L = 5mH$ Test Circuit (Figure 20) | | - | 22 | 30 | ns |
| Current Rise Time | $t_{rI}$ | | | - | 12 | 16 | ns |
| Current Turn-Off Delay Time | $t_{d(OFF)I}$ | | | - | 180 | 250 | ns |
| Current Fall Time | $t_{fI}$ | | | - | 280 | 350 | ns |
| Turn-On Energy | $E_{ON}$ | | | - | 400 | 500 | µJ |
| Turn-Off Energy (Note 3) | $E_{OFF}$ | | | - | 640 | 700 | µJ |

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**Electrical Specifications** $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Current Turn-On Delay Time | $t_{d(ON)I}$ | IGBT and Diode at $T_J = 150^oC$<br>$I_{CE} = 5.5A$<br>$V_{CE} = 960V$<br>$V_{GE} = 15V$<br>$R_G = 25\Omega$<br>L = 5mH<br>Test Circuit (Figure 20) | - | 20 | 25 | ns |
| Current Rise Time | $t_{rI}$ | | - | 12 | 16 | ns |
| Current Turn-Off Delay Time | $t_{d(OFF)I}$ | | - | 225 | 300 | ns |
| Current Fall Time | $t_{fI}$ | | - | 350 | 400 | ns |
| Turn-On Energy | $E_{ON}$ | | - | 1 | 1.2 | mJ |
| Turn-Off Energy (Note 3) | $E_{OFF}$ | | - | 1 | 1.1 | mJ |
| Diode Forward Voltage | $V_{EC}$ | $I_{EC} = 5.5A$ | - | 2.4 | 3.3 | V |
| Diode Reverse Recovery Time | $t_{rr}$ | $I_{EC} = 5.5A$, $dI_{EC}/dt = 200A/\mu s$ | - | 48 | 60 | ns |
| | | $I_{EC} = 1A$, $dI_{EC}/dt = 200A/\mu s$ | - | 30 | 40 | ns |
| Thermal Resistance Junction To Case | $R_{\theta JC}$ | IGBT | - | - | 0.75 | $^oC/W$ |
| | | Diode | - | - | 1.9 | $^oC/W$ |

NOTE:

3. Turn-Off Energy Loss ($E_{OFF}$) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

## *Typical Performance Curves* Unless Otherwise Specified

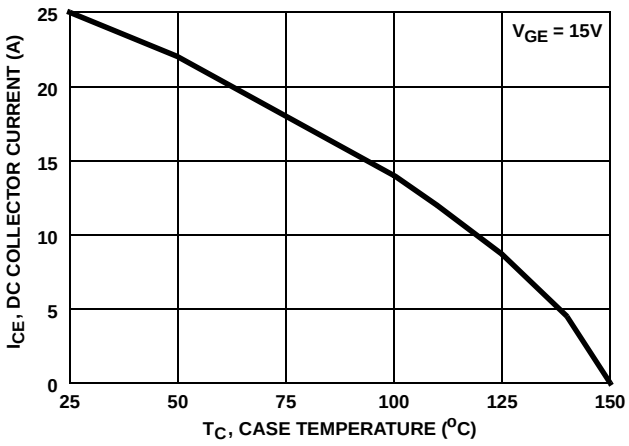


**FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE**

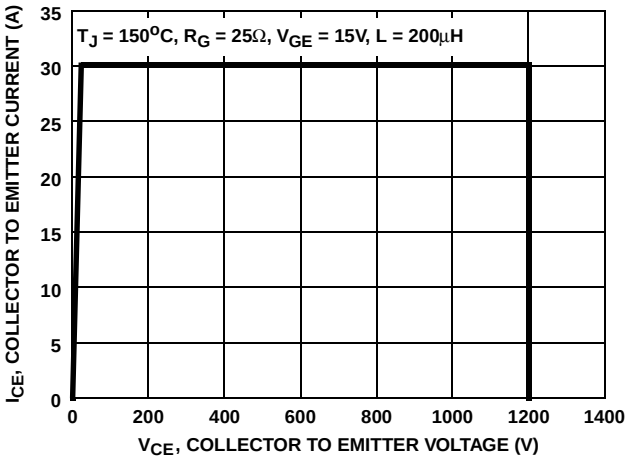


**FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA**

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## Typical Performance Curves Unless Otherwise Specified (Continued)

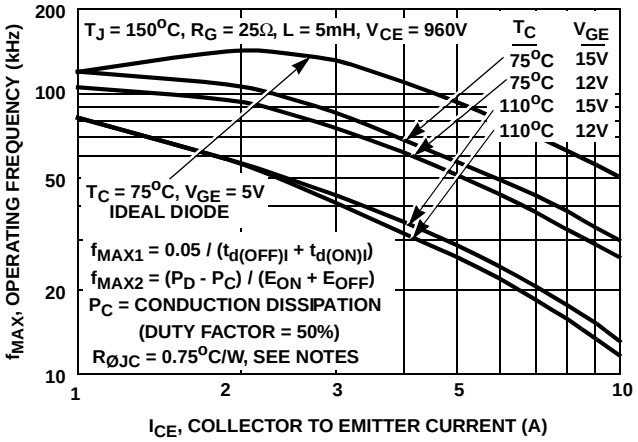


FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

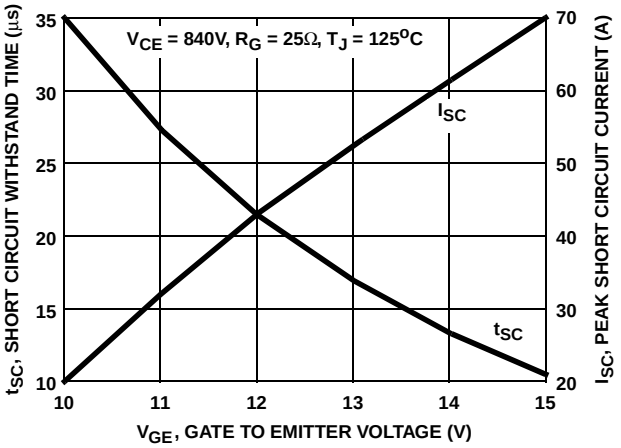


FIGURE 4. SHORT CIRCUIT WITHSTAND TIME

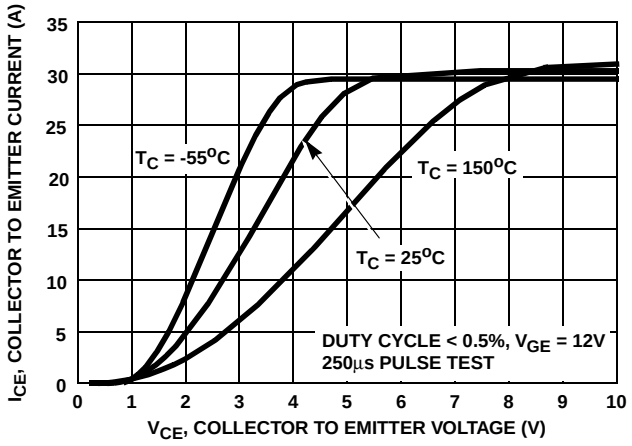


FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

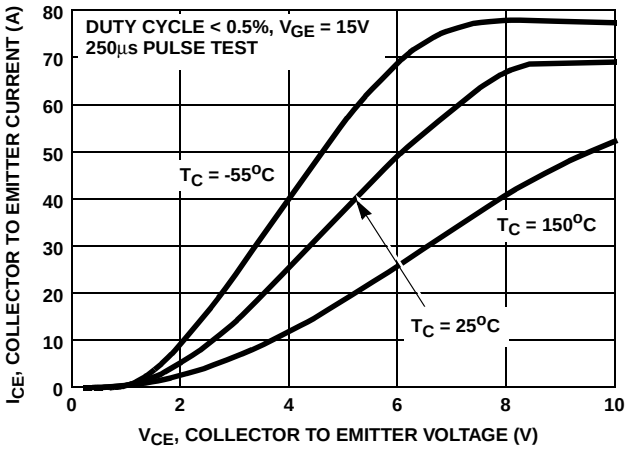


FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

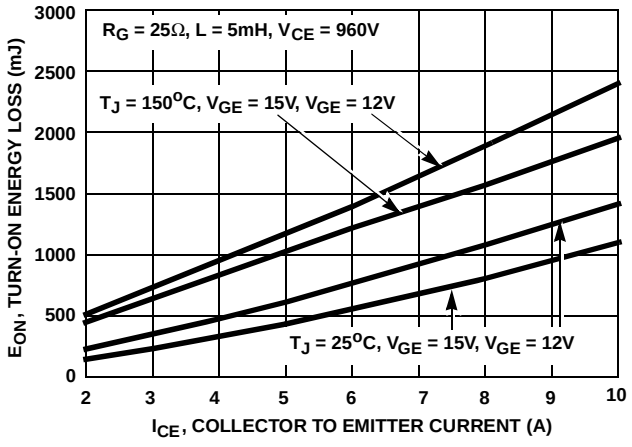


FIGURE 7. TURN-ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

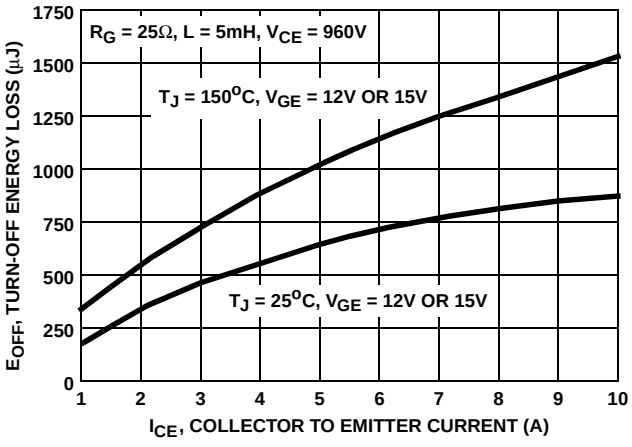


FIGURE 8. TURN-OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

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## Typical Performance Curves Unless Otherwise Specified (Continued)

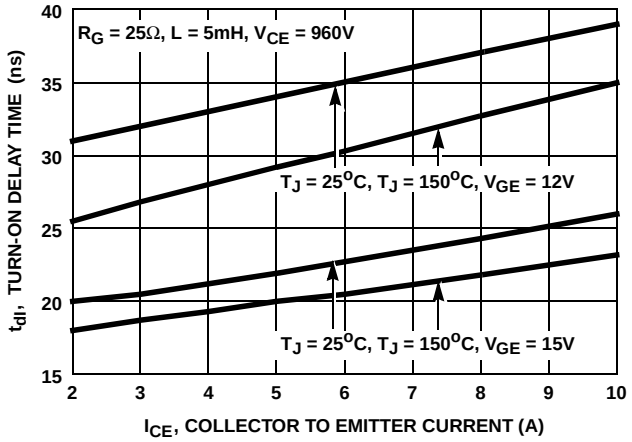


FIGURE 9. TURN-ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

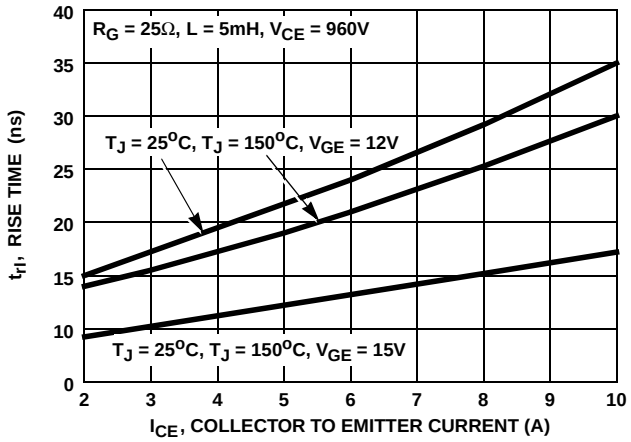


FIGURE 10. TURN-ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

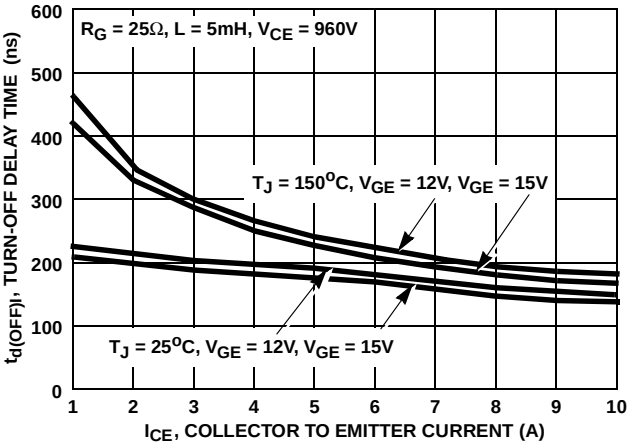


FIGURE 11. TURN-OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

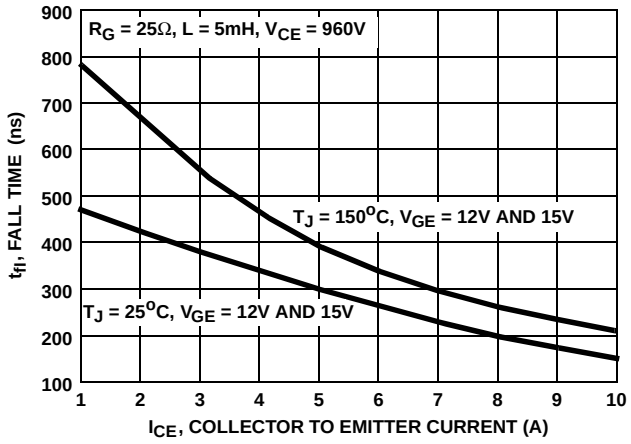


FIGURE 12. FALL TIME vs COLLECTOR TO EMITTER CURRENT

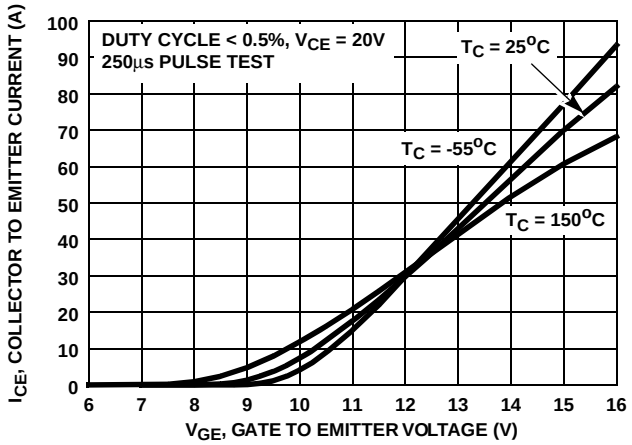


FIGURE 13. TRANSFER CHARACTERISTIC

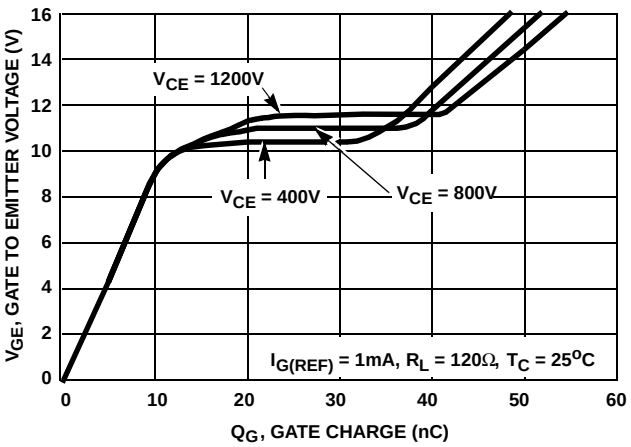


FIGURE 14. GATE CHARGE WAVEFORMS

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## Typical Performance Curves Unless Otherwise Specified (Continued)

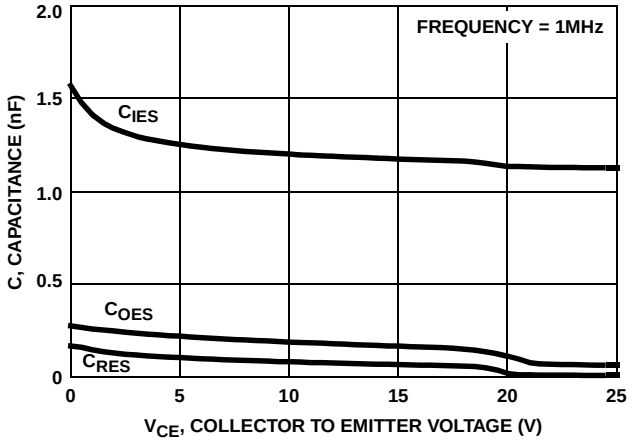


FIGURE 15. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

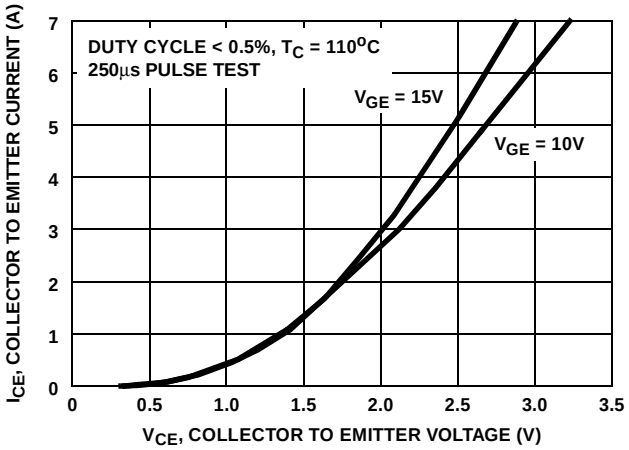


FIGURE 16. COLLECTOR TO EMITTER ON-STATE VOLTAGE

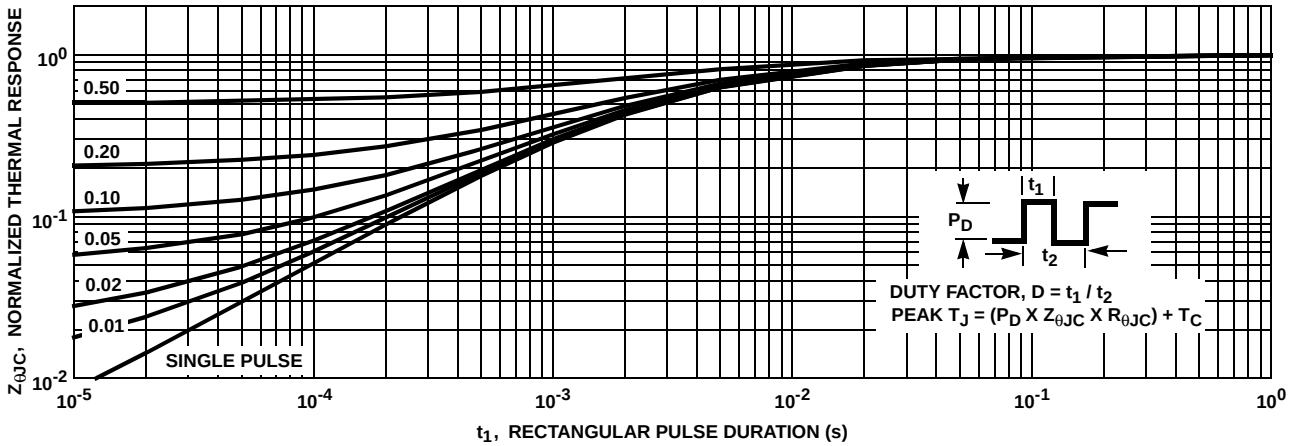


FIGURE 17. NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

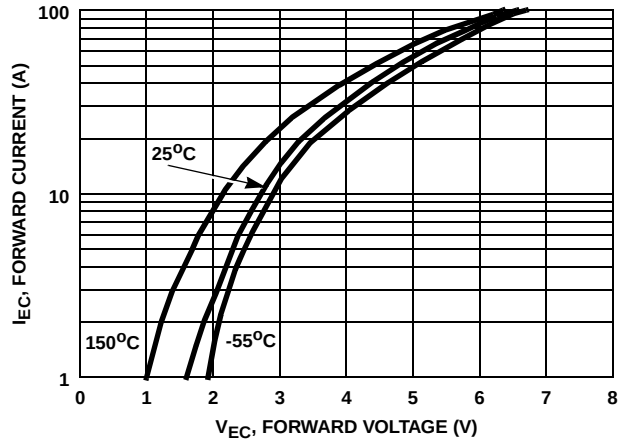


FIGURE 18. DIODE FORWARD CURRENT vs FORWARD VOLTAGE DROP

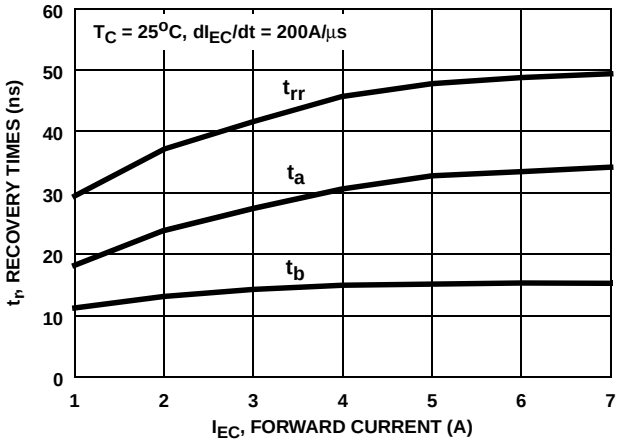


FIGURE 19. RECOVERY TIMES vs FORWARD CURRENT

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## Test Circuit and Waveforms

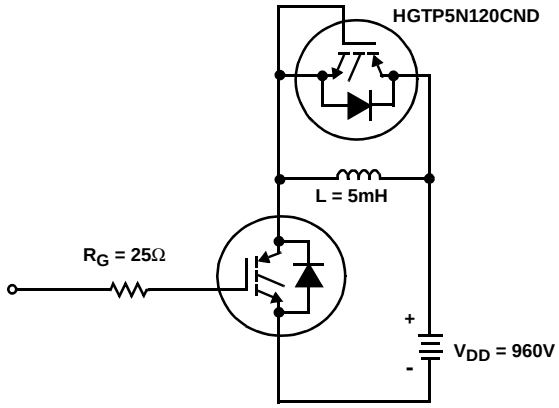


FIGURE 20. INDUCTIVE SWITCHING TEST CIRCUIT

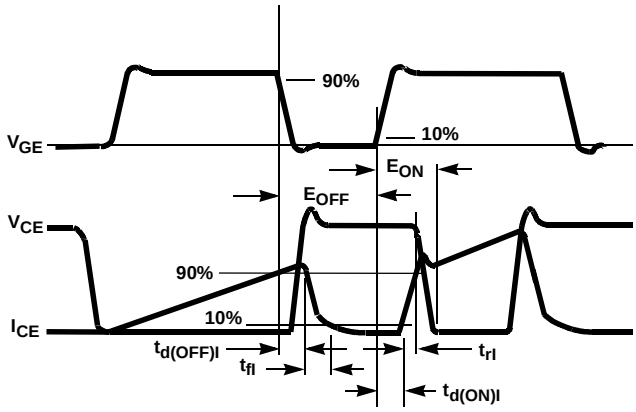


FIGURE 21. SWITCHING TEST WAVEFORMS

## Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of $V_{GEM}$. Exceeding the rated $V_{GE}$ can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

## Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current ($I_{CE}$) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows $f_{MAX1}$ or $f_{MAX2}$; whichever is smaller at each point. The information is based on measurements of a typica ldevice and is bounded by the maximum rated junction temperature.

$f_{MAX1}$ is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 21. Device turn-off delay can establish an additional frequency limiting condition for an application other than $T_{JM}$. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

$f_{MAX2}$ is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation ($P_D$) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed $P_D$. A 50% duty factor was used (Figure 3) and the conduction losses ($P_C$) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

$E_{ON}$ and $E_{OFF}$ are defined in the switching waveforms shown in Figure 21. $E_{ON}$ is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and $E_{OFF}$ is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for $E_{OFF}$; i.e., the collector current equals zero ($I_{CE} = 0$).

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| Bottomless™ | FASTr™ | OPTOPLANAR™ | STAR*POWER™ | |
| CoolFET™ | FRFET™ | PACMAN™ | Stealth™ | |
| *CROSSVOLT*™ | GlobalOptoisolator™ | POP™ | SuperSOT™-3 | |
| DenseTrench™ | GTO™ | Power247™ | SuperSOT™-6 | |
| DOME™ | HiSeC™ | PowerTrench® | SuperSOT™-8 | |
| EcoSPARK™ | ISOPLANAR™ | QFET™ | SyncFET™ | |
| $E^2$CMOS™ | LittleFET™ | QS™ | TinyLogic™ | |
| EnSigna™ | MicroFET™ | QT Optoelectronics™ | TruTranslation™ | |
| FACT™ | MicroPak™ | Quiet Series™ | UHC™ | |
| FACT Quiet Series™ | MICROWIRE™ | SILENT SWITCHER® | UltraFET® | |

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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**Definition of Terms**

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