HARRIS
Semiconductor

HA4244

OBSOLETE PRODUCT
No Recommended Replacement

September 1998   *File Number   4078.2*

# 480MHz, 1 x 1 Video Crosspoint Switch with Synchronous Enable

The HA4244 is a very wide bandwidth 1 x 1 crosspoint switch ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation, excellent differential gain and phase, high off isolation, symmetric slew rates, fast switching, and a latched enable signal. When disabled, the output is switched to a high impedance state, making the HA4244 ideal for routing matrix equipment.

The latched enable input allows for synchronized channel switching. When CLK is low the master control latch loads the next EN, while the closed slave control latch maintains the crosspoint in its current state. CLK switching high closes the master latch, loads the now open slave latch, and enables or disables the HA4244 according to the current state of the EN input.
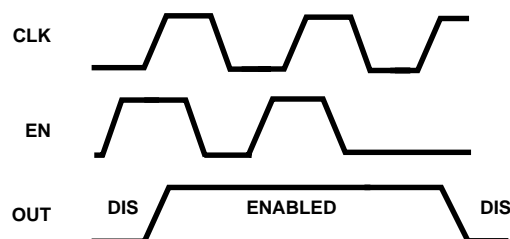
This crosspoint's design ensures that it powers up in the disabled state to eliminate bus contention concerns, and to minimize supply current draw at power up.

For applications requiring an asynchronous crosspoint switch, please refer to the HA4201 and HA4600 data sheets.

Functional Diagram
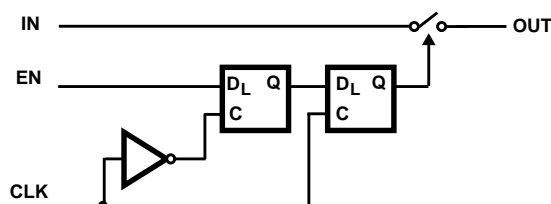
Timing Diagram

Features

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1700V/μs
- 0.1dB Gain Flatness. 250MHz
- -3dB Bandwidth 480MHz
- Off Isolation (100MHz) 85dB
- Differential Gain and Phase . . . . 0.01%/0.01 Degrees
- High ESD Rating . . . . >1800V
- TTL Compatible Control Signals
- Latched Enable Input for Synchronous Switching
- Powers-Up in Disabled State; Avoids Bus Contention
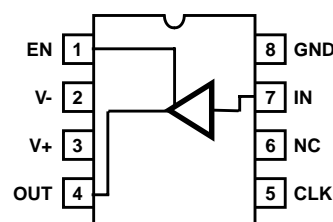
Applications

- Professional Video Switching and Routing
- Video Multiplexers
- Computer Graphics
- RF Switching and Routing
- PCM Data Routing

Part Number Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA4244CB (H4244C)	0 to 70	8 Ld SOIC	M8.15

Pinout

HA4244 (SOIC)
TOP VIEW

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage . . . . V_{SUPPLY}
Digital Input Current (Note 2). . . . . ±25mA
Output Current 20mA

Operating Conditions

Temperature Range . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
    SOIC Package   158
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
    (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

2. If an input signal is applied before the supplies are powered up, the input current must be limited to this maximum value.

Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, V_{EN} = 2.0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA4244			UNITS
			MIN	TYP	MAX	
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	V_{EN} = 2.0V	25, 70	-	10.5	13	mA
	V_{EN} = 2.0V	0	-	-	14.5	mA
	V_{EN} = 0.8V	25, 70	-	-	275	µA
	V_{EN} = 0.8V	0	-	-	325	µA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing without Clipping	V_{OUT} = V_{IN} ± V_{IO} ± 20mV	25, 70	±2.7	±2.8	-	V
		0	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	µA
Output Offset Voltage		25	-10	-	10	mV
Output Offset Voltage Drift (Note 3)		Full	-	25	50	µV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		25	-	160	-	ns
Turn-Off Time		25	-	320	-	ns
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
EN Input Current	V_{EN} = 0 to 4V	Full	-2	-	2	µA
CLK Input Current	V_{CLK} = 0 to 4V	Full	-10	-	10	µA
EN Setup Time to CLK Rising Edge		Full	-	25	-	ns
EN Hold Time after CLKRising Edge		Full	-	10	-	ns

Electrical Specifications $V_{SUPPLY} = \pm 5V$, $R_L = 10k\Omega$, $V_{EN} = 2.0V$, Unless Otherwise Specified **(Continued)**

| PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA4244 MIN	HA4244 TYP	HA4244 MAX	UNITS
AC CHARACTERISTICS						
Insertion Loss	$1V_{P-P}$	Full	-	0.04	0.05	dB
-3dB Bandwidth	$R_S = 82\Omega$, $C_L = 10pF$	25	-	480	-	MHz
	$R_S = 43\Omega$, $C_L = 15pF$	25	-	380	-	MHz
	$R_S = 36\Omega$, $C_L = 21pF$	25	-	370	-	MHz
$\pm 0.1dB$ Flat Bandwidth	$R_S = 82\Omega$, $C_L = 10pF$	25	-	250	-	MHz
	$R_S = 43\Omega$, $C_L = 15pF$	25	-	175	-	MHz
	$R_S = 36\Omega$, $C_L = 21pF$	25	-	170	-	MHz
Input Resistance		Full	200	400	-	$k\Omega$
Input Capacitance		Full	-	1.0	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance	$V_{EN} = 0.8V$	Full	-	2.0	-	pF
Differential Gain	4.43MHz, Note 3	25	-	0.01	0.02	%
Differential Phase	4.43MHz, Note 3	25	-	0.01	0.02	Degrees
Off Isolation	$1V_{P-P}$, 100MHz, $V_{EN} = 0.8V$, $R_L = 10\Omega$	Full	-	85	-	dB
Slew Rate (1.5V_{P-P}, +SR/-SR)	$R_S = 82\Omega$, $C_L = 10pF$	25	-	1750/1770	-	V/μs
	$R_S = 43\Omega$, $C_L = 15pF$	25	-	1460/1360	-	V/μs
	$R_S = 36\Omega$, $C_L = 21pF$	25	-	1410/1360	-	V/μs
Total Harmonic Distortion	Note 3	Full	-	0.01	0.1	%
Disabled Output Resistance		Full	-	12	-	$M\Omega$

NOTE:

3. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.

AC Test Circuit
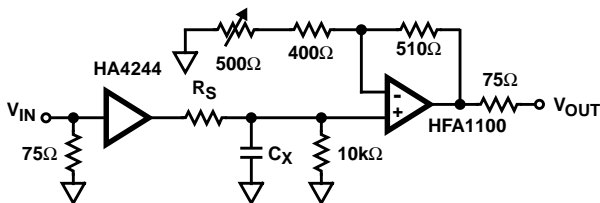
NOTE: $C_L = C_X$ + Test Fixture Capacitance.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

Application Information

General

The HA4244 is a synchronous 1 x 1 crosspoint switch that is ideal for the matrix element in small, high input-to-output isolation switchers and routers. The HA4244's low input capacitance and high input resistance provide excellent video terminations when used with an external 75Ω resistor. This crosspoint contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled (EN = 0).

Synchronizing Latches

The HA4244 contains two latches which gate the EN input, thereby allowing all the crosspoints in a matrix to switch states synchronously. The latches also allow the EN input to be changed without affecting the current state of the HA4244. Thus, the next channel switch can be set up, and isn't acted upon until the next rising CLK edge. As long as the EN signals meet a setup and hold time relative to the rising CLK edge, all of the HA4244s will assume their new state at the same time.

Power-Up Disable Function

The double latched EN signal, and single CLK input prevent the user from controlling the crosspoint state at power-up. To rectify this situation, the HA4244 incorporates power-up circuitry to ensure that the crosspoint powers up in the disabled state. Disabling the HA4244 prevents bus contention between multiplexed outputs, and minimizes the switching matrix supply current during power-up. Consider, for example, a matrix of 625 crosspoints that power-up randomly. If 50% of them power-up enabled, the required matrix supply current is 3.3A (313 x 10.5mA), neglecting output current. If HA4244s are utilized the power-up current is reduced to 0.125A (625 x 200μA).

Frequency Response

Most applications utilizing the HA4244 require a series output resistor, R_S, to tune the response for the specific load capacitance, C_L, driven. Bandwidth and slew rate degrade as C_L increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. As an example, -3dB bandwidth decreases to 160MHz for C_L = 100pF, R_S = 0Ω. In big matrix configurations where C_L is large, better frequency response is obtained by cascading two levels of crosspoints in the case of multiplexed outputs, or distributing the load between two drivers if C_L is due to bussing and subsequent stage input capacitance.

Control Signals

EN - The ENABLE input is a TTL/CMOS compatible, active high input. When driven low this input forces the output to a true high impedance state and reduces the power dissipation by two orders of magnitude.

CLK - An active high, TTL/CMOS compatible input that controls the synchronizing latches. When CLK transitions low, the current state of the EN input is latched in the IC. This allows the EN input to be changed to the value corresponding to the next channel switch, without affecting the HA4244's current state. The HA4244 assumes the new state on the next rising edge of CLK.

Power Up Considerations

No signals should be applied to the digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

Harris' Crosspoint Family

Harris offers a variety of 1 x 1 and 4 x 1 crosspoint switches. In addition to the HA4244, the 1 x 1 family includes the HA4600, which is an essentially similar device but without the synchronizing latches, and the HA4201 asynchronous crosspoint with a Tally output (enable indicator). The 4 x 1 family is comprised of the HA4314, HA4404, and HA4344. The HA4314 is a 14 lead basic 4 x 1 crosspoint. The HA4404 is a 16 lead device with Tally outputs to indicate the selected channel. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0, A1, $\overline{CS}$). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.
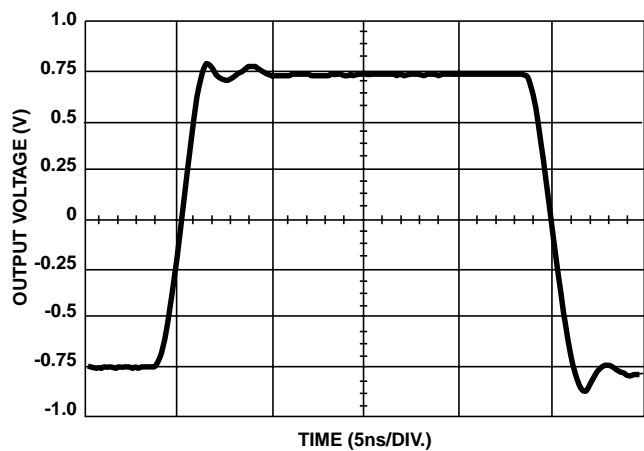
Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $T_A = 25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified

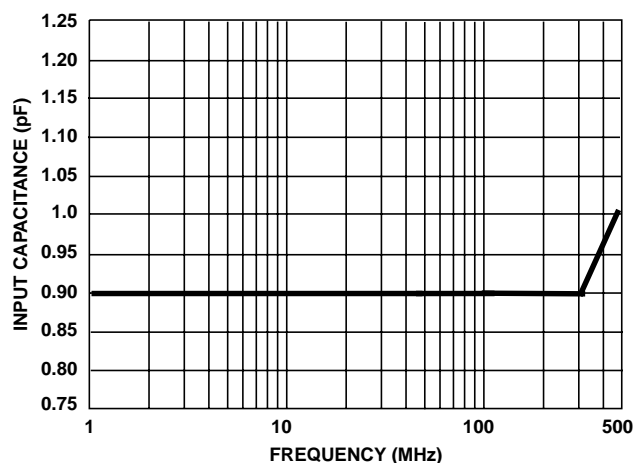**FIGURE 1. LARGE SIGNAL PULSE RESPONSE**

FIGURE 2. INPUT CAPACITANCE vs FREQUENCY

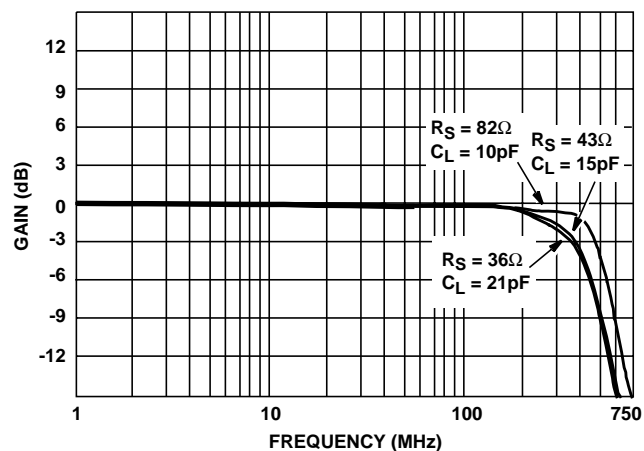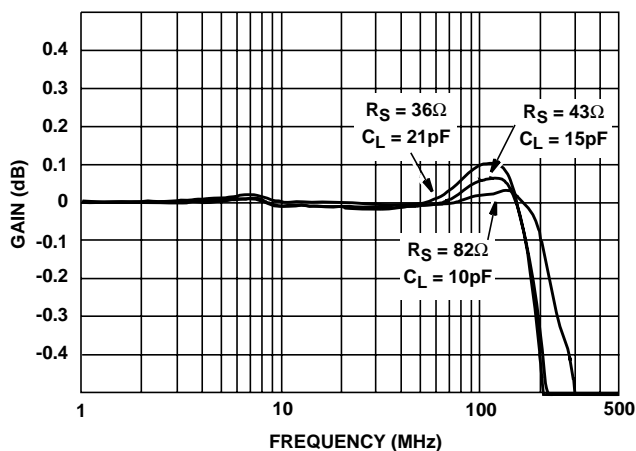**FIGURE 3. FREQUENCY RESPONSE**
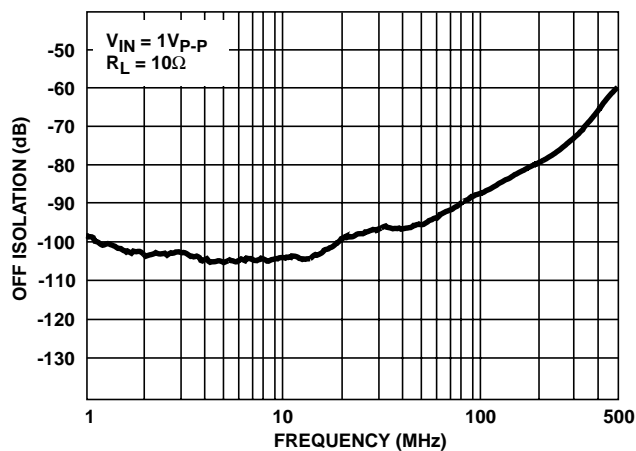

FIGURE 4. GAIN FLATNESS

FIGURE 5. OFF ISOLATION

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Die Characteristics

DIE DIMENSIONS:

51 mils x 36 mils x 19 mils
1290μm x 910μm x 483μm

METALLIZATION:

Type: Metal 1: AlCu (1%)/TiW
Thickness: Metal 1: 6kÅ ±0.8kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±1.1kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

53

SUBSTRATE POTENTIAL (Powered Up):

V-

Metallization Mask Layout

HA4244